VRSPV Soft-Start Strategy and AICS Technique for Boost Converters to Improve the Start-Up Performance

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***Abstract*—Soft-start strategy is very important for boost converters to guarantee the stability of the output voltage. However, previous methods may cause large initial inrush current and long output voltage settling time. In this paper, a variable ramp-slope with predefined voltage (VRSPV) soft-start strategy is proposed. As a result, one branch of the initial inrush current is successfully eliminated and the output settling time of the boost converter is shortened by using the variable slope soft-start voltage. Also, an adaptive inrush current suppressing (AICS) technique is designed. The series resistance of the output capacitor is adaptively regulated by AICS technique to further suppress the initial inrush current. Finally, the VRSPV strategy and AICS technique are combined and implemented in a voltage-mode boost converter. The measurement results show that the peak initial inrush current and settling time are decreased by 60% and 40%, respectively. The output voltage of the boost converter increases smoothly during the soft-start period and finally achieves stability. The proposed method of combining VRSPV strategy and AICS technique is very suitable to be integrated on a chip to save the printed circuit board area and cost.**

***Index Terms*—Adaptive inrush current suppressing (AICS), boost converter, predefined voltage, soft-start, variable ramp-slope.**

I. Introduction

SWITCHING dc–dc converters have become indispensable solutions for power managements due to the good features of wide input and output ranges, large driving capacity, and high efficiency. However, large initial inrush current and output overshoot appearing in the start-up period are long thorny problems, which possibly cause severe damages to the power systems [1]–[4]. Besides, output voltage-drop [1], settling time and system stability [5], [6] also need to be concerned in the start-up process. Soft-start methods with small inrush current and fast output voltage settling time have attracted widespread attentions [7], [8].

Soft-start methods based on generating different types of ramping voltage were presented in previous designs. Fig. 1 shows the structure of a voltage-mode boost converter including different soft-start schemes. The ramping voltage $V_{\rm soft}$ is generated by the soft-start circuit to substitute the reference voltage $V_{\rm ref}$ in the start-up period. Conventionally, a resistor–capacitor (*RC*) circuit is utilized to generate exponential $V_{\rm soft}$. In [9] and [10], the linear ramping voltage was generated to minimize the output voltage overshoot and reduce the inrush current, but this method requires additional pads and discrete capacitor to promote the accuracy of the output voltage [11]. A nanocurrent has been used to shrink the capacitor to produce a linear ramping soft-start voltage, but it is difficult to control the nanoamp grade current because it is easily affected by the fabrication process [12], [13]. A clock-based soft-start circuit was presented in [10] and [14] for the buck converter to realize a step-changed ramping voltage, in which both the output voltage and the inductor current increase smoothly without any oscillation or overshoot. Same results were also shown in [15], in which an on-chip nonlinear clamping soft-start voltage is generated to reduce the overcurrent. Another nonlinear method to increase $V_{\rm soft}$ exponentially was designed in a paralleled power system [16]. A two-stage soft-start circuit is implemented to greatly reduce the start-up current in the boost converter, in which it needs an automatic substrate switching circuit [17], [18]. For digital-controlled dc–dc converters, digital-based soft-start strategy can be embedded in the controller [19].

Some other methods are also used to reduce the inrush current passing through the power stage of the boost converter during the start-up period. For example, in order to reduce the inductor inrush current, an additional passing path was provided by using an MOS transistor parallel connected with the inductor [2], by using a diode to directly charge the current to the output capacitor [7], [20], or by using a special circuit to precharge the output and the flying capacitors [8], [21]. However, the inrush current passing through the output capacitor is still great for the

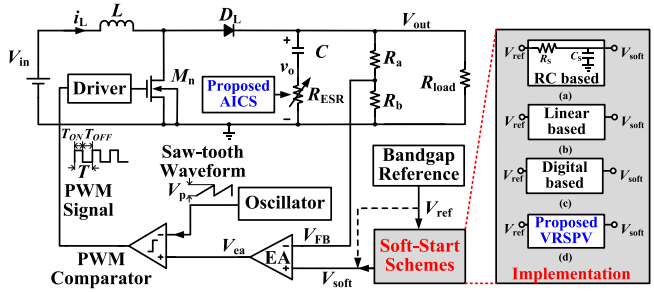

Fig. 1. Voltage-mode boost converter including different soft-start strategies and AISC technique.

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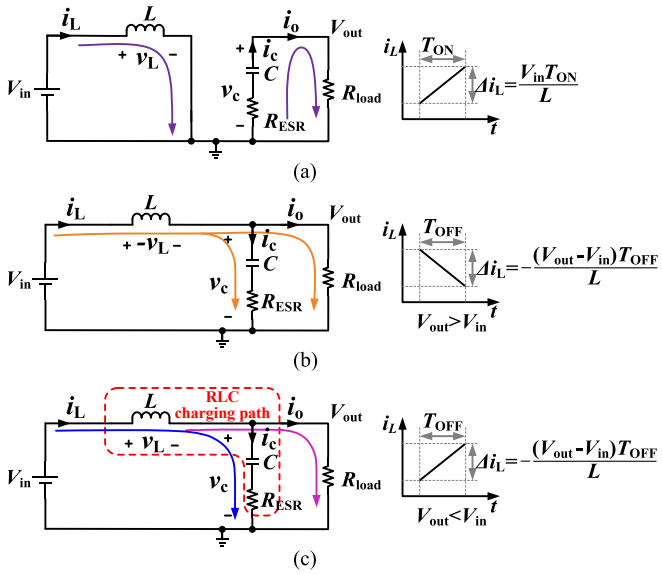

Fig. 2. (a) Charging path. (b) Discharging path when $V_{\rm out} > V_{\rm in}$. (c) Charging path when $V_{\rm out} < V_{\rm in}$.

above methods. Another way to suppress the inductor inrush current is to employ a resistor and a switch series connecting in the power stage [22], which needs additional time control logic. An active inrush current limiter with the MOSFET connected in series in the power stage was described in [23]. In order to eliminate the influence of control accuracy caused by parasitical gate–drain capacitance of the MOSFET, an additional big value discrete capacitor is needed to connect in parallel between gate and drain, which is very hard to be integrated on a chip.

Deep sight in the soft-start process is seldom involved in previous publications. The purpose of this paper is to present a soft-start technique which could be easily implemented in the embedded power managements with better performance than those of the currently existing soft-start strategies. In Section II, energy delivering and the inductor inrush current during the start-up period are discussed for a boost converter. Then, variable ramp-slope with predefined voltage (VRSPV) soft-start strategy is presented in Section III. In Section IV, adaptive inrush current suppressing (AICS) technique is designed to further reduce the inrush current. Experiment results verify the good performance of the proposed method in Section V. Finally, the conclusions are made in Section VI.

II. Energy Delivering and Inrush Current Analysis

The structure of a voltage-mode boost converter is shown in Fig. 1. Energy is transferred from supply to output by charging and discharging the inductor *L* as shown in Fig. 2. The output divider provides a feedback voltage V_{FB} which is fed into an error amplifier (EA). The difference between V_{FB} and the reference voltage $V_{\rm ref}$ is amplified to obtain the error voltage $V_{\rm ea}$ which is compared to a saw-tooth waveform with a peak-to-peak value of V_p to generate pulse width modulation (PWM) signals. PWM signals control the ON/OFF of the switching transistor M_n to regulate the output voltage $V_{\rm out}$.

The charging and discharging paths of the inductor in different states are shown in Fig. 2. When M_n is turned ON, the inductor current i_L increases linearly during $T_{\rm ON}$, thus energy is stored in the inductor *L*, meanwhile the output capacitor *C* offers the energy needed by load, as shown in Fig. 2(a). When M_n is turned OFF, if $V_{\rm out} > V_{\rm in}$, the supply and inductor together discharge the energy to the output capacitor and load. Assume that the output voltage constant i_L decreases linearly during $T_{\rm OFF}$, as shown in Fig. 2(b). However, at the beginning of the soft-start process $V_{\rm out} < V_{\rm in}$. *L*, *C*, and the equivalent series resistor $R_{\rm ESR}$ constitute a resistor–inductor–capacitor (*RLC*) charging path, as shown in Fig. 2(c), thus i_L increases further until $V_{\rm out} > V_{\rm in}$. Therefore, the total inrush current of the boost converter consists of two branches of i_L in the start-up period, as shown in Fig. 2(a) and (c), respectively. Two aspects could be considered to decrease the inrush current. One is to eliminate the inductor current shown in Fig. 2(a) by maintaining M_n OFF before $V_{\rm out} > V_{\rm in}$. Another way is to suppress the inductor current shown in Fig. 2(c) by designing *L*, *C*, and $R_{\rm ESR}$ reasonably.

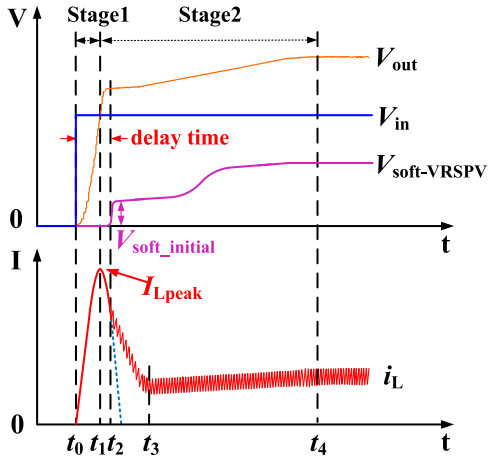

Fig. 3. Soft-start process of the proposed VRSPV scheme.

III. Design Details of VRSPV Strategy

A. VRSPV Strategy

As shown in Fig. 2(a), the current passing through M_n is proportional to the total on-time of M_n. The total on-time is determined by the duty ratios which are normally controlled by soft-start strategy. In this paper, VRSPV strategy is proposed. The diagrammatic sketch of the VRSPV process is shown in Fig. 3. During Stage 1 ($t_0 - t_1$), the soft-start voltage $V_{\text{soft-VRSPV}}(t)$ remains zero to keep the duty ratio to be equal to zero to avoid the current passing through M_n, until the inductor current reaches its peak value, which means that one branch of the inrush current mentioned previously is eliminated during Stage 1. In Stage 1, the peak inductor current $I_{\rm Lpeak}$ and t_1 are decided by the *RLC* charging circuit, as shown in Fig. 2(c), which can be calculated as

$$\begin{cases} I_{\rm Lpeak} = V_{\rm in}\sqrt{\dfrac{C}{L}} + \dfrac{V_{\rm in}}{R_{\rm load}} \approx V_{\rm in}\sqrt{\dfrac{C}{L}} \\ t_1 = \sqrt{LC}\arctan\left(-2R_{\rm load}\sqrt{\dfrac{C}{L}}\right) \approx \dfrac{\pi}{2}\sqrt{LC} \\ \qquad (r_{\rm ESR} = 0, R_{\rm load} >> 0). \end{cases} \tag{1}$$

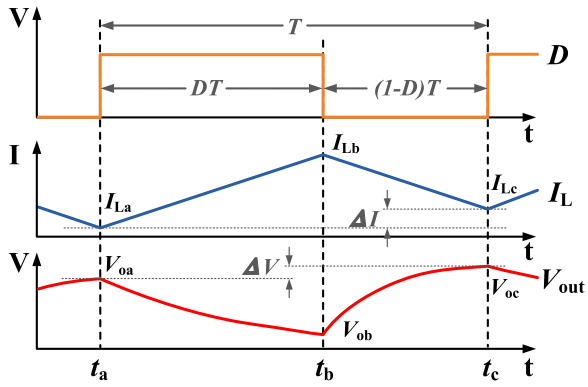

Fig. 4. Waveform variation in one switching period.

According to (1), I_{Lpeak} decreases with the increase of L or the decrease of C. Meanwhile, t_1 increases with the increase of LC. Thus, the proper design of the power stage is an effective way to reduce the inrush current.

During Stage 2 ($t_1 - t_4$) as shown in Fig. 3, $V_{\mathrm{out}} > V_{\mathrm{in}}$. When M_n turns OFF, the inductor begins to discharge energy to the output and the inductor current decreases during T_{OFF}, as shown in Fig. 2(b). From t_1 to t_2, $V_{\text{soft-VRSPV}}(t)$ remains zero to ensure the decreasing of i_L. After a short-time interval, a step-up change of the soft-start voltage $V_{\text{soft\_initial}}$ is set at t_2 to immediately increase the duty ratio, which increases the inductor charging time to prevent the rapid dropping of i_L. The time interval from t_0 to t_2 is called the delay time of $V_{\text{soft\_initial}}$, which is designed as a constant slightly larger than t_1. After t_2, $V_{\text{soft-VRSPV}}(t)$ changes with variable ramp slopes. At beginning, $V_{\text{soft-VRSPV}}(t)$ increases gradually to ensure that the inductor obtains enough energy to avoid the boost converter entering into the discontinuous conduction mode (DCM). At t_3, the inductor current stops decreasing and begins to increase. Then, $V_{\text{soft-VRSPV}}(t)$ increases quickly to promote the increasing rate of the output voltage. Finally, $V_{\text{soft-VRSPV}}(t)$ increases slowly again to ensure a smooth changing of the output voltage until t_4 when $V_{\text{soft-VRSPV}}(t)$ attains the reference voltage and the soft-start process finishes. After that, the boost converter reaches its steady state.

1) Initial Duty Ratio and $V_{\text{soft\_initial}}$: $V_{\text{soft\_initial}}$ can be calculated by analyzing the increments of the inductor current ΔI and the output voltage ΔV. For one switching period of PWM signals, i.e., from t_a to t_c, as shown in Fig. 4, the equations can be established in each period as follows:

$$\begin{cases} I_{Lb} = \int_{ta}^{tb} \dfrac{V_{\mathrm{in}}}{L} dt = I_{La} + \dfrac{V_{\mathrm{in}} DT}{L} \\ I_{Lc} = \int_{tb}^{tc} -\dfrac{V_{\mathrm{out}} - V_{\mathrm{in}}}{L} dt = I_{Lb} - \dfrac{(V_{\mathrm{out}} - V_{\mathrm{in}})(1-D)T}{L} \end{cases} \tag{2}$$

$$\begin{cases} V_{ob} = V_{oa} e^{-\dfrac{DT}{R_{\mathrm{load}} C}} \\ V_{oc} = \int_{tb}^{tc} \left[\dfrac{I_{Lc} - I_{Lb}}{(1-D)T} (t - t_b) + I_{Lb} - \dfrac{V_{\mathrm{out}}}{R_{\mathrm{load}}} \right] dt. \end{cases} \tag{3}$$

Thus, the increment expression can be obtained as

$$\Delta I = I_{Lc} - I_{La} = \frac{V_{\mathrm{in}} - V_{\mathrm{out}}(1-D)}{L} T \tag{4}$$

$$\Delta V = V_{oc} - V_{oa} = \frac{1}{C} \left[\frac{(I_{Lc} - I_{Lb})}{2} + \left(I_{Lb} - \frac{V_{\mathrm{out}}}{R_{\mathrm{load}}} \right) \right] (1-D)T + V_{ob} - V_{oa} \tag{5}$$

where V_{out} and R_{load} are the output voltage and load resistance, respectively. Since V_{out} almost does not change during a switching period, V_{out} in (4) could be substituted by V_{oa}. If $\Delta I = 0$ is assumed, the duty ratio D_1 can be calculated as

$$D_1 = \frac{V_{oa} - V_{\mathrm{in}}}{V_{oa}}. \tag{6}$$

If $D > D_1, \Delta I > 0$. The inductor current keeps increasing.

Besides, a good soft-start strategy should keep the output voltage increasing continuously, i.e., $\Delta V > 0$. If $\Delta V = 0$ is assumed in (5), the expression of the duty ratio D_2 can be obtained as

$$\left(\frac{I_{Lc} + I_{Lb}}{2} - \frac{V_{\mathrm{out}}}{R_{\mathrm{load}}} \right) (1 - D_2)T + C(V_{ob} - V_{oa}) = 0. \tag{7}$$

Since V_{out} almost does not change during a switching period, V_{out} in (7) also could be substituted by V_{oa}. Combining with (2), (7) can be simplified as

$$(V_{oa} + V_{\mathrm{in}}) T D_2^2 + 2(I_{La} L - V_{oa} T) D_2 + (V_{oa} - V_{\mathrm{in}}) T + \frac{2 V_{oa} L}{R_{\mathrm{load}}} - 2 I_{La} L = 0. \tag{8}$$

Normally, I_{La} is very small and R_{load} is very large. Thus, $V_{oa} T >> I_{La} L$, (8) can be further simplified as

$$(V_{oa} + V_{\mathrm{in}}) D_2^2 - 2 V_{oa} D_2 + (V_{oa} - V_{\mathrm{in}}) \approx 0. \tag{9}$$

Thus, the duty ratio D_2 can be obtained as

$$D_2 \approx \frac{V_{oa} - V_{\mathrm{in}}}{V_{oa} + V_{\mathrm{in}}}, \quad \text{another root } D_{2'} \approx 1 \text{ is discard.} \tag{10}$$

If $D > D_2, \Delta V > 0$, which means the output voltage keeps on increasing.

From (6) and (10), we can see that because $V_{oa} < V_{\mathrm{in}}$ in Stage 1, the values of D_1 and D_2 are all smaller than 0. It means both the inductor current and the output voltage increase in Stage 1. In Stage 2, $V_{\mathrm{out}} > V_{\mathrm{in}}$, thus $D_1 > D_2 > 0$. At t_2, the initial duty ratio D_{initial} should satisfy $D_1 > D_{\mathrm{initial}} > D_2$ to ensure that the output voltage increases, but the inductor current decreases. From t_2 to t_3, the inductor current decreases slowly to effectively use the energy stored in the inductor to increase the output voltage faster. After t_3, when the inductor current falls to be a little more than the load current required by the boost converter, D is increased to be higher than D_1 to satisfy that both the output voltage and the inductor current increase quickly.

If the type-III compensation network shown in Fig. 5 is employed in the boost converter, the relationship between V_{soft} and

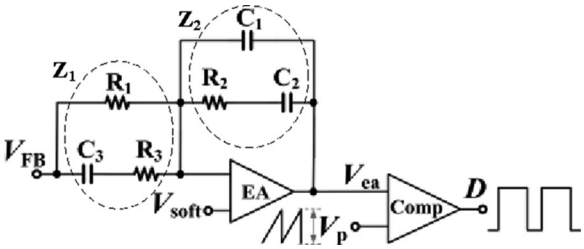

Fig. 5. Type-III compensation network and PWM generation circuit.

D satisfies

$$\begin{cases} V_{\rm ea} = \dfrac{(Z_1+Z_2)V_{\rm soft} - Z_2 V_{FB}}{Z_1} \\ D = \dfrac{V_{\rm ea}}{V_p} \end{cases} \tag{11}$$

where

$$Z_1 = \frac{R_1\left(R_3+\dfrac{1}{j\omega C_3}\right)}{R_1+R_3+\dfrac{1}{j\omega C_3}}, \quad Z_2 = \frac{\left(R_2+\dfrac{1}{j\omega C_2}\right)\dfrac{1}{j\omega C_1}}{R_2+\dfrac{1}{j\omega C_1}+\dfrac{1}{j\omega C_2}},$$

$$V_{FB} = \beta V_{\rm out}, \quad \beta = \frac{R_b}{R_a+R_b}$$

where β is the feed-back factor, V_p is the peak-to-peak value of the saw-tooth waveform, Z_1 and Z_2 are the input low-pass and the bypass bandpass impedances of the type-III compensator, respectively.

Therefore, the relationship between *D* and $V_{\rm soft}$ can be obtained as

$$V_{\rm soft} = \frac{Z_1 V_p D + Z_2 \beta V_{\rm out}}{Z_1+Z_2} = \frac{\dfrac{Z_1}{Z_2}V_p D + \beta V_{\rm out}}{\dfrac{Z_1}{Z_2}+1}. \tag{12}$$

Compared with the start-up period, time constant caused by *RC* in the type-III compensator is very small, which means that the voltage response of $V_{\rm soft}$ in the time domain is very fast and the hysteretic response hardly has influence on the start-up process. Thus, when a step-up change of the soft-start voltage occurs, the response time in the time domain can be ignored. In dc analysis, $\omega = 0$. Thus, $Z_1 = R_1$ and $Z_2 \to \infty$. If $V_{\rm out} = V_{\rm in}, V_{\rm soft}$ can be simplified as

$$V_{\rm soft} \approx \beta V_{\rm in}. \tag{13}$$

Therefore, in case of $V_{\rm out} = V_{\rm in}$, the dc value of $V_{\rm soft}$ can be calculated by (13), which indicates that the initial value of the soft-start voltage $V_{\rm soft\_initial}$ at t_2 as shown in Fig. 3 can be obtained by (13), which shows a feed-forward coefficient from the input voltage by employing the feedback factor of β to simply the circuit implementation. The initial voltage is designed to be a little larger than the theoretical value because after the inductor current passes the peak value and begins to decrease, the output voltage is a little higher than the input voltage.

2) Variation Range of the Duty Ratio: The variation range of the duty ratio is worthy of discussing. For a good soft-start process, the output voltage should always increase and the inductor current should begin to increase after t_3, as shown in Fig. 3. We can obtain ΔI and ΔV in (4) and (5) from the *i*th and the (*i*+*1*)th periods. Therefore, the increment of the duty ratio ΔD_i versus ΔI satisfies

$$\Delta D_i = D_{i+1} - D_i \approx \frac{(\Delta I_{i+1} - \Delta I_i)L}{V_{{\rm out}(i)}T}. \tag{14}$$

If ΔD_i is large enough, the inductor current can be raised quickly.

The mathematical expression between ΔD_i and $V_{\rm out}$ is hard to obtain. But, the conceptional relationship between them is known. In the steady state of a boost converter, when the duty ratio increases suddenly, the charging time of the inductor increases while the discharging time decreases. The energy transferred from the inductor to the output decreases, so $V_{\rm out}$ reduces. But, in the start-up process as shown in Fig. 3, after t_3, the inductor current is little larger than the requirement of load. Thus, there exists a duty ratio range to keep the energy stored in inductor and output capacitor both increase. With the increase in the duty ratio, discharging time decreases. However, the energy transferred from the inductor to the output may increase, so the output voltage may also increase. Thus, it has a critical $\Delta D_{\rm Pi}$ in the start-up process. When $\Delta D_i < \Delta D_{\rm Pi}$, both the inductor current and the output voltage increase. When $\Delta D_i = \Delta D_{\rm Pi}$, the inductor current increases and the output voltage does not change. When $\Delta D_i > \Delta D_{\rm Pi}$, the inductor current increases quickly, however, the output voltage decreases. In the above discussion, when the duty ratio increases, the output voltage should follow the increase. But, the inductor charging time increases. Thus, there has two possibilities: one is that the inductor current meets the requirement of load, the output voltage first decreases, and then increases. Another is that the inductor current is little larger than the requirement of load, the output voltage may always increases. Those processes match the influence of right-half-plane zero of the boost converters.

$$\Delta D_{\rm Pi} = \frac{\sqrt{(\Delta I_i L)^2 + A_i^2 + 2\Delta I_i L B_i} - (\Delta I_i L + A_i)}{(V_{oa(i)}+V_{\rm in})T} = \frac{2(B_i - \sqrt{B_i^2 - C_i})\Delta I_i L}{(V_{oa(i)}+V_{\rm in})T(\sqrt{(\Delta I_i L + B_i)^2 - C_i} + (\Delta I_i L + \sqrt{B_i^2 - C_i}))}$$

$$\text{where} \begin{cases} A_i = \sqrt{B_i^2 - C}, B_i = I_{La(i)}L + V_{\rm in}T \\ C_i = 2(V_{oa(i)} + V_{\rm in})\dfrac{V_{oa(i)}TL}{R_{\rm load}} \end{cases} \tag{15}$$

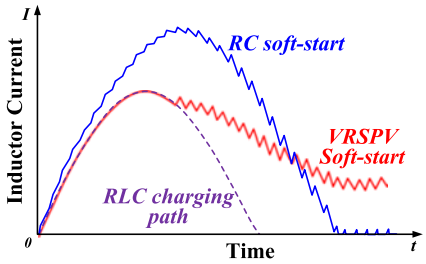

Fig. 6. Inductor current comparison.

According to (4) and (5), ΔD_{Pi} is derived from the *i*th and the $(i+1)$th periods by assuming that $V_{oa(i)} = V_{oa(i+1)}$

According to (15) as shown at the bottom of the previous page, if $\Delta I_i = 0$, $\Delta D_{\mathrm{Pi}} = 0$. It means that if the duty ratio remains constant, the inductor current remains unchanged.

Based on the same approximation above, where $R_{\mathrm{load}} >> 0, \Delta I_i \approx 0$. Thus, $\Delta I_i L << B_i$ and $C_i << B_i$. Therefore, (15) can be further simplified as

$$\Delta D_{\mathrm{Pi}} \approx \frac{C_i \Delta I_i L}{2B_i^2 (V_{oa(i)} + V_{\mathrm{in}})T} = \frac{V_{oa(i)} L^2}{(I_{La(i)} L + V_{\mathrm{in}} T)^2 R_{\mathrm{load}}} \Delta I_i. \tag{16}$$

Therefore, ΔD_{Pi} is approximately proportional to ΔI_i. If the inductor current increases quickly, ΔD_{Pi} is large, which means there is a large available incremental range of the duty ratio to guarantee that both the inductor current and the output voltage increase.

3) Comparison of Different Soft-Start Strategies: We make a comparison among the inductor current in the *RLC* circuit shown in Fig. 2(c) and the inductor current in the boost converter by using RC and VRSPV soft-start schemes, respectively, as shown in Fig. 6, where the same parameters are used. The peak current passing through *L* in the *RLC* circuit is the same as that of the VRSPV scheme, which is lower than that of the RC soft-start scheme. The reason is that the duty ratio keeps zero to turn-off M_n before the inductor current reaches its peak value in the VRSPV scheme, which results in a smaller inrush current in the start-up process.

B. Circuit Implementation of Soft-Start Strategy

1) Structure of the Soft-Start Circuit: The proposed circuit structure to achieve soft-start strategy is shown in Fig. 7, which includes an 8-bit counter, a 7-bit R-2R DAC, a two-channel multiplexer, a CLK divider, and seven 1-bit binary switches. The 8-bit counter produces a series of *Q* signals with different frequencies. These signals control the on/off state of the binary switches, and the binary switches determine the connection ways of the 7-bit R-2R DAC to obtain the waveform of V_{soft}. The PV node is used to set the initial soft-start voltage.

At first, "Reset" in Fig. 7 is set as "1" to reset circuit. The 8-bit counter generates digital codes, $Q[8:1] = 8'b0000\_0000$, to control the binary switches. The binary switches are implemented by using analog mux2_1. When "EN" is "1," "OUT" node is connected to X; when "EN" is "0," "OUT" node is connected to Y. The CLK divider is controlled by *Q* to get different divider

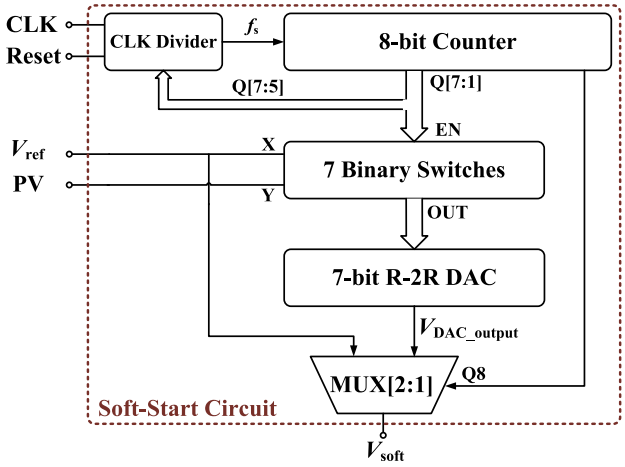

Fig. 7. Structure of the soft-start circuit.

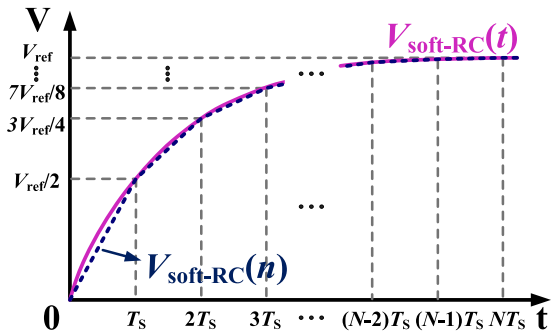

Fig. 8. Quantized waveform of $V_{\mathrm{soft\text{-}RC}}$.

ratios. When the soft-start process begins, $Q[8:1]$ is added 1 per rising edge of CLK. When $Q[8:1] = 8'b1000\_0000$, the output of the two-channel multiplexer changes to V_{ref}. Then, the soft-start process ends and the boost converter operates in the normal conversion stage. According to the circuit structure, V_{soft} can be written as

$$V_{\mathrm{soft}} = (V_{\mathrm{ref}} - V_{\mathrm{PV}}) \frac{B(Q)}{B_{\max}} + V_{\mathrm{PV}} \tag{17}$$

where $B(Q) = \frac{Q_1}{2^1} + \frac{Q_2}{2^2} + \cdots + \frac{Q_N}{2^N}$ $(N = 7)$, $B_{\max}$ is the biggest value of $B(Q)$, Q_i $(i = 1, 2, \ldots 7)$ is the *i*th bit of $Q[8:1]$, and V_{PV} presents the node voltage of "PV."

2) Implementation of Different Soft-Start Strategies: In order to compare the features of different soft-start strategies, RC, linear, VRS, and VRSPV strategies are all implemented by employing the same soft-start circuit. The circuit demonstrates strong compatibility and different shapes of V_{soft} could be obtained by reasonable design of the CLK divider.

a) For RC soft-start strategy: the soft-start voltage $V_{\mathrm{soft\_RC}}$ presents an exponential variation. The relationship between $V_{\mathrm{soft\text{-}RC}}(t)$ and *t* is illustrated in Fig. 8, and the equation can be expressed as

$$V_{\mathrm{soft\text{-}RC}}(t) = V_{\mathrm{ref}}(1 - e^{-\frac{t}{R_S C_S}}) \tag{18}$$

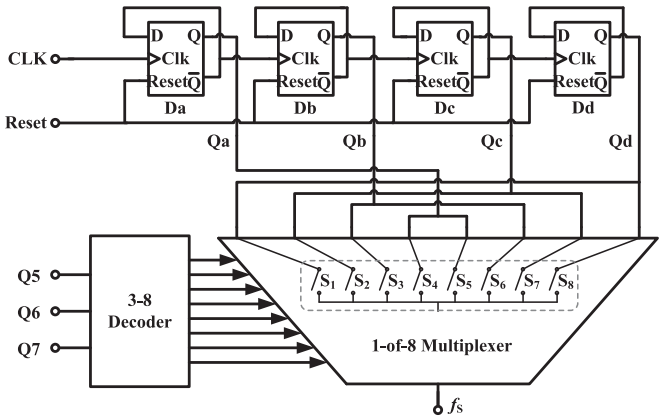

Fig. 9. Structure of the CLK divider for VRS and VRSPV strategies.

where R_S and C_S are the resistance and capacitance of RC soft-start circuit, respectively. If *t* is quantized, the discrete $V_{\text{soft-RC}}$ (*n*) can be written as

$$V_{\text{soft-RC}}(n) = V_{\text{ref}}(1 - e^{-\frac{nT_s}{R_S C_S}})(n = 0, 1, 2, ..., N) \quad (19)$$

where T_s is the sample period. *N* is determined by the resolution of R-2R DAC. In this study, $N = 7$. If $T_s = R_s C_s ln2$ is assumed, (19) becomes

$$V_{\text{soft-RC}}(n) = \frac{2^n - 1}{2^n} V_{\text{ref}} = \left(1 - \frac{1}{2^n}\right) V_{\text{ref}}. \quad (20)$$

For RC soft-start strategy, the frequency of output signals of the CLK divider $f_{S-\text{RC}}(n)$ is expressed as

$$f_{S-\text{RC}}(n) = \frac{1}{2^n} f_{S0-\text{RC}}. \quad (21)$$

$f_{S-\text{RC}}(n)$ is decreased to half of previous frequency every T_s. The initial frequency $f_{S0-\text{RC}}$ is determined by T_s. In this study, $f_{S0-\text{RC}} = 2^{N-1}/T_s = 64/T_s$. The total soft-start time satisfies

$$T_{\text{soft-RC}} = NT_s = N\frac{2^{N-1}}{f_{\text{CLK}}} = \frac{448}{f_{\text{CLK}}}. \quad (22)$$

b) For linear soft-start strategy: The input frequency of the CLK divider keeps constant, which is equal to the output of the CLK divider. Thus, the total soft-start time of linear strategy satisfies

$$T_{\text{soft-linear}} = \frac{2^N}{f_{\text{CLK}}} = \frac{128}{f_{\text{CLK}}}. \quad (23)$$

c) For VRS and VRSPV soft-start strategies: same CLK divider is adopted. The difference between them is that there is a delay time to ensure M_n turned OFF and a predefined voltage $V_{\text{soft\_initial}}$ is connected to the "PV" node for VRSPV strategy. The "PV" node is connected to GND for VRS strategy.

The CLK divider is designed to generate different frequency of f_S, which determined the variation rate of *Q*[8:1], and produce soft-start voltages in different steps of the soft-start process. Fig. 9 shows the structure of the CLK divider. *Q*[7:5] are generated by a 8-bit counter, which divides the whole soft-start process into eight steps. A fixed frequency clock signal, CLK, is used to generate four frequency signals, Q_a, Q_b, Q_c, and Q_d, which are selected by the sequence from Q_d to Q_a and then from Q_a to Q_d to form a new clock f_S in the eight steps, with frequency relationship of

$$f_{\text{CLK}} = 2f_{Qa} = 4f_{Qb} = 8f_{Qc} = 16f_{Qd}. \quad (24)$$

The total soft-start time $T_{\text{soft}-V}$ of VRS and VRSPV strategies is decided by

$$T_{\text{soft}-V} = 2\left(\frac{2^{N-3}}{f_{Qa}} + \frac{2^{N-3}}{f_{Qb}} + \frac{2^{N-3}}{f_{Qc}} + \frac{2^{N-3}}{f_{Qd}}\right) = \frac{15 \times 2^{N-1}}{f_{\text{CLK}}} = \frac{960}{f_{\text{CLK}}}. \quad (25)$$

According to (22), (23), and (25), same soft-start time could be obtained if proper f_{CLK} is designed in different soft-start strategies, which gives a good way to make a comparison among the different strategies.

C. Brief Summary

In order to avoid large inrush inductor current and output voltage-drop, the VRSPV method is designed before t_2, *D* keeps 0, thus M_n is turned OFF. At t_2, $V_{\text{soft\_initial}}$ is set to obtain a stepped increment of the duty ratio to promote energy transferring from supply to the load. The inductor obtains enough energy and the inductor current does not decrease much, which avoids the DCM period. Then, the soft-start voltage increases gradually to keep the output voltage increasing. After that, the soft-start voltage increases quickly to promote the increasing rate of the output voltage. Finally, the soft-start voltage increases slowly again to ensure a smooth changing of the output voltage without overshoots or undershoots.

IV. AICS Technique to Further Reduce the Inrush Current

A. Circuit Implementation

Based on the analysis above, one branch of the inrush current passing through M_n shown in Fig. 2(a) is eliminated by using VRSPV strategy, while another branch of the inrush current flowing through the output filter *C*, shown in Fig. 2(c), might be still large. Increasing r_{ESR} is an effective way to reduce this part of the inrush current. When $V_{\text{out}} < V_{\text{in}}$, a large r_{ESR} is required to suppress the peak current. However, when $V_{\text{out}} > V_{\text{in}}$, r_{ESR} should be reduced to lower the output ripple. According to (1), if $L = 10$ μH and $C = 4.7$ μF in the power stage of the boost converter, the calculated time interval between t_0 and t_1 shown in Fig. 3 is only 10 μs, which means that r_{ESR} should be regulated in 10 μs. In this study, the AICS circuit is designed, as shown in Fig. 10. It includes an additional equivalent series resistor R_{ESR}, a switch *SW*, a Schmitt trigger, a capacitor C_f, and a resistor R_f.V_f is the input of Schmitt trigger to control the on/off state of SW. The value of R_{ESR} is designed according to the allowed peak value of the inrush current.

For a capacitor *C*, the relationship between V_C and i_C satisfies

$$i_C = C\frac{dV_C}{dt}. \quad (26)$$

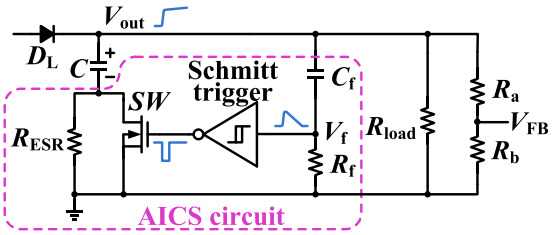

Fig. 10. AICS circuit and its signal response.

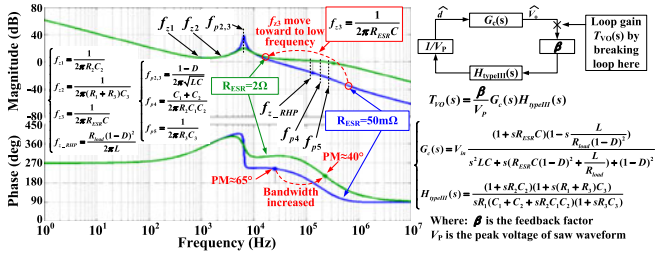

Fig. 11. Loop gain of the boost converter with different $R_{\rm ESR}$.

In this study, dV_C/dt is detected to observe i_C by cascading C_f and R_f, as shown in Fig. 10, which acts a detector. When the boost converter is powered ON, $V_{\rm out} < V_{\rm in}$, the output capacitor C is charged, the growth rate of $V_{\rm out}$ is high. At the same time, ac signals of the output pass the high-pass filter of C_f and R_f, thus V_f increases. When V_f reaches to the high threshold voltage of the Schmitt trigger, the trigger flips to turn OFF SW, and $R_{\rm ESR}$ is in series connection with C to suppress the initial inrush current. When $V_{\rm out} > V_{\rm in}$, the growth rate of $V_{\rm out}$ becomes slow, V_f decreases. When V_f descends to the low threshold voltage of the Schmitt trigger, the trigger flips to turn ON SW. $R_{\rm ESR}$ is shorted and the AICS circuit stops operating. The transfer function of the high-pass filter satisfies

$$H(s) = \frac{V_f}{V_{\rm out}} = \frac{sR_fC_f}{1+sR_fC_f}. \tag{27}$$

This function has a zero at dc and a pole at $1/(R_fC_f)$. The pole frequency represents the cutoff frequency of the high-pass filter, which means that the signals with frequency higher than the pole can pass the filter in time, while the signals with frequency lower than the pole will be attenuated. The resonance frequency of LC is equal to $1/\sqrt{LC}$. If $R_fC_f \approx \sqrt{LC}$ is designed, the voltage variation slope of the capacitor generated by the initial inrush current can be sensed in time by the high-pass filter. The AICS circuit has a very fast transient response to turn ON or turn OFF $r_{\rm ESR}$ to suppress the inrush current in the start-up period or lower the output voltage ripples in the conversion operation.

B. Stability Analysis

In the AICS circuit, a zero is generated by $R_{\rm ESR}$ and C. If the zero shift is near to the crossover frequency of the boost converter, the loop bandwidth will increase and additional phase margin is provided. Thus, the steady and transient features of the boost converter are both improved. However, if $R_{\rm ESR}$ is too big, the zero frequency might be less than the one-tenth of the loop crossover frequency of the boost converter. Although the loop bandwidth could be further increased, the phase margin will decrease by the influence of the high-frequency pole and the right-half-plan zero, which may lead to instability. Reasonable $R_{\rm ESR}$ is designed to avoid this problem. By using MATLAB software, the simulated loop gain of the boost converter is shown in Fig. 11. When AICS works, the loop bandwidth increases ten times and the phase margin satisfies the stability requirement of the boost converter.

C. Brief Summary

AICS technique is a good solution in the field where the inrush current passing through C needs to be strictly suppressed. Compared with the previous current limiter by using MOSFET, combining VRSPV strategy with AICS technique can not only suppress the inrush current but also shorten the start-up time effectively, which is also easily fully integrated on a chip. The proposed technique is more suitable to be applied in the systems in which fast transient response is especially required.

V. Experimental Results and Discussion

VRSPV strategy and AICS technique have been implemented and verified in a boost converter with 1-MHz switching frequency. The input voltage is 5 V and the output voltage is 18 V with 120-mA load current. The inductor and the capacitor are chosen as 10 μH and 4.7 μF, respectively. $R_{\rm ESR}$ is 2 Ω. R_f and C_f are designed as 100 Ω and 47 nF, respectively. SW is selected as TI-CSD16301Q1. According to (1) and (13), the calculated time interval t_1 is approximately equal to 10 μs and the predefined initial voltage $V_{\rm soft\_initial}$ is approximately 0.28 V in case of $V_{\rm out} = V_{\rm in}$. Considering the growth rate of the input voltage when power is ON and parameter errors of the inductor and the capacitor, the delay time t_2 is designed as 16 μs. At t_2, the output voltage increases up to nearly 8 V. The calculated $V_{\rm soft\_initial}$ is 0.44 V. Finally, $V_{\rm soft\_initial} \approx 0.45$ V is adopted in practical implementation. The boost converter including its power stage and controller, AICS circuit, 7-bit R-2R DAC, and 2-channel multiplexer are implemented on printed circuit board, the clock generator and 8-bit counter are realized by using a field-programmable gate array, as shown in Fig. 12.

Figs. 13–15 show the measured waveforms of on-chip RC soft-start scheme, linear soft-start scheme, and VRS soft-start scheme, respectively. Soft-start times for all strategies are fixed to 1.5 ms. Output voltage-drop and DCM operation with large inrush current and long settling time could be found in these three test results. Fig. 16 presents the measured results of VRSPV strategy. The output voltage continues to increase without any drop. The peak inrush current is restricted within 2.2 A. The settling time is 1.7 ms without DCM period.

Fig. 17 presents the measured results of the method combining VRSPV and AICS techniques. Fig. 18 shows the detailed inrush current response of the designed method. When power is ON, $V_{\rm out}$ increases rapidly, the high-frequency signal of $V_{\rm out}$ passes the filter and SW is turned OFF by the flipping of the

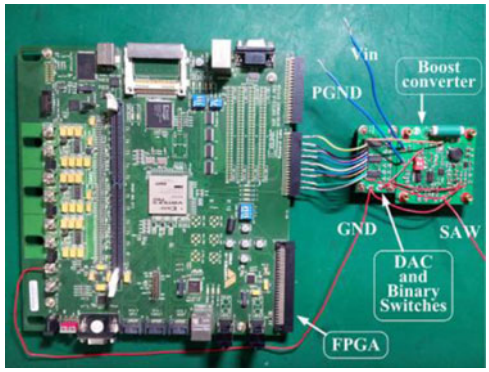

Fig. 12. Photo of the boost converter.

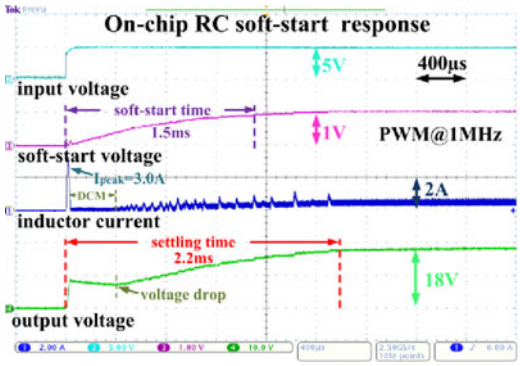

Fig. 13. Experiment results of the on-chip RC soft-start scheme.

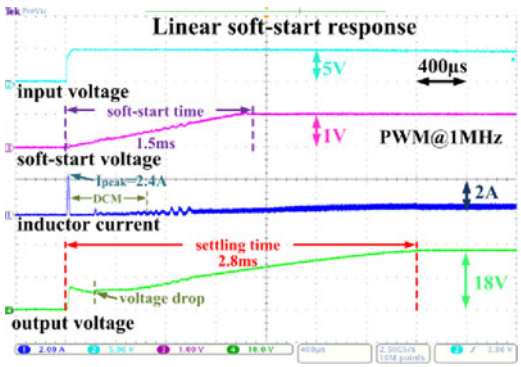

Fig. 14. Experiment results of the linear soft-start scheme.

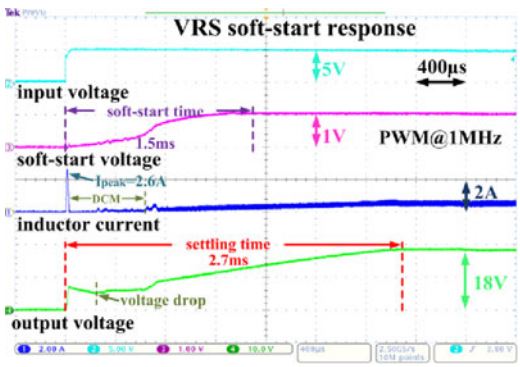

Fig. 15. Experiment results of the VRS soft-start scheme.

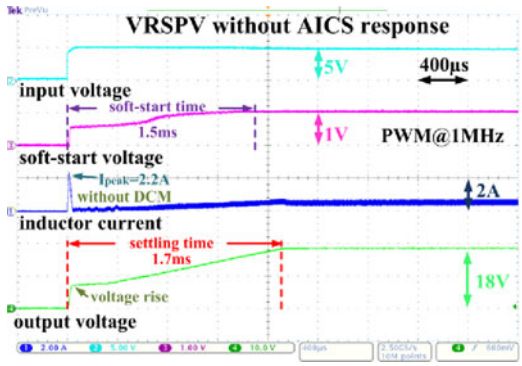

Fig. 16. Experiment results of the VRSPV soft-start scheme.

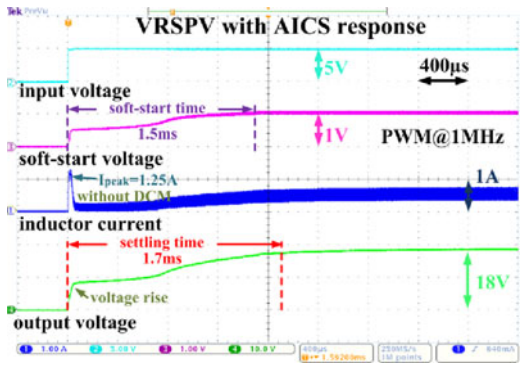

Fig. 17. Experiment results of VRSPV with AICS scheme.

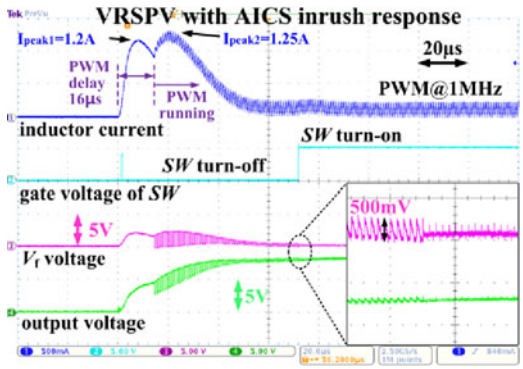

Fig. 18. Detailed response of VRSPV with AICS scheme.

Schmitt trigger. As the result, the equivalent series resistance of the capacitor increases to 2 Ω. The peak initial inrush current is restricted within 1.2 A after a delay time of 16 μs. During the delay time, the initial soft-start voltage remains 0 V to keep M_n turned OFF. Then, a step-up change of the soft-start voltage is set to immediately increase the duty ratio. Thus, another peak inrush current with 1.25 A appears to lift the output voltage. After several switching periods, the Schmitt trigger flips again to turn ON SW. The AICS circuit finishes operating. There are two current peaks in the soft-start period, which ensures the inductor and the capacitor obtain more energy. DCM is avoided.

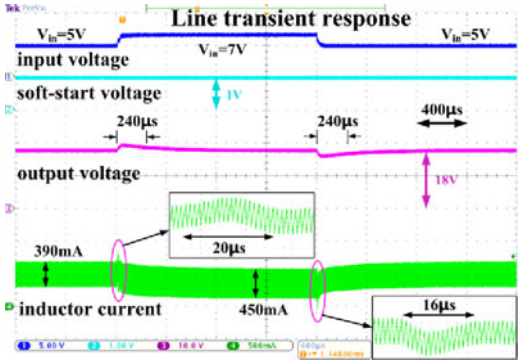

Fig. 19. Measured waveforms of line transient response.

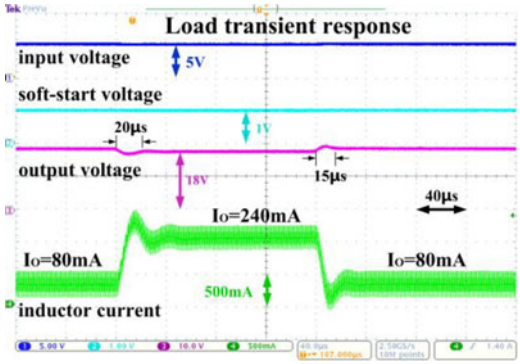

Fig. 20. Measured waveforms of load transient response.

The settling time of 1.7 ms is obtained, which is the same as that of the VRSPV scheme without AICS.

The dynamic responses caused by the variations of the input voltage and the load current are also measured, as shown in Figs. 19 and 20. Fig. 19 shows the measured waveforms of line transient response when the input voltage changes between 5 and 7 V. Fig. 20 shows the measured waveforms of load transient response when the load current changes between 80 and 240 mA. The measurement results show good dynamic performance of the designed boost converter.

To sum up, the output voltage of the boost converter is determined by the input voltage and the duty ratio. In the steady state, when load transient occurs (ignoring all parasitical parameters), the output voltage immediately changes, which causes the variation in the duty ratio. Then, the output voltage is regulated again through the feedback loop. In this process, the dc value of the inductor current changes but the ac value remains unchanged. The measured regulating period is only 20 μs as shown in Fig. 20. If load transient occurs during the soft-start period, it will bond to an influence to the start-up process. But the start-up period is usually several milliseconds, which is much longer than the load transient response time. In addition, the soft-start process can be approximately considered as a reference tracking process. During the start-up period, the reference voltage increases continuously and the output voltage of the boost converter is regulated by the close loop control. The proposed VRSPV strategy produces the soft-start voltage to substitute the conventional soft-start voltage, which does not influence the loop control of the dc–dc converter. The strategy could also be well applied in current-mode-controlled dc–dc converters. Besides, for hardware implementation, VRSPV is easy to be implemented because only several DFFs, binary switches, resistors, and basic logic are needed. Furthermore, because the peak inrush current is significantly suppressed by AICS technique, the size of M_n and D_L could be reduced. From this perspective, the cost of the integrated boost converter could be decreased. The comparisons are summarized in Table I. VRSPV strategy with AICS technique shows the best features among these schemes. VRSPV strategy with AICS technique shows advantages such as small size, fully integrated on a chip, no DCM, no output voltage-drop, the lowest inrush current, and the shortest settling time. It could be universally utilized in other converters such as buck or buck-boost converters with asynchronous or synchronous and voltage-mode or current-mode dc–dc converter architectures.

TABLE I
EXPERIMENTAL RESULT COMPARISON

Soft-Start Strategy	DCM Process	Output Drop	Inrush Current (A)	Settling time (ms)
RC	yes	yes	3.0	2.2
linear	yes	yes	2.4	2.8
VRS	yes	yes	2.6	2.7
VRSPV without AICS	no	no	2.2	1.7
VRSPV with AICS	no	no	1.25 (↓60%)	1.7 (↓40%)

VI. CONCLUSION

In this paper, the components of the inductor inrush current and stages of the soft-start process are analyzed. The VRSPV soft-start strategy combining AICS technique is proposed and the detailed design is given. Both VRSPV strategy and AICS circuit are successfully verified in a prototype boost converter. Experiment results show the rationality, practicability, and effectiveness of the proposed method, which is a good solution to improve the soft-start performance of the boost converter. In addition, because the off-chip resistor and the capacitor are not needed, I/O pads for external passive components are no longer required. Therefore, the facility of power managements is significantly improved.

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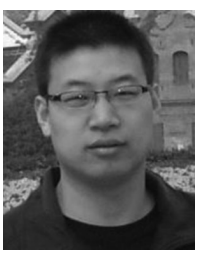

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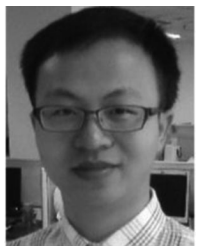

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