Pseudo-Constant Switching Frequency in On-Time Controlled Buck Converter with Predicting Correction Techniques

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***Abstract*—The predicting correction technique (PCT) is proposed to achieve an adaptive on-time control for ripple-based buck converters. The switching frequency f_{SW} variation is suppressed when the PCT technique considers complete parasitic resistances of the components and devices. Even without extra clock-controlled circuits and current sensing circuits, the buck converter operates with a nearly constant f_{SW} over a wide load range. Parasitic resistances almost cause no influence and restriction on f_{SW}. Only input voltage is used to predict the adaptive on-time. Measurement results show only 0.32% in $\Delta f_{SW}/f_{SW}$ and 5.7 kHz/A in $\Delta f_{SW}/\Delta I_{LOAD}$ in case of 1.4 A load current change and f_{SW} is 2.5 MHz. Consequently, a pseudo-constant f_{SW} with well-defined noise spectrum strongly benefits the solution of electromagnetic interference (EMI) for system-on-a-chip (SoC) applications.**

***Index Terms*—Adaptive on-time control, dc–dc converter, direct current resistance, on resistance, on time control, predicting correction technique (PCT), switching frequency.**

I. Introduction

DUE to the progress of advanced nanometer scaling down process in Fig. 1, drastic increase in transistor density for system-on-a-chip (SoC) results in that power density obviously increases although the supplying voltage is scaled down from 5 V in 0.5 μm to 0.85 V in 10 nm. The trend follows and even may be beyond the Moore's law. Consequently, power managements or named as smart power converters, which feature high power and high performance, are urgently demanded for today's consumer electronics.

Table I concludes the performance of three common control methods for dc–dc buck power converters. Ripple-based on-time control (RBOTC) [1]–[24] for buck converters is a superior control method to meet the requirements for SoC because it features best performance in comparison with pulsewidth-modulated (PWM) current-mode control (CMC) and PWM voltage-mode control (VMC) [14], [25]–[32]. For the RBOTC, the constraint of output capacitor with large equivalent-series resistance (ESR) is successfully overcome so that output ripple can be further reduced by using multilayer ceramic capacitors (MLCCs) [5]–[7], [9]–[13], [32]. However, the RBOTC is a clock-free architecture owing to its ripple-based control architecture. It reveals that the RBOTC suffers from severe switching frequency variation (Δf_{SW}) if any disturbances from input voltage V_{IN}, output voltage V_{OUT}, and loading current I_{LOAD} occur.

In other words, power converter with the RBOTC, which becomes a frequency interference source in the range of $f_{SW} \pm 0.5\Delta f_{SW}$, is an obvious disadvantage. Analog circuits, such as RF, audio system, analog-to-digital (ADC) converters, digital-to-analog (DAC) converters, and phase-locked-loop (PLL) circuits, are sensitive to certain variation of switching frequency (f_{SW}) because the frequency variation degrades the performance of those analog circuits as shown in Fig. 2. Furthermore, if considering the frequency interference to surrounding circuit through electromagnetic interference (EMI), expected noise spectrum, from a constant f_{SW} switching converter and even with a small Δf_{SW}, can be utilized to design the filtering

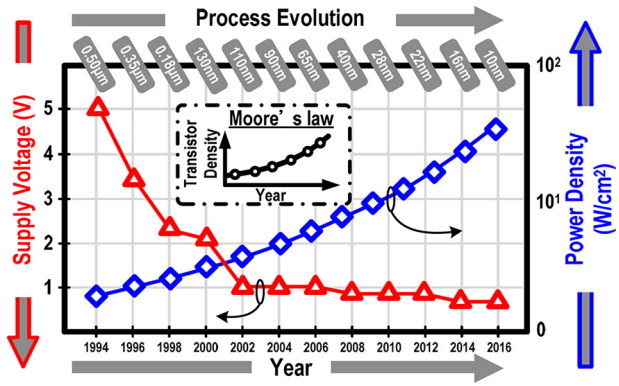

Fig. 1. Trend in supply voltage and power density with the evolution of process technology.

TABLE I
Characteristics of Three Common Control Methods for DC–DC Buck Converter

	PWM CMC	PWM VMC	RBOTC
Efficiency enhancement at light loads	Complex	Complex	Excellent (Inherence)
Rejection of frequency variation at CCM	Excellent	Excellent	Poor

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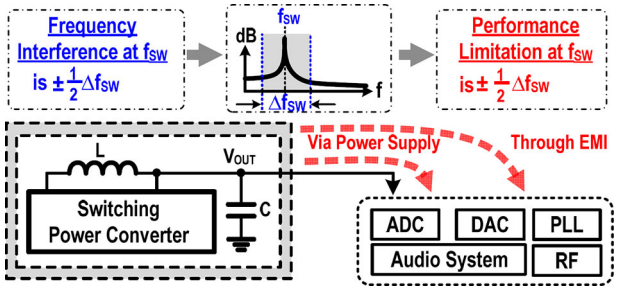

Fig. 2. Frequency interference cause by switching power converter makes the performance limitation of analog circuits at $f_{\rm SW}$ is $\pm 0.5\Delta f_{\rm SW}$.

circuits for low EMI. Therefore, frequency variation of RBOTC power converter needs to be suppressed to improve the SoC performance.

If the output voltage provided by power converters is scaled down below 1 V for the circuits in advanced process, $f_{\rm SW}$ also increases to several mega-Hertz for compact size and small output ripple. Fig. 3 shows the characteristics of switching frequency and load condition when conventional on-time control is used. Ideally, the switching frequency is constant and independent of load conditions. In reality, $\Delta f_{\rm SW}$ greatly increases if $V_{\rm OUT}$ and $f_{\rm SW}$ become lower and higher, respectively, at different load conditions. When the target $f_{\rm SW}$ is 600 kHz and load current change is 1.5 A, 2.5 V and 1 V of $V_{\rm OUT}$ cause 88 and 200 kHz variations in $f_{\rm SW}$, respectively. In contrast, 2.5 and 1 V of $V_{\rm OUT}$ cause 290 and 700 kHz variations in $f_{\rm SW}$, respectively, when the same load current change occurs and the target $f_{\rm SW}$ is 2 MHz.

Fig. 4 shows conventional architecture of dc–dc buck converter with the on-time control. The pre-regulator converts input voltage ($V_{\rm IN}$) to core voltage ($V_{\rm core}$), which supplies the controllers designed by core devices. The feedback controller monitors the feedback voltage ($V_{\rm FB}$) by the voltage divider to regulate $V_{\rm OUT}$. The feedback controller is mainly consists of a comparator (CMP), on-time control, SR latch. The on-time control generates a pulse to determine the on-time period ($T_{\rm ON}$). The operation during $T_{\rm ON}$ refers to the charging path for increasing inductor current (I_L). $T_{\rm ON}$ starts if $V_{\rm FB}$ falls below the reference voltage ($V_{\rm REF}$). According to the input voltage $V_{\rm IN}$ and the output voltage $V_{\rm OUT}$, the duty ratio (D) is determined. Consequently, $f_{\rm SW}$ of on-time control can be determined correspondingly by the predefined $T_{\rm ON}$ and its corresponding D [3], [25].

Because of the clock-free architecture of RBOTC, several techniques in previous literatures proposed the technique to alleviate the variation. Extra external clocks or PLLs are utilized at the cost of circuit complexity, silicon area, and cost [14]–[16], [26]–[29]. In contrast, the techniques use $V_{\rm IN}$ and $V_{\rm OUT}$ information to generate adaptive on time to maintain constant $f_{\rm SW}$ at different $V_{\rm IN}$ and $V_{\rm OUT}$ [10], [20], [32]. However, the performance is still constrained, and these works have no ability to ensure constant $f_{\rm SW}$ at different load conditions because practical parasitic resistances are not taken into consideration. Even though the load current information is applied by replacing $V_{\rm IN}$ by $V_{\rm LX}$, the improvement of $\Delta f_{\rm SW}$ is not effective [10]. Besides, one previous technique applies load information to revise the on-time period but the compensation values amounts lack of analysis. It is hard to decide the amount of compensation accurately [20]. Once over compensation occurs, $\Delta f_{\rm SW}$ even becomes worse. Furthermore, it's not complete to derive the quantitative analysis for $\Delta f_{\rm SW}$, $V_{\rm OUT}$, $V_{\rm IN}$, and $I_{\rm LOAD}$ because of the assumption conditions [20]. Tsai *et al.* [32] utilized the *RC* network to sense I_L and to adjust the adaptive on time for getting output voltage droop as the well-known adaptive voltage position (AVP) technique. However, the assumption of equal on-resistance value at both high-side and low-side power MOSFETs is necessary. Unfortunately, it is hard to maintain this assumption. Besides, many resistors and direct current resistance (DCR) of inductor should be matching exactly, so the design difficulty is increased.

Reduction of $\Delta f_{\rm SW}$ needs to suitably control the on time and alleviating $\Delta f_{\rm SW}$ also reduces EMI problems. Consequently, this paper induces the complete quantitative analysis and provides proposed predicting correction technique (PCT) to modulate an adaptive on time for constant $f_{\rm SW}$ under possible different conditions, including $V_{\rm IN}$, $V_{\rm OUT}$, and wide-range $I_{\rm LOAD}$, especially. Complete parasitic resistances of each component are taken into consideration without any assumption or simplification. Besides, only the driving signal of power MOSFET ($V_{\rm GP}$) is needed to achieve constant $f_{\rm SW}$ in the proposed on-time circuit. It greatly reduces the complexity compared to the previous works which need additional $V_{\rm IN}$, $V_{\rm OUT}$, $V_{\rm LX}$, current sensing circuit, and parasitic resistance of components of power stage.

This paper is organized as follows. Frequency variation analysis of the on-time control is explained in Section II. The proposed PCT is illustrated in Section III. Circuit implementation is shown in Section IV. Experimental results are reported in Section V. Finally, conclusions are made in Section VI.

II. Analysis of Switching Frequency Variation

A. Operation of On-Time-Controlled Switching Converter

Fig. 5 illustrates the timing diagram of on-time-controlled buck converter according to Fig. 4. The inductor current I_L conforms to voltage–second balance for stable regulation. Switching cycle begins at the rising edge of $T_{\rm ON}$ that is triggered by $V_{\rm SET}$ and terminated by $V_{\rm RESET}$. $V_{\rm SET}$ is the output of CMP and reflects the output voltage situation. On the other hand, $V_{\rm SET}$ can switch on-time operation into off-time operation. The $T_{\rm ON}$ in steady state charges the inductor and, in turn, I_L rises to a corresponding level. At the end of the switching cycle, I_L falls back to the value equal to the value of the beginning of $T_{\rm ON}$, and the CMP triggers $V_{\rm SET}$ again to start next switching cycle. As a result, the off-time ($T_{\rm OFF}$) and the switching period ($T_{\rm SW}$) are correspondingly determined.

B. Full Analysis of Switching Frequency Variation for On-Time Control

The switching frequency of buck converter in CCM can be expressed as follows:

$$f_{\rm SW} = D \cdot \frac{1}{T_{\rm ON}}. \tag{1}$$

Ideally, the slope of I_L is proportional to "$V_{\rm IN} - V_{\rm OUT}$" and "$-V_{\rm OUT}$" during on-time and off-time periods, respectively. The ideal duty ratio ($D_{\rm ideal}$) is equal to the ratio of $V_{\rm OUT}$ to $V_{\rm IN}$

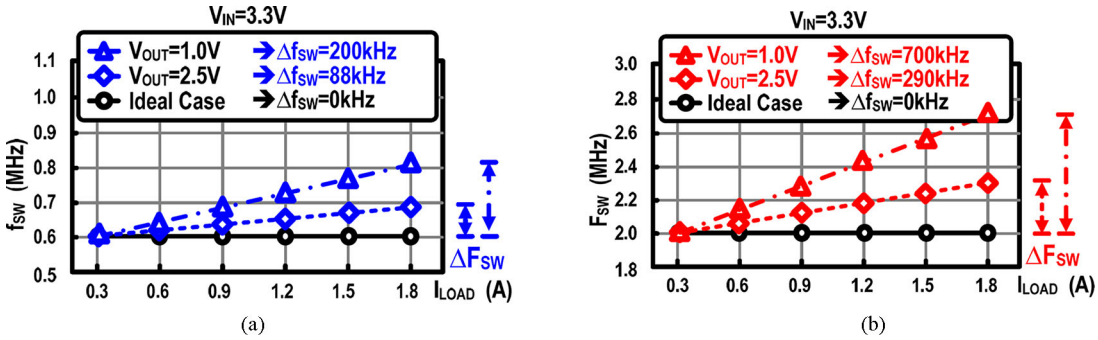

Fig. 3. Characteristic of $\Delta f_{\rm SW}$ and $I_{\rm LOAD}$ with conventional on-time control. (a) Target $f_{\rm SW} = 0.5$ MHz. (b) Target $f_{\rm SW} = 2$ MHz.

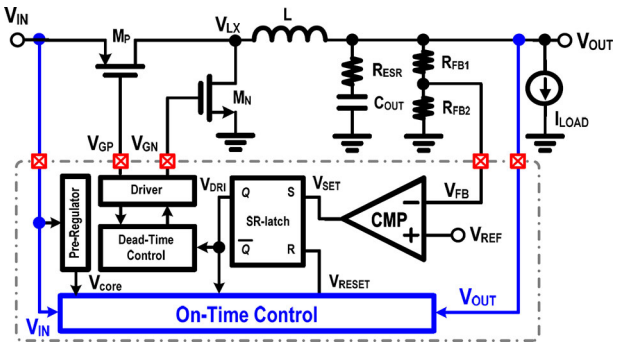

Fig. 4. Architecture of dc–dc buck converter with conventional RBOTC.

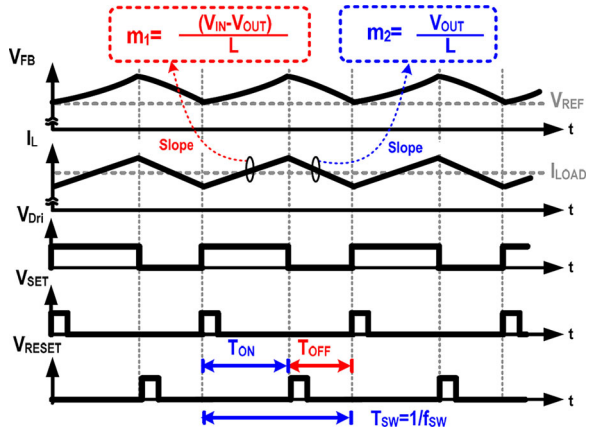

Fig. 5. Timing diagram of on-time-controlled buck converter.

in a lossless ideal case

$$D_{\rm ideal} = \frac{V_{\rm OUT}}{V_{\rm IN}}. \tag{2}$$

Similarly, the ideal on-time period $T_{\rm ON(ideal)}$ in conventional method should be proportional to $V_{\rm OUT}/V_{\rm IN}$ in (3) for keeping constant $f_{\rm SW}$

$$T_{\rm ON(ideal)} = \frac{V_{\rm OUT}}{V_{\rm IN}} \cdot T_{\rm SW} = D_{\rm ideal} \cdot T_{\rm SW} = \frac{D_{\rm ideal}}{f_{\rm SW}}. \tag{3}$$

Therefore, $f_{\rm SW}$ can be expressed as

$$f_{\rm SW} = D_{\rm ideal} \cdot \frac{1}{T_{\rm ON(ideal)}}. \tag{4}$$

On the other hand, (5) expresses the actual duty ratio $D_{\rm actual}$, which is defined as the ratio of the actual on-time period $T_{\rm ON(actual)}$ and $T_{\rm SW}$ in (6)

$$D_{\rm actual} = \frac{T_{\rm ON(actual)}}{T_{\rm SW}} = T_{\rm ON(actual)} \cdot f_{\rm SW} \tag{5}$$

where

$$T_{\rm SW} = T_{\rm ON(actual)} + T_{\rm OFF(actual)} \tag{6}$$

In practical, $D_{\rm actual}$ is larger than $D_{\rm ideal}$ because more energy is derived from the power source if taking all parasitic effects into consideration. Besides, $f_{\rm SW}$ is drastically perturbed by different $V_{\rm IN}$, $V_{\rm OUT}$, and loading current $I_{\rm Load}$ since $T_{\rm ON(ideal)}$ in (3) has no ability to compensate the change of $D_{\rm actual}$. To analyze completely the influence on $\Delta f_{\rm SW}$, parasitic resistances are included in Fig. 6(a). The parasitic resistances include $R_{\rm DCR}$ of inductor and on-resistances $R_{{\rm on},P}$ and $R_{{\rm on},N}$ of power MOSFETs M_P and M_N, respectively. Fig. 6(b) shows the complex model of power stage in a practical buck converter by considering parasitic resistances. Fig. 6(c) and (d) illustrates the energy-delivering paths, path I and path II, during $T_{\rm ON}$ and $T_{\rm OFF}$, respectively. Parasitic resistances cause the voltage drops, $V_{{\rm on},P}$, $V_{{\rm on},N}$, and $V_{\rm DCR}$, dependent of $I_{\rm LOAD}$.

Fig. 7 illustrates the frequency variation caused by parasitic resistances. $V_{{\rm on},P}$, $V_{{\rm on},N}$, and $V_{\rm DCR}$ lead the voltage variation across the inductor L. The waveform shows the voltage of nodes V_{LX1} and V_{LX2}, affect the cross voltage of $L_{\rm ideal}$, and subsequently causes gradual steep rising and falling slopes with extra term, "$-(V_{{\rm on},P} + V_{\rm DCR})$" and "$V_{{\rm on},N} + V_{\rm DCR}$", respectively. In other words, the cross voltage of inductor is decreased and increased as I_L flow through path I and path II, respectively. The voltages of V_{LX1} and V_{LX2} in the cases with and without considering parasitic resistance effect are listed in Table II. That is, even $V_{\rm IN}$ and $V_{\rm OUT}$ are not changed, the constant $T_{\rm ON}$ at different load conditions results in the frequency variation because different slope of I_L occurs at different load conditions.

According to voltage–second balance in steady state, (7) and (8) are obtained by assuming that I_L raises and falls linearly during $T_{\rm ON}$ and $T_{\rm OFF}$, respectively, where ΔI_L is the

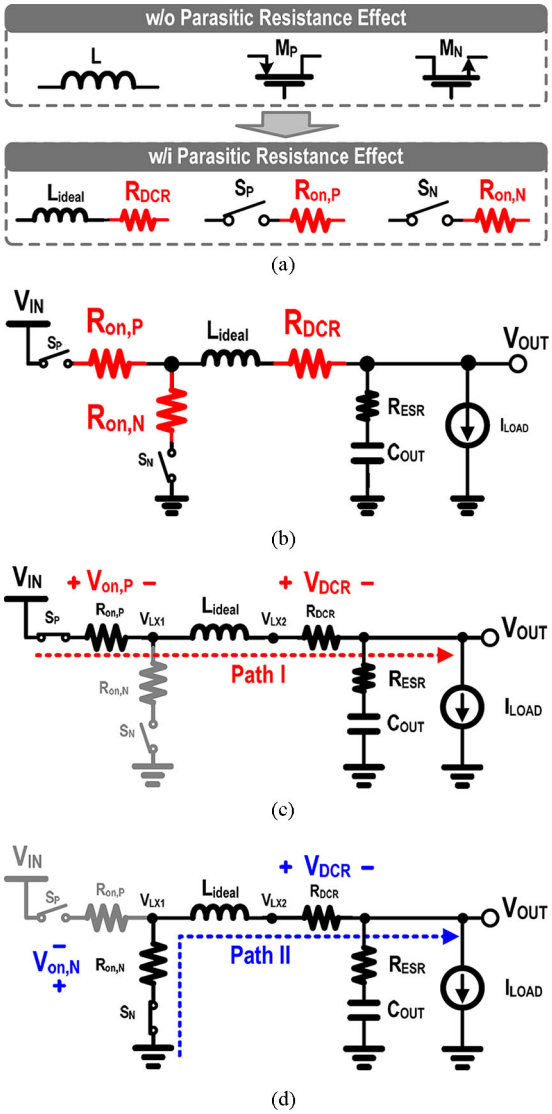

Fig. 6. (a) Consideration of parasitic resistance. (b) The power stage of buck converter by considering the parasitic resistance. (c) Energy-delivering path during T_{ON}. (d) Energy-delivering path during T_{OFF}.

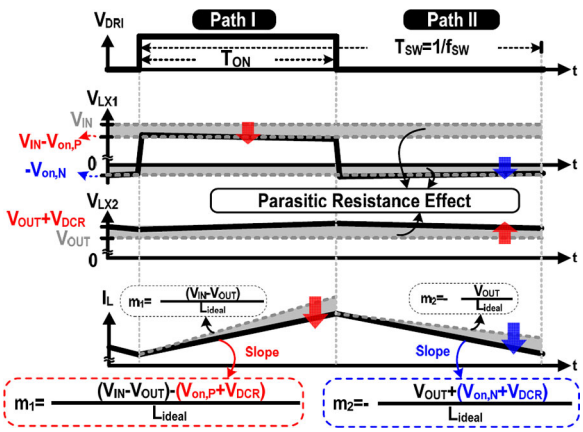

Fig. 7. Influence of parasitic resistances on V_{LX1}, V_{LX2}, and I_L slope.

TABLE II
VOLTAGE ACROSS THE INDUCTOR W/I AND W/O CONSIDERING PARASITIC RESISTANCES

	Idea Case w/o parasitic resistance effect		Actual Case w/i parasitic resistance effect	
	V_{LX1}	V_{LX2}	V_{LX1}	V_{LX2}
Path I	V_{IN}	V_{OUT}	$V_{\mathrm{IN}} - V_{\mathrm{on},P}$	$V_{\mathrm{OUT}} + V_{\mathrm{DCR}}$
Path II	0	V_{OUT}	$-V_{\mathrm{on},N}$	$V_{\mathrm{OUT}} + V_{\mathrm{DCR}}$

peak-to-peak ripple current of I_L

$$[(V_{\mathrm{IN}} - V_{\mathrm{OUT}}) - (V_{\mathrm{on},P} + V_{\mathrm{DCR}})] = L_{\mathrm{ideal}} \cdot \frac{\Delta I_L}{D \cdot T_{\mathrm{SW}}} \tag{7}$$

$$[V_{\mathrm{OUT}} + (V_{\mathrm{on},N} + V_{\mathrm{DCR}})] = L_{\mathrm{ideal}} \cdot \frac{\Delta I_L}{(1-D) \cdot T_{\mathrm{SW}}}. \tag{8}$$

The actual duty cycle in (9) can be derived from (7) and (8), respectively, during T_{ON} and T_{OFF}, respectively

$$\begin{aligned} D_{\mathrm{actual}} &= \frac{V_{\mathrm{OUT}} + (R_{\mathrm{on},N} + R_{\mathrm{DCR}}) \cdot I_{\mathrm{LOAD}}}{V_{\mathrm{IN}} - (R_{\mathrm{on},P} - R_{\mathrm{on},N}) \cdot I_{\mathrm{LOAD}}} \\ &= \frac{D_{\mathrm{ideal}} + ((R_{\mathrm{on},N} + R_{\mathrm{DCR}}) \cdot I_{\mathrm{LOAD}})/V_{\mathrm{IN}}}{1 - ((R_{\mathrm{on},P} - R_{\mathrm{on},N}) \cdot I_{\mathrm{LOAD}})/V_{\mathrm{IN}}}. \end{aligned} \tag{9}$$

By substituting (9) into (1), the switching frequency in practical is derived as

$$f_{\mathrm{SW}} = \frac{D_{\mathrm{ideal}} + ((R_{\mathrm{on},N} + R_{\mathrm{DCR}}) \cdot I_{\mathrm{LOAD}})/V_{\mathrm{IN}}}{1 - ((R_{\mathrm{on},P} - R_{\mathrm{on},N}) \cdot I_{\mathrm{LOAD}})/V_{\mathrm{IN}}} \cdot \frac{1}{T_{\mathrm{ON(actual)}}}. \tag{10}$$

Comparison of (4) and (10) reveals that the switching frequency depends on several parasitic factors. Fig. 8 provides four cases to depict Δf_{SW} at different V_{OUT}, V_{IN}, and I_{LOAD}, according to (10). The desired f_{SW} is 800 kHz in case (a) and case (b), and the desired f_{SW} is 2.5 MHz in case (c) and case (d). In all of these cases, the change in I_{LOAD} results in more significant Δf_{SW} when V_{OUT} is at lower values. In comparison of case (a) with case (b), Δf_{SW} in case (b) is worse because of serious parasitic effect. Similar result is also shown in case (c) and case (d). Besides, by comparing the desired f_{SW} of 800 kHz with 2.5 MHz, the case with a higher desired f_{SW} suffers from worse Δf_{SW} in case of load change from 0.3 to 1.7 A. Fig. 9 depicts Δf_{SW} with certain load changes versus the desired f_{SW} and V_{OUT}. This characteristic can be also got by (10). Considering that V_{OUT}, V_{IN}, and parasitic resistances remain constant, $\Delta D_{\mathrm{actual}}$ with certain load change remains constant. However, higher desired f_{SW} represents shorter $T_{\mathrm{ON(actual)}}$, and Δf_{SW} is amplified from D_{actual} by a larger value of $1/T_{\mathrm{ON(actual)}}$.

In conclusion, Δf_{SW} should not be neglected. Conventional $T_{\mathrm{ON(ideal)}}$ in (3) has no ability to compensate the variation of D_{actual} in (10). Furthermore, (10) also reveals that designing a proper T_{ON} to compensate completely parasitic effects is the challenge for on-time control if keeping a constant f_{SW}.

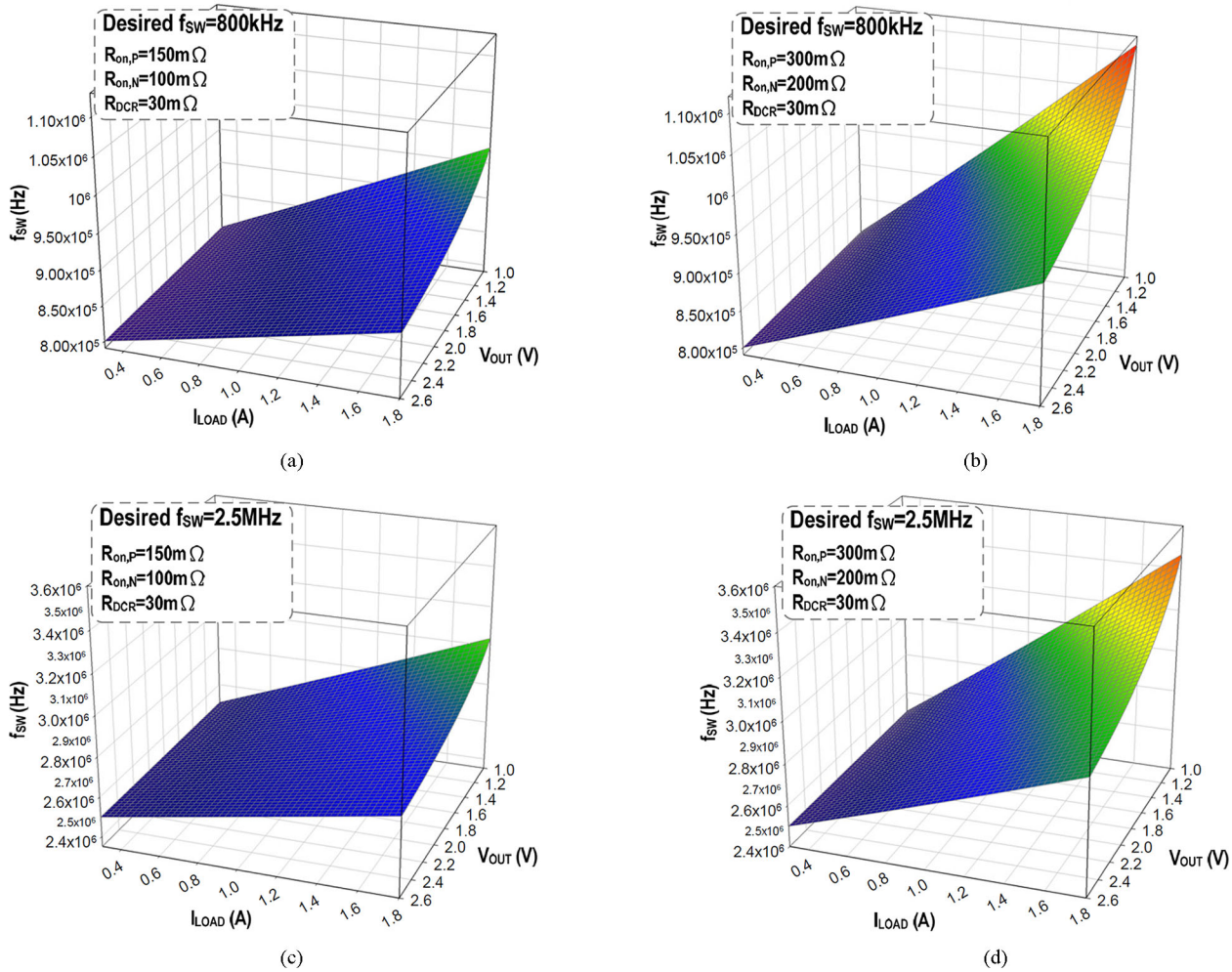

Fig. 8. Relationship between $f_{\rm SW}$, $I_{\rm LOAD}$, and $V_{\rm OUT}$ when $V_{\rm IN} = 3.3$ V. (a) The desired $f_{\rm SW}$ is 800 kHz. $R_{{\rm on},P} = 150$ mΩ, $R_{{\rm on},N} = 100$ mΩ, and $R_{\rm DCR} = 30$ mΩ. (b) The desired $f_{\rm SW}$ is 800 kHz. $R_{{\rm on},P} = 300$ mΩ, $R_{{\rm on},N} = 200$ mΩ, and $R_{\rm DCR} = 30$ mΩ. (c) The desired $f_{\rm SW}$ is 2.5 MHz. $R_{{\rm on},P} = 150$ mΩ, $R_{{\rm on},N} = 100$ mΩ, and $R_{\rm DCR} = 30$ mΩ. (d) The desired $f_{\rm SW}$ is 2.5 MHz. $R_{{\rm on},P} = 300$ mΩ, $R_{{\rm on},N} = 200$ mΩ, and $R_{\rm DCR} = 30$ mΩ.

C. Proposed Algorithm for an Adaptive On Time

To compensate completely $\Delta f_{\rm SW}$ by the proposed approach, (11) is derived by rearranging (7) and (8)

$$\begin{aligned} V_{\rm IN} D_{\rm actual} = {} & V_{\rm OUT} + D_{\rm actual} \cdot (R_{{\rm on},P} \cdot I_{\rm LOAD}) \\ & + (1 - D_{\rm actual}) \cdot (R_{{\rm on},N} \cdot I_{\rm LOAD}) \\ & + R_{\rm DCR} \cdot I_{\rm LOAD}. \end{aligned} \tag{11}$$

An equivalent output voltage $V_{\rm OUT\_eq}$ is defined in (12) where $\Delta V_{\rm par}$ in (13) represents the voltage variation when parasitic effects are taken into consideration. Parasitic effects refer to the series parasitic equivalent resistance $R_{\rm par}$ as is expressed in

$$V_{\rm OUT\_eq} = V_{\rm OUT} + \Delta V_{\rm par} \tag{12}$$

where

$$\begin{aligned} \Delta V_{\rm par} = {} & R_{\rm par} \cdot I_{\rm LOAD} \quad \text{and} \quad R_{\rm par} = D_{\rm actual} \cdot R_{{\rm on},P} \\ & + (1 - D_{\rm actual}) \cdot R_{{\rm on},N} + R_{\rm DCR}. \end{aligned} \tag{13}$$

Here $V_{\rm OUT\_eq}$ is therefore expressed by $D_{\rm actual}$ as

$$V_{\rm OUT\_eq} = D_{\rm actual} \cdot V_{\rm IN}. \tag{14}$$

The average model for power stage of buck converter is illustrated in Fig. 10. All the parasitic resistances are taken into consideration. Consequently, instead of using $V_{\rm OUT}$ in conventional design, $V_{\rm OUT\_eq}$ can be synthesized by the proposed PCT. This paper utilizes $V_{\rm IN}$ and $V_{\rm OUT\_eq}$ to generate an optimum $T_{\rm ON}$ according to (1) and (14). The solution for effectively alleviating $\Delta f_{\rm SW}$ can be realized at different $V_{\rm IN}$, $V_{\rm OUT}$, and $I_{\rm LOAD}$ conditions.

III. Proposed Adaptive On-Time Buck Converter with Predicting Correction Technique

The proposed architecture is shown in Fig. 11 where the PCT includes a fully linear voltage-to-current generator (FLVCG), an equivalent output-voltage synthesizer (EOVS), an on-time modulator (OTM), and a voltage clamper.

Without the need of $V_{\rm OUT}$, $V_{\rm IN}$, V_{LX}, and the sensing signals, only $V_{\rm GP}$ is needed for proposed PCT circuit to achieve a pseudo-constant $f_{\rm SW}$. Basing on (1), the optimum $T_{\rm ON}$ must

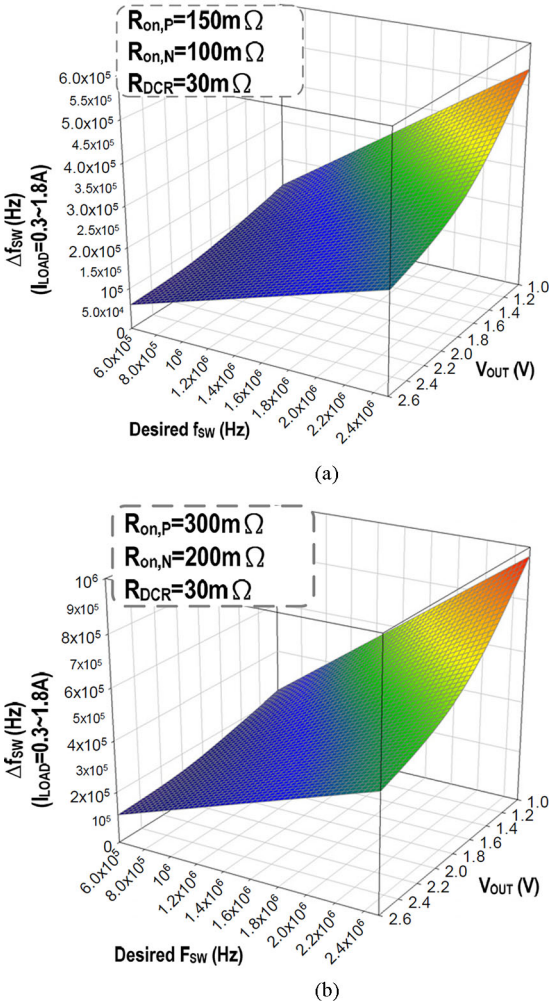

Fig. 9. Variation of $f_{\rm SW}$ in case of load change from 0.3 to 1.8 A versus different desired $f_{\rm SW}$ and $V_{\rm OUT}$ when (a) $R_{{\rm on},P} = 150$ mΩ, $R_{{\rm on},N} = 100$ mΩ, and $R_{\rm DCR} = 30$ mΩ and when (b) $R_{{\rm on},P} = 300$ mΩ, $R_{{\rm on},N} = 200$ mΩ, and $R_{\rm DCR} = 30$ mΩ.

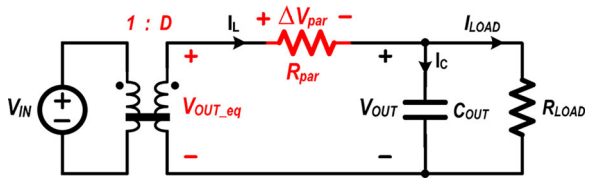

Fig. 10. Average model for power stage of buck converter when all parasitic resistances are taken into consideration.

be the value proportional to $D_{\rm actual}$. Although $D_{\rm actual}$ in (9) is determined by many factors, the proposed PCT circuit can use $V_{\rm IN}$ and $V_{\rm GP}$ to generate optimum $T_{\rm ON}$ to compensate $D_{\rm actual}$. According to (14), the FLVCG converts $V_{\rm IN}$ to the current ($i_{\rm ON}$), which is linear to $V_{\rm IN}$. The EOVS modulates the equivalent output voltage ($V_{\rm OUT\_eq}$) by $V_{\rm IN}$ and the driving signal $V_{\rm GP}$. The OTM then determines $T_{\rm ON}$ by $i_{\rm ON}$ and $V_{\rm OUT\_eq}$.

When $V_{\rm OUT\_eq}$ is directly realized by (12) and (13), the complex current sensing circuit is needed because $V_{\rm OUT\_eq}$ includes many parasitic on resistances. To reduce the complexity, $V_{\rm OUT\_eq}$ is synthesized by $V_{\rm IN}$ and $V_{\rm GP}$ according to (14). Consequently, $T_{\rm ON}$ is expressed as (15) to achieve a pseudo-constant $f_{\rm SW}$

$$T_{\rm ON} = \frac{V_{\rm OUT\_eq}}{V_{\rm IN}} \cdot T_{\rm SW} = \frac{D_{\rm actual} \cdot V_{\rm IN}}{V_{\rm IN}} \cdot T_{\rm SW} = \frac{D_{\rm actual}}{f_{\rm SW}}. \tag{15}$$

In comparison of the fixed $T_{\rm ON}$ and with the proposed optimum $T_{\rm ON}$, Fig. 12 explains that variable $D_{\rm actual}$ at different load conditions has some effects on $\Delta f_{\rm SW}$. $m_{1,L}$ and $m_{2,L}$ are raising slope and falling slope at light loads, respectively. $m_{1,H}$ and $m_{2,H}$ are rising slope and falling slopes at heavy loads, respectively. Increasing $I_{\rm LOAD}$ causes $m_{1,H}$ smaller than $m_{1,L}$ and $m_{2,H}$ larger than $m_{2,L}$. As a result, at heavier load conditions, $T_{\rm ON}$is required to increase adequately to keep f_{SW} constant at heavier load conditions owing to the expanding duty ratio, and vice versa.

Fig. 13 illustrates that the PCT can modulate the adequate $V_{\rm OUT\_eq}$ and $T_{\rm ON}$. Different load conditions reflect the corresponding $D_{\rm acutal}$ with certain $V_{\rm OUT}$ and $V_{\rm IN}$ because of parasitic resistance effects. This figure includes three cases with

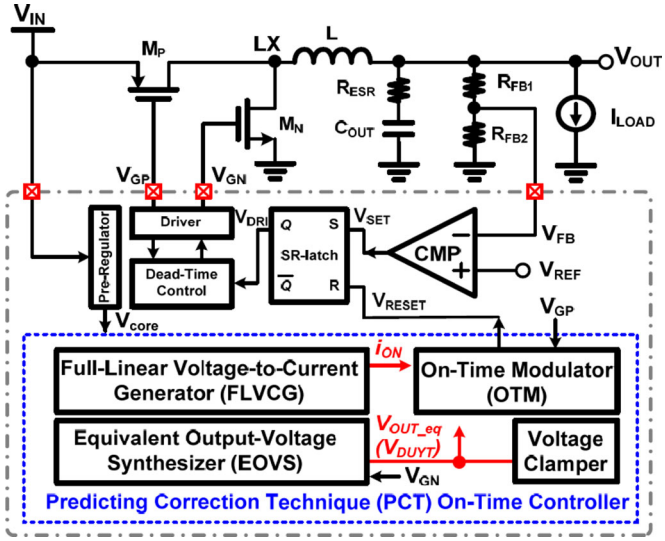

Fig. 11. Proposed architecture of dc–dc buck converter with the PCT.

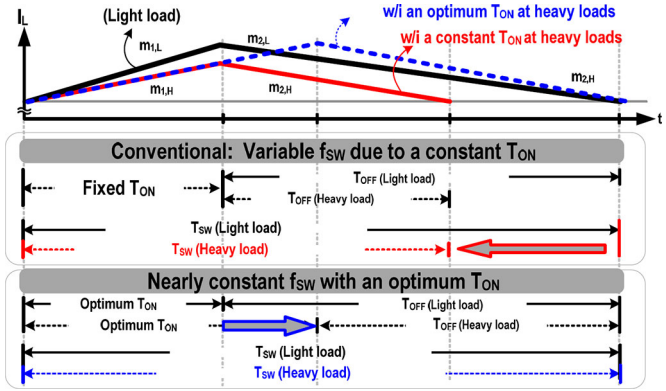

Fig. 12. Variable $f_{\rm SW}$ with fixed $T_{\rm ON}$ and fixed $f_{\rm SW}$ with optimum $T_{\rm ON}$ at different load current.

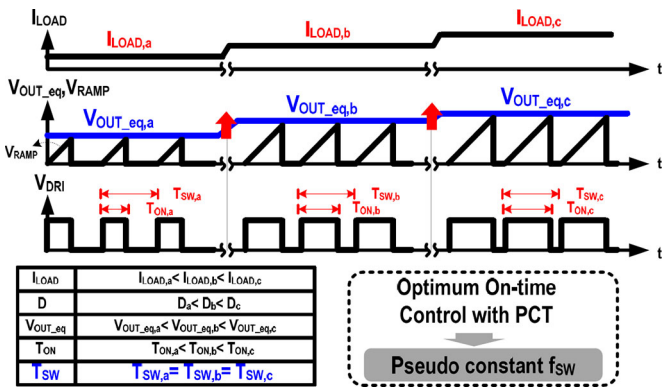

Fig. 13. Operation of the proposed on-time control with the PCT.

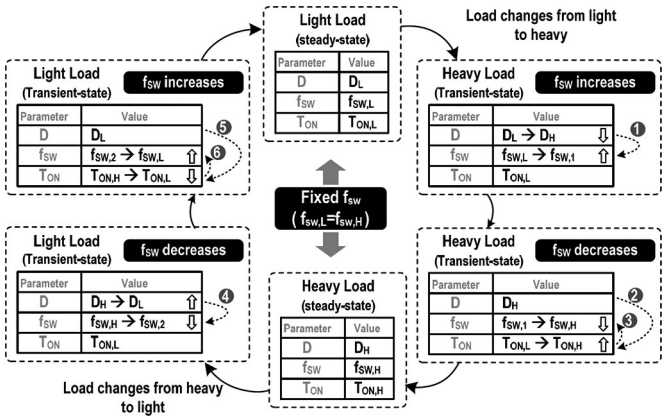

Fig. 14. Operation of the on-time control with the PCT.

the load conditions, $I_{\mathrm{LOAD},a}$, $I_{\mathrm{LOAD},b}$, and $I_{\mathrm{LOAD},c}$, where $I_{\mathrm{LOAD},a} < I_{\mathrm{LOAD},b} < I_{\mathrm{LOAD},c}$. Larger I_{LOAD} makes the duty ratio expanded as shown in (9). In turn, the PCT predicts and generates the higher $V_{\mathrm{OUT\_eq}}$ to generate a longer T_{ON}. Contrarily, lower $V_{\mathrm{OUT\_eq}}$ generates shorter T_{ON} when D_{acutal} shrinks at smaller I_{LOAD}.

Fig. 14 explains how to recover the constant f_{SW} during the load transient. In light-load steady state, the values of D, f_{SW}, and T_{ON} are D_L, $f_{\mathrm{SW},L}$, and $T_{\mathrm{ON},L}$, respectively. In heavy-load steady state, the values of D, f_{SW}, and T_{ON} are D_H, $f_{\mathrm{SW},H}$, and $T_{\mathrm{ON},H}$, respectively. In comparison of light load and heavy load, the expected result is to achieve that $f_{\mathrm{SW},L}$ is equal to $f_{\mathrm{SW},H}$ for getting a constant switching frequency. Now, observe the change of D, f_{SW}, and T_{ON} if using a light-to-heavy load transient as an example. When load current changes from light to heavy, f_{SW} increases temporarily, that is, f_{SW1} is larger than $f_{\mathrm{SW},L}$, because D decreases, that is, D_H is less than D_L, and T_{ON} is not changed yet. Meanwhile, the PCT circuit adjusts T_{ON} for getting a larger value, that is, $T_{\mathrm{ON},H}$ is larger than $T_{\mathrm{ON},L}$ according to the increasing duty D_H. As a result, the shorter T_{ON} can modify f_{sw} back to $f_{\mathrm{SW},H}$ from the increasing value $f_{\mathrm{SW},1}$, where $f_{\mathrm{SW},1}$ is larger than $f_{\mathrm{SW},H}$. Finally, the system enters into heavy-load steady state. According to (5) and (14), T_{ON} adjusted by PCT circuit can achieve that $f_{\mathrm{SW},L}$ is equal to $f_{\mathrm{SW},H}$. In contrast, the procedure is similar even when the load current changes from heavy to light.

Besides, the voltage level of $V_{\mathrm{OUT\_eq}}$ would be very high or low during the start-up period, extremely load transient or DCM operation occurs because $V_{\mathrm{OUT\_eq}}$ is synthesized by V_{GP}. According to (12) and (13), this range of the window is designed to tolerate $V_{\mathrm{OUT\_eq}}$. Consequently, the voltage clamper in Fig. 11 is used to ensure the voltage level of $V_{\mathrm{OUT\_eq}}$ within the adequate range.

Consequently, the proposed technique achieves pseudo-constant f_{SW} in CCM. The on-time period is adjusted to a small value when the decreasing loading current results in D_{actual} becoming larger. In DCM, the proposed voltage clamper can limit the minimum on-time period so that the inherent advantage of reducing f_{SW} can be maintained for high efficiency.

IV. Circuit Implantation of Proposed PCT

This paper proposed two types of PCT circuit, and the structures are illustrated in Fig. 15. The type-I PCT realize the circuit implementation directly based on the analysis in Section II and (15). Besides, the type-II PCT removes the matching requirement in type-I PCT so that the performance can be further improved.

A. Type-I PCT With $V_{\mathrm{OUT\_eq}}$

The proposed PCT includes the FLVCG, the EOVS, and the OTM. Fig. 16(a) shows that the FLVCG implemented by low-voltage core devices is supplied by V_{CORE}. Although V_{IN} is higher beyond the voltage level for core devices, the structure of resistor R_1 and diode-connected MOSFET M_1 benefits the avoidance of using high-voltage MOSFET. i_1 and i_2 are generated by V_{IN} as shown in (16), but i_1 is not completely linear to V_{IN} because of the term $V_{GS,M1}$, which represents the gate-to-source voltage of MOSFET M_1

$$i_1 = \frac{1}{2} i_2 = \frac{V_{\mathrm{IN}} - V_{GS,M1}}{R_1}. \tag{16}$$

To compensate the unexpected term $V_{GS,M1}$, M_5 forms the source-generation structure to generate compensated current i_3 as expressed in (17). $V_{GS,M1}$ and $V_{GS,M5}$ can be nearly equal by setting M_1 and M_5 with the same aspect ratio and removing the body effect. In turn, i_3 is composed of $V_{GS,M5}$ and derived in (18)

$$i_3 = \frac{V_1 - V_{GS,M5}}{R_3} = \frac{i_1 R_2 - V_{GS,M5}}{R_3} \tag{17}$$

$$i_3 = \frac{R_2 V_{\mathrm{IN}} - (R_1 + R_2) V_{GS,M1}}{R_1 R_3}. \tag{18}$$

By conducting i_2 and i_3 into the node by opposite directions, i_{ON} is generated as shown

$$\begin{aligned} i_{\mathrm{ON}} &= i_2 - i_3 \\ &= \frac{(2R_3 - R_2)\, V_{\mathrm{IN}} + (R_1 + R_2 - 2R_3)\, V_{GS,M1}}{R_1 R_3}. \end{aligned} \tag{19}$$

With equal value of $2R_1$, $2R_2$, and R_3, the current i_{ON} is in turn obtained as shown in (20). Consequently, i_{ON} is converted from V_{IN} by FLVCG and i_{ON} is proportional to V_{IN}. Current i_{ON} then is used to charge into C_{ON} so that V_{RAMP} is raising

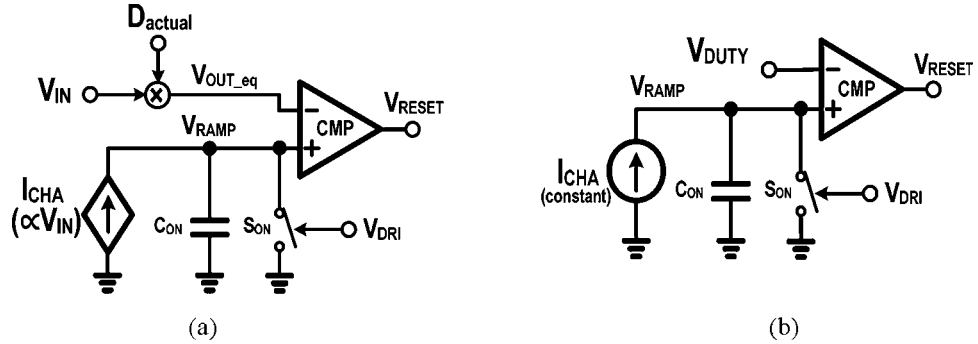

Fig. 15. Structure of (a) type-I PCT with $V_{\mathrm{OUT\_eq}}$ and (b) type-II PCT with V_{DUTY}.

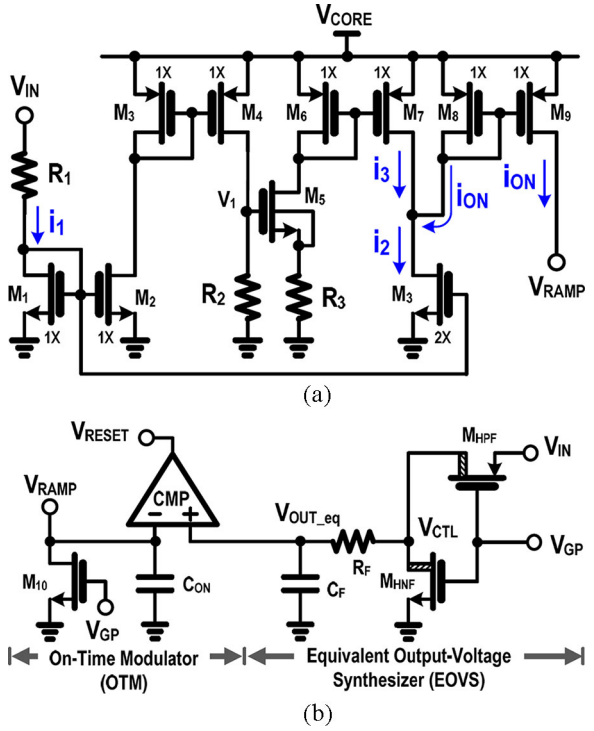

Fig. 16. Implementation of type-I PCT circuit, including the (a) FLVCG and (b) OTM and EOVS.

voltage and the raising rate is proportional to V_{IN}

$$i_{\mathrm{ON}} = \frac{3}{2}\frac{V_{\mathrm{IN}}}{R_1}. \tag{20}$$

In contrast, Fig. 16(b) shows implementation of proposed EOVS and OTM. All devices are implanted by low-voltage except that M_{HPF} and M_{HNF} are the high-voltage MOSFETs because of V_{IN} and V_{GP}. The right portion is EOVS and is structured by M_{HPF}, M_{HNF}, R_F, and C_F. The signals V_{IN} and V_{GP} control EOVS to produce $V_{\mathrm{OUT\_eq}}$. Signal $V_{\mathrm{OUT\_eq}}$ can be express as shown in (21), because V_{GP} is driving signal to control high-side power MOSFET M_P, and the duty of V_{GP} is equal to the ration of T_{ON} and T_{SW}

$$V_{\mathrm{OUT\_eq}} = V_{\mathrm{IN}} \cdot D_{\mathrm{actual}}. \tag{21}$$

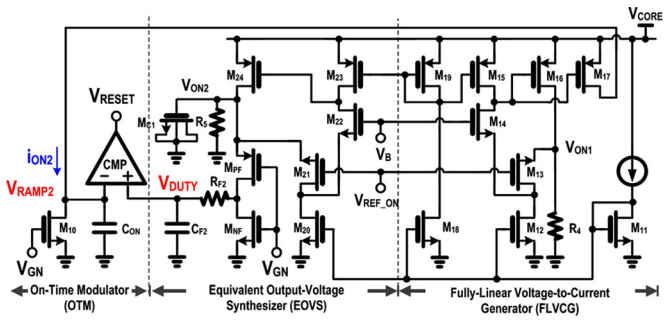

Fig. 17. Implementation of type-II PCT circuit, including the OTM, the EOVS, and the FLVCG.

By comparing V_{RAMP} and $V_{\mathrm{OUT\_eq}}$, T_{ON} can be determined by OTM according to the duration when V_{RAMP} is below than $V_{\mathrm{OUT\_eq}}$. Consequently, T_{ON} can be proportional to D_{actual}, which is derived as in (22) by $V_{\mathrm{OUT\_eq}}$, C_{ON}, and i_{ON}

$$\begin{aligned} T_{\mathrm{ON}} &= \frac{C_{\mathrm{ON}} \cdot V_{\mathrm{OUT\_eq}}}{i_{\mathrm{ON}}} = \frac{2}{3} C_{\mathrm{ON}} \cdot R_1 \cdot \frac{V_{\mathrm{IN}} \cdot D_{\mathrm{actual}}}{V_{\mathrm{IN}}} \\ &\propto D_{\mathrm{actual}}. \end{aligned} \tag{22}$$

Substituting (22) into (1), T_{SW} is thoroughly constant by the independence of V_{IN}, V_{OUT}, D_{actual}, I_{LOAD}, and parasitic resistances. Besides, the ripple of $V_{\mathrm{OUT\_eq}}$ can be derived approximately in (23). To ensure this ripple is small enough, C_F is 1 pF and R_F is 5 MΩ when V_{IN} is 3.3 V, V_{OUT} is 1.05 V, and f_{SW} is 2.5 MHz in this paper

$$V_{\mathrm{OUT\_eq,pp}} = T_{\mathrm{ON}} \cdot \frac{V_{\mathrm{IN}}}{R_F \cdot C_F}. \tag{23}$$

B. Type-II PCT With V_{DUTY}

In addition, Fig. 17 provides another circuit implementation to realize the optimum T_{ON}. The complexity of the new FLVCG can be reduced, and the new EOVS can remove the necessary of using high-voltage MOSFETs. Furthermore, only one control signal V_{GP} is needed. $V_{\mathrm{REF\_ON}}$ is a reference voltage with a constant value, and V_B is a voltage to bias M_{22} and M_{14}. In the FLVCG of the right portion, M_{13} is the voltage follower to determine V_{ON1} from $V_{\mathrm{REF\_ON}}$. The R_4 and M_{13}–M_{17} structured by negative feedback then determine the current of M_{17}

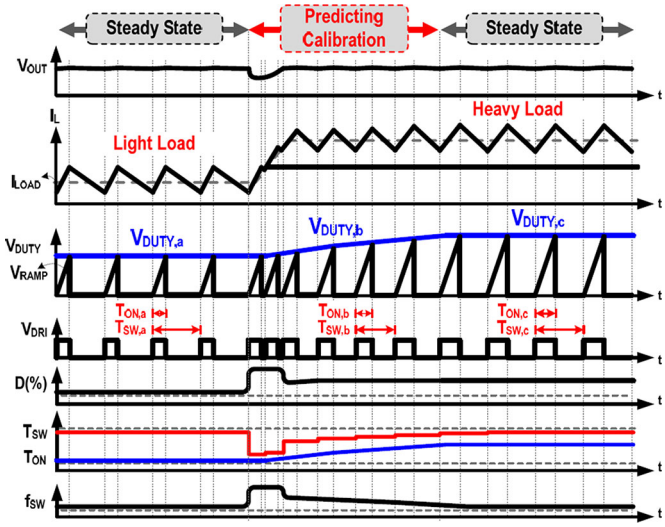

Fig. 18. Timing diagram of the PCT technique shows a nearly constant switching frequency in steady state.

as given in

$$i_{\mathrm{ON}} = \frac{V_{\mathrm{REF\_ON}} + V_{GS,M13}}{R_4}. \tag{24}$$

In the EOVS of the middle portion, M_{21} is the voltage follower to determine V_{ON2} from $V_{\mathrm{REF\_ON}}$. The MOSFETs M_{21}–M_{24}, structured by negative feedback, then provide the driving capability to regulate V_{ON2} as shown

$$V_{\mathrm{ON2}} = V_{\mathrm{REF\_ON}} + V_{GS,M21}. \tag{25}$$

Here, R_5 and M_{C1} are used to bias M_{24} and to assist the regulation, respectively. V_{GP} then utilizes M_{PF}, M_{NF}, R_{F2}, and C_{F2} to generate V_{DUTY} as shown

$$V_{\mathrm{DUTY}} = V_{\mathrm{ON2}} \cdot D_{\mathrm{actual}}. \tag{26}$$

Consequently, the OTM in the left portion can use V_{DUTY} and i_{ON2} to determine T_{ON} as derived in (27). That is, the optimum T_{ON} proportional to D_{actual} can be obtained because $V_{\mathrm{RER\_ON}}$, V_{GS21}, V_{GS13}, and C_{ON} are constant

$$T_{\mathrm{ON}} = \frac{C_{\mathrm{ON}} \cdot V_{\mathrm{DUTY}}}{i_{\mathrm{ON2}}} = C_{\mathrm{ON}} \cdot \frac{(V_{\mathrm{REF\_ON}} + V_{GS21}) \cdot D_{\mathrm{actual}}}{(V_{\mathrm{REF\_ON}} + V_{GS13}) \cdot (1/R_4)} \propto D_{\mathrm{actual}}. \tag{27}$$

Fig. 18 illustrates the timing diagram of the PCT circuit in case of any load current change. At light loads, the EOVS circuit modulates V_{DUTY} as $V_{\mathrm{DUTY},a}$ and T_{ON} as $T_{\mathrm{ON},a}$. When the load current changes from light to heavy, T_{SW} decreases because T_{ON} is too short to provide adequate energy to handle heavy-load condition. In this period, the switching frequency is not constant temperately. Instantly, the PCT circuit processes the predicting calibration to adjust adaptively T_{ON}. According to V_{IN} and a larger D_{actual} value that reflects the information of parasitic effects and loading condition, the EOVS circuit can get a large V_{DUTY} corresponding to an optimum value $V_{\mathrm{DUTY},c}$. Subsequently, T_{ON} is expanded by the OTM circuit to increase effective value of T_{SW}. That is, f_{SW} is regulated back to its value equivalently equal to that at light loads. Finally, f_{SW} is nearly constant without being affected by any disturbances.

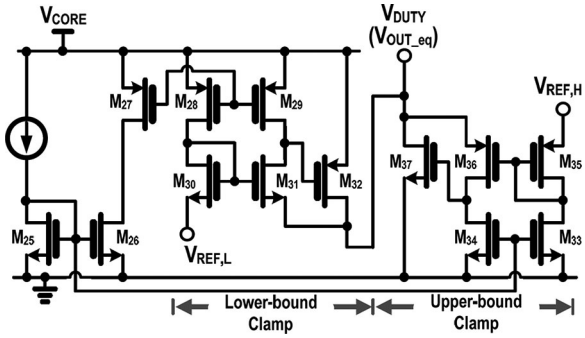

Fig. 19. Voltage clamper.

Fig. 19 shows the voltage clamper including lower bound clamp and upper bound clamp. When $V_{\mathrm{OUT\_eq}}$ is lower than the lower bound voltage $V_{\mathrm{REF},L}$, M_{30} and M_{31} can drive M_{32} to clamp $V_{\mathrm{OUT\_eq}}$ at the voltage level of $V_{\mathrm{REF}L}$. On the other hand, when $V_{\mathrm{OUT\_eq}}$ is higher than the upper-bound voltage $V_{\mathrm{REF},H}$, M_{35} and M_{36} can drive M_{37} to clamp $V_{\mathrm{OUT\_eq}}$ at the voltage level of $V_{\mathrm{REF},H}$. That is, the swing range of $V_{\mathrm{OUT\_eq}}$ can be ensured in the window between $V_{\mathrm{REF},L}$ and $V_{\mathrm{REF}H}$. Besides, the MOSFETs M_{31}, M_{32}, M_{36}, and M_{37} can be off and make no influence on $V_{\mathrm{OUT\_eq}}$ when $V_{\mathrm{OUT\_eq}}$ is in the window. Table III concludes the characteristic of various on-time controllers. The type II only needs the controlling voltage V_{GP} and supplying voltage V_{CORE}. The parameters of $\Delta f_{\mathrm{SW}}/\Delta V_{\mathrm{IN}}$, $\Delta f_{\mathrm{SW}}/V_{\mathrm{OUT}}$, and $\Delta f_{\mathrm{SW}}/\Delta I_{\mathrm{LOAD}}$ represent the frequency variation influenced by different V_{IN}, V_{OUT}, and I_{LOAD}, respectively. The fixed T_{ON} has no ability to compensate any variation. The adaptive T_{ON} in both [8] and [10] try to compensate D_{ideal}, but the performance is limited. Even though the adaptive T_{ON} in [10] further utilizes V_{LX} to obtain load information, the information of parasitic effects are still not complete. The proposed optimum T_{ON}, which is implemented by type I and type II, compensates D_{actaul} so that the information of parasitic effects can be obtained and the frequency variation can be compensated with excellent performances. Besides, the proposed optimum T_{ON} implemented by type II reduces the needed information of V_{OUT} and V_{IN}. Type-II PCT can release the strict design considerations, which include the matching design of resistor and current mirror, high linearity between V_{IN} and charging current, and the usage of high-voltage devices.

V. Experimental Results

The proposed on-time control with type-II PCT was fabricated by UMC 28 nm CMOS technology. The specifications include $V_{\mathrm{IN}} = 3.3$ V, $V_{\mathrm{OUT}} = 1.05$ V, $L = 1$ μH, $C_{\mathrm{OUT}} = 4.7$ μF, and $f_{\mathrm{SW}} = 2.5$ MHz. In measured results, $R_{\mathrm{on},P}$ and $R_{\mathrm{on},N}$ are 300 and 200 mΩ, respectively. R_{DCR} of the inductor is 30 mΩ. Fig. 20 shows the waveforms of conventional on-time controller when I_{LOAD} changes from 1.7 to 0.3 A and vice versa. The on-time period keeps constant at different load conditions in conventional design. However, the slope of I_L and D_{actual} change obviously due to the parasitic effects. The f_{SW} is 2.5 and 3.4 MHz when I_{LOAD} is 0.3 and 1.7 A, respectively.

TABLE III
COMPARISON OF DIFFERENT ON-TIME CONTROLLER

	Fixed T_{ON}	Basic Adaptive T_{ON} [8]	Adaptive T_{ON} with V_{LX} [10]	Proposed optimum T_{ON} [type-I]	Proposed optimum T_{ON} [type-II]
Needed information	V_{GP}	V_{IN} V_{OUT} V_{GP}	V_{LX} V_{OUT} V_{GP}	V_{IN} V_{OUT} V_{GP}	V_{GP}
Design issue		• Matching issue should be designed carefully. • Charging current is necessary fully linear to V_{IN}. • High-voltage devices are needed because of the usage of V_{IN}.			
$\Delta f_{SW}/\Delta V_{IN}$	Poor	Good	Good	Excellent	Excellent
$\Delta f_{SW}/V_{OUT}$	Poor	Good	Good	Excellent	Excellent
$\Delta f_{SW}/\Delta I_{LOAD}$	Poor	Poor	Good	Excellent	Excellent

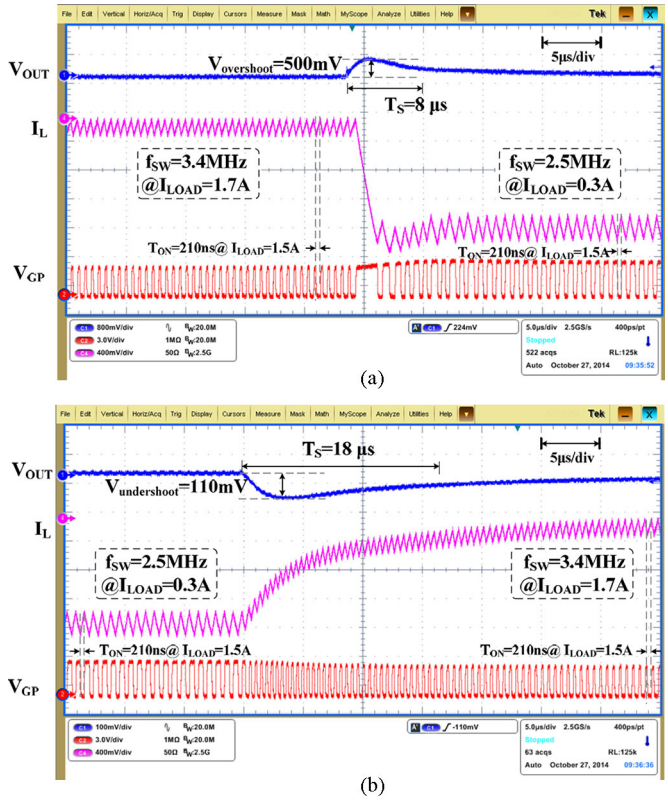

Fig. 20. Frequency variation in conventional COT controller when I_{LOAD} changes (a) from heavy to light load and (b) from light to heavy load.

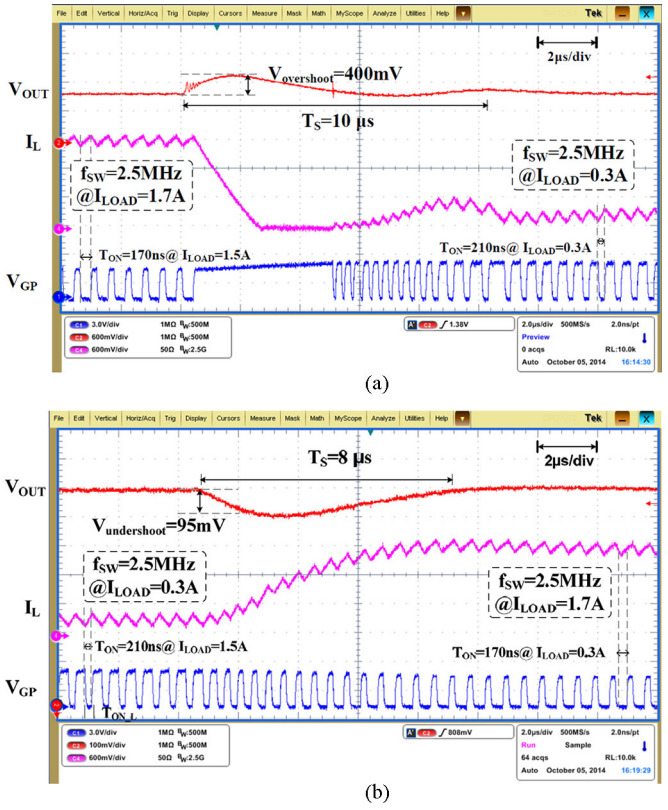

Fig. 21. Pseudo-constant frequency in proposed PCT controller when I_{LOAD} changes (a) from heavy to light load and (b) from light to heavy load.

The f_{SW} variation is approximately 0.9 MHz in case of 1.4 A change at I_{LOAD}. In contrast, Fig. 21 demonstrates the function of PCT. Fig. 22 provides its zoom-in waveforms in steady state. Although the slope of I_L and D_{actual} still change obviously at different load conditions due to the parasitic effects, f_{SW} maintains nearly constant at 2.5 MHz during adjustable on-time periods. T_{ON} is 170 ns and duty cycle is 0.35 at light loads while T_{ON} is adjusted to 210 ns and duty cycle is 0.52 at heavy loads. Δf_{SW} is approximately 8 kHz when the I_{LOAD} change is 1.4 A.

Table IV shows the comparison with prior arts. The performance of f_{SW} variation is indicated by $\Delta f_{\mathrm{SW}}/f_{\mathrm{SW}}$ and $\Delta f_{\mathrm{SW}}/\Delta I_{\mathrm{LOAD}}$. The designs in [14], [15], and [28] achieve good performance at $\Delta f_{\mathrm{SW}}/f_{\mathrm{SW}}$ and $\Delta f_{\mathrm{SW}}/\Delta I_{\mathrm{LOAD}}$, but the extra clock signal and complex PLL-based loop should be employed. Besides, the design in [20] reduces the complexity of controller, and the designs in [16] and [32] remove the need of extra clock signal and achieve adaptive on time but the performance of Δf_{SW} of these designs are withdrawn. Fig. 23 concludes the performance, which includes [16] and [32]. The design in [16] using current sense performs $\Delta f_{\mathrm{SW}}/f_{\mathrm{SW}}$ of 9.5% and $\Delta f_{\mathrm{SW}}/\Delta I_{\mathrm{LOAD}}$ of 129 kHz/A. The design in [32] utilizes the *RC* network but f_{SW} changes from 600 to 800 kHz when load changes from 200 to 900 mA, according to the measured transient waveforms. The $\Delta f_{\mathrm{SW}}/f_{\mathrm{SW}}$ is 25% and

TABLE IV
COMPARISON TABLE

	[28]	[15]	[14]	[16]	[20]	[32]	Conventional	Proposed
Control method	PLL-based	PLL-based	PLL-based	DADC	Load Sensing	SLCC	Constant on-time	PCT
V_{IN}	3 V	2.7–4.5 V	2.5 V	2.7–3.3 V	3.3 V	2.7–3.6	3.3 V	3.3 V
V_{OUT}	1.8 V	2 V	0.7–1.8 V	0.9–2.1 V	1.2 V	1–1.2	1.05 V	1.05 V
L	4.7 μH	4.7 μH	1–5 μH	2.2 μH	4.7 μH	N/A	1 μH	1 μH
C_{OUT}	4.7 μF	10 μF	10 μF	4.4 μF	8.9 μF	N/A	4.7 μF	4.7 μF
$R_{on,P}$, $R_{on,N}$, R_{DCR}	N/A	N/A	N/A	N/A	N/A	N/A	300 mΩ, 200 mΩ, 30 mΩ	300 mΩ, 200 mΩ, 30 mΩ
f_{SW}	1 MHz	1 MHz	1 MHz	3 MHz	750 kHz	800 kHz	2.5 MHz	2.5 MHz
Δf_{SW}	15 kHz	2 kHz	5 kHz	100 kHz	84 kHz	200 kHz	900 kHz	8 kHz
$\Delta f_{SW}/f_{SW}$	1.5%	0.2%	0.5%	3.3%	11.2%	25%	36%	0.32%
ΔI_{LOAD}	0.25 A	0.4 A	0.6 A	0.45 A	0.65 A	700 mA	1.4 A	1.4 A
$\Delta f_{SW}/\Delta I_{LOAD}$	60 kHz/A	5 kHz/A	8 kHz/A	222.2 kHz/A	129 kHz/A	285.7 kHz/A	642.8 kHz/A	5.7 kHz/A
Extra V_{CLK}	Need	Need	Need	Need	No need	No need	No need	No need
Max. efficiency	95%	95.5%	93%	93%	87%	88.2	89%	89%

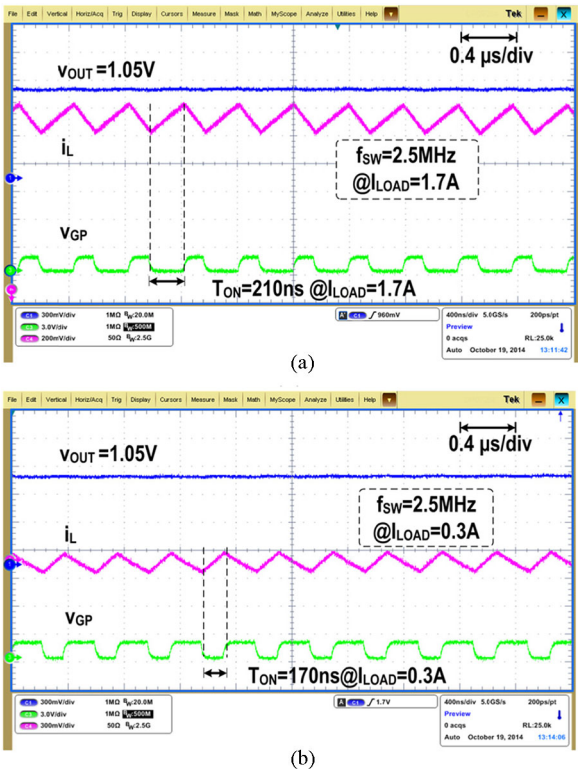

Fig. 22. Steady state of the buck controller with proposed PCT. (a) I_{LOAD} = 1.7 A, (b) I_{LOAD} = 0.3 A.

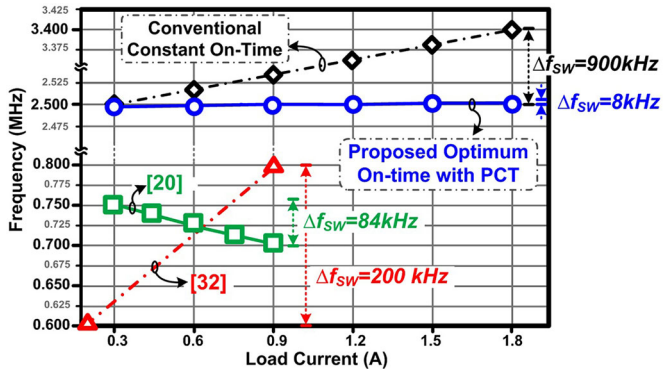

Fig. 23. Switching frequency variation during different load conditions.

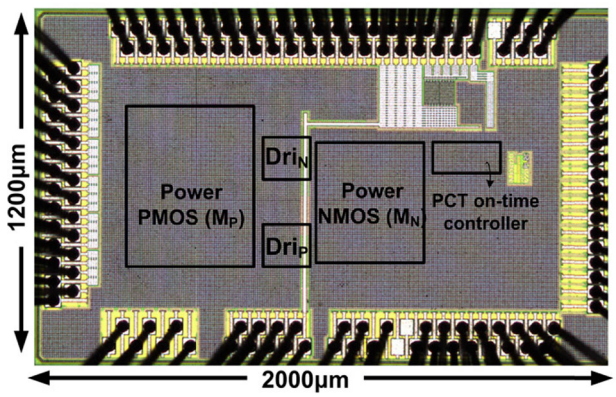

Fig. 24. Die photo.

$\Delta f_{SW}/\Delta I_{LOAD}$ of 285.7 kHz/A. In contrast, the proposed PCT ensures f_{SW} variation is lower than 8 kHz, when f_{SW} is 2.5 MHz. The f_{SW} is nearly constant even when parasitic effects are more serious, that is, $R_{on,P}$ and $R_{on,N}$ are 300 and 200 mΩ, respectively. The proposed PCT has good performances of $\Delta f_{SW}/f_{SW} = 0.32\%$ and $\Delta f_{SW}/\Delta I_{LOAD} =$ 5.7 kHz/A at $f_{SW} = 2.5$ MHz. In this paper, the peak efficiency is 89%, which is dominated by the on resistance of power stage. The values of these on resistances are designed larger than that of general design for the purpose to demonstrate the performance of proposed PCT. Consequently, although the power stage contains serious parasitic effect, the proposed PCT can achieve pseudo-constant f_{SW}, which has competitive performance to the design applied by PLL. Fig. 24 shows the die photo fabricated by 28 nm process.

VI. CONCLUSION

The proposed PCT modulates the optimum on-time for rippled-based controlled buck converter to guarantee f_{SW} is constant over wide load ranges. This paper completely analyzes the facts causing f_{SW} variation by considering V_{IN}, V_{OUT}, I_{LOAD}, and effect of parasitic resistances. The PCT thoroughly solve the effect of parasitic resistances with only

information comparing to the prior arts with complex PLL-base and load sensing method. Pseudo-constant f_{SW} is realized without any sacrifice in regulation and efficiency performance. Experimental results demonstrate 0.32% $\Delta f_{SW}/f_{SW}$ and 5.7 kHz/A $\Delta f_{SW}/\Delta I_{LOAD}$, when V_{IN} is 3.3 V, V_{OUT} is 1.05 V, and f_{SW} is 2.5 MHz. Consequently, the proposed on-time control buck converter with the PCT is suitable for nowadays SoC requirement for a wide load range operation with a nearly constant switching frequency.

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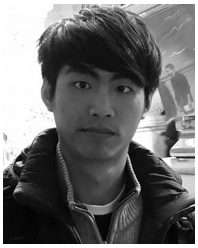

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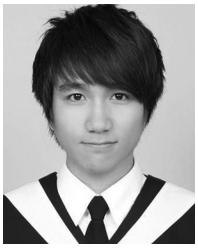

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