

# Modeling and Analysis of Class EF and Class E/F Inverters With Series-Tuned Resonant Networks

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**Abstract**—Class EF and Class E/F inverters are hybrid inverters that combine the improved switch voltage and current waveforms of Class F and Class F<sup>-1</sup> inverters with the efficient switching of Class E inverters. As a result, their efficiency, output power and power output capability can be higher in some cases than the Class E inverter. Little is known about these inverters and no attempt has been made to provide an in depth analysis on their performance. The design equations that have been previously derived are limited and are only applicable under certain assumptions. This paper is the first to provide a comprehensive set of analytical analysis of Class EF and Class E/F inverters. The Class EF<sub>2</sub> inverter is then studied in further detail and three special operation cases are defined that allow it to either operate at maximum power-output capability, maximum switching frequency, or maximum output power. Final design equations are provided to allow for rapid design and development. Experimental results are provided to confirm the accuracy of the performed analysis based on a 23-W Class EF<sub>2</sub> inverter at 6.78-MHz and 8.60-MHz switching frequencies. The results also show that the Class EF<sub>2</sub> inverter achieved an efficiency of 91% compared to a 88% efficiency when operated as a Class E inverter.

**Index Terms**—Class EF inverters, Class E inverters, high-frequency inverters.

## I. INTRODUCTION

EMERGING technologies such as wireless power transfer (WPT) and small-size radio-frequency plasma sources demand efficient, powerful, and multimegahertz switching resonant inverters. These demands have imposed increased challenges in the design and construction of dc/ac inverters and amplifiers. At the circuit level, the switching frequency and output power of an inverter is limited by the currently available devices for a desired efficiency. For instance, the input gate charge, output capacitance, and on-state resistance of a certain MOSFET will have a significant effect of the performance of an inverter in terms of its efficiency and output power capability. The layout of the printed circuit board (PCB), the availability and choice of low-loss passive components, measurement, and evaluation become more difficult.

Resonant topologies are seen to be the most suitable design choice for a multimegahertz switching power inverters due to their reduced switching losses. One particular topology that has

recently been of increasing interest is the Class E inverter. The Class E inverter is capable of operating efficiently at switching frequencies above 1 MHz due to its operation at zero-voltage switching (ZVS) and zero-derivative voltage switching (ZDS) conditions, can deliver more power than other classes for a certain input voltage and is simple to construct because of its low component-count. Class E inverters are well documented in the literature [1]–[5] and have been widely used in WPT applications [6]–[8].

It has been reported in [9]–[12] that the efficiency of the Class E inverter can be improved and its voltage or current stresses can be reduced by adding a resonant network either in parallel or series to its load network. The method of adding resonant networks to the load network is used in Class F and Class F<sup>-1</sup> inverters, and by applying it to the Class E inverter results in a hybrid inverter, which has been referred to as the Class EF<sub>n</sub> or Class E/F<sub>n</sub> inverter. The subscript *n* refers to the ratio of the resonant frequency of the added resonant network to the switching frequency of the inverter and is an integer number greater or equal than 2. The “EF<sub>n</sub>” term is used if *n* is an even integer and the “E/F<sub>n</sub>” term is used if *n* is an odd integer. The added resonant network or networks could be in the form of a series *LC* lumped network that is connected in parallel with the load network as shown in [10], [11], [13], [14], a parallel *LC* lumped network that is connected in series with the load network as shown in [9] or a combination of both series and parallel *LC* lumped networks that are connected in series and in parallel with the load network as shown in [12]. A  $\lambda/4$  transmission line that is inserted between the supply source and the inverter can be also be used as shown in [15] and [16].

The concept of combining Class E and Class F or Class F<sup>-1</sup> inverters was introduced by Kee in 2002 [12]. Since 2002, the research and contribution has been limited with fewer than ten journal papers published regarding Class EF and Class E/F inverters. In his paper, Kee presented an overview of the Class E/F inverter and a generalized frequency-domain-based analysis method to determine the voltage and current waveforms for any combination of added lumped *LC* resonant networks. However, in this early work, Kee did not provide final design equations to determine component values and other parameters, such as output power and maximum power-output capability, for a specific combination of added *LC* resonant network. In addition, the analysis that was presented only considered resonant *LC* networks with a large energy storage capacity or high loaded quality (*Q*) factors.

A subsequent publication by Grebennikov [10] presented closed-form analytical equations for the Class EF and Class E/F inverters with an added series *LC* lumped network in parallel

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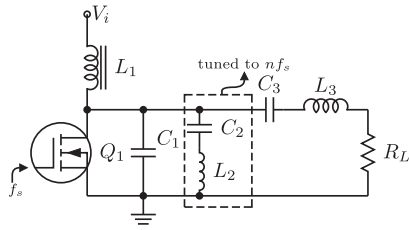


Fig. 1. Circuit diagram of the Class EF or Class E/F inverter.

with the load network as shown in Fig. 1. Design equations were derived specifically for the Class E/F<sub>3</sub> inverter based on the assumption that the added series  $LC$  resonant network has a large energy storage capacity such that the current flowing in it is sinusoidal with a frequency equal to its resonant frequency, and the duty cycle is at 50%. Another publication by Kaczmarczyk [11] presented a piecewise-linear state-space model for the Class EF<sub>2</sub> and Class E/F<sub>3</sub> inverters with a series  $LC$  resonant network in parallel with the load network. The model was solved numerically to obtain the components' values for ZVS and ZDS conditions for any desired duty cycle and for any loaded  $Q$ 's of the added series  $LC$  resonant network and the output network. Kaczmarczyk's model provided the values of duty cycles that will maximize the power-output capability and showed that maximum power-output capability of the Class EF<sub>2</sub> and Class E/F<sub>3</sub> inverters is higher than that of the Class E inverter. Other published papers about Class EF and Class E/F inverters use iterative impedance tuning methods [14] and customized radio-frequency (RF) optimization software [9] to design and optimize the inverter. These methods provide little insight on how the inverter operates and do not aid the reader in designing a specific Class EF or Class E/F inverter.

It is noted that the inverter presented in [14], which has the same circuit diagram of the Class EF inverter shown in Fig. 1, has been referred to as the Class  $\phi_2$  inverter by the authors. The difference lies in the fact that the Class  $\phi_2$  inverter uses a finite input choke ( $L_1$  in Fig. 1) as opposed to a infinite inductance input choke in the Class EF inverter. Using a finite inductance input choke makes the choke a part of the load network and has the effect of increasing the maximum switching frequency of the inverter. This is similar to the case of the "Class E inverter with finite dc-feed inductance" where the maximum switching frequency of a Class E inverter is increased by a factor of approximately four by using a finite inductance input choke [2].

Based on the previous review, it can be noticed that all the analysis that has been performed has not provided an in-depth "power electronic" view of the performance of Class EF and Class E/F inverters in terms of its efficiency, maximum voltage and current stresses, power-output capability, input dc resistance, and maximum switching frequency and how do they compare with the Class E inverter. The analysis has been limited due to the assumption that duty cycle is exactly 50% and the energy capacity or  $Q$  of the added  $LC$  resonant network is high. It can be practically difficult to implement a high  $Q$   $LC$  resonant network at several megahertz especially for power applications. This is because the equivalent series resistance (ESR) of in-

ductors become large, which leads to excessive power losses and can, therefore, limit the advantages of using a Class EF or Class E/F inverter over a Class E inverter. Magnetic cores should also be avoided as they cause additional losses and can limit the power delivered by the inverter due to saturation. Consequently, a low  $Q$  resonant  $LC$  network with a small inductance should be considered as this allows for air-cored inductors consisting of a few turns to be used.

Having identified the limitations in the early analysis, this paper will provide a comprehensive and closed-form expressions of Class EF and Class E/F inverters for any  $Q$  value of an added series  $LC$  lumped resonant network and at any duty cycle. The Class EF<sub>2</sub> inverter will be studied in detail and special cases will be defined. Performance parameters such as efficiency, power-output capability, maximum frequency, maximum voltage, and current stresses will be evaluated for all of the defined special cases. Final design equations will be derived that will allow a designer to calculate the required components' values in a similar way to what has been previously performed on the Class E inverter. The efficiency of all special cases of the Class EF<sub>2</sub> inverter will be compared to that of the Class E inverter. Finally, experimental results will be shown to confirm the validity of the performed analysis and the derived design equations.

## II. MODELING AND ANALYSIS

Fig. 1 shows the circuit diagram of the Class EF and Class E/F inverters. Inductor  $L_2$  and capacitor  $C_2$  are the added series  $LC$  network. Inductor  $L_3$  is divided into an inductance  $L$  that resonates with  $C_3$  at the switching frequency and a residual inductance  $L_x$ . The analysis will be based on the following assumptions:

- 1) the transistor and its body diode form an ideal switch whose ON resistance is zero, OFF resistance is infinity, and switching times are zero;
- 2) the choke inductance is high enough such that the input current  $I_{IN}$  is a dc current;
- 3) the loaded quality factor of the  $L_3 C_3 R_L$  branch is high enough such that the current  $i_o$  through it is sinusoidal;
- 4) the shunt capacitance  $C_1$  is assumed to be constant and absorbs the output capacitance of the transistor;
- 5) there are no losses in the circuit so that all the power supplied by the source is delivered to the load  $R_L$ .

This paper will follow the general method that has been used in the literature for Class E switching circuits in which the analysis that will be presented is for optimum switching operation with a fixed load only [3]–[5], [9], [10], [15]. Fig. 2 shows the circuit of the Class EF or Class E/F inverter based on the aforementioned assumptions. The output current  $i_o$  is sinusoidal and is given by

$$i_o(\omega t) = i_m \sin(\omega t + \phi) \quad (1)$$

where  $i_m$  is the output current's magnitude and  $\phi$  is its phase. For the period  $0 \leq \omega t < 2\pi D$ , the switch is ON, therefore

$$v_{DS}(\omega t) = 0, \text{ for } 0 \leq \omega t < 2\pi D \quad (2)$$

$$i_{C_1}(\omega t) = 0, \text{ for } 0 \leq \omega t < 2\pi D. \quad (3)$$

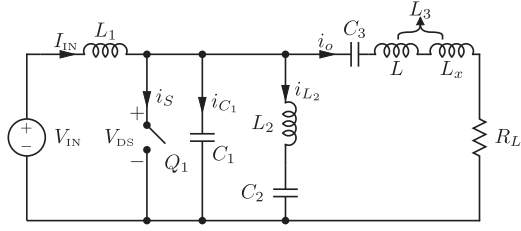


Fig. 2. Circuit diagram of the Class EF or Class E/F inverter for analysis.

By applying the KCL at the switch's drain node, the current in the switch is

$$i_S(\omega t) = I_{IN} - i_{L_2}(\omega t) - i_o(\omega t), \text{ for } 0 \leq \omega t < 2\pi D. \quad (4)$$

Since the switch is ON, the total voltage across the series tuned  $L_2C_2$  network is zero. The  $L_2C_2$  network now is a source-free undamped circuit and its current ( $i_{L_2}$ ) normalized with respect to the input dc current ( $I_{IN}$ ) is given by

$$\frac{i_{L_2}}{I_{IN}}(\omega t) = A_1 \cos(q_1 \omega t) + B_1 \sin(q_1 \omega t) \quad (5)$$

where  $q_1$  is the ratio of the resonant frequency of  $L_2C_2$  to the switching frequency and is given by

$$q_1 = n = \frac{1}{\omega \sqrt{L_2 C_2}}. \quad (6)$$

The coefficients  $A_1$  and  $B_1$  are to be determined based on equation's boundary conditions.

For the period  $2\pi D \leq \omega t < 2\pi$ , the switch is turned OFF, therefore

$$i_S(\omega t) = 0, \text{ for } 2\pi D \leq \omega t < 2\pi. \quad (7)$$

By applying the KCL at the drain node, the current in the series tuned  $L_2C_2$  network is

$$\begin{aligned} i_{L_2}(\omega t) &= I_{IN} - i_o(\omega t) - i_{C_1}(\omega t) \\ &= I_{IN} - i_m \sin(\omega t + \phi) - \omega C_1 \frac{dv_{DS}(\omega t)}{d\omega t}. \end{aligned} \quad (8)$$

The switch's voltage is equal to the total voltage across the  $L_2C_2$  network and is given by

$$\begin{aligned} v_{DS}(\omega t) &= \omega L_2 \frac{di_{L_2}(\omega t)}{d\omega t} \\ &+ \frac{1}{\omega C_2} \int_{2\pi D}^{\omega t} i_{L_2}(\omega t) d\omega t + v_{C_2}(2\pi D). \end{aligned} \quad (9)$$

Differentiating the aforementioned equation gives

$$\frac{dv_{DS}(\omega t)}{d\omega t} = \omega L_2 \frac{d^2 i_{L_2}(\omega t)}{d\omega t^2} + \frac{1}{\omega C_2} i_{L_2}(\omega t). \quad (10)$$

Substituting (10) into (8) and normalizing with respect to the input current gives

$$\begin{aligned} \frac{i_{L_2}}{I_{IN}}(\omega t) &= 1 - \frac{i_m}{I_{IN}} \sin(\omega t + \phi) \\ &- \omega^2 L_2 C_1 \frac{d^2 i_{L_2}}{I_{IN}}(\omega t) - \frac{C_1}{C_2} \frac{i_{L_2}}{I_{IN}}(\omega t). \end{aligned} \quad (11)$$

Equation (11) is a linear nonhomogeneous second-order differential equation, which has the following general solution

$$\begin{aligned} \frac{i_{L_2}}{I_{IN}}(\omega t) &= A_2 \cos(q_2 \omega t) + B_2 \sin(q_2 \omega t) \\ &- \frac{q_2^2 p}{q_2^2 - 1} \sin(\omega t + \phi) + \frac{1}{k + 1} \end{aligned} \quad (12)$$

where

$$k = \frac{C_1}{C_2} \quad (13)$$

$$q_2 = \frac{1}{\omega} \sqrt{\frac{C_1 + C_2}{L_2 C_1 C_2}} = q_1 \sqrt{\frac{k + 1}{k}} \quad (14)$$

$$p = \frac{C_2}{C_1 + C_2} \frac{i_m}{I_{IN}} = \frac{1}{k + 1} \frac{i_m}{I_{IN}} \quad (15)$$

and the coefficients  $A_2$  and  $B_2$  are to be determined based on the equation's boundary conditions. The boundary conditions are determined from the current and voltage continuity conditions when the switch turns ON and OFF, which can be described by

$$i_{L_2}(2\pi D^-) = i_{L_2}(2\pi D^+) \quad (16)$$

$$i_{L_2}(0) = i_{L_2}(2\pi) \quad (17)$$

$$\left. \frac{di_{L_2}(\omega t)}{d\omega t} \right|_{\omega t=2\pi D^-} = \left. \frac{di_{L_2}(\omega t)}{d\omega t} \right|_{\omega t=2\pi D^+} \quad (18)$$

$$\left. \frac{di_{L_2}(\omega t)}{d\omega t} \right|_{\omega t=0} = \left. \frac{di_{L_2}(\omega t)}{d\omega t} \right|_{\omega t=2\pi} \quad (19)$$

The current through capacitor  $C_1$  for the period  $2\pi D \leq \omega t < 2\pi$  is

$$i_{C_1}(\omega t) = I_{IN} - i_o(\omega t) - i_{L_2}(\omega t). \quad (20)$$

and normalizing with respect to the input current and using (13) gives

$$\frac{i_{C_1}}{I_{IN}}(\omega t) = 1 - p(k + 1) \sin(\omega t + \phi) - \frac{i_{L_2}}{I_{IN}}(\omega t). \quad (21)$$

The drain voltage for the period  $2\pi D \leq \omega t < 2\pi$  is

$$v_{DS}(\omega t) = \frac{I_{IN}}{\omega C_1} \int_{2\pi D}^{\omega t} \frac{i_{C_1}}{I_{IN}}(\tau) d\tau \quad (22)$$

where  $\tau$  is a dummy variable. Substituting the ZVS ( $v_{DS}(2\pi) = 0$ ) and ZDS ( $i_{C_1}(2\pi) = 0$ ) conditions into the aforementioned

equation gives the following two equations:

$$2\pi \frac{k}{k+1} (1-D) + p(\cos(2\pi D + \phi) - \cos \phi) \left( \frac{q_2^2}{q_2^2 - 1} - (k+1) \right) + \frac{A_2}{q_2} (\sin(2\pi D q_2) - \sin(2\pi q_2)) + \frac{B_2}{q_2} (\cos(2\pi q_2) - \cos(2\pi D q_2)) = 0 \quad (23)$$

$$\frac{k}{k+1} + p \sin \phi \left( \frac{q_2^2}{q_2^2 - 1} - (k+1) \right) - (A_2 \cos(2\pi q_2) + B_2 \sin(2\pi q_2)) = 0. \quad (24)$$

Equations (16)–(19) and (23)–(24) are six simultaneous equations with six unknown parameters which are  $A_1$ ,  $A_2$ ,  $B_1$ ,  $B_2$ ,  $p$ , and  $\phi$ . The equations can be solved for specific values of  $q_1$ , duty cycle  $D$  and  $k$ . An analytical solution exists, however the resulting expressions are too complex and do not provide any insight. Therefore we have solved these equations numerically using the MATLAB function `fsolve`.

#### A. Voltage and Current Waveforms

Equation (22) can be written as

$$v_{DS}(\omega t) = \frac{I_{IN}}{\omega C_1} \beta(\omega t) \quad (25)$$

where

$$\beta(\omega t) = \int_{2\pi D}^{\omega t} \frac{i_{C1}}{I_{IN}}(\tau) d\tau. \quad (26)$$

The dc component (or average) of the drain voltage is equal to the input voltage supply, i.e.

$$V_{IN} = \frac{I_{IN}}{2\pi\omega C_1} \int_{2\pi D}^{2\pi} \beta(\omega t) d\omega t. \quad (27)$$

By substituting (27) into (25), the normalized drain voltage with respect to the input voltage can be written as

$$\frac{v_{DS}}{V_{IN}}(\omega t) = \begin{cases} 0, & \text{for } 0 \leq \omega t < 2\pi D \\ \frac{2\pi\beta(\omega t)}{\int_{2\pi D}^{2\pi} \beta(\omega t) d\omega t}, & \text{for } 2\pi D \leq \omega t < 2\pi. \end{cases} \quad (28)$$

Using (15), the normalized switch current with respect to the input dc current can be written as

$$\frac{i_S}{I_{IN}}(\omega t) = \begin{cases} 1 - p(k+1) \sin(\omega t + \phi) - (A_1 \cos(q_1 \omega t) + B_1 \sin(q_1 \omega t)), & \text{for } 0 \leq \omega t < 2\pi D \\ 0, & \text{for } 2\pi D \leq \omega t < 2\pi. \end{cases} \quad (29)$$

By using the numerical solutions for  $A_1$ ,  $A_2$ ,  $B_1$ ,  $B_2$ ,  $p$ , and

$\phi$ , the voltage and current waveforms throughout the inverter can be plotted for given values of  $q_1$ , duty cycle and  $k$ . Fig. 3 shows switch's voltage and current waveforms and the current of inductor  $L_2$  for selected values of  $q_1$ , duty cycle and  $k$ .

It can be noticed from the plotted waveforms that the switch peak drain voltage and peak drain current and the shape of their waveform change according to the duty cycle. As the duty cycle decreases the switch peak drain voltage increases and its peak drain current decreases. The shape of the current waveform of inductor  $L_2$  is mainly affected by the value of  $k$ . The current is almost sinusoidal and high  $k$  values and its frequency ratio to the switching frequency is equal to the value  $q_1$  over the entire switching period. The current becomes less sinusoidal, or contains additional harmonics, at low  $k$  values. For the case when  $q_1 = 2$ , the slope of the switch current at the instant when it is turned OFF is positive at a higher  $k$ , and is negative at a lower  $k$ .

#### B. Input DC Resistance

The dc component (or average) of the switch current is equal to the dc input current, hence

$$\frac{1}{2\pi} \int_0^{2\pi} \frac{i_S}{I_{IN}}(\omega t) d\omega t = 1 = \frac{p}{2\pi} (\cos(2\pi D + \phi) - \cos \phi) (k+1) + D - \frac{1}{2\pi q_1} (A_1 \sin(2\pi D q_1) + 2B_1 \sin^2(\pi D q_1)). \quad (30)$$

Solving (30) for  $p$  gives

$$p = \frac{2\pi(1-D) + \frac{A_1}{q_1} \sin(2\pi D q_1) + \frac{2B_1}{q_1} \sin^2(\pi D q_1)}{(k+1)(\cos(2\pi D + \phi) - \cos \phi)}. \quad (31)$$

Substituting (31) into (15) gives the normalized value of  $i_m$  with respect to the input dc current

$$\frac{i_m}{I_{IN}} = \frac{2\pi(1-D) + \frac{A_1}{q_1} \sin(2\pi D q_1) + \frac{2B_1}{q_1} \sin^2(\pi D q_1)}{\cos(2\pi D + \phi) - \cos \phi}. \quad (32)$$

All the power supplied by the source will be consumed in the load, thus

$$P_{IN} = P_o = V_{IN} I_{IN} = \frac{1}{2} i_m^2 R_L. \quad (33)$$

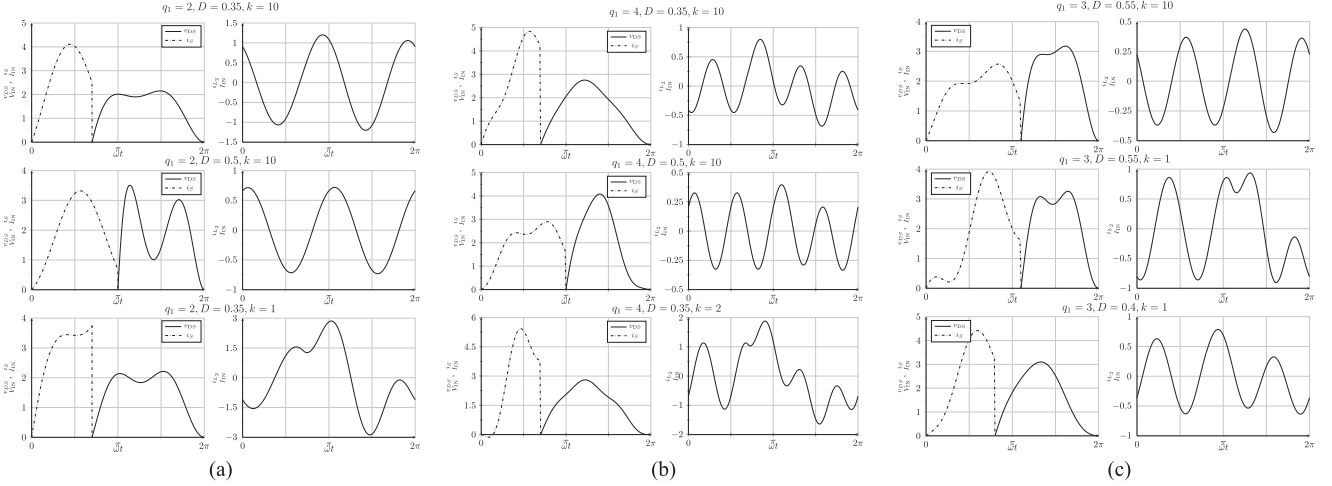


Fig. 3. Theoretical voltage and current waveforms for  $q_1 = 2, 3$ , and  $4$  at different duty cycle and  $k$  values (a)  $q_1 = 2$  (Class EF<sub>2</sub>) (b)  $q_1 = 3$  (Class E/F<sub>3</sub>) (c)  $q_1 = 4$  (Class EF<sub>4</sub>).

Rearranging the aforementioned equation and using (32) gives in the input dc resistance seen by the source

$$\frac{V_{IN}}{I_{IN}} = R_{DC} = \frac{1}{2} \left( \frac{i_m}{I_{IN}} \right)^2 R_L \quad (34)$$

$$\frac{R_{DC}}{R_L} = \frac{1}{2} \left( \frac{2\pi(1-D) + \frac{A_1}{q_1} \sin(2\pi D q_1) + \frac{2B_1}{q_1} \sin^2(\pi D q_1)}{\cos(2\pi D + \phi) - \cos \phi} \right)^2 \quad (35)$$

### C. Voltage and Current Stresses

The peak voltage across the switch can be calculated by differentiating (28) and setting it to zero

$$\frac{d v_{DS}}{d \omega t} = 0 \quad (36)$$

which leads to the following equation:

$$\frac{d \beta(\omega t)}{d \omega t} = \frac{i_{C1}}{I_{IN}}(\omega t) = 0. \quad (37)$$

An explicit solution does not exist for (37), it can however be solved numerically for specific values of  $q_1$ , duty cycle, and  $k$ . Another approach to determine the peak voltage across the switch is to search for a value for  $\omega t$  that maximizes the switch voltage. The MATLAB function `fminbnd()` can be used to determine the switch voltage peaks for a certain  $q_1$  value over a duty cycle range and a  $k$ .

The peak switch current can either occur during the switch on-state period  $0 \leq \omega t < 2\pi D$  or at the end of the switch on-state period  $\omega t = 2\pi D^-$ . The peak switch current during the switch on-state period can be obtained by differentiating (29)

and setting it to zero and solved for  $\omega t$

$$\frac{d i_S}{d \omega t}(\omega t) = 0. \quad (38)$$

The calculated value of  $\omega t$  should be substituted back into (29) and the evaluated peak switch current should be compared with the switch current value at  $\omega t = 2\pi D$  and the switch maximum current is the greater value of the two. Alternatively, the peak switch current can be found by searching for a value for  $\omega t$  that maximizes the switch current. Fig. 4 shows the switch's maximum voltage and current normalized with respect to the input voltage and input dc current, respectively, for  $q_1 = 2, 3$  &  $4$  and for selected values of  $k$ . It can be noted from the figures that higher values of  $k$  have a slight effect on the peak values of the switch voltage and current, whereas the duty cycle has a much more significant effect.

### D. Power-Output Capability

The power-output capability is defined as the ratio of the output power to the maximum voltage and current stresses of the switch. It is an indication of the switch utilization for a certain output power. It can be represented as

$$c_p = \frac{P_o}{v_{DSmax} i_{Smax}}. \quad (39)$$

Since it has been assumed that the inverter is ideal, therefore, all the power supplied by the source is consumed in the load, the power-output capability can be written as

$$c_p = \frac{V_{IN} I_{IN}}{v_{DSmax} i_{Smax}}. \quad (40)$$

Using the solutions obtained from (37) and (38) the power-output capability can be calculated for specific values of  $q_1$ . Fig. 5 shows the variation of the power-output capability with duty cycle for  $q_1 = 2$ ,  $q_1 = 3$ ,  $q_1 = 4$ , and for selected values of  $k$ .

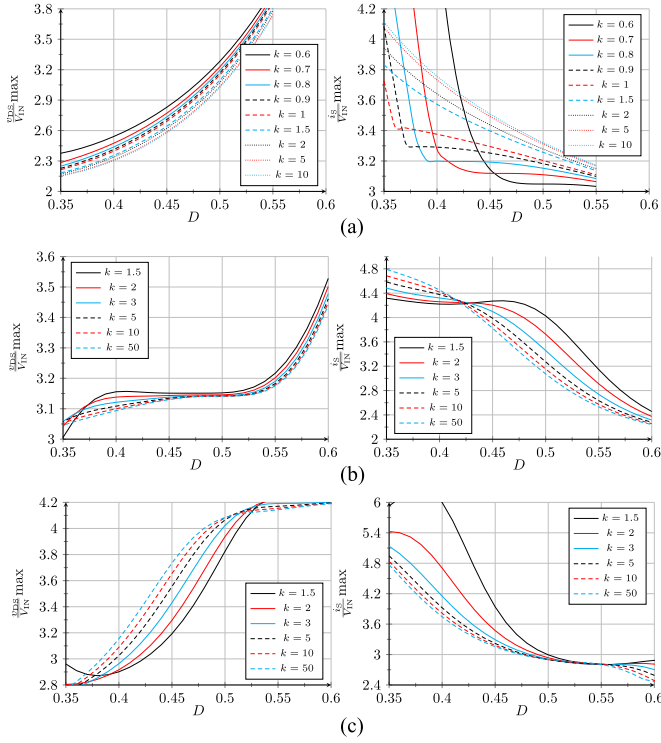


Fig. 4. Maximum switch voltage and current for  $q_1 = 2, 3,$  and  $4$  (a)  $q_1 = 2$  (Class EF<sub>2</sub>) (b)  $q_1 = 3$  (Class E/F<sub>3</sub>) (c)  $q_1 = 4$  (Class EF<sub>4</sub>).

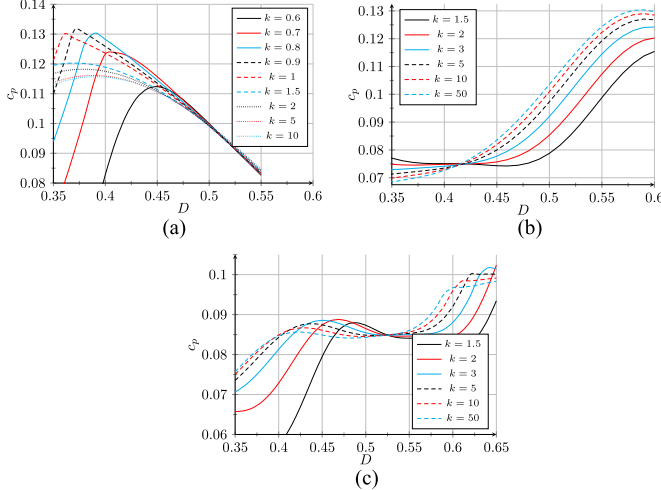


Fig. 5. Power-output capability variations for  $q_1 = 2, 3,$  and  $4$  (a)  $q_1 = 2$  (Class EF<sub>2</sub>) (b)  $q_1 = 3$  (Class E/F<sub>3</sub>) (c)  $q_1 = 4$  (Class EF<sub>4</sub>).

### III. DESIGN EQUATIONS AND SPECIAL CASES FOR THE CLASS EF<sub>2</sub> INVERTER

#### A. Power-Output Capability as a Function of $k$

Since the inverter can operate at any given value of  $q_1$ , duty cycle, and  $k$ , it is of interest to operate the inverter at its highest power-output capability point. It will be assumed that series  $L_2C_2$  is tuned to the second harmonic of the switching frequency, i.e.,  $q_1 = 2$  (Class EF<sub>2</sub>). The aim now is for a given

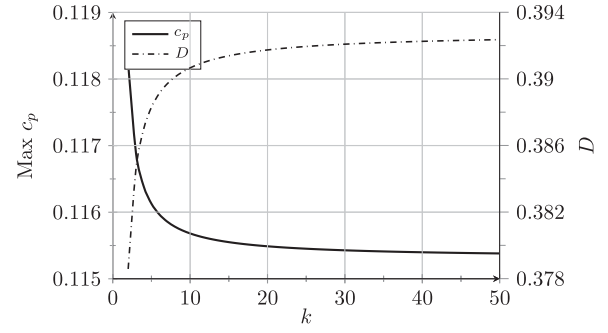


Fig. 6. Path of maximum  $c_p$  and associated duty cycle as a function  $k$ .

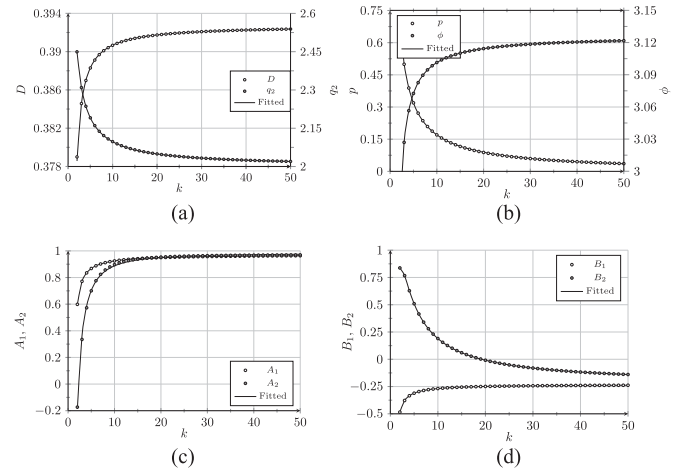


Fig. 7. Variation of parameters with  $k$  for highest  $c_p$  (a) duty cycle and  $q_2$  (b)  $p$  and  $\phi$  (c)  $A_1$  and  $A_2$  (d)  $B_1$  and  $B_2$ .

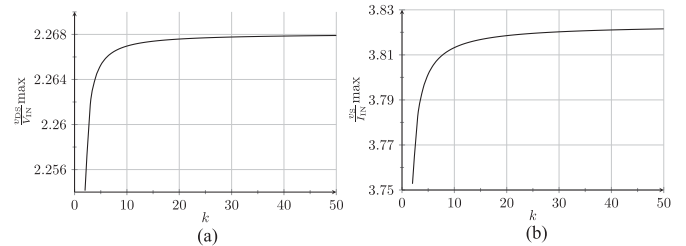


Fig. 8. Variation of the switch's peak drain voltage and current with  $k$  for highest  $c_p$  (a) peak drain voltage (b) peak drain current.

$k$  to find the value of duty cycle that will result in the highest power-output capability operation. Fig. 6 shows the path of maximum power-output capability as  $k$  and the duty cycle vary. Fig. 7 shows the variation of the parameters  $A_1$ ,  $A_2$ ,  $B_1$ ,  $B_2$ ,  $q_2$ ,  $p$ , and  $\phi$  along the maximum power-output capability path.

Fig. 8 shows the variation of the switch's peak drain voltage and current with  $k$ . It can be noticed from Fig. 7 that as  $k$  increases the value of  $q_2$  approaches the value of  $q_1$  which is 2. The values of the coefficients  $A_1$  and  $A_2$  begin to approach each other and the values of the coefficients  $B_1$  and  $B_2$  approach each other as well. This means that the current in inductor  $L_2$  becomes sinusoidal with a frequency equal to  $q_1\omega$  or  $2\omega$  for the case when  $q_1 = 2$ .

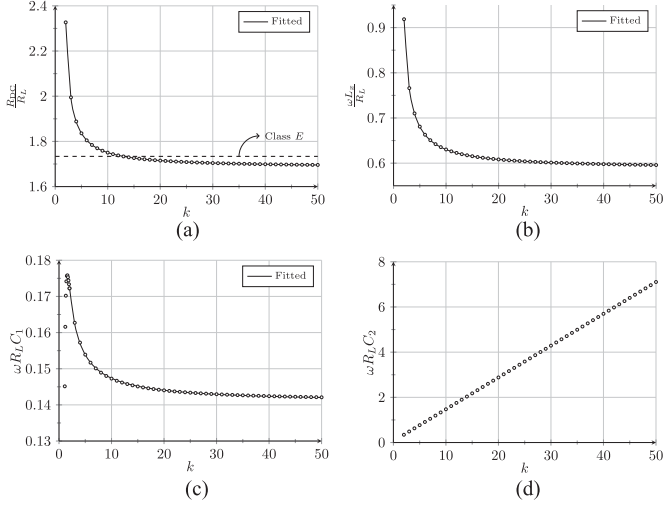


Fig. 9. Variation of  $R_L$ ,  $L_x$ ,  $C_1$  and  $C_2$  with  $k$  for maximum power output capability (a)  $R_{DC}/R_L$  (b)  $\omega L_x/R_L$  (c)  $\omega R_L C_1$  (d)  $\omega R_L C_2$ .

Based on the previous analysis, the graphical solutions of the normalized values of the input resistance  $R_{DC}$ , capacitors  $C_1$ ,  $C_2$ , and residual impedance  $L_x$  can be plotted as shown in Fig. 9. It can be noticed in Fig. 9(a) that for a  $k$  value below 12 the input resistance is higher than that of the Class E inverter and this means that at a certain input voltage and load resistance the Class EF inverter provides less power throughput than the Class E inverter. For  $k$  values higher than 12, the input resistance is lower than that of the Class E inverter, this means that the Class EF inverter will provide more power than the Class E inverter for a certain load resistance and input voltage. Using the Curve Fitting Toolbox in MATLAB, the following equations have been obtained that provide an accurate fit to the graphical solutions in Fig. 9:

$$D(k) = \frac{0.39275k - 0.26593}{k - 0.62755} \quad (41)$$

$$\frac{R_{DC}}{R_L}(k) = \frac{1.6835k - 1.1984}{k - 1.0681} \quad (42)$$

$$\omega R_L C_1(k) = \frac{0.14069k + 0.08613}{k + 0.1315} \quad (43)$$

$$\omega R_L C_2(k) = \omega R_L C_1(k)k \quad (44)$$

$$\frac{\omega L_2}{R_L}(k) = \frac{1}{4\omega R_L C_2(k)} \quad (45)$$

$$\frac{\omega L_x}{R_L}(k) = \frac{0.58805k - 0.10034}{k - 0.82871} \quad (46)$$

$$\omega R_L C_3(k) = \frac{1}{Q_L - \frac{\omega L_x}{R_L}(k)}. \quad (47)$$

Equations (42)–(47) can be used to determine the values of capacitors  $C_1$ ,  $C_2$ , and  $C_3$  and the required duty cycle for a given  $k$ , load resistance  $R_L$ , switching frequency and output network quality factor  $Q_L$  that will result in the highest power output capability operation.

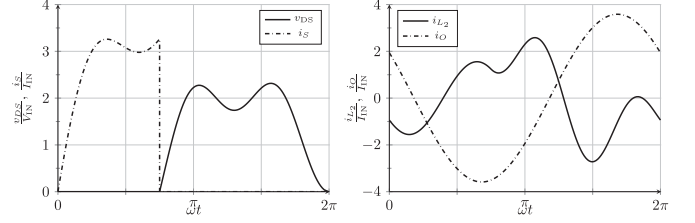


Fig. 10. Voltage and current waveforms for the maximum power output capability case ( $q_1 = 2$ ,  $D = 0.375$ ,  $k = 0.867$ ).

### B. Special Case I: Solution for Global Maximum Power-Output Capability Operation

For the case when  $q_1 = 2$ , the global maximum power-output capability is 0.1323, which occurs when the duty cycle is 0.375 and  $k$  is 0.867. In this case, the values of  $A_1 = -0.9394$ ,  $A_2 = -0.8589$ ,  $B_1 = -1.2405$ ,  $B_2 = -1.2276$ ,  $p = 1.9204$ ,  $\phi = 2.5701$  rad  $q_2 = 2.9349$ , and  $\int_{2\pi D}^{2\pi} \beta(\omega t) = \int_{0.75\pi}^{2\pi} \beta(\omega t) = 5.3241$ . The values of the normalized output current, input resistance, and maximum voltage and current stresses are given in Table II. The switch's voltage, switch's current, and the current through inductor  $L_2$  for this particular case are

$$\frac{v_{DS}}{V_{IN}}(\omega t) = \begin{cases} 0, & \text{for } 0 \leq \omega t < 0.75\pi \\ -1.4510 + 0.5481\omega t - 1.6673 \sin(\omega t + 57.26^\circ) \\ \quad + 0.6024 \sin(2.9349\omega t - 55.02^\circ), & \text{for } 0.75\pi \leq \omega t < 2\pi \end{cases} \quad (48)$$

$$\frac{i_{DS}}{I_{IN}}(\omega t) = \begin{cases} 1 - 3.5853 \sin(\omega t + 147.25^\circ) + 1.5560 \sin(2\omega t - 142.86^\circ), & \text{for } 0 \leq \omega t < 0.75\pi \\ 0, & \text{for } 0.75\pi \leq \omega t < 2\pi \end{cases} \quad (49)$$

$$\frac{i_{L_2}}{I_{IN}}(\omega t) = \begin{cases} 1.5560 \sin(2\omega t - 142.86^\circ), & \text{for } 0 \leq \omega t < 0.75\pi \\ 0.5356 + 1.4982 \sin(2.9349\omega t - 145.02^\circ) \\ \quad - 2.1726 \sin(\omega t + 147.25^\circ), & \text{for } 0.75\pi \leq \omega t < 2\pi. \end{cases} \quad (50)$$

Fig. 10 shows the voltage and current waveforms for this particular case. The normalized maximum voltage across the switch is 2.3162, which occurs at  $\omega t = 4.9349$ , the normalized maximum switch current is 3.2632, which occurs at  $\omega t = 1.1310$  and at  $\omega t = 2\pi D = 2.3562$ .

Next, the values of the components will be determined for this particular case. Starting with  $C_1$ , referring to (26) and (27), the average voltage of the switch voltage is

$$V_{IN} = \frac{I_{IN}}{2\pi\omega C_1} \int_{0.75\pi}^{2\pi} \beta(\omega t) d\omega t = 5.3241 \frac{I_{IN}}{2\pi\omega C_1} \quad (51)$$

and using (35)

$$\frac{V_{IN}}{I_{IN}} = R_{DC} = 6.4273R_L = 5.3241 \frac{1}{2\pi\omega C_1}. \quad (52)$$

Therefore, the normalized reactance value of  $C_1$  with respect to the load is

$$\frac{1}{\omega R_L C_1} = 7.5851. \quad (53)$$

Using (13), the normalized value of  $C_2$  is

$$\frac{1}{\omega R_L C_2} = 6.5762. \quad (54)$$

Using (6), the normalized value of  $L_2$  is

$$\frac{\omega L_2}{R_L} = 1.6441. \quad (55)$$

The value of the residual impedance is equal to

$$\omega L_x = \frac{v_x}{i_m} \quad (56)$$

where  $v_x$  is the amplitude of the voltage across the residual impedance and is equal to

$$v_x = \frac{1}{\pi} \int_{2\pi D}^{2\pi} v_{DS}(\omega t) \cos(\omega t + \phi) d\omega t. \quad (57)$$

Using (28),  $v_x$  is also equal to

$$\frac{v_x}{V_{IN}} = \frac{2 \int_{0.75\pi}^{2\pi} \beta(\omega t) \cos(\omega t + \phi) d\omega t}{\int_{0.75\pi}^{2\pi} \beta(\omega t) d\omega t} = 1.1346. \quad (58)$$

Using (32) and (35), the normalized value of the residual impedance is

$$\frac{\omega L_x}{R_L} = 2.0339 \quad (59)$$

and the normalized reactance value of  $C_3$  is

$$\frac{1}{\omega R_L C_3} = Q_L - \frac{\omega L_x}{R_L} = Q_L - 2.0339. \quad (60)$$

### C. Special Case II: Solution for Operation at High $k$ Values

The analysis and design equations can be simplified for operation at a value of  $k$  higher than 20. The following assumptions can be concluded based on the previous sections as  $k$  begins to increase,  $p \rightarrow 0$ ,  $q_2 \approx q_1$ ,  $A_2 \approx A_1$  and  $B_2 \approx B_1$ . Applying these aforementioned assumptions to (5) and (12), the current through inductor  $L_2$  for the period  $0 \leq \omega t < 2\pi$  can be written as

$$\frac{i_{L_2}}{I_{IN}}(\omega t) = A_1 \cos(q_1 \omega t) + B_1 \sin(q_1 \omega t), \text{ for } 0 \leq \omega t < 2\pi. \quad (61)$$

The aforementioned equation shows that the current through inductor  $L_2$  is sinusoidal for the entire switching signal with a frequency equal to the resonant frequency of  $L_2$  and  $C_2$ , which is equal to  $q_1 \omega$ . The current in the switch when it is turned ON

$$\begin{aligned} \frac{i_S}{I_{IN}}(\omega t) &= 1 - \frac{i_o}{I_{IN}}(\omega t) - \frac{i_{L_2}}{I_{IN}}(\omega t) \\ &= 1 - \frac{i_m}{I_{IN}} \sin(\omega t + \phi) - A_1 \cos(q_1 \omega t) \\ &\quad - B_1 \sin(q_1 \omega t), \text{ for } 0 \leq \omega t < 2\pi D. \end{aligned} \quad (62)$$

The harmonic content of the current in the switch consists of a dc component, a component at the fundamental switching frequency  $\omega$  and a component at the resonant frequency of  $L_2 C_2$ , which here is  $q_1 \omega$ . The components with frequency  $q_1 \omega$  can be calculated using two quadrature current Fourier components at  $q_1 \omega$ . These two quadrature Fourier components are equal to  $A_1$  and  $B_1$ , respectively, as follows:

$$\begin{aligned} A_1 &= -\frac{1}{\pi} \int_0^{2\pi D} \frac{i_S}{I_{IN}}(\omega t) \cos(q_1 \omega t) d\omega t \\ &= -\frac{\sin(2\pi D q_1)}{q_1 \pi} \left( 1 - \frac{B_1 \sin(2\pi D q_1)}{2} \right) \\ &\quad + \frac{A_1}{\pi} \left( \frac{\sin(4\pi D q_1)}{4q_1} + \pi D \right) \\ &\quad - \frac{i_m}{\pi} \left( \frac{\cos \phi}{q_1^2 - 1} + \frac{\cos(\phi + 2\pi D(q_1 + 1))}{2(q_1 + 1)} \right. \\ &\quad \left. - \frac{\cos(\phi - 2\pi D(q_1 - 1))}{2(q_1 - 1)} \right) \end{aligned} \quad (63)$$

$$\begin{aligned} B_1 &= -\frac{1}{\pi} \int_0^{2\pi D} \frac{i_S}{I_{IN}}(\omega t) \sin(q_1 \omega t) d\omega t \\ &= -\frac{2 \sin^2(\pi D q_1)}{q_1 \pi} \left( 1 - \frac{A_1}{4} \right) \\ &\quad - \frac{B_1}{\pi} \left( \frac{\sin(4\pi D q_1)}{4q_1} - \pi D \right) \\ &\quad - \frac{i_m}{\pi} \left( \frac{-\sin \phi}{q_1^2 - 1} + \frac{\sin(\phi + 2\pi D(q_1 + 1))}{2(q_1 + 1)} \right. \\ &\quad \left. + \frac{\sin(\phi - 2\pi D(q_1 - 1))}{2(q_1 - 1)} \right). \end{aligned} \quad (64)$$

The current in capacitor  $C_1$  when the switch is turned OFF is

$$\begin{aligned} \frac{i_{C_1}}{I_{IN}}(\omega t) &= 1 - \frac{i_o}{I_{IN}}(\omega t) - \frac{i_{L_2}}{I_{IN}}(\omega t) = 1 - \frac{i_m}{I_{IN}} \sin(\omega t + \phi) \\ &\quad - A_1 \cos(q_1 \omega t) - B_1 \sin(q_1 \omega t), \text{ for } 2\pi D \leq \omega t < 2\pi. \end{aligned} \quad (65)$$

From (28), the voltage developed across capacitor  $C_1$  is

$$\frac{v_{DS}}{V_{IN}}(\omega t) = \frac{2\pi \beta'(\omega t)}{\int_{2\pi D}^{2\pi} \beta'(\omega t) d\omega t}, \text{ for } 2\pi D \leq \omega t < 2\pi \quad (66)$$

where

$$\begin{aligned} \beta'(\omega t) = & \int_{2\pi D}^{\omega t} \frac{i_{C_1}}{I_{IN}}(\tau) d\tau = \omega t - 2\pi D + \frac{i_m}{I_{IN}} (\cos(\omega t + \phi) \\ & - \cos(\phi + 2\pi D)) - \frac{A_1}{q_1} (\sin(q_1 \omega t) - \sin(2\pi D q_1)) \\ & + \frac{B_1}{q_1} (\cos(q_1 \omega t) - \cos(2\pi D q_1)). \end{aligned} \quad (67)$$

Substituting the ZVS ( $v_{DS}(2\pi) = 0$ ) and ZDS ( $i_{C_1}(2\pi) = 0$ ) conditions into (66) gives the following two equations:

$$\begin{aligned} 2\pi(1 - D) + \frac{i_m}{I_{IN}} (\cos \phi - \cos(2\pi D + \phi)) - \frac{A_1}{q_1} (\sin(2\pi q_1) \\ - \sin(2\pi D q_1)) + \frac{B_1}{q_1} (\cos(2\pi q_1) - \cos(2\pi D q_1)) = 0 \end{aligned} \quad (68)$$

$$1 - A_1 \cos(2\pi q_1) - B_1 \sin(2\pi q_1) - \frac{i_m}{I_{IN}} \sin \phi = 0. \quad (69)$$

Equations (63), (64), (68) and (69) are four simultaneous equations that can be solved numerically for  $\frac{i_m}{I_{IN}}$ ,  $\phi$ ,  $A_1$  and  $B_1$  for a given value of  $q_1$  and duty cycle. The MATLAB function `fsolve` can be used to solve these equations.

The peak drain current can be obtained by differentiating (62) and setting it to zero, which results in the following equation:

$$A_1 q_1 \sin(q_1 \omega t) - B_1 q_1 \cos(q_1 \omega t) - \frac{i_m}{I_{IN}} \cos(\omega t + \phi) = 0 \quad (70)$$

which can be solved numerically. The peak drain voltage can be obtained by differentiating (66) and setting it to zero, which results in the following equation:

$$1 - \frac{i_m}{I_{IN}} \sin(\omega t + \phi) - A_1 \cos(q_1 \omega t) - B_1 \sin(q_1 \omega t) = 0 \quad (71)$$

which can also be solved numerically. It should be noted that drain voltage may contain two local maximum points depending on the set duty cycle. Therefore, the maximum drain voltage is the highest of the two local maximum voltages. The power-output capability can then be calculated from (40).

The aforementioned equations can be used to proceed with the calculations of the values of the components and other parameters. However, by observing Fig. 6(b), it can be noticed that the maximum power-output capability and the associated duty cycle approach 0.115 and 0.392, respectively, as  $k$  increases when  $q_1 = 2$ . By approximating the duty cycle value for maximum power-output capability to 0.40, the solved values of  $A_1 = 0.96012$ ,  $B_1 = -0.18365$ ,  $\frac{i_m}{I_{IN}} = 1.8099$ ,  $\phi = 3.1196$ , and  $\int_{0.8\pi}^{2\pi} \beta'(\omega t) d\omega t = 1.3195$ . From (34), the normalized input dc resistance is

$$\frac{R_{DC}}{R_L} = \frac{1}{2} \left( \frac{i_m}{I_{IN}} \right)^2 = 1.6379 \quad (72)$$

and the output power is

$$P_o = 0.6105 \frac{V_{IN}^2}{R_L}. \quad (73)$$

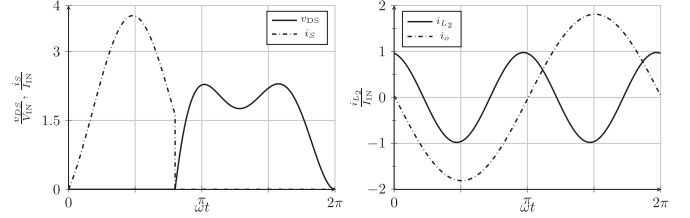


Fig. 11. Voltage and current waveforms for the case  $q_1 = 2$ ,  $D = 0.4$ ,  $k > 20$ .

From (26) and (27) and using (72) and the solved value of  $\int \beta'(\omega t) d\omega t$ , the normalized value of capacitor  $C_1$  is

$$\frac{1}{\omega R_L C_1} = 2\pi \frac{R_{DC}}{R_L} \frac{1}{\int_{0.8\pi}^{2\pi} \beta'(\omega t) d\omega t} = 7.7993. \quad (74)$$

From (58), the voltage across the residual impedance is

$$\frac{v_x}{V_{IN}} = \frac{2 \int_{0.8\pi}^{2\pi} \beta'(\omega t) \cos(\omega t + \phi) d\omega t}{\int_{0.8\pi}^{2\pi} \beta'(\omega t) d\omega t} = 0.62424. \quad (75)$$

From (56) and using (72) and the solved value of  $\frac{i_m}{I_{IN}}$ , the normalized value of the residual impedance is

$$\frac{\omega L_x}{R_L} = 0.56491 \quad (76)$$

and from (60), the normalized value of capacitor  $C_3$  is

$$\frac{1}{\omega R_L C_3} = Q_L - \frac{\omega L_x}{R_L} = Q_L - 0.56491. \quad (77)$$

The values of  $L_2$  and  $C_2$  should be chosen such that their resonant frequency is equal to  $2\omega$  and  $k$  is larger than 20. Fig. 11 shows voltage and current waveforms for this particular case. The values of the normalized output current and maximum voltage and current stresses are given in Table II.

#### D. Maximum Switching Frequency and Special Case III

Based on the performed analysis, there is a certain value for capacitor  $C_1$  to achieve optimum switching operation. This value decreases as the switching frequency increases as dictated by (53). Therefore, there is a maximum switching frequency that the circuit can operate at before the value of capacitor  $C_1$  becomes smaller than the output capacitance of the switch. The maximum switching frequency that the Class EF<sub>2</sub> inverter can operate at is when the value of  $C_1$  equals the output capacitance of the switch  $C_o$  (assuming that the switch's output capacitance is constant). For the global maximum power-output capability case ( $q_1 = 2$ ,  $D = 0.375$ ,  $k = 0.867$ ), the maximum switching frequency at which the ZVS and ZDS conditions can be achieved can be determined from (53) as

$$f_{\max} = \frac{1}{7.5851 \times 2\pi R_L C_o} = \frac{0.02098}{R_L C_o}. \quad (78)$$

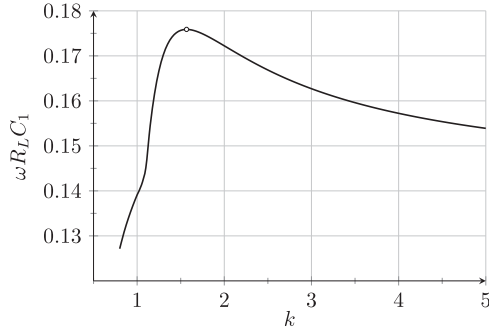


Fig. 12. Peak value of  $\omega R_L C_1$  for determining the maximum frequency that can be achieved.

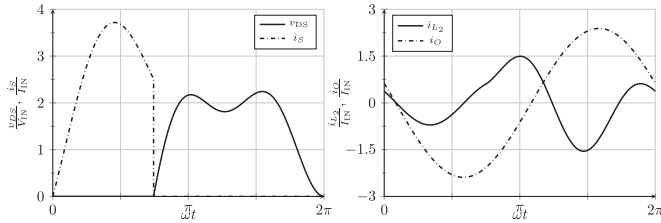


Fig. 13. Voltage and current waveforms for the maximum frequency operation case.

which is about 0.7 times that of the Class E inverter. For the case when  $k > 20$ , the maximum frequency at which the ZVS and ZDS conditions can be achieved is determined from (74) as

$$f_{\max} = \frac{1}{7.7993 \times 2\pi R_L C_o} = \frac{0.02041}{R_L C_o} \quad (79)$$

which is also about 0.7 times that of the Class E inverter.

By examining Fig. 9(c), the maximum switching frequency the Class EF<sub>2</sub> inverter can operate at and at the same time operate at the maximum power-output capability is at the maximum value of  $\omega R_L C_1$ . Fig. 12 shows a closer look at the variation of  $\omega R_L C_1$  with  $k$ , the peak value is 0.17588 when  $k = 1.567$  and  $D = 0.3718$ . The maximum frequency here at which the ZVS and ZDS conditions can be achieved is

$$f_{\max} = \frac{0.17588}{2\pi R_L C_o} = \frac{0.02799}{R_L C_o} \quad (80)$$

which approximately equals to the maximum frequency of the Class E inverter. The design equations for this particular case (maximum frequency case), which can be calculated in a similar manner to what has been done for Case I, are given in Table II. The values of the normalized output current, maximum voltage and current stresses, input dc resistance and output power are also given in Table II. Fig. 13 shows the voltage and current waveforms for this particular case.

### E. Minimum Input Choke Inductance

The minimum inductance value of the input choke will be determined here for all of the special cases. When the switch is ON, the voltage across the input choke is

$$v_{L_1}(\omega t) = V_{IN} \quad (81)$$

and the current through the choke inductance is

$$\begin{aligned} i_{L_1}(\omega t) &= \frac{1}{\omega L_1} \int_0^{\omega t} v_{L_1}(\omega t) d\omega t + i_{L_1}(0) \\ &= \frac{V_{IN}}{\omega L_1} \omega t + i_{L_1}(0). \end{aligned} \quad (82)$$

The current in the input choke at the end of the on period is

$$i_{L_1}(2\pi D) = 2\pi D \frac{V_{IN}}{\omega L_1} + i_{L_1}(0). \quad (83)$$

Therefore, the peak-to-peak ripple in the input current is

$$\Delta i_{L_1} = i_{L_1}(2\pi D) - i_{L_1}(0) = 2\pi D \frac{V_{IN}}{\omega L_1}. \quad (84)$$

The minimum input choke inductance required for the maximum peak-to-peak current ripple is

$$L_{1\min} = 2\pi D \frac{V_{IN}}{\omega \Delta i_{L_1\max}}. \quad (85)$$

Using (34), the minimum input choke inductance can be written as

$$L_{1\min} = 2\pi D \frac{R_{DC}}{\omega \frac{\Delta i_{L_1}}{I_{IN}}}. \quad (86)$$

The aforementioned equation gives the minimum input choke inductance for a certain maximum input current ripple percentage. Table II lists the minimum input choke inductance in all special cases for a 10% ( $\Delta i_{L_1}/I_{IN} = 0.1$ ) maximum input ripple current.

### F. Efficiency

The losses and efficiency will be considered for all special cases. The efficiency is defined as  $\eta = P_o/P_{IN}$ . Beginning with the input choke, it's losses can be represented by a series resistor  $r_f$  which includes the winding resistance and core losses. According to the first assumption, the current in the input choke is constant, therefore, the loss in the input choke is equal to

$$P_{L_1} = I_{IN}^2 r_f = \frac{2}{\left(\frac{i_m}{I_{IN}}\right)^2} \frac{r_f}{R_L} P_o. \quad (87)$$

The switch conduction power loss due to its on resistance  $r_{DS}$  is determined first by calculating the rms value of the switch current from (29) as follows:

$$i_{S\text{rms}} = I_{IN} \sqrt{\frac{1}{2\pi} \int_0^{2\pi D} \frac{i_S^2}{I_{IN}^2}(\omega t) d\omega t} \quad (88)$$

and the conduction power loss is

$$P_{DS} = i_{S\text{rms}}^2 r_{DS} = \frac{1}{\pi \left(\frac{i_m}{I_{IN}}\right)^2} \int_0^{2\pi D} \frac{i_S^2}{I_{IN}^2}(\omega t) d\omega t \frac{r_{DS}}{R_L} P_o. \quad (89)$$

The power loss in the shunt capacitor  $C_1$  due to its resistance  $r_{C_1}$  is determined first by calculation the rms value of it's current

from (21) as follows:

$$i_{C_1 \text{ rms}} = I_{\text{IN}} \sqrt{\frac{1}{2\pi} \int_{2\pi D}^{2\pi} \frac{i_{C_1}^2}{I_{\text{IN}}^2}(\omega t) d\omega t} \quad (90)$$

and the power loss is

$$P_{C_1} = i_{C_1 \text{ rms}}^2 r_{C_1} = \frac{1}{\pi \left(\frac{i_m}{I_{\text{IN}}}\right)^2} \int_{2\pi D}^{2\pi} \frac{i_{C_1}^2}{I_{\text{IN}}^2}(\omega t) d\omega t \frac{r_{C_1}}{R_L} P_o. \quad (91)$$

The power loss in the series tuned  $L_2C_2$  branch due to the ESR of the inductor  $r_{L_2}$  and the resistance loss of the capacitor  $r_{C_2}$  is first determined by calculated the rms current value of inductor  $L_2$  as from (5) and (12) as follows:

$$i_{L_2 \text{ rms}} = I_{\text{IN}} \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \frac{i_{L_2}^2}{I_{\text{IN}}^2}(\omega t) d\omega t} \quad (92)$$

and the total power loss is

$$\begin{aligned} P_{L_2C_2} &= i_{L_2 \text{ rms}}^2 (r_{L_2} + r_{C_2}) \\ &= \frac{1}{\pi \left(\frac{i_m}{I_{\text{IN}}}\right)^2} \int_0^{2\pi} \frac{i_{L_2}^2}{I_{\text{IN}}^2}(\omega t) d\omega t \left(\frac{r_{L_2} + r_{C_2}}{R_L}\right) P_o. \end{aligned} \quad (93)$$

The power loss in the output load network  $L_3C_3$  due to the inductor's ESR  $r_{L_3}$  and the capacitor's resistance  $r_{C_3}$  is

$$P_{L_3C_3} = \frac{r_{L_3} + r_{C_3}}{R_L} P_o. \quad (94)$$

The turn-on switching power loss of the switch is assumed to be zero if the ZVS condition is achieved. The turn-off switching power loss can be estimated as follows [1]. The switch current during turn-off  $t_f$  can be assumed to decrease linearly. Using (29), the switch's current can be represented as

$$\begin{aligned} \frac{i_S}{I_{\text{IN}}}(\omega t) &= \frac{i_S}{I_{\text{IN}}}(2\pi D) \left(1 - \frac{\omega t - 2\pi D}{\omega t_f}\right) \\ &\text{for } 2\pi D < \omega t \leq 2\pi D + \omega t_f \end{aligned} \quad (95)$$

and the current in the shunt capacitor  $C_1$  can be approximated by

$$\begin{aligned} \frac{i_{C_1}}{I_{\text{IN}}}(\omega t) &\approx \frac{i_S}{I_{\text{IN}}}(2\pi D) \left(\frac{\omega t - 2\pi D}{\omega t_f}\right) \\ &\text{for } 2\pi D < \omega t \leq 2\pi D + \omega t_f. \end{aligned} \quad (96)$$

The voltage across the switch is

$$\begin{aligned} v_{\text{DS}}(\omega t) &= \frac{I_{\text{IN}}}{\omega C_1} \frac{i_S}{I_{\text{IN}}}(2\pi D) \int_{2\pi D}^{\omega t} \frac{i_{C_1}}{I_{\text{IN}}}(\tau) d\tau \\ &= \frac{I_{\text{IN}}}{\omega C_1} \frac{i_S}{I_{\text{IN}}}(2\pi D) \frac{(\omega t - 2\pi D)^2}{\omega t_f} \end{aligned} \quad (97)$$

TABLE I  
NUMERICALLY CALCULATED POWERS

Normalized Power	Class EF <sub>2</sub> Case I (max $c_p$ )	Class EF <sub>2</sub> Case II $k > 20$	Class EF <sub>2</sub> Case III (max $f$ )	Class E $D = 0.5$
$P_{L_1}$	0.15559	0.61054	0.35108	0.57666
$P_{\text{DS}}$	0.45421	1.8298	1.0876	1.3648
$P_{C_1}$	0.23159	0.072434	0.17394	0.21188
$P_{L_2C_2}$	0.35497	0.29170	0.24449	-
$P_{t_f}$	$\approx \frac{\omega t_f}{12}$	$\approx \frac{\omega t_f}{12}$	$\approx \frac{\omega t_f}{12}$	$\approx \frac{\omega t_f}{12}$

and using (26) and (27), the voltage across switch can be represented as

$$\frac{v_{\text{DS}}}{V_{\text{IN}}}(\omega t) = \frac{2\pi}{\int_{2\pi D}^{2\pi} \beta(\omega t) d\omega t} \frac{i_S}{I_{\text{IN}}}(2\pi D) \frac{(\omega t - 2\pi D)^2}{\omega t_f}. \quad (98)$$

The average power dissipated in the switch is

$$\begin{aligned} P_{t_f} &= \frac{V_{\text{IN}} I_{\text{IN}}}{2\pi} \int_{2\pi D}^{2\pi D + \omega t_f} \frac{i_S}{I_{\text{IN}}}(\omega t) \frac{v_{\text{DS}}}{V_{\text{IN}}}(\omega t) d\omega t \\ &\approx P_o \frac{\frac{i_S}{I_{\text{IN}}}(2\pi D)}{\int_{2\pi D}^{2\pi D + \omega t_f} \beta(\omega t) d\omega t} \int_{2\pi D}^{2\pi D + \omega t_f} \left(1 - \frac{\omega t - 2\pi D}{\omega t_f}\right) \frac{(\omega t - 2\pi D)^2}{\omega t_f} d\omega t \\ &= P_o \frac{\frac{i_S}{I_{\text{IN}}}(2\pi D)}{\int_{2\pi D}^{2\pi D + \omega t_f} \beta(\omega t) d\omega t} \frac{\omega t_f^2}{24} = P_o \frac{(\omega t_f)^2}{12}. \end{aligned} \quad (99)$$

The efficiency of the inverter is

$$\eta = \frac{1}{1 + P_{L_1} + P_{\text{DS}} + P_{C_1} + P_{L_2C_2} + P_{L_3C_3} + P_{t_f}}. \quad (100)$$

Table I lists the numerical evaluations for all the power loss equations for the special cases described in the previous section. Fig. 14 compares the efficiencies of all special cases of the Class EF<sub>2</sub> with the Class E as the load resistance varies for two MOSFETs with different on resistances. All of the special case Class EF<sub>2</sub> inverters and the Class E have the same loss resistances of their components. It can be noticed that the Class EF<sub>2</sub> inverter at special cases I and III have the highest efficiencies especially at low load resistance values and with MOSFETs that have a large on resistance. The efficiency improvement of the Class EF<sub>2</sub> become less significant at large load resistances and with MOSFETs that have low on resistances.

### G. Effect of Load Variation

Similar to the Class E inverter, the Class EF<sub>2</sub> inverter is designed to operate at optimum switching conditions for fixed value of  $R_L$ . However, it is interesting to investigate how variations in the load resistance will affect the performance, mainly

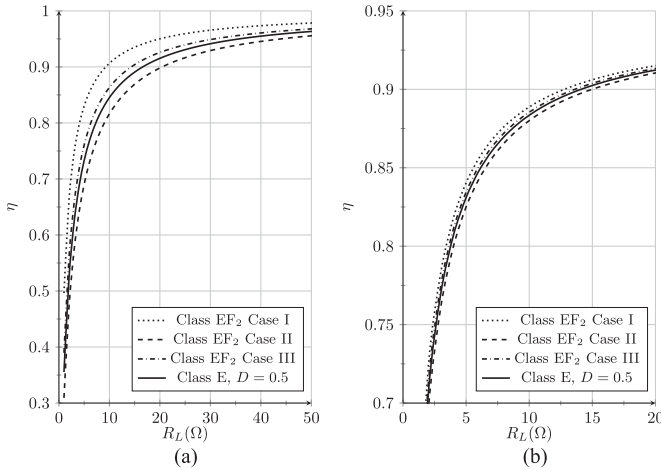


Fig. 14. Comparison between the efficiencies of the Class EF<sub>2</sub> special cases and the Class E for two MOSFETs with different on resistances. The values of the of  $r_f = 0.15 \Omega$ ,  $r_{C_1} = 0.076 \Omega$ ,  $r_{L_2} + r_{C_2} = 0.1 \Omega$ ,  $r_{L_3} + r_{C_3} = 0.55 \Omega$ ,  $t_f = 20\text{ns}$  and  $f = 6.78\text{MHz}$  (a)  $r_{DS} = 0.95 \Omega$  (b)  $r_{DS} = 0.045 \Omega$ .

the switching conditions, of the designed inverter. Fourier analysis will be used to perform the investigation, similar to what was done in [17] for the Class E inverter. The fundamental Fourier component of the switch drain voltage is given by

$$\begin{aligned} \frac{v_{DS1}}{V_{IN}}(\omega t) &= v_{R_L} \sin(\omega t + \phi) + v_{L_x} \cos(\omega t + \phi) \\ &= i_m R_L \sin(\omega t + \phi) + i_m \omega L_x \cos(\omega t + \phi) \end{aligned} \quad (101)$$

where  $v_{R_L}$  and  $v_{L_x}$  are the Fourier coefficients which are also the magnitudes of the voltages across  $R_L$  and  $L_x$ , respectively. Using (15), the voltage magnitudes are equal to

$$p(k+1)R_L = \frac{1}{\pi} \int_{2\pi D}^{2\pi} \frac{v_{DS}}{V_{IN}}(\omega t) \sin(\omega t + \phi) d\omega t \quad (102)$$

$$p(k+1)\omega L_x = \frac{1}{\pi} \int_{2\pi D}^{2\pi} \frac{v_{DS}}{V_{IN}}(\omega t) \cos(\omega t + \phi) d\omega t. \quad (103)$$

Since the series tuned  $L_2 C_2$  network is tuned to the second harmonic of the switching frequency, it therefore, has a zero impedance at the second harmonic. Consequently, the second Fourier component of the switch drain voltage should be zero and this condition results in the following two equations:

$$\int_{2\pi D}^{2\pi} \frac{v_{DS}}{V_{IN}}(\omega t) \sin(2\omega t + \phi) d\omega t = 0 \quad (104)$$

$$\int_{2\pi D}^{2\pi} \frac{v_{DS}}{V_{IN}}(\omega t) \cos(2\omega t + \phi) d\omega t = 0. \quad (105)$$

Equations (102)–(105) in addition to either (16)–(17) or (18)–(19) are now six simultaneous equations with six unknown parameters which are  $p$ ,  $\phi$ ,  $A_1$ ,  $A_2$ ,  $B_1$ , and  $B_2$ , they can be solved for given values of  $k$ ,  $D$ ,  $R_L$ ,  $C_1$ ,  $L_x$ . The voltage and current waveforms throughout the inverter can now be plotted (see Fig. 15) for fixed normalized values of  $k$ ,  $D$ ,  $C_1$ ,  $L_x$  (which are given in Table II) and for different values of  $R_L$ . The resistance  $R_{opt}$  is the value of  $R_L$  at which the inverter was designed to operate at optimum switching conditions.

It can be noticed from the switch drain waveforms in Fig. 15 for all special cases that the inverter operates at a suboptimum switching condition, i.e., ZVS only, when  $R_L$  decreases below its optimum value, and the inverter operates at a nonoptimum switching condition, i.e., hard-switching, when  $R_L$  increases above its optimum value. This switching behavior is similar to that of the Class E inverter [1], [17] in which the operation at a suboptimum switching condition causes the switch drain voltage to become negative before the switch turn-on signal is applied. However, since power MOSFETs are commonly used, their body diode will start to conduct just as the drain voltage reaches  $-0.7\text{V}$ . The inverter in this switching conduction does not suffer from increased voltage and current stress but it suffers from additional turn-on power loss due to the conduction of the body diode. This power loss is usually insignificant [1], [2] and high efficiency can still be maintained for  $R_L < R_{opt}$ . Operation at a nonoptimum switching condition causes the switch drain voltage to remain positive when the switch turn-on signal is applied, and therefore, the switch turns ON at a positive voltage. Consequently, all the energy stored in capacitor  $C_1$  will be dissipated in the switch. The inverter in this switching condition suffers from increased current stresses and additional power loss due to the current impulse resulting from discharging capacitor  $C_1$ . The power loss can be significant, and therefore, the operation when  $R_L > R_{opt}$  is not recommended [1], [2].

#### H. Summary of Design Equations and Parameters for all Special Cases of the Class EF<sub>2</sub> Inverter

Table II summarizes all the design equations and parameters for all the special cases of the Class EF<sub>2</sub> inverter in comparison with the Class E inverter.

## IV. EXPERIMENTAL VERIFICATION AND RESULTS

Experimental verification for all of the defined special cases of the Class EF<sub>2</sub> inverter have been carried out on a 23-W system. A switching frequency of 6.78 MHz was chosen for Cases I and II, and a 8.60-MHz switching frequency was chosen for Case III to demonstrate its capability to operate at higher frequencies. In order to ensure a fair comparison, the same MOSFET, load resistance and inductance  $L_3$  were used when verifying all of the special cases.

### A. Experimental Setup

Beginning with the MOSFET, according to Table II, the peak voltage across the MOSFET is approximately 2.2 times the input voltage. Therefore, it is important to select a MOSFET with a voltage rating that can withstand this voltage in addition to considering a certain safety margin. The inductance of the MOSFET's package should be as small as possible to allow for these megahertz switching frequencies to be achieved and to allow for clean voltage waveforms to be achieved. In addition, the MOSFET's total gate charge should be reasonably low to reduce gate drive losses. Finally, the MOSFET's output capacitance ( $C_o$ ) should be as low as possible, ideally below 500 pF. This is important because a large output capacitance

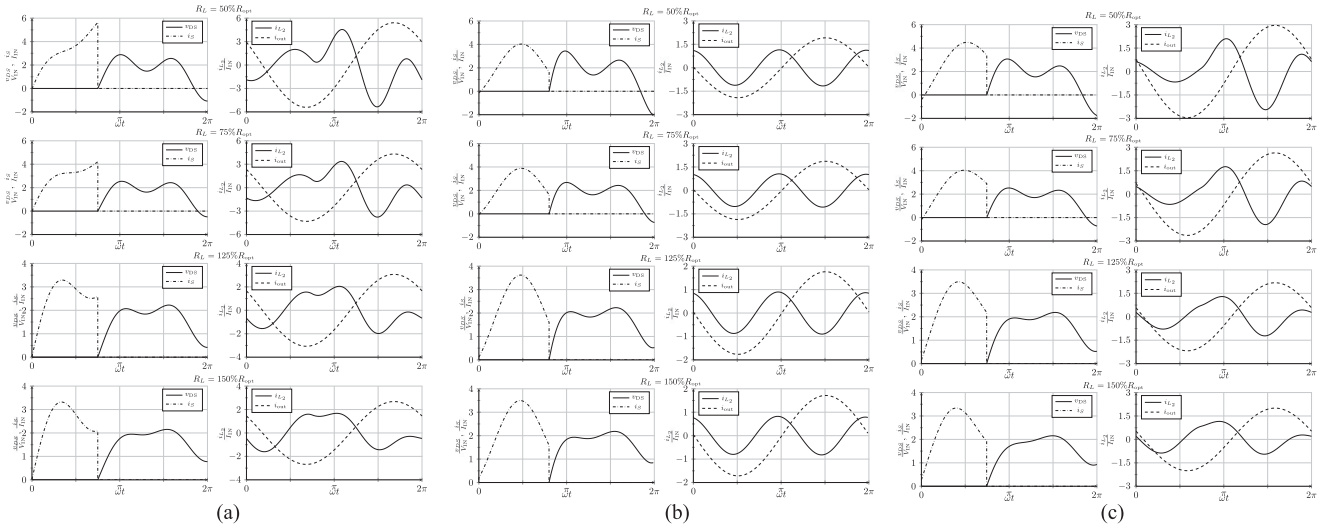


Fig. 15. Voltage and current waveforms of the Class  $EF_2$  inverter for different values of  $R_L$ . Suboptimum switching operation is achieved when  $R_L < R_{opt}$  and nonoptimum switching operation is achieved when  $R_L > R_{opt}$  (a) Case I (b) Case II (c) Case III.

TABLE II  
SUMMARY OF ALL DESIGN EQUATIONS AND PERFORMANCE PARAMETERS

Parameter	Class $EF_2$ Case I (max $c_p$ )	Class $EF_2$ Case II $k \geq 20$	Class $EF_2$ Case III (max $f$ )	Class E $D = 0.5$
$D$	0.3750	0.4000	0.3718	0.5000
$k$	0.867	$\geq 20$	1.567	-
$q_2$	2.9349	$\approx 2$	2.5598	-
$\frac{1}{\omega R_L C_1}$	7.5851	7.7993	5.6857	5.4466
$\frac{1}{\omega R_L C_2}$	6.5762	-	8.9095	-
$\frac{\omega L_x}{R_L}$	2.0339	0.5649	1.1167	1.1525
$\frac{f L_{1min}}{R_L}$	24.1024	6.5516	10.5952	8.6685
$\frac{R_{DC}}{R_L}$	6.4273	1.6379	2.8497	1.7337
$c_p$	0.1323	0.1152	0.1199	0.0981
$\frac{1}{f_{max} R_L C_o}$	47.6644	48.9956	35.7270	19.7394
$\frac{P_o R_L}{V_{IN}^2}$	0.1556	0.6105	0.3509	0.5768
$\frac{v_{DS} \max}{V_{IN}}$	2.3162	2.2964	2.2433	3.5620
$\frac{i_S \max}{I_{IN}}$	3.2632	3.7790	3.7191	2.8620

would prevent the desired switching frequency to be achieved and the nonconstant device capacitances can affect the performance of the inverter. The MOSFET Si892ADN (100 V, 28 A) from Vishay (in a surface mount 1212 package) was found to be suitable. It's maximum on resistance is  $0.047 \Omega$  and has a maximum input capacitance of approximately 850 pF. Its output capacitance is below 400 pF for dc drain voltages above 16 V. The peak voltage across the MOSFET is expected to be 72 V and its peak current is expected to be up to 6 A. The gate driver UCC27321 from Texas Instruments was used and a maximum gate drive voltage of 7.0 V was set for all cases.

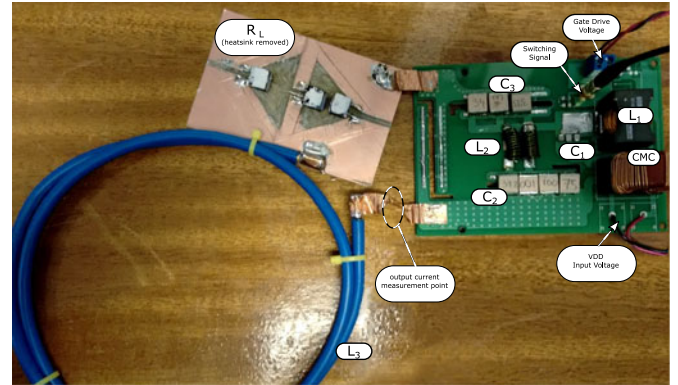


Fig. 16. Photograph of the Class  $EF_2$  inverter and the load inductance.

All the capacitors used were multilayer ceramic capacitors from AVX Corporation. The capacitors belong to the manufacturer's "Hi-Q" series and are designed for RF and microwave applications. Their ESR is below  $0.04 \Omega$  for frequencies below 30 MHz. Inductance  $L_3$  had to be an air-core inductor to avoid the excessive core power losses. It was formed using a coil that consisted of two turns with a diameter of approximately 15 cm and using four AWG copper wire. It's inductance was measured to be approximately  $1.25 \mu\text{H}$  and its ESR is approximately  $0.21 \Omega$ . The load consists of three paralleled  $15\text{-}\Omega$  35-W thick film resistors from Bourns. Each resistor had a maximum inductance of  $0.1 \mu\text{H}$ . Obtaining voltage and current measurements can be difficult when the switching frequency is several megahertz since any voltage and current probe will have an impact on the inverter due to their capacitance and inductance. Therefore, only the MOSFET's drain voltage and the output current will be acquired since the voltage probe's capacitance and the current probe's inductance can be absorbed in the circuit. The current probe N2783A from Keysight Technologies was used to record the output current. The total inductance of the current probe and

TABLE III  
THEORETICAL AND MEASURED PARAMETERS

Power	Class EF <sub>2</sub>		Class EF <sub>2</sub>		Class EF <sub>2</sub>		Class E	
	Case I (max $c_p$ )		Case II ( $k = 20$ )		Case III (max $f$ )		$D = 0.5$	
	Exp.	Theory	Exp.	SPICE	Exp.	Theory	Exp.	SPICE
$C_1$ (pF)	$257 + C_o^*$	589.48	$47 + C_o^*$	$50 + C_o^*$	$257 + C_o^*$	619.98	$330 + C_o^*$	$220 + C_o^*$
$C_2$ (pF)	667	679.92	29.30	28.66	392	395.65	-	-
$C_3$ (pF)	500	501.24	419.20	430.37	268	275.86	447	463
$L_1$ ( $\mu$ H)	47	18.66	47	4.83	47	6.47	47	6.39
$L_2$ (nH)	215	202.61	4800	4810	215	216.41	-	-
$L_3$ ( $\mu$ H)	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35
$R_L$ ( $\Omega$ )	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
$f$ (MHz)	6.78	6.78	6.78	6.78	8.60	8.60	6.78	6.78
$D$	-	0.375	-	0.400	-	0.37	-	0.500
$V_{IN}$ (V)	30.0	30.25	17.49	17.50	20	20.38	16.0	16.0
$I_{IN}$ (A)	0.83	0.83	1.49	1.40	1.20	1.24	1.31	1.38
$P_{IN}$ (W)	24.9	24.97	26.06	24.55	24.0	25.15	20.96	22.08
$P_o$ (W)	22.67	23.00	19.92	18.70	21.26	23.00	18.59	20.00
$\eta$ (%)	$91.1 \pm 2$	92.11	$76.44 \pm 2$	76.17	$88.6 \pm 2$	91.03	$88.7 \pm 2$	90.6
$v_{DSmax}$	72	70.06	48.80	42.26	42.90	44.87	60.1	60.1

$C_o$  is the value of the MOSFET's output capacitance calculated at  $V_{IN}$ .

the load resistors was assumed to be 0.1  $\mu$ H according to their datasheets and was added to the inductance of  $L_3$ . The output power was calculated using the reading of the current probe which has accuracy of about 2%. Fig. 16 shows a photograph of the Class EF<sub>2</sub> inverter hardware.

### B. Global Maximum $c_p$ Case (Case I)

For Case I, the values of capacitors  $C_1$ ,  $C_2$ , and  $C_3$ , in addition to all other parameters, were calculated for a switching frequency of 6.78 MHz using the design equations given in Table II and their values are all listed in Table III. The input voltage was calculated to be 30.25 V and the MOSFET's output capacitance at this voltage was deducted for the calculated value of  $C_1$ . Capacitors  $C_2$  and  $C_3$  each consisted of four parallel capacitors. The difference between the used total capacitance value of  $C_2$  and the theoretical value is due to the parasitic capacitance of the PCB. The value of inductor  $L_2$  was calculated to be 202.61 nH. This inductor was formed by using two paralleled 430 nH air-core inductors from Coilcraft (2929SQ series). The shape of the parallel coils were slightly altered to achieve the desired inductance. According to (50), the current in inductor  $L_2$  contains several frequency components (first, second, and third harmonics), therefore, the inductor's ESR will be different for each one of these components. For simplification, the ESRs at 6.78, 13.56, and 20.34 MHz were calculated according to the manufacturer's datasheet and their average was considered as a constant ESR for the entire switching period, which was equal to 0.18  $\Omega$ . Adding the dc resistance of the paralleled coils and the ESR of capacitor  $C_2$  makes the total ESR in the  $L_2C_2$  branch approximately 0.20  $\Omega$ .

The measured input and output powers, input current and maximum MOSFET voltage are listed in Table III and are compared with their theoretical values. It can be noticed that error between measurements and theory is low. The recorded waveforms of the MOSFET's drain voltage and output current are

shown in Fig. 17(a) and the theoretical waveforms are shown in comparison. It can be noticed that recorded and theoretical waveforms are a close match. The phase shift in the recorded current waveform is due to the response of the current probe. The measured efficiency for this case is  $91.1 \pm 2\%$ .

### C. Maximum Frequency Case (Case III)

The verification and design process for Case III was similar to that of Case I. The switching frequency was increased to 8.60 MHz to show that the Class EF<sub>2</sub> inverter in this case can be operated at higher switching frequencies. This specific switching frequency was chosen in order to keep the same parallel coils for inductor  $L_2$  that were used in Case I. The average ESR for inductor  $L_2$  is now approximately 0.25  $\Omega$ .

The measured input and output powers, input current and maximum MOSFET voltage for this case are listed in Table III. The error between measurements and theory for this case are minor. The recorded waveforms of the MOSFET's drain voltage and output current are shown in Fig. 17(b). and the theoretical waveforms are shown in comparison. The recorded and theoretical waveforms are a close match as well. The measured efficiency for this case is  $88.6 \pm 2\%$ .

### D. $k = 20$ Case (Case II)

For Case II, the switching frequency was decreased back to 6.78 MHz. A  $k$  value of 20 was chosen in order to obtain the lowest inductance value for  $L_2$ , which was calculated to be 4.81  $\mu$ H. The magnetic core T106-2 from Mircometals had to be used to achieve this inductance. The input voltage for a 23-W output power was calculated to be approximately 15.5 V. Although the MOSFET's output capacitance at this voltage is below the required  $C_1$  capacitance, it's nonlinearity in addition to the losses and saturation of the magnetic core of inductor  $L_2$  were quite significant and had an impact on inverter's performance. Therefore, the SPICE model was used to verify the

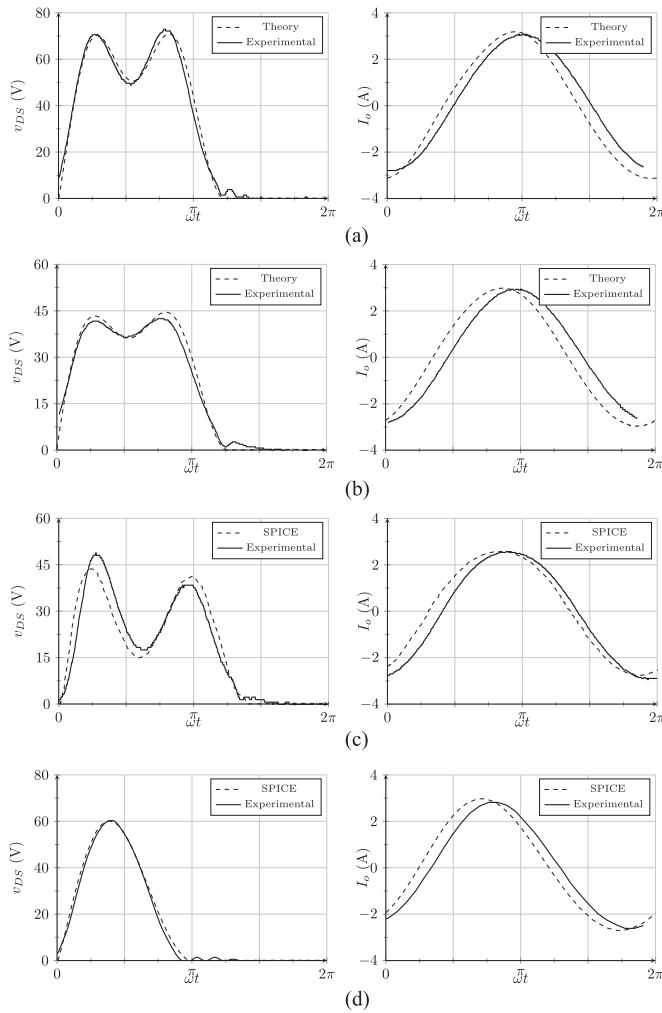


Fig. 17. Measured drain voltage and output current waveforms for Cases I, II, III and for Class E operation (a) Case I (b) Case III (c) Case II (d) Class E operation.

performance of the inverter in this case by simulating the experimental setup. Table II compares the values of all components and the measured input and output powers, input current, and maximum MOSFET voltage in comparison with those of the SPICE simulation. Fig. 17(c) compares between the recorded MOSFET's drain voltage and output current waveforms with the SPICE simulation. It can be noticed that the recorded waveforms are in good agreement with the SPICE simulation. The calculated efficiency was  $76 \pm 2\%$ , the low efficiency is due to the excessive losses and possible saturation in the magnetic core used for inductor  $L_2$ .

### E. Class E Operation

The designed Class EF<sub>2</sub> inverter was then operated as a Class E inverter in order to proof that Case I and III can be more efficient. The switching frequency was kept at 6.78 MHz. The components' values, input and output powers, input current, and maximum MOSFET voltage were calculated from the design equations in [1]. The calculated input voltage was 16 V and

it was also found that the nonlinearity of the MOSFET's output capacitance affected the performance of the inverter, therefore, the SPICE model was used for verification. The component values and measured parameters are listed in Table III. The recorded MOSFET's drain voltage and output current waveforms shown in Fig. 17(d) and an excellent agreement can be seen with the SPICE simulation. The calculated efficiency was  $88.7 \pm 2\%$  which is lower than what had been achieved with Case I and is similar to what had been achieved with Case III as predicted by the theory.

## V. CONCLUSION

This paper presented a detailed analytical analysis on the operation and performance of Class EF and Class E/F inverters. The analysis was performed to investigate the initial reports in the literature about their improved efficiency, reduced voltage, and current stresses compared to the Class E inverter. The Class EF<sub>2</sub> inverter was studied in further detail and three special cases of operation were defined. The special cases are operating at maximum power output capability, maximum frequency operation, and maximum output power. The following conclusions can be made regarding the Class EF<sub>2</sub> inverter.

- 1) The peak voltage across the MOSFET is about 2.2–2.3 times the input dc voltage compared to about 3.56 times the input dc voltage for the Class E inverter.
- 2) Class EF<sub>2</sub> inverters in all special cases have a higher power-output capability than Class E and Class D inverters. Their optimum duty cycle range is between 0.37 and 0.40 compared to a single optimum value of 0.50 for the Class E inverter.
- 3) It was shown that Class EF<sub>2</sub> inverters can operate more efficiently with a low energy storage, or low  $Q$ , series resonant  $LC$  network especially at high frequencies. This is because air-core inductors can be used, which can be designed to have low losses compared to a magnetic-core-based inductor.
- 4) The maximum frequency of operation of the Class EF<sub>2</sub> inverter at maximum power-output capability, as defined in Case III, is slightly less than that of Class E inverters.
- 5) The power dissipation in the MOSFET's on resistance is lower than that of the Class E inverter. This makes special Cases I and III of the Class EF<sub>2</sub> inverter more efficient than Class E inverters especially for on resistances above  $0.04 \Omega$ . The efficiency improvement becomes less significant for MOSFETs with very low on resistances where the Class E inverter might be a better design choice because of its lower number of components.
- 6) For a given load resistance and required output power, the input voltage required for Cases I and III of the Class EF<sub>2</sub> is higher than that of the Class E inverter. A higher input voltage might be beneficial because the input dc current and ripple will be lower, and the MOSFET's nonlinear output capacitance will have a lower impact of the inverter's performance as observed in the experimental results section.

- 7) Special Case II of the Class  $EF_2$  inverter can deliver more power to a load compared to the Class E inverter, however, the efficiency will be lower due to the increased losses in the added resonant network.
- 8) Similar to Class E inverters, Class  $EF_2$  inverters operate at suboptimum switching conditions when  $R_L < R_{opt}$  and nonoptimum switching conditions when  $R_L > R_{opt}$ .

Future work may involve investigating the performance of the Class  $EF_2$  inverter for variations in circuit parameters and loading conditions and identifying the safe operating regions for suboptimum switching conditions. In addition to researching into methods to control and regulate the output power.

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