# A ZVS Grid-Connected Full-Bridge Inverter With a Novel ZVS SPWM Scheme

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***Abstract*—A zero-voltage switching (ZVS) grid-connected full-bridge inverter and its modulation schemes are investigated. A novel sinusoidal pulse width modulation scheme for the ZVS full-bridge inverter (ZVS SPWM) is proposed in this paper. The ZVS SPWM is evolved from the double-frequency SPWM by adding gate drive to the auxiliary switch. The ZVS condition is analyzed and the circulation loss of the resonant branch is optimized by adjusting the energy storage in the resonant inductor. The reverse recovery of the body-diode of MOSFET is relieved and ZVS is realized for both main and auxiliary switches. The filter inductors are significantly reduced with higher switching frequency. The design guideline of resonant parameters and the implementation of ZVS SPWM in DSP controller are introduced. The ZVS SPWM scheme is verified on a 3-kW inverter prototype. According to the experimental result, peak efficiency as 98.8% is achieved.**

***Index Terms*—Full-bridge inverter, pulse width modulation, zero-voltage switching (ZVS).**

## I. Introduction

THE full-bridge inverter is widely used in residential PV generation systems and uninterrupted power supply systems [1]. To reduce the filter size, the inverter is expected to operate with higher frequency whereas the switching frequency is usually limited by switching loss of the power devices. Power MOSFET and IGBT are mostly used in these applications. The switching frequency of MOSFET in full-bridge topology is mainly limited by the inferior dynamic performance of the body-diode. The high *di/dt* and *dv/dt* during the reverse recovery process may also damage the device. IGBT with fast antiparallel diode is used more often than MOSFET in the hard-switching full-bridge inverter. However, IGBT's switching is relatively slower. For these reasons, the switching frequency of hard-switching full-bridge inverter is usually restricted below 20 kHz, which leads to larger filters and lower power density [2].

To relieve the reverse recovery problem of MOSFET, topologies have been proposed by predecessors. Compared to the full-bridge inverter, two extra transistors and two diodes are added in the H6 inverter [3] to deactivate the body-diodes of MOSFETs. The dual buck inverters [4]–[6] use four phase legs which consist of one MOSFET in series with one external diode. Totally four filter inductors are needed. The body-diodes of MOSFETs are bypassed by the external circuit and the reverse recovery loss is reduced in these topologies. However, the switching devices in these topologies still work in hard-switching mode and the switching frequency is still limited by the switching loss.

Another solution to reduce the switching loss and suppress the reverse recovery is the soft-switching technique, which has been investigated by predecessors. The resonant dc link three-phase inverter (RDCL) in [7] and active-clamping resonant dc link three-phase inverter (ACRDCL) in [8] achieve zero-voltage switching for all switching devices. However, both RDCL and ACRDCL inverter use discrete pulse modulation, which causes undesirable subharmonics. In [9], the space vector modulation is adapted to a 30 kW active-clamping three-phase inverter. The reverse recovery of the antiparallel diodes is suppressed successfully and the power quality is improved. A number of soft-switching single-phase inverters are also proposed in recent years [10]–[19]. Active-clamping technique and classical bipolar PWM scheme are applied to the resonant dc-link full-bridge inverter [10]. External slow recovery antiparallel diodes are used and the ZVS condition is obtained by using their high reverse recovery energy. However, the voltage stress of the inverters discussed above is higher than the dc bus voltage. The device voltage of the ZVS dc link single-phase inverter in [11] is clamped to the dc bus voltage by changing the configuration of the auxiliary resonant branch and a modified unipolar PWM scheme is applied to achieve the zero-voltage switching. Besides, soft-switching technique is also applied in the ac side of full-bridge inverters. The full-bridge inverter using a simple ZVS PWM commutation cell [12] achieves zero-voltage switching for main switches and zero-current switching for auxiliary switches. The voltage stress is the same as the dc bus voltage whereas two auxiliary switches are needed. The ZVS inverter proposed in [13] solves the magnetizing current resetting problem in classical coupled-magnetic type ZVS inverter with two coupled inductors in each resonant pole. The maximum efficiency is 98.2%, but its auxiliary circuit is complex. Some key parameters of these soft-switching full-bridge inverters are listed in Table I.

According to the predecessors' research, the dc side ZVS full-bridge inverters [10], [11] have the simplest structure. With this principal advantage, this paper mainly focuses on improving the efficiency and power density of dc side ZVS full-bridge inverter. The ZVS full-bridge inverter is based on the topology proposed in [10]. High circulation loss is found with existing modulation scheme. In order to optimize the efficiency, a novel

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TABLE I
KEY PARAMETERS OF SOFT-SWITCHING FULL-BRIDGE INVERTERS

| Topology | Auxiliary switches | $P_o$ | $f_s$ | Maximum efficiency |
|---|---|---|---|---|
| Active-clamping dc link [10] | 1 | 7 kW | 20 kHz | 90.2% |
| ZVS dc link [11] | 1 | 0.3 kW | 50 kHz | 96.0% |
| ZVS PWM commutation cell [12] | 2 | 3 kW | 32 kHz | 94.6% |
| ZVS PWM coupled magnetics [13] | 4 | 3 kW | 20 kHz | 98.2% |

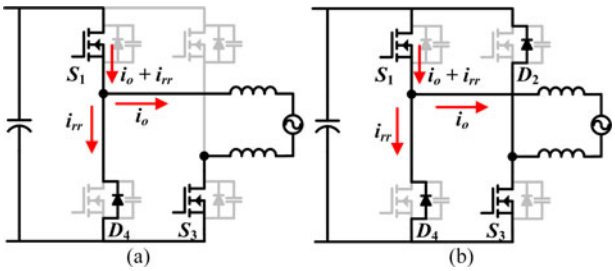


Fig. 1. (a) Commutation at one phase leg. (b) Commutations at both phase legs.

ZVS SPWM scheme is proposed. For the purpose of realizing the ZVS condition, an adjustable short-circuit stage controlled by the short-circuit pulse in every switching cycle is designed to reset the energy in the auxiliary resonant branch [20], [21]. The duration of the short-circuit stage varies according to the different load condition for optimizing the efficiency in both light and heavy load cases. The ZVS condition will be analyzed and the design procedure for the ZVS SPWM will be presented in this paper. MOSFETs are utilized and zero-voltage switching for both main and auxiliary switches is realized. The filter is reduced with higher switching frequency and a 3 kW prototype is built to verify the theoretical analysis.

## II. NOVEL ZVS SPWM SCHEME FOR ZVS FULL-BRIDGE INVERTER

The reverse recovery of the body-diode is a severe trouble in the MOSFET full-bridge inverter, which occurs during the commutation from the body-diode to the MOSFET. Fig. 1 shows two types of such commutation in the MOSFET full-bridge inverter. For unipolar SPWM and double-frequency (DF) SPWM the commutation appears at only one phase leg as shown in Fig. 1(a). Fig. 1(b) shows the commutation process at both phase legs when bipolar SPWM is used. The simplified switching waveforms in Fig. 2 show that the MOSFET ($S_1$) suffers not only the load current ($i_o$) but also the high reverse recovery current ($i_{rr}$) of the body-diode ($D_4$) during the hard-switching turn-on process, which not only makes higher turn-on loss, but also cause high current stress to the switch.

In Fig. 3, an auxiliary branch is installed between the dc bus and the inverter. It is composed of an auxiliary MOSFET $S_{\rm a}$, clamping capacitor $C_c$, resonant inductor $L_r$ and resonant capacitor $C_{ra}$. The capacitors $C_{r1} \sim C_{r4}$ are paralleled capacitors to the main switches. Before the commutation from body-diode to MOSFET in Fig. 3, the auxiliary switch $S_a$ is turned off and the dc voltage $V_{\rm dc}$ across the phase leg can be resonated to zero by the resonant process. Therefore, the main switches achieve ZVS turn-on.

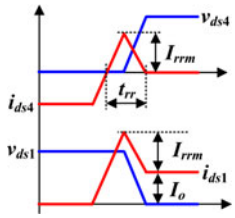


Fig. 2. Hard-switching turn-on waveforms.

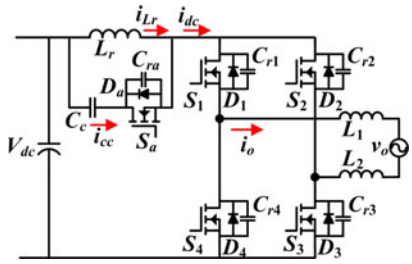


Fig. 3. ZVS full-bridge inverter.

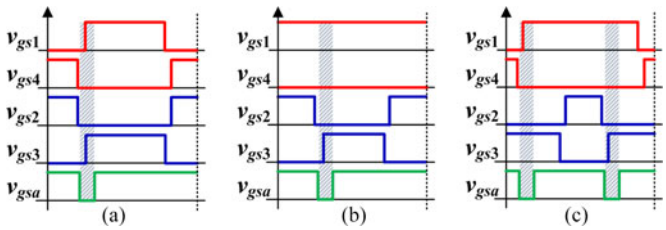


Fig. 4. $v_{gsa}$ with (a) bipolar SPWM, (b) unipolar SPWM, (c) DF SPWM.

The drive pulses based on bipolar SPWM proposed in [10] is shown in Fig. 4(a). The waveforms show the situation in the positive half cycle with unity power factor. In one switching period, the auxiliary switch is turned off by drive pulse $v_{gsa}$ before main switch $S_1$ and $S_3$ are turned on. Since there is no reverse recovery during the commutation from $S_1$ to $D_4$ and $S_3$ to $D_2$, the auxiliary switch does not need to take switching action.

Similarly the drive pulse $v_{gsa}$ based on unipolar SPWM and DF SPWM can be derived from the bipolar SPWM as shown in Fig. 4(b) and (c). For unipolar SPWM the auxiliary switch is turned off and on once in a switching period while it is turned off and on twice for DF SPWM. The reason is that in the case of DF SPWM the modulation waves of each phase leg have a 180° phase shift so that the commutations from body-diode to MOSFET of each phase leg are separated.

With different SPWM schemes the resonant process after turning off the auxiliary switch can be separated into two types. Fig. 5 shows the resonant circuit with bipolar SPWM and its

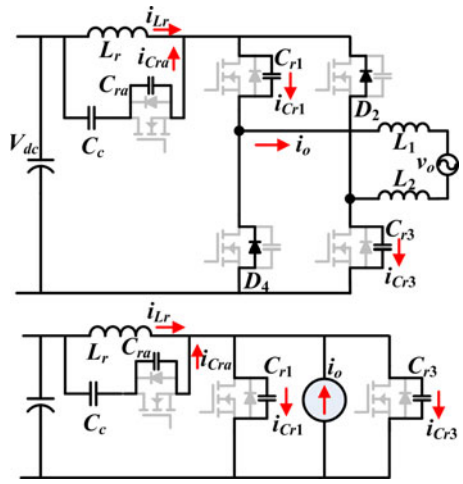


Fig. 5. Resonant circuit with bipolar SPWM in [10].

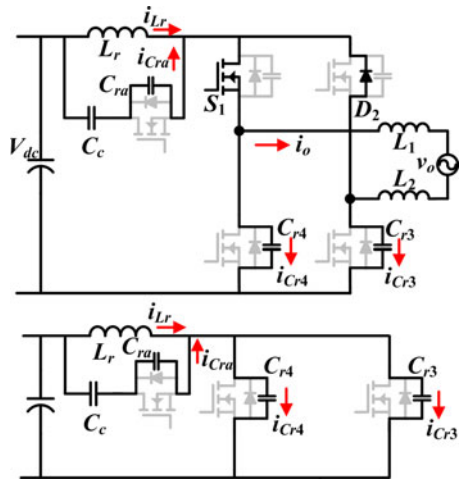


Fig. 6. Resonant circuit with unipolar and DF SPWM.

equivalent circuit. The arrows signify the reference direction of the currents. The relationship of the resonant currents is given in (1)

$$i_{Lr} + i_{Cra} + i_o = i_{Cr1} + i_{Cr2}. \tag{1}$$

Equation (2) is derived from (1) with consideration of their actual directions. It shows that the current in the resonant inductor $L_{\rm r}$ not only discharges the parallel capacitors but also provides the load current

$$i_{Lr} = -|i_{Cr1}| - |i_{Cr2}| - |i_{Cra}| - |i_o| = -|i_{Lr}|. \tag{2}$$

Fig. 6 shows the resonant circuit with unipolar SPWM and DF SPWM. The current in the resonant inductor $L_{\rm r}$ discharges the parallel capacitors of main switches and charges the parallel capacitor of auxiliary switch. The load current is still freewheeling and does not participate in the resonant process. Their relationship can be obtained

$$i_{Lr} + i_{Cra} = i_{Cr1} + i_{Cr2} \tag{3}$$

$$i_{Lr} = -|i_{Cr3}| - |i_{Cr4}| - |i_{Cra}| = -|i_{Lr}|. \tag{4}$$

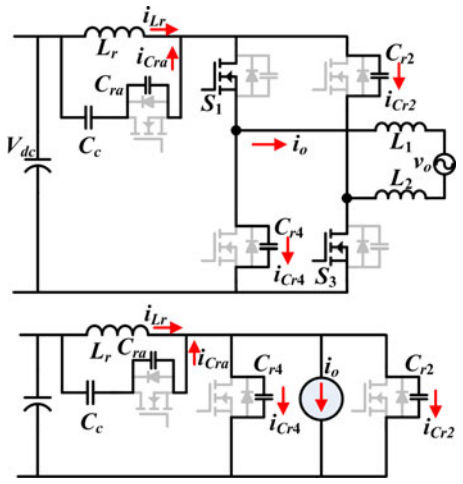


Fig. 7. Second resonant process for ZVS turn-on of auxiliary switch.

According to (2) and (4), it can be found that the amplitude of resonant current $i_{Lr}$ is larger with bipolar SPWM, which may cause higher loss in the resonant inductor.

Another advantage of the ZVS full-bridge inverter is that the auxiliary switch is also ZVS turned on, which is realized by the second resonant process after the ZVS turn-on of main switches. After this commutation $S_2$ and $S_4$ should be turned off with all the three SPWM schemes so the paralleled capacitors of main switches $S_2$ and $S_4$ are charged in the second resonant process. The resonant circuit is shown in Fig. 7. Similarly, (5) and (6) are derived

$$i_{Lr} + i_{Cra} = i_{Cr2} + i_{Cr4} + i_o \tag{5}$$

$$i_{Lr} = |i_{Cr2}| + |i_{Cr4}| + |i_{Cra}| + |i_o| = |i_{Lr}|. \tag{6}$$

Eq. (6) indicates that the actual direction of the resonant current $i_{Lr}$ is reversed and its amplitude before the second resonant process must be charged larger than the sum of the load current and the resonant currents in the paralleled capacitors. A charging method with the reverse recovery current of diode is used in [10]. The main switches $S_1$ and $S_3$ are ZVS turned on after the resonant process in Fig. 6. The diodes $D_2$ and $D_4$ begin their reverse recovery stage and the resonant inductor is charged by the reverse recovery current. In order to guarantee enough resonant energy for a wide power range, four external diodes with high reverse recovery current are used to antiparallel with each main switch. However, the uncontrollable reverse recovery current increases the circulation loss in light load condition.

In this paper, a novel resonant inductor energy charging method using the short-circuit pulse is proposed. The charging circuits and the proposed charging method with DF SPWM are presented in Fig. 8(b) and (c). A short-circuit pulse is superposed over each drive pulse of main switches. Instead of the antiparalleled diodes, the charging path is realized by turning on the four main switches with the short-circuit pulse. The resonant inductor is charged by the dc side voltage source and its energy can be adjusted by the width of the short-circuit pulse according to the instant amplitude of load current.

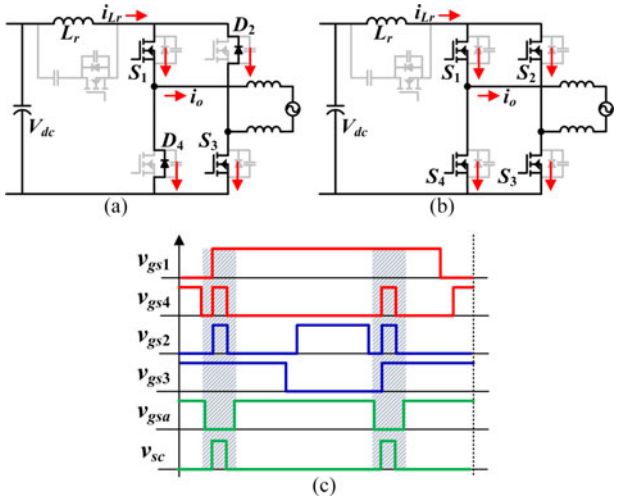


Fig. 8. (a) Charging circuit with bipolar SPWM. (b) Charging circuit with proposed method. (c) Drive pulse of proposed method with DF SPWM.

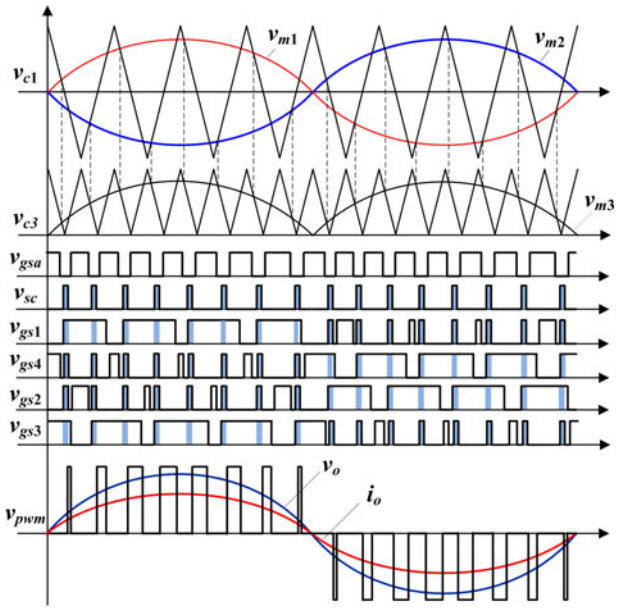


Fig. 9. Novel ZVS SPWM scheme.

Comparing with the unipolar SPWM, DF SPWM has the advantage of lower current ripple and reduced harmonics [22], which is beneficial to reduce the filter. Hence, the novel ZVS SPWM proposed in this paper is the combination of the DF SPWM and the short-circuit pulse. The switching sequence for unity power factor application is presented in Fig. 9. In the positive half cycle of the load current the reverse recovery of body-diode appears during the commutation from $D_4$ to $S_1$ (falling edge of $v_{c1}$ equals to $v_{m1}$) and $D_2$ to $S_3$ (rising edge of $v_{c1}$ equals to $v_{m2}$). In the negative half cycle the commutation from body-diode to MOSFET occurs when the falling edge of $v_{c1}$ equals to $v_{m2}$ ($D_3$ to $S_2$) and rising edge of $v_{c1}$ equals to $v_{m1}$ ($D_1$ to $S_4$). In every cycle of the triangle carrier $v_{c1}$ there are two such commutations so the frequency of triangle carrier $v_{c3}$ is designed to be twice of the triangle carrier $v_{c1}$ to synchronize the auxiliary switch (falling edge of $v_{c3}$ equals to $v_{m3}$). The short-circuit pulse ($v_{\rm sc}$) is complementary to the auxiliary drive pulse ($v_{gsa}$) with small delay.

## III. Operation Stages With Novel ZVS SPWM

The operation stages with the proposed ZVS SPWM are given as follows. The switching waveforms in a switching period and operation circuits are shown in Figs. 10 and 11. The analysis is based on the steady operation state. The output filters ($L_1$ and $L_2$) and the clamping capacitor ($C_c$) are supposed to be large enough so the load current and the voltage across the clamping capacitor ($V_{cc}$) could be treated as constants in a switching period. The output filters and the grid are replaced by an ideal sinusoidal current source for simplification. The resonant capacitor paralleled with MOSFET represents the parasitic capacitance and the external capacitor. The resonant capacitors of the main switches have equal capacitance.

*Stage 1 (Freewheel, $t_0 - t_1$):* The load current $i_{\rm o}$ is freewheeling through the main switches $S_3$ and $S_4$. The voltage across the resonant inductor $L_r$ is clamped to $-V_{cc}$ and the slope of its current $i_{Lr}$ is

$$di_{Lr}/dt = -V_{cc}/L_r. \tag{7}$$

*Stage 2 (Freewheel, $t_1 - t_2$):* The main switch $S_4$ is turned off at $t_1$ by SPWM. The load current $i_o$ is freewheeling through the main switch $S_3$ and the body diode $D_4$.

*Stage 3 (Resonance, $t_2 - t_3$):* The gate-source voltage ($v_{gsa}$) of auxiliary switch $S_a$ is set to zero at $t_2$ by ZVS SPWM. Thanks to the ultrafast switching speed of the superjunction MOSFET, the drain-source channel of $S_a$ is turned off rapidly. The resonant capacitors $C_{r1}$ and $C_{r2}$ are discharged while $C_{ra}$ is charged by the resonant inductor. The initial resonant current $i_{Lr}$ at $t_2$ is defined as $I_{\rm res1}$. During the resonant process the current $i_{Lr}$ reaches its minimum value $I_{\rm min}$. Stage 3 ends when the voltage across capacitors $C_{r1}$ and $C_{r2}$ is discharged to zero. The equivalent circuit of stage 3 is the same as the equivalent circuit in Fig. 6.

*Stage 4 (Charging, $t_3 - t_4$):* After the voltage of main switches $S_1$ and $S_2$ resonates to zero, the body-diodes ($D_1$ and $D_2$) turn on. The voltage of both phase legs is clamped to zero and the ZVS turn-on of main switches $S_1$ and $S_2$ is achieved. The voltage across the resonant inductor $L_r$ is clamped to $V_{\rm dc}$. The current in resonant inductor begins to increase and the slope is

$$di_{Lr}/dt = V_{\rm dc}/L_r. \tag{8}$$

Then the short-circuit pulse is sent to all the main switches before the current in resonant inductor increases to zero and Stage 4 is finished.

*Stage 5 (Short-Circuit and Charging, $t_4 - t_5$):* Main switches $S_1$, $S_2$ and $S_4$ are ZVS turned on by the short-circuit pulse at $t_4$. The current $i_{Lr}$ keeps increase through the MOSFETs with the same slope. The body-diodes are bypassed because of the low on resistance of MOSFET and the reverse recovery is relieved. At $t_5$, the current $i_{Lr}$ is equal to $I_{\rm sc}$.

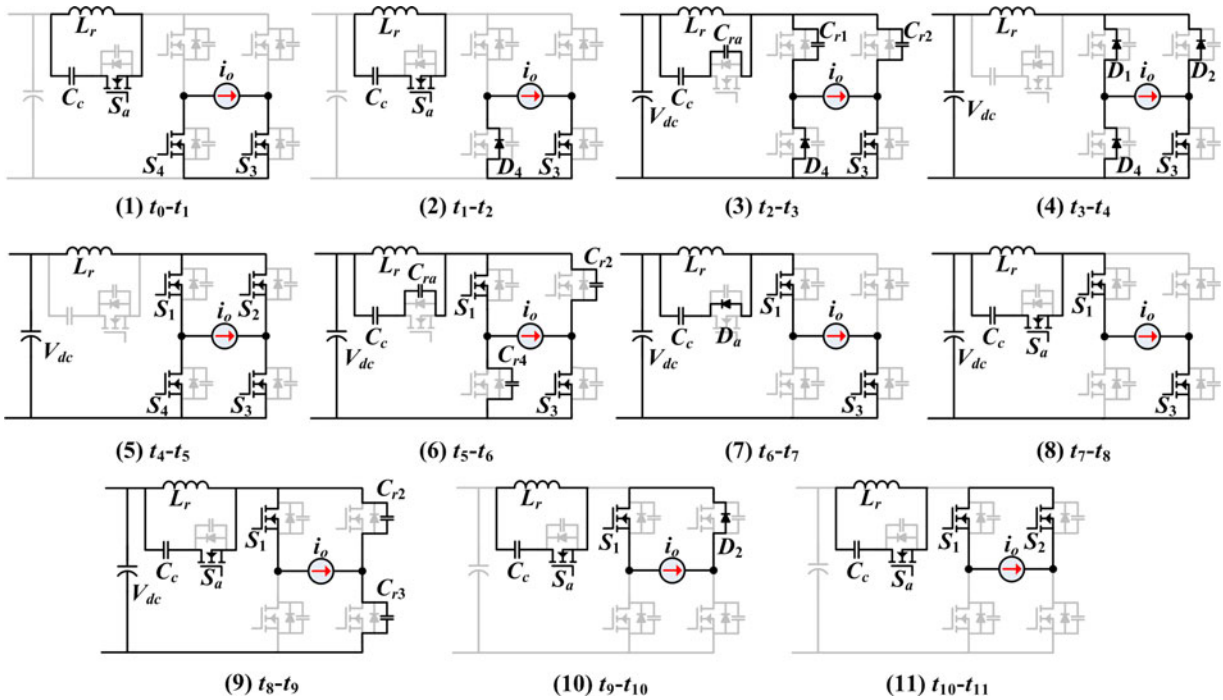


Fig. 10. Operation stages with ZVS PWM.

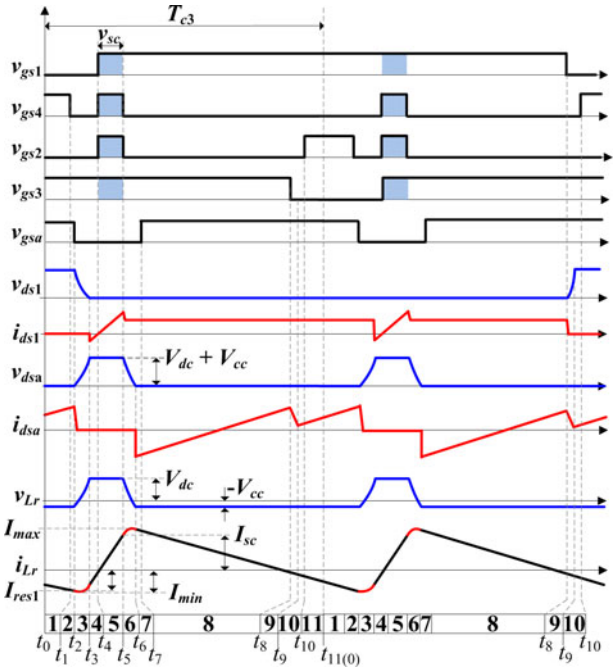


Fig. 11. Voltage and current waveforms of proposed ZVS SPWM.

*Stage 6 (Resonance, $t_5 - t_6$):* At $t_5$, the short-circuit pulse $v_{\rm sc}$ is removed from all the main switches. $S_1$ and $S_3$ keep turning on by the high level drive pulse of DF SPWM. The drain-source channels of $S_2$ and $S_4$ are turned off rapidly without the short-circuit pulse. Then capacitors $C_{r2}$ and $C_{r4}$ are charged while $C_{ra}$ is discharged by the resonant inductor. The current in resonant inductor $i_{Lr}$ reaches its maximum value $I_{\rm max}$ during the resonant process. Stage 6 ends when the voltage across capacitor $C_{ra}$ is discharged to zero. The load current $i_o$ flows through main switches $S_1$ and $S_3$ and the commutation from the body-diode $D_3$ to main switch $S_1$ finishes. Similarly as stage 3, the equivalent circuit of stage 6 is the same as that in Fig. 7.

*Stage 7 (Clamping, $t_6 - t_7$):* The body-diode ($D_a$) of auxiliary switch turns on at $t_6$. The drain-source voltage $v_{dsa}$ is clamped to zero and the voltage across the resonant inductor is $-V_{cc}$. The dc voltage source begins to transfer energy to the grid.

*Stage 8 ($t_7 - t_8$):* The auxiliary switch $S_a$ is ZVS turned on at $t_7$. The durations from $t_6$ to $t_8$ depend on the SPWM.

*Stage 9 ($t_8 - t_9$):* The drain-source channel of $S_3$ is turned off rapidly at $t_8$ by SPWM. The charging of capacitor $C_{r3}$ and the discharging of capacitor $C_{r2}$ both help the ZVS turn-on of main switch $S_2$ and ZVS turn-off of main switch $S_3$.

*Stage 10 ($t_9 - t_{10}$):* The voltage across resonant capacitor $C_{r2}$ is discharged to zero by the load current $i_{\rm o}$ and the body-diode ($D_2$) of main switch $S_2$ turns on at $t_9$. Main switch $S_2$ is ZVS turned on by SPWM at $t_{10}$. The duration of stage 9 and stage 10 ($t_8 \sim t_{10}$) is the dead-time of SPWM.

*Stage 11 ($t_{10}$–$t_{11}$):* Main switch $S_2$ is ZVS turned on by the SPWM. This stage is similar to stage 1.

## IV. Analysis of ZVS Condition

The resonant inductor experiences four operation modes: charging by $V_{\rm dc}$ ($t_3 - t_5$), discharging by $V_{cc}$($t_0 - t_2, t_6 - t_{11}$) and two resonant processes ($t_2 - t_3$, $t_5 - t_6$) in a switching cycle. The operation modes are very similar to the buck-boost converter and the clamping capacitor $C_{\rm c}$ can be treated as the output capacitor. In steady operation the voltage-second balance

principle is used for the resonant inductor

$$\Delta i_{Lr} = \frac{1}{L_r}\int_0^{t_{11}} v_{Lr}dt = \frac{1}{L_r}\left(-\int_0^{t_2} V_{cc}dt + \int_{t_2}^{t_3} v_{Lr}dt + \int_{t_3}^{t_5} V_{dc}dt + \int_{t_5}^{t_6} v_{Lr}dt - \int_{t_6}^{t_{11}} V_{cc}dt\right) = 0. \quad (9)$$

Since the resonant processes are shorter, if we ignore the resonant stages, (9) can be simplified as follows:

$$V_{dc}\left(t_6 - t_2\right) - V_{cc}\left(T_{c3} - \left(t_6 - t_2\right)\right) \approx 0 \quad (10)$$

where $T_{c3}$ is the switching period of the carrier wave $v_{c3}$. The voltage of the clamping capacitor can be derived

$$V_{cc} = V_{dc}\left(1 - D_a\right)/D_a, D_a = \left(T_{c3} - \left(t_6 - t_2\right)\right)/T_{c3}. \quad (11)$$

$D_a$ is also defined as the duty ratio of the auxiliary switch. It can be found that the voltage of the clamping capacitor is controlled by the duty ratio of the auxiliary switch.

According to the equivalent circuit of stage 3 in Fig. 6, following equations can be derived to describe the resonant process:

$$\begin{cases} L_r\dfrac{di_{Lr}}{dt} + v_{Crm} = V_{\rm dc} \\ i_{Lr} + C_{ra}\dfrac{dv_{Cra}}{dt} = 2C_{rm}\dfrac{dv_{Crm}}{dt} \\ \dfrac{dv_{Cra}}{dt} + \dfrac{dv_{Crm}}{dt} = 0 \end{cases} \quad (12)$$

where it is assumed that $C_{r1} = C_{r2} = C_{r3} = C_{r4} = C_{rm}$. The initial condition of (12) can be given as

$$i_{Lr}\left(t_2\right) = I_{\rm res1}, v_{Crm}\left(t_2\right) = V_{\rm dc} + V_{cc}. \quad (13)$$

Solving the resonant equations with (13), we get

$$v_{Crm}(t) = V_{\rm dc} - \sqrt{V_{cc}^2 + |I_{res1}|^2 Z_r^2}\sin\left(\omega(t - t_2) - \varphi_1\right) \quad (14)$$

$$i_{Lr}(t) = -\frac{1}{Z_r}\sqrt{V_{cc}^2 + |I_{\rm res1}|^2 Z_r^2}\cos\left(\omega(t - t_2) - \varphi_1\right) \quad (15)$$

where

$$\omega = \frac{1}{\sqrt{L_r\left(2C_{rm} + C_{ra}\right)}},\ Z_r = \sqrt{\frac{L_r}{2C_{rm} + C_{ra}}},$$
$$\varphi_1 = \arctan\left(\frac{V_{cc}}{|I_{res1}|\,Z_r}\right). \quad (16)$$

The theoretical waveforms of $i_{Lr}$ and $v_{Crm}$ from $t_2$ to $t_3$ are drawn in Fig. 12 with (14) and (15). To realize ZVS condition for main switches in the full-bridge inverter, voltage $v_{Crm}$ represented by (14) is expected to resonate to zero. Therefore, the following inequality needs to be satisfied:

$$v_{Crm\_\min} = V_{\rm dc} - \sqrt{V_{cc}^2 + |I_{\rm res1}|^2 Z_r^2} \le 0. \quad (17)$$

Then $I_{\rm res1}$ needs to satisfy the inequality

$$|I_{\rm res1}| \ge \sqrt{V_{\rm dc}^2 - V_{Cc}^2}/Z_r. \quad (18)$$

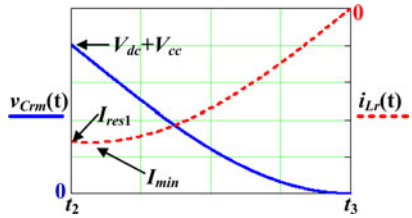


Fig. 12. Theoretical resonant waveforms of stage 3.

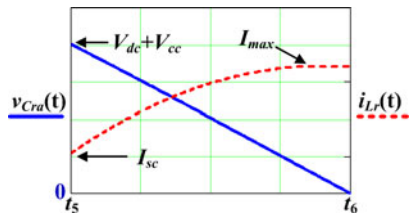


Fig. 13. Theoretical resonant waveforms of stage 6.

For another resonant stage, i.e., stage 6, similarly the resonant equation is obtained

$$\begin{cases} L_r\dfrac{di_{Lr}}{dt} + V_{cc} = v_{Cra} \\ i_{Lr} + C_{ra}\dfrac{dv_{Cra}}{dt} = 2C_{rm}\dfrac{dv_{Crm}}{dt} + |i_o| \\ \dfrac{dv_{Cra}}{dt} + \dfrac{dv_{Crm}}{dt} = 0. \end{cases} \quad (19)$$

The initial condition of (19) is

$$i_{Lr}\left(t_5\right) = I_{\rm sc}, v_{Cra}\left(t_5\right) = V_{\rm dc} + V_{cc}. \quad (20)$$

By solving (19) with (20), we obtain

$$v_{Cra}(t) = V_{cc} - \sqrt{V_{\rm dc}^2 + (I_{\rm sc} - |i_o|)^2 Z_r^2}\sin\left(\omega\left(t - t_5\right) - \varphi_2\right) \quad (21)$$

$$i_{Lr}(t) = \sqrt{V_{\rm dc}^2/Z_r^2 + (I_{sc} - |i_o|)^2}\cos\left(\omega\left(t - t_5\right) - \varphi_2\right) + |i_o| \quad (22)$$

$$\varphi_2 = \arctan\left(\frac{V_{dc}}{(I_{sc} - |i_o|)\,Z_r}\right). \quad (23)$$

The theoretical resonant waveforms are shown in Fig. 13. Similarly, we can get the ZVS condition

$$v_{Cra\_\min} = V_{cc} - \sqrt{V_{\rm dc}^2 + (I_{\rm sc} - |i_o|)^2 Z_r^2} \le 0. \quad (24)$$

If $V_{cc} < V_{\rm dc}$, the ZVS condition in (24) is always satisfied. Therefore, the voltage across the clamping capacitor must be lower than the dc side voltage. With (11), we get

$$V_{\rm dc}\left(1 - D_a\right)/D_a \le V_{\rm dc}, D_a \ge 0.5. \quad (25)$$

The condition above is generally satisfied with proper resonant parameters in the practice. Therefore, the ZVS condition for stage 6 can be always taken as exist.

So far the ZVS conditions for the main switches and auxiliary switch are given in (18) and (25). In order to make the ZVS condition more clear, further derivations are made. First the relationship among currents in the resonant branch can be derived from Fig. 3

$$i_{\rm dc} = i_{cc} + i_{Lr} \tag{26}$$

where $i_{\rm dc}$ is the input current from the dc side and it is also equal to the load current from $t_6$ to $t_8$

$$i_{\rm dc} = \begin{cases} |i_o|, & t_6 \le t \le t_8 \\ 0, & 0 \le t < t_6 \ or \ t_8 < t \le t_{11}. \end{cases} \tag{27}$$

Then the average value of $i_{\rm dc}$ in a switching cycle is obtained

$$\langle i_{dc} \rangle_{T_{c3}} = \langle i_{cc} \rangle_{T_{c3}} + \langle i_{Lr} \rangle_{T_{c3}} = |i_o| (t_8 - t_6) / T_{c3}. \tag{28}$$

The clamping capacitor is supposed large enough and the ampere-second balance principle is also satisfied in steady operation

$$\Delta v_{Cc} = \frac{1}{C_c} \int_0^{T_{c3}} i_{cc} dt = \frac{1}{C_c} \langle i_{Cc} \rangle_{T_{c3}} = 0. \tag{29}$$

Combining (28) with (29), we get

$$\langle i_{Lr} \rangle_{T_{c3}} = |i_o| (t_8 - t_6) / T_{c3} = D_o |i_o| \tag{30}$$

where $D_{\rm o}$ is the duty ratio of the SPWM in each switching cycle. The current waveform of the resonant inductor in Fig. 11 is similar to a triangular wave and the average current of the resonant current can be approximately expressed as (31)

$$\langle i_{Lr} \rangle_{T_{c3}} \approx (I_{\max} + I_{\min}) / 2 = D_o |i_o|. \tag{31}$$

$I_{\min}$ and $I_{\max}$ in (31) represent the minimum current and the maximum current of resonant inductor in each switching cycle. They can be obtained respectively from (15) and (22)

$$I_{\min} = -\sqrt{V_{cc}^2 + |I_{\rm res1}|^2 Z_r^2} / Z_r \le -V_{\rm dc} / Z_r \tag{32}$$

$$I_{\max} = |i_o| + \sqrt{V_{\rm dc}^2 + (I_{\rm sc} - |i_o|)^2 Z_r^2} / Z_r. \tag{33}$$

Combining (32), (33) with (31), we can get the expression of the undetermined $I_{\rm sc}$

$$I_{\rm sc} \ge \begin{cases} \sqrt{|i_o| \cdot (2D_o - 1) \left( |i_o| \cdot (2D_o - 1) + 2 \dfrac{V_{\rm dc}}{Z_r} \right)} + |i_o|, \\ \qquad\qquad 2D_o - 1 \ge 0 \\ |i_o|, \quad 2D_o - 1 < 0. \end{cases} \tag{34}$$

Eq. (34) describes the energy required in resonant inductor for ZVS, which is also equivalent to the ZVS condition of stage 3. The minimum amplitude of $I_{\rm sc}$ is decided by the dc input voltage, the load current and the resonant parameters. And it can be controlled by the width of the short-circuit pulse, which is from $t_4$ to $t_5$

$$I_{\rm sc} = (t_5 - t_4) V_{\rm dc} / L_r. \tag{35}$$

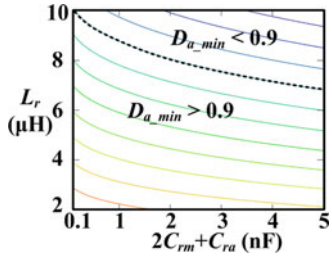


Fig. 14. Resonant parameters with $Da_{\min} < 0.9$.

## V. Design of ZVS Parameters

The rate power of the prototype is 3 kW. The dc bus voltage $V_{\rm dc}$ is 360 V and the grid voltage $V_o$ is 230 V (rms). The frequency of carrier wave $v_{\rm c1}$ in Fig. 9 with the proposed ZVS SPWM is 50 kHz. Therefore, the frequency of $v_{c3}$ and the ripple frequency of the load current is 100 kHz. This paper mainly focuses on the modulation scheme and the efficiency of ZVS full-bridge inverter. For this reason single L-type filter is used to simplify the ZVS analysis and control model. Each filter inductor is designed to be 190 $\mu$H so that the maximum ripple (peak to peak) is less than 25% with full load and EE55 ferrite core is utilized to reduce the core loss with such high frequency. The resonant parameters are designed based on the following guideline.

### A. Duty Ratio of Auxiliary Switch $S_a$

The duty ratio of auxiliary switch $S_a$ is defined in (11). If we ignore the short resonant processes, $D_a$ can be approximately calculated by (36)

$$D_a \approx 1 - L_r \frac{I_{\max} - I_{\min}}{V_{\rm dc} T_{c3}} = 1 - \frac{2D_o |i_o| L_r}{V_{\rm dc} T_{c3}} - \frac{2L_r}{Z_r T_{c3}}. \tag{36}$$

First $D_a$ should be larger than 0.5 according to (25). Then $D_a$ is expected to be as large as possible to reduce the voltage of clamping capacitor according to (11). When the auxiliary switch is turned off by $v_{gsa}$, the voltage across both phase legs is clamped to zero and the inverter cannot transfer active power to the grid. In order to guarantee the active power capability the maximum duration from stage 3 to stage 6 should be smaller than the freewheeling time of SPWM. Therefore, the duty ratio of auxiliary switch $S_{\rm a}$ is designed to be equal or greater than 0.9. The minimum duty ratio $D_{a\_\min}$ in (36) occurs with the peak load current of 3 kW. The values of resonant capacitors and inductor are numerically solved and shown in Fig. 14.

### B. Maximum Current of MOSFET

In stage 3 the current in body-diode $D_4$ is the sum of load current and the resonant current of $C_{r1}$. The maximum current in $D_4$ is

$$\begin{aligned} I_{sd\_\max} &= |i_o| + C_{rm} \omega \sqrt{V_{cc}^2 + |I_{\rm res1}|^2 Z_r^2} \\ &= |i_o| + C_{rm} \omega V_{\rm dc}. \end{aligned} \tag{37}$$

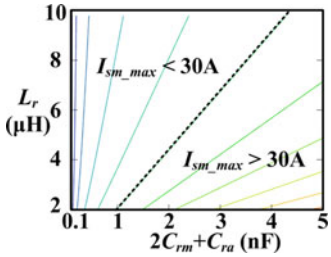


Fig. 15. Resonant parameters with $Ism_{\max} < 30$ A.

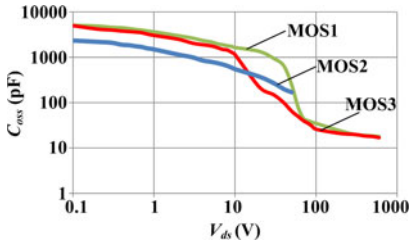


Fig. 16. Output capacitance of MOSFETs.

In stage 6 the load current and the resonant current flow through the main switches $S_1$ and $S_3$. The maximum current in $S_1$ and $S_3$ is

$$I_{sm\_\max} = |i_o| + C_{rm}\omega\sqrt{V_{\rm dc}^2 + (I_{\rm sc} - |i_o|)^2 Z_r^2}. \quad (38)$$

The maximum current of auxiliary switches occurs at $t_6$ and it can be approximately calculated by (39)

$$\begin{aligned} I_{sa\_\max} &= i_{sa}(t_6) \approx I_{\max} - |i_o| \\ &= \sqrt{V_{\rm dc}^2 + (I_{\rm sc} - |i_o|)^2 Z_r^2}/Z_r. \end{aligned} \quad (39)$$

Comparing (37), (38) and (39), we find that $I_{sm\_\max}$ is the maximum one. The maximum continuous drain current of the 650 V superjunction MOSFET is usually below 60 A. For safety operation and higher efficiency the maximum current of the MOSFET is designed to be lower than 30 A. Then the second solution region of the resonant parameters can be solved as shown in Fig. 15.

### C. Resonant Capacitor

Unlike the ZVS turn-on process, switching loss still exists in the turn-off processes in stage 3, stage 6 and stage 9. In the previous assumption the resonant capacitor includes the parasitic output capacitance $C_{oss}$ of the MOSFET and external capacitor. The output capacitance from the datasheet is shown in Fig. 16. The capacitance is relatively high with low drain-source voltage, which keeps the rise rate of the drain-source voltage very low. Meanwhile the drain-source channel is rapidly cut off in less than 10 ns so that the turn-off loss of superjunction MOSFET is quite low [23].

According to the definition in the datasheet the parasitic capacitance can be replaced by the energy related output capacitor ($C_{osse}$), which is usually from 100 to 300 pF for a 650 V superjunction MOSFET. The external capacitors ($C_{\rm ext}$) are still needed for the main switches in case of the inconsistency of the parasitic capacitance. The resonant capacitors of the auxiliary switch and main switches can be regarded as

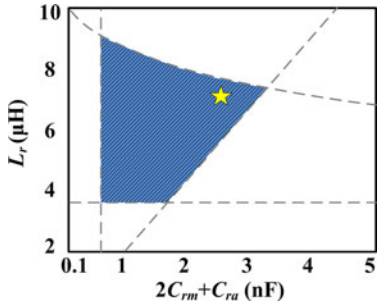


Fig. 17. Solution region of resonant parameters.

$$C_{ra} = C_{osse}, C_{rm} = C_{osse} + C_{\rm ext}. \quad (40)$$

The selected MOSFET is FCH041N65F (MOS1) with $C_{osse}$ of 192 pF. Therefore

$$2C_{rm} + C_{ra} > 3C_{osse} = 576\,\text{pF}. \quad (41)$$

### D. Resonant Inductor

The resonant inductor should limit the *di/dt* of the reverse recovery current below 100 A/$\mu$s

$$L_r \geq \frac{V_{\rm dc}}{100\,\text{A}/\mu\text{s}} = 3.6\,\mu\text{H}. \quad (42)$$

So far the solution region of the resonant inductor and the resonant capacitors has been constrained to a small area in Fig. 17. Finally, the resonant inductor is chosen as 7.2 $\mu$H. Each main switch is paralleled with a 1 nF external film capacitor with low ESR.

### E. Clamping Capacitor

The clamping capacitor $C_c$ should be large enough as the previous assumption. The voltage ripple of the clamping capacitor can be calculated with (43)

$$\begin{aligned} \Delta v_{Cc} = \frac{1}{C_c}\int_0^{T_{c3}} i_{cc}dt = \frac{1}{C_c}\left(\int_0^{t_2} -i_{Lr}dt \right. \\ \left. + \int_{t_6}^{t_8} (|i_o| - i_{Lr})\,dt + \int_{t_9}^{t_{11}} -i_{Lr}dt\right). \end{aligned} \quad (43)$$

The capacitance of the clamping capacitor is selected as 20 $\mu$F and the voltage fluctuation of $V_{cc}$ in a switching cycle is less than 2%. Two paralleled 10 $\mu$F film capacitors are used as the clamping capacitor in the prototype to reduce the ESR.

### F. Resonant Time

The resonant period can be calculated using the selected resonant parameters

$$T_r = 2\pi/\omega = 2\pi\sqrt{L_r(2C_{rm} + C_{ra})} = 856\,\text{ns}. \quad (44)$$

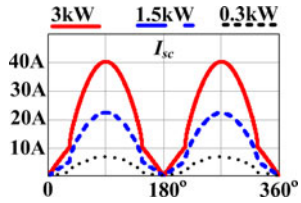


Fig. 18. $I_{\rm sc}$ with load power.

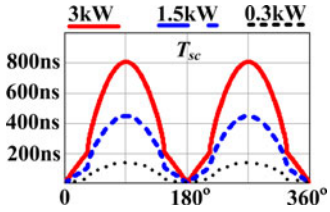


Fig. 19. $T_{\rm sc}$ with load power.

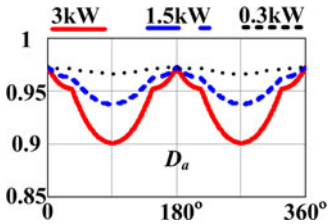


Fig. 20. $D_a$ with load power.

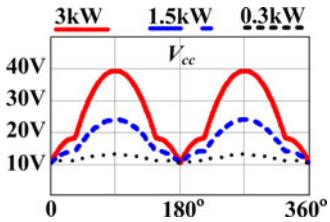


Fig. 21. $V_{cc}$ with load power.

TABLE II
PARAMETERS OF THE PROTOTYPE

| Parameter | Symbol | Value |
|---|---|---|
| Dc voltage | $V_{\rm dc}$ | 360 V |
| Grid voltage | $V_o$ | 230 V |
| Dc bus capacitor | $C_{\rm bus}$ | 1.5 mF |
| Inductor ripple frequency | $f_s$ | 100 kHz |
| Filter inductor | $L_1$ and $L_2$ | 190 $\mu$H |
| Resonant inductor | $L_r$ | 7.2 $\mu$H |
| Clamping capacitor | $C_c$ | 20 $\mu$F |
| Parallel capacitor | $C_{\rm ext}$ | 1 nF |
| Parasitic capacitor | $C_{osse}$ | 0.192 nF |

Stage 3 and stage 6 should be long enough for the completion of the resonant process and the longest resonant time is 1/4 of the resonant period (214 ns). The rising time and falling time of the drive circuit are also considered. Different interval time is tried in experiment and finally it is set as 377 ns in the PWM module of the DSP controller.

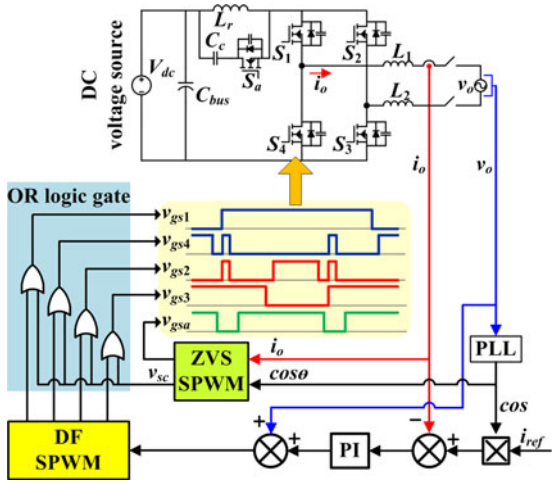


Fig. 22. Control diagram of ZVS grid-connected full-bridge invert.

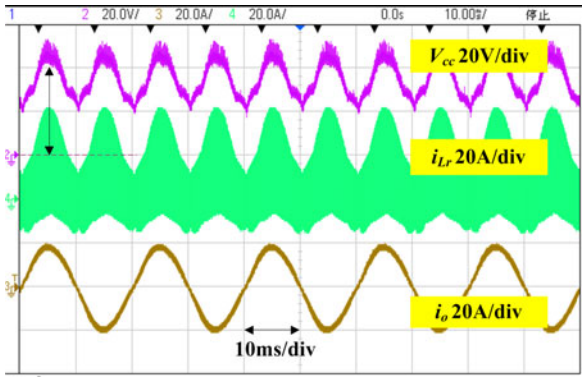


Fig. 23. $V_{cc}$, $i_{Lr}$ and $i_o$ with 3 kW grid-connected load, 10 ms/div.

### G. Short-Circuit Current and Short-Circuit Pulse

The amplitude of short-circuit current is calculated with (34) and shown in Fig. 18. The horizontal axis represents the phase of the sinusoidal load current. The required $I_{\rm sc}$ for ZVS condition changes with different load power and phase. Then the width of the short-circuit pulse $T_{\rm sc}$ can be determined with (35). The curve of $T_{\rm sc}$ with different load is presented in Fig. 19, which has the same shape with $I_{\rm sc}$. However, (35) is very complex for real-time calculation in DSP controller. The data of $T_{\rm sc}$ with different load power are precalculated and stored in the memory of the controller.

The theoretical value of the duty ratio of auxiliary switch $D_a$ and the voltage of clamping capacitor $V_{cc}$ are calculated with the selected resonant parameters. The minimum $D_a$ is 0.9 and the maximum $V_{cc}$ is 40 V as shown in Figs. 20 and 21.

## VI. EXPERIMENTS

The parameters of the experiment prototype are listed in Table II. The control diagram is shown in Fig. 22. The DSP controller is the TMS320F28069 from Texas Instruments. The ZVS SPWM block and the DF SPWM block are both

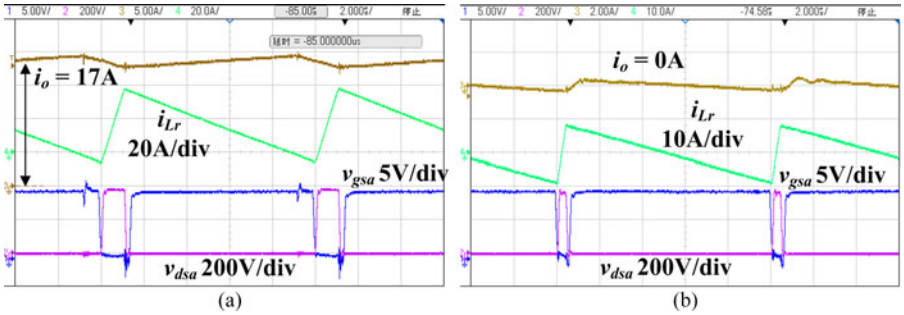


Fig. 24. Drain-source voltage and gate-source voltage of $S_a$ with (a) $i_o = 17$ A, (b) $i_o = 0$ A, 2 $\mu$s/div.

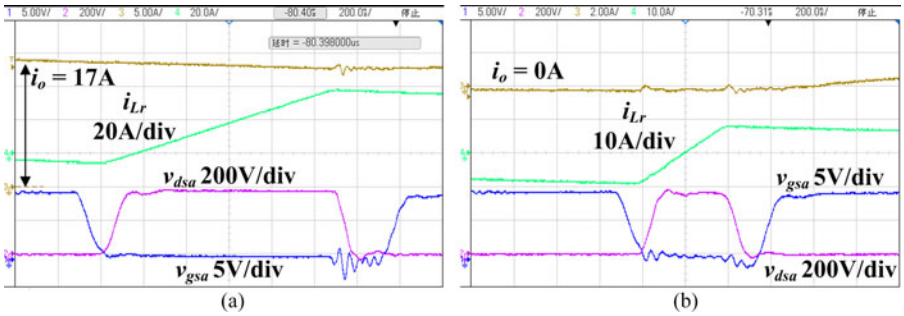


Fig. 25. Zoom-in switching waveforms of $S_a$ with (a) $i_o = 17$ A, (b) $i_o = 0$ A, 200 ns/div.

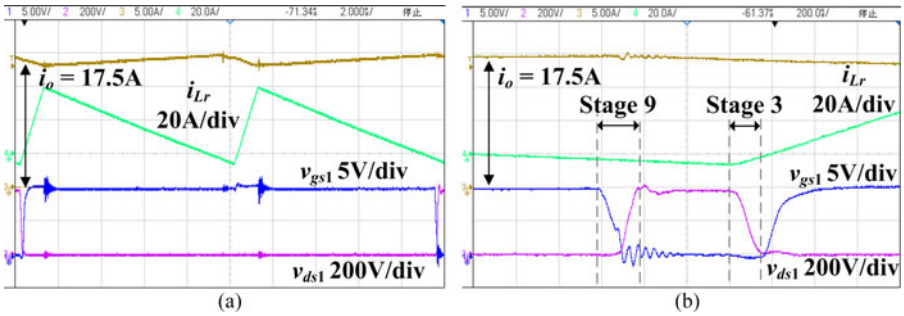


Fig. 26. Drain-source voltage and gate-source voltage of $S_1$ with $i_o = 17.5$ A. (a) 2 $\mu$s/div. (b) 200 ns/div.

implemented by the enhanced pulse width modulator module [24] in DSP controller. The amplitude and phase of load current are sampled and sent to the ZVS SPWM block to determine the width of short-circuit pulse. The short-circuit pulse is superposed over the DF SPWM pulses by the OR logic gate.

The clamping capacitor voltage $V_{cc}$, the resonant inductor current $i_{Lr}$ and the load current $i_o$ with 3 kW load are shown in Fig. 23. The maximum current of resonant inductor is 41 A and maximum voltage of clamping capacitor is 42 V, which come with the peak load current. Their amplitudes are smaller with small load current and the loss of the resonant inductor is reduced.

The ZVS waveforms of auxiliary switch are shown in Figs. 24 and 25. The duty ratio of the auxiliary switch also changes with the amplitude of the load current. The zoom-in waveforms in Fig. 25 show the drain-source voltage $v_{dsa}$ of $S_a$ resonates to zero before the rising edge of gate-source voltage $v_{gsa}$ and ZVS turn-on is realized. During the turn-off process of $S_a$ the overlapping area of $v_{gsa}$ and $v_{dsa}$ is very small, which means the turn-off loss is also significantly reduced.

The switching waveforms of main switch $S_1$ when the load current is 17.5 A are shown in Fig. 26. The drain-source voltage $v_{ds1}$ of $S_1$ resonates to zero before the rising edge of gate-source voltage $v_{gs1}$ and ZVS turn-on is realized in stage 3. The turn-off loss in stage 9 is also reduced with small overlapping area of $v_{gs1}$ and $v_{ds1}$.

The waveforms of main switch $S_1$ with the load current in the negative half cycle are given in Figs. 27 and 28. When $i_o = -18$A, the width of the short-circuit pulse is 800 ns and the duration of stage 5 is nearly 900 ns because of the driver circuit's delay. And the width of short-circuit pulse is shorter with smaller load current. The zoom-in waveform in Fig. 28 shows the ZVS turn-on is realized and the turn-off loss of main switch is also reduced.

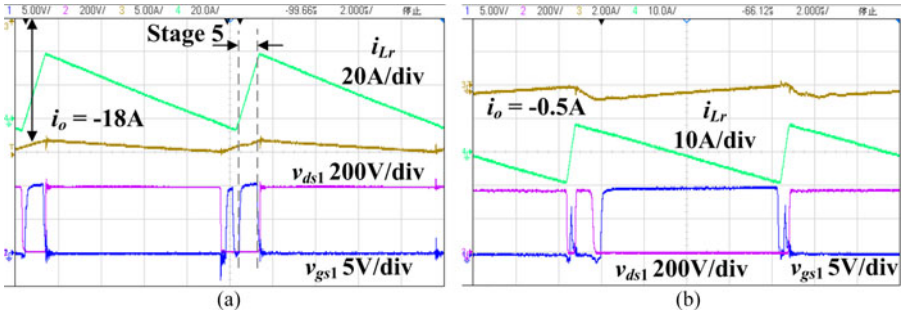


Fig. 27. Drain-source voltage and gate-source voltage of $S_1$ with (a) $i_o = -18$ A, (b) $i_o = -0.5$ A, 2 $\mu$s/div.

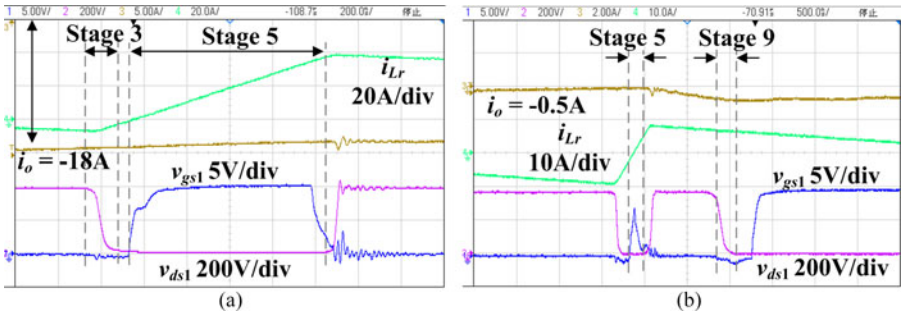


Fig. 28. Zoom-in switching waveforms of $S_1$ with (a) $i_o = -18$ A, 200 ns/div, (b) $i_o = -0.5$ A, 500 ns/div.

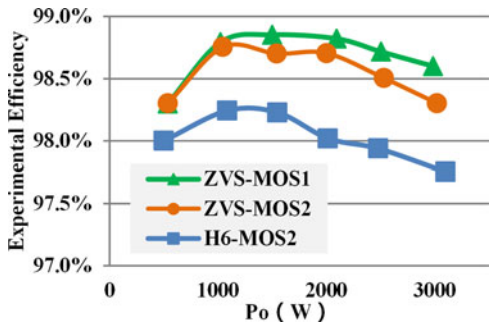


Fig. 29. Efficiency curve.

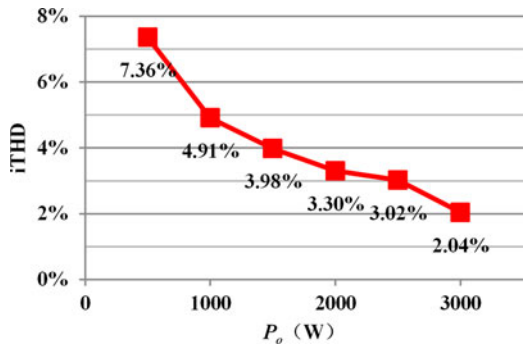


Fig. 30. THD of load current.

The efficiency of the ZVS full-bridge inverter with proposed ZVS SPWM is shown in Fig. 29 (exclude the auxiliary power supply). MOS1 is FCH041N65F with 41-m$\Omega$-$R_{\rm dson}$ and MOS2 is FCH47N60F with 73-m$\Omega$-$R_{\rm dson}$. The inverter's efficiency using MOS2 is 0.3% lower than MOS1 with 3 kW load because of the larger $R_{\rm dson}$. However, the difference disappears with light load because the conduction loss of MOSFET is quite small with low current. The efficiency of a H6 hard-switching inverter using MOS2 is also tested. The switching frequency of the H6 inverter is 20 kHz and two 0.86 mH inductors are used, which is more than four times of the filter in ZVS full-bridge inverter. Due to the small filter inductor and the realization of ZVS, the efficiency of the ZVS full-bridge inverter is higher than the H6 inverter and the maximum efficiency is 98.8% with 1.5 kW.

The total harmonic distortion (THD) of load current is shown in Fig. 30. The THD of full load current is 2.04%. The temperature of the prototype without cooling fan is shown in Fig. 31. The shell temperature of MOSFETs, the surface temperature of external resonant capacitor and the core temperature of both filter inductor and resonant inductor are measured. The temperature

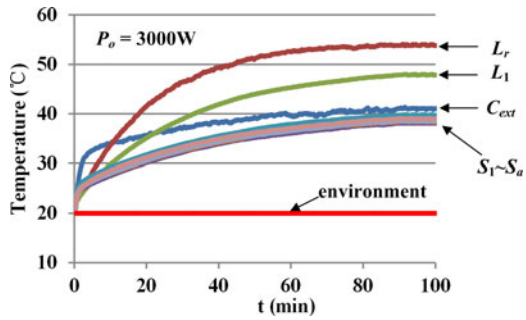


Fig. 31. Temperature test.

rise of both main switches and auxiliary switch in ZVS operation is less than 20 °C. The hottest component is the resonant inductor, which is 53.8 °C after working 100 min with 3 kW load. The temperature test also shows that the ZVS full-bridge inverter has good thermal performance.

## VII. Conclusion

A ZVS grid-connected full-bridge inverter with a novel ZVS SPWM scheme is proposed in this paper. Both main switches and auxiliary switch can realize ZVS operation and the reverse recovery of the body-diode is relieved. Comparing with the existing ZVS full-bridge inverter, external parallel diodes are removed and smaller filter is used with higher switching frequency to save the cost and reduce the size. High efficiency from light load to heavy load is achieved by adjusting the resonant energy. The ZVS full-bridge inverter is attractive for high efficiency application such as residential PV systems.

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