Soft-Switching Operation of Isolated Modular DC/DC Converters for Application in HVDC Grids

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***Abstract*—High-voltage dc/dc converters play an important role in HVDC grids. Isolated modular dc/dc converters (IMDCCs) based on modular multilevel converter technology provide a good solution to high-voltage applications. In order to reduce the size of the system, the IMDCC is required to be operated with a high ac-link frequency, but this will lead to increased switching loss and thus degraded efficiency. This paper proposes a soft-switching operation scheme for such an IMDCC. In this scheme, a quasi-square-wave (QSW) modulation method is employed, where the chain-links generate quasi-square terminal voltages with reduced *dv/dt*. With such chain-link terminal voltages, the arm currents which provide good condition for the soft-switching operation of the QSW-IMDCC can be obtained. Since soft switching can be achieved for the power switches, the proposed scheme will suffer less switching loss, thus improving the efficiency of the converter. Moreover, a capacitor voltage-balancing control strategy is proposed. This strategy does not need any arm current sensors, thus reducing the cost. The proposed soft-switching operation scheme and capacitor voltage-balancing control strategy are verified by the simulation results.**

***Index Terms*—DC/DC converter, high-voltage direct current (HVDC) grid, modular multilevel converter (MMC), soft Switching.**

I. Introduction

HIGH-VOLTAGE direct current (HVDC) power transmission has been rapidly developing in recent years since it is economical for long-distance bulky-power transmission and capable of asynchronous interconnections [1], [2]. At present, most of the existing HVDC projects employed point-to-point configuration which is relatively simple and mature in technique. HVDC grids integrating multiple HVDC lines [3]–[6] have the advantages of higher control flexibility, higher security, and lower capital and operating costs [6]; thus, they are suitable for collecting power from remote or offshore generation sources, supplying power to urban load centers, and facilitating power exchange and trading between regions and power systems [3], [4].

When HVDC grids with different voltage levels are to be interconnected or the existing two-terminal HVDC lines are to be connected to HVDC grids, dc/dc converters are a necessity to match the voltages and exchange power. Additionally, if remote low-voltage dc sources are to be integrated into HVDC grids or urban dc loads are to extract power from HVDC lines, dc/dc converters are also required.

There are various topologies for dc/dc converters, and they have been widely applied in dc/dc power conversions with low voltage levels. The basic dc/dc converters (buck, boost, and buck–boost) and their isolated versions have simple configuration and are easy to control [7]. However, when these dc/dc converters are used in HVDC applications, many power switches have to be connected in series to sustain the high voltage, thus suffering unequal voltage distribution among the switches under transient and steady-state operations [8]. Furthermore, the extremely high voltage change rate *dv/dt* may cause destructive damage to the transformer or inductor which has considerable interturn capacitance in HVDC applications. The dual-active bridge (DAB) dc/dc converter [9]–[11] allows bidirectional power conversion and incorporates inherent soft-switching feature, which can be applied in HVDC grids potentially. However, just like the isolated versions of the basic dc/dc converters, the DAB will also encounter the problems of voltage unbalance among the series-connected power switches and very high *dv/dt* acting on the transformer.

The recently emerging modular multilevel converter (MMC) technology [12]–[17] provides a possible solution to building dc/dc converters for high-voltage applications since the series-connected submodules in MMCs can lower the voltage stresses of individual switches. If two MMCs are connected front to front sharing a common ac link, they can operate as a bidirectional dc/dc converter which has the ability of interrupting the power flow under fault condition without using a circuit breaker [18]–[21]. Fig. 1(a) shows the single-phase topology of such dc/dc conversion system, where half-bridge submodules (HBSMs) shown in Fig. 1(b) are adopted. The HBSM has two working states in normal operation. When T_1 is ON and T_2 is OFF, the HBSM is in *inserted* state and the terminal voltage of the HBSM v_{sm} is equal to the energy-storage capacitor voltage v_{Csm}. And when T_1 is OFF and T_2 is ON, the HBSM is in *bypassed* state and v_{sm} is equal to zero. The series-connected HBSMs in each arm are usually called a chain-link. This dc/dc

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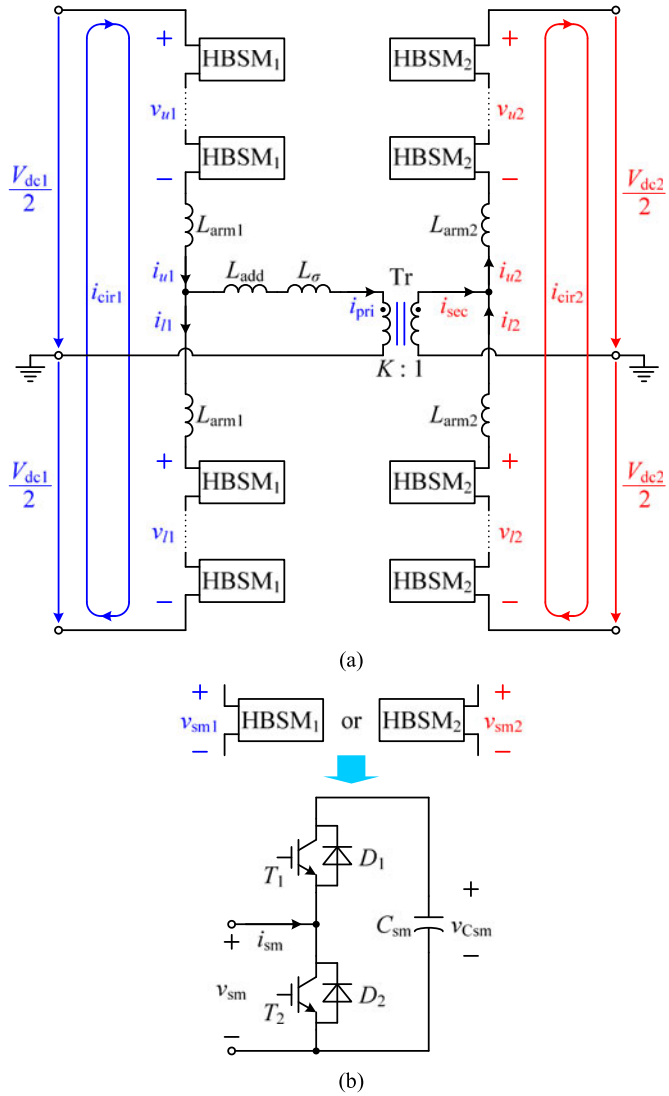

Fig. 1. IMDCC. (a) Main circuit. (b) Structure of the HBSM.

converter is called *isolated modular dc/dc converter* (IMDCC) hereinafter.

Basically, the ac-link voltages can be sinusoidal voltages synthesized by staircase waveforms approximately [18], [19]. However, since a square wave features a higher dc voltage utilization ratio and a stronger power transfer capability than the sinusoidal one with the same amplitude [22], it is more attractive to employ square-wave ac-link voltages in the IMDCC. By doing so, the arm currents can be reduced. Such square-wave scheme is applied in [20], but the high *dv/dt* at the rising and falling edges of the ac-link voltages will bring the problems mentioned earlier when applied in HVDC grids. To avoid this problem, a quasi-two-level (Q2L) operation scheme for the IMDCC is proposed in [21], where the converter generates quasi-square ac-link voltages with staircase rising and falling transitions of controllable time duration. With such arrangement, the *dv/dt* of the ac-link voltages is reduced. In the Q2L-IMDCC, each side of the ac link operates more like a two-level voltage-source converter than a traditional MMC [12]–[17], [23], [24]. Except for the voltage changing transitions, the chain-link functions like a single switch. When all the HBSMs in the chain-link are in *bypassed* state, the terminal voltage of the chain-link equals zero, and the chain-link functions like a turned-on switch with the transformer current flowing through it. When all the HBSMs in the chain-link are in *inserted* state, the terminal voltage of the chain-link equals the corresponding dc-side voltage, and the chain-link functions like a turned-off switch with no current flowing through it.

In order to reduce the size of the energy-storage capacitors, the transformer, and the inductors in the IMDCC, it is preferred to increase the frequency of the quasi-square ac-link voltages. This needs to increase the switching frequency of the power switches, however, leading to increased switching loss and thus degraded efficiency. Soft switching is a good solution to this problem, but its application to the IMDCC has not been studied by the literature so far.

This paper proposes a soft-switching operation scheme for the IMDCC with a high ac-link frequency. In this scheme, a quasi-square-wave (QSW) modulation method is employed. The QSW-IMDCC generates quasi-square chain-link terminal voltages with reduced *dv/dt*, which have similar waveforms but controllable high- and low-level values compared to the Q2L-IMDCC. Besides, in the QSW-IMDCC, each of the two arms in the same phase will conduct half of the transformer current, and each arm current will contain a circulating component. With such arm currents, soft switching can be achieved for the power switches, so the QSW-IMDCC can suffer less switching loss. Furthermore, the QSW-IMDCC does not need any arm current sensors in the capacitor voltage-balancing control, thus reducing the cost.

This paper is organized as follows. Section II presents the QSW modulation method. Section III explains the power characteristics of the QSW-IMDCC. Section IV describes the soft-switching operation of the IMDCC. Section V introduces the proposed capacitor voltage-balancing control strategy. Section VI shows the simulation results. Section VII summarizes the main findings.

II. QSW Modulation Method

Before the analysis, some assumptions are made to simplify the discussion and facilitate an easy understanding of the illustration. The HBSM shown in Fig. 1(b) is comprised of two semiconductor switches T_1 and T_2 with the antiparallel diodes D_1 and D_2 and an energy-storage capacitor C_{sm}. The value of C_{sm} is usually large enough, so the ripple of the capacitor voltage v_{Csm} can be ignored. In normal operation, the sum of the capacitor voltages in the HBSMs is approximately equal to $V_{\rm dc1}$ (or $V_{\rm dc2}$), and these capacitor voltages are well balanced. Thus, $V_{\rm dc1}$-side (or $V_{\rm dc2}$-side) submodule capacitor voltage, v_{Csm1} (or v_{Csm2}), is approximately equal to $V_{\rm dc1}/N_1$ (or $V_{\rm dc2}/N_2$), where N_1 and N_2 are the numbers of the HBSMs in each arm at $V_{\rm dc1}$ and $V_{\rm dc2}$ side, respectively.

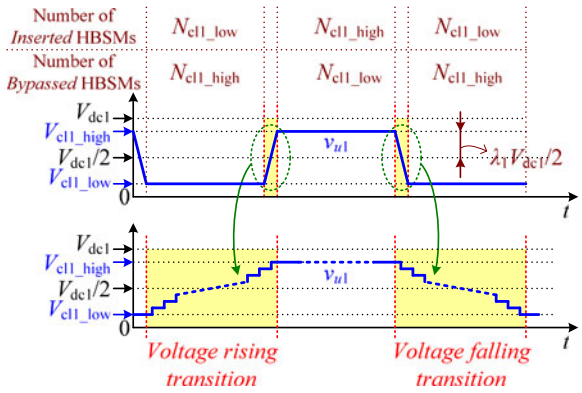

Fig. 2. Modulation waveform of v_{u1} in the QSW-IMDCC.

A. QSW Modulation Waveforms

The modulation waveforms are the ideal terminal voltage waveforms we want the chain-links to output. In this paper, a QSW modulation method is employed by the IMDCC. We can take the chain-link in $V_{\rm dc1}$-side upper arm as an example to illustrate this modulation method.

The modulation waveform of the chain-link terminal voltage v_{u1} in the QSW-IMDCC is shown in Fig. 2. Similar to the Q2L-IMDCC, v_{u1} employs voltage changing transitions to reduce the *dv/dt*. v_{u1} is a QSW with its voltage rising and falling transitions intentionally arranged to be staircase shaped. During the voltage rising (or falling) transition of v_{u1}, the HBSMs are inserted (or bypassed) one by one. By doing so, the height of each stair is limited to one submodule capacitor voltage, thus reducing the *dv/dt* of v_{u1}.

The modulation waveforms of the other chain-link terminal voltages are generated in a similar way to v_{u1}. As a result, similar to the traditional MMC, the chain-link terminal voltages v_{u1} and v_{l1} (or v_{u2} and v_{l2}) in the QSW-IMDCC will contain an identical dc component $V_{\rm dc1}/2$ (or $V_{\rm dc2}/2$) but an inverse ac component, that is

$$\begin{cases} v_{uj} = -v_{\rm acj} + \dfrac{V_{\rm dcj}}{2} \\ v_{lj} = v_{\rm acj} + \dfrac{V_{\rm dcj}}{2} \end{cases} \quad (j = 1, 2) \tag{1}$$

where v_{ac1} (or v_{ac2}) represents the ac component which is symmetrical in the positive and negative half-cycles. Since the maximum value of v_{u1} and v_{l1} (or v_{u2} and v_{l2}) will not exceed $V_{\rm dc1}$ (or $V_{\rm dc2}$), then according to (1), the amplitude of $v_{\rm ac1}$ (or $v_{\rm ac2}$), $V_{{\rm ac1}_a mp}$ (or $V_{{\rm ac2}_a mp}$), must be smaller than or equal to $V_{\rm dc1}/2$ (or $V_{\rm dc2}/2$), i.e., $V_{{\rm ac1}_a mp} \le V_{\rm dc1}/2$ (or $V_{{\rm ac2}_a mp} \le V_{\rm dc2}/2$).

As mentioned in Section I, the high- and low-level values of v_{u1} in the Q2L-IMDCC are $V_{\rm dc1}$ and 0, respectively. In the QSW-IMDCC, however, the high-level value of v_{u1} can be controlled to be equal to or lower than $V_{\rm dc1}$, while the low-level value of v_{u1} can be controlled to be equal to or higher than 0. It can be seen later that the controllability of the high- and low-level values of the chain-link terminal voltages provides additional degrees of freedom in the power flow control of the QSW-IMDCC.

As shown in Fig. 2, $V_{cl1_{\rm high}}$ and $V_{cl1_{\rm low}}$ are the high- and low-level values of $v_{\rm u1}$, respectively. As mentioned earlier, the capacitor voltage of $V_{\rm dc1}$-side HBSM is approximately equal to $V_{\rm dc1}/N_1$, so when v_{u1} equals $V_{cl1_{\rm high}}$, the number of the HBSMs working in *inserted* state is $N_{cl1_{\rm high}} = V_{cl1_{\rm high}}/(V_{\rm dc1}/N_1)$ while the number of the HBSMs working in *bypassed* state is $N_{cl1_{\rm low}} = V_{cl1_{\rm low}}/(V_{\rm dc1}/N_1)$. According to (1), we have $V_{cl1_{\rm high}} = V_{{\rm ac1}_a mp} + V_{\rm dc1}/2$ and $V_{cl1_{\rm low}} = -V_{{\rm ac1}_a mp} + V_{\rm dc1}/2$, so $V_{{\rm ac1}_a mp} = (V_{cl1_{\rm high}} - V_{cl1_{\rm low}})/2 = (N_{cl1_{\rm high}} - N_{cl1_{\rm low}})/N_1 \cdot V_{\rm dc1}/2$. Define that $\lambda_1 = (N_{cl1_{\rm high}} - N_{cl1_{\rm low}})/N_1$, then we have

$$V_{\rm ac1\_amp} = \lambda_1 \cdot \frac{V_{\rm dc1}}{2}. \tag{2}$$

Whether N_1 is even or odd makes little difference to the analysis, so an even N_1 is taken as an example. It can be analyzed from Fig. 2 that when N_1 is even, $\lambda_1 \in \{0, 2/N_1, 4/N_1, \ldots, (N_1 - 2)/N_1, 1\}$. Equation (2) indicates that λ_1 is the ratio of the amplitude of $v_{\rm ac1}$ to half of $V_{\rm dc1}$-side dc voltage, thus representing $V_{\rm dc1}$-side dc voltage utilization ratio. A larger λ_1 leads to a higher $V_{\rm dc1}$-side dc voltage utilization ratio, thus smaller arm currents. λ_1 is called $V_{\rm dc1}$-side *voltage amplitude ratio* hereinafter. Likewise, λ_2 is $V_{\rm dc2}$-side voltage amplitude ratio.

In the QSW-IMDCC, the two arm inductors in the same phase have a large and identical value. Thus, similar to the traditional MMC, the transformer current ($i_{\rm pri}$ or $i_{\rm sec}$) will be distributed evenly in the corresponding upper and lower arms and each arm current will contain a circulating component in the QSW-IMDCC. That is, the arm currents i_{uj} and $i_{lj} (j = 1, 2)$ can be expressed as

$$\begin{cases} i_{u1} = \dfrac{i_{\rm pri}}{2} + i_{\rm cir1} \\ i_{l1} = -\dfrac{i_{\rm pri}}{2} + i_{\rm cir1} \end{cases}, \quad \begin{cases} i_{u2} = \dfrac{i_{\rm sec}}{2} + i_{\rm cir2} \\ i_{l2} = -\dfrac{i_{\rm sec}}{2} + i_{\rm cir2} \end{cases} \tag{3}$$

where $i_{\rm cir1}$ and $i_{\rm cir2}$ are the circulating currents. The ripples of $i_{\rm cir1}$ and $i_{\rm cir2}$ are usually much smaller compared to their dc components, thus $i_{\rm cir1}$ and $i_{\rm cir2}$ can be regarded as dc currents approximately. With the assumption that the conversion efficiency is 100%, the HBSMs, the inductors and the transformer will consume no active power, so $i_{\rm cir1}$ and $i_{\rm cir2}$ can be expressed as

$$i_{\rm cir1} = \frac{P}{V_{\rm dc1}}, \quad i_{\rm cir2} = \frac{P}{V_{\rm dc2}} \tag{4}$$

where P is the power transferred by the QSW-IMDCC.

B. Simplified Equivalent Circuit of the QSW-IMDCC

With such a modulation method, the circuit of the QSW-IMDCC can be simplified. As shown in Fig. 1(a), Tr is the galvanic isolation transformer with the primary-to-secondary winding turns ratio of K, L_σ is the transformer leakage inductor, $L_{\rm add}$ is an additional inductor while L_{arm1} and L_{arm2} are the arm inductors. According to (1), the IMDCC shown in Fig. 1(a) can be simplified into the circuit depicted in Fig. 3(a), where the dc components in v_{u1} and v_{l1} (or v_{u2} and v_{l2}) counteract the corresponding dc voltage $V_{\rm dc1}/2$ (or $V_{\rm dc2}/2$) and they are

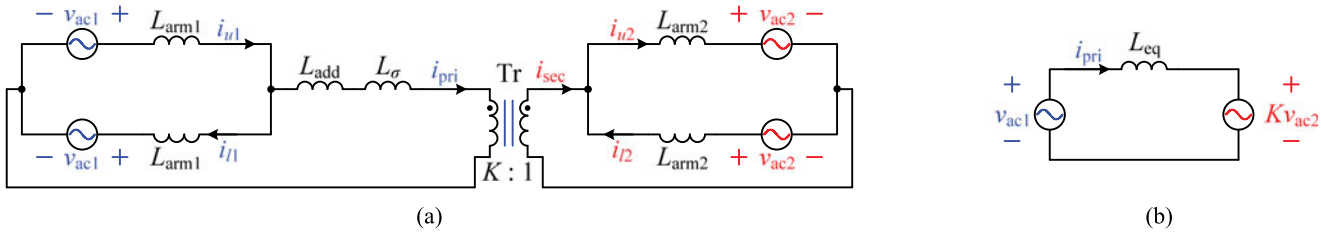

Fig. 3. Simplified circuits of the QSW-IMDCC. (a) Replace the chain-links with equivalent voltage sources. (b) Simplest circuit referred to the primary side.

no longer shown in the figure. Merging the two equivalent ac voltage sources at the same side of the IMDCC into one and converting the circuit at the secondary side of the transformer to the primary side, the circuit can be further simplified as Fig. 3(b) shows, where $L_{\rm eq}$ is the total equivalent interconnection inductor referred to the primary side and expressed as

$$L_{\rm eq} = \frac{L_{\rm arm1}}{2} + L_{\rm add} + L_\sigma + K^2 \cdot \frac{L_{\rm arm2}}{2}. \tag{5}$$

The simplified equivalent circuit shown in Fig. 3(b) is the basis of the power analysis of the QSW-IMDCC. From Fig. 3(b), it can be concluded that the power conversion of a QSW-IMDCC can be viewed as the power exchange between two equivalent ac voltage sources $v_{\rm ac1}$ and $Kv_{\rm ac2}$ through $L_{\rm eq}$. Thus, the characteristics of the transferred power are determined by $v_{\rm ac1}$ and $Kv_{\rm ac2}$.

C. Voltage and Current Waveforms in the QSW-IMDCC

With the modulation waveforms described earlier, the chain-links in the QSW-IMDCC can output the desired terminal voltages by properly inserting and bypassing the HBSMs. Then, we can obtain the ideal voltage and current waveforms shown in Fig. 4, where the power is transferred from $V_{\rm dc1}$ to $V_{\rm dc2}$ as an example. In Fig. 4, $T_{\rm ac}$ is the ac-link period, $t_{\rm stair1}$ is the duration of the voltage changing transitions of v_{u1} and v_{l1}, $t_{\rm stair2}$ is the duration of the voltage-changing transitions of v_{u2} and v_{l2}, and t_φ is the time by which $v_{\rm ac2}$ lags $v_{\rm ac1}$. In general, both $t_{\rm stair1}$ and $t_{\rm stair2}$ are relatively smaller than $T_{\rm ac}/2$ and t_φ. In order to simplify the mathematical analysis, the voltage changing transitions have been simplified into oblique lines.

III. Power Characteristics of the QSW-IMDCC

According to Fig. 3(b), there is

$$L_{\rm eq}\frac{di_{\rm pri}(t)}{dt} = v_{\rm ac1}(t) - Kv_{\rm ac2}(t). \tag{6}$$

According to Fig. 4, $v_{\rm ac1}$ and $v_{\rm ac2}$ during $[0, T_{\rm ac}/2]$ can be expressed as

$$v_{\rm ac1}(t) = \begin{cases} \dfrac{\lambda_1 V_{\rm dc1}}{t_{\rm stair1}}t - \dfrac{\lambda_1 V_{\rm dc1}}{2}, & t \in [0, t_{\rm stair1}] \\ \dfrac{\lambda_1 V_{\rm dc1}}{2}, & t \in [t_{\rm stair1}, T_{\rm ac}/2] \end{cases} \tag{7a}$$

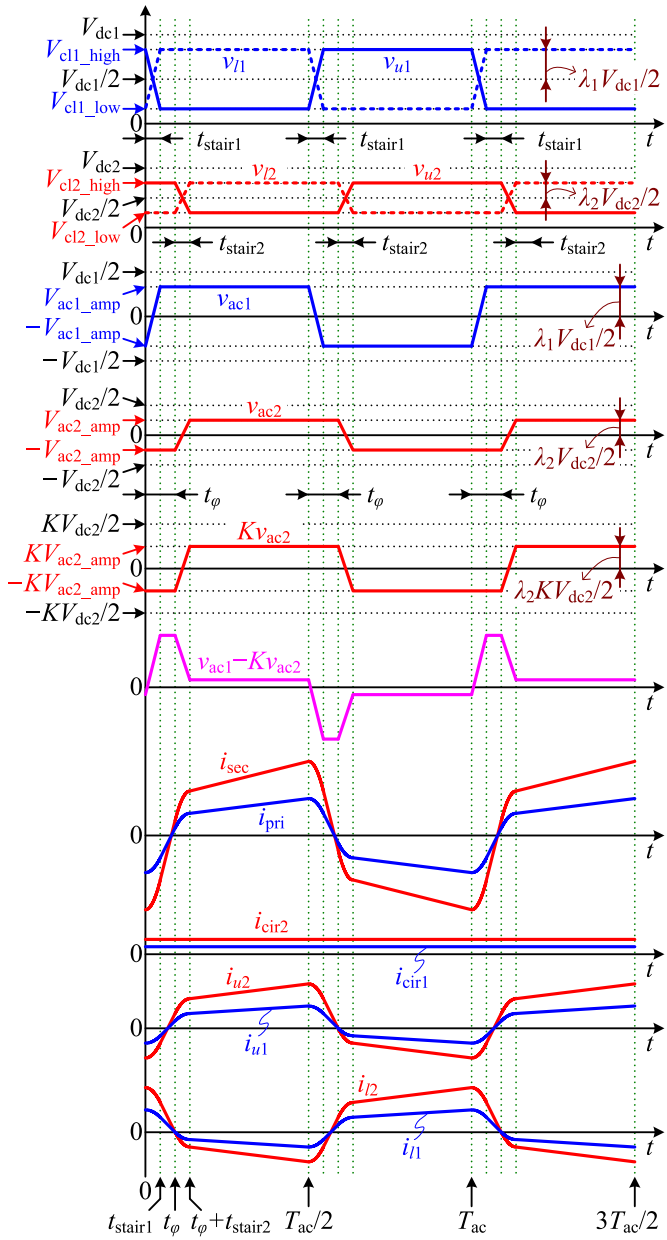

Fig. 4. Ideal voltage and current waveforms in the QSW-IMDCC.

$$v_{\mathrm{ac2}}(t) = \begin{cases} -\dfrac{\lambda_2 V_{\mathrm{dc2}}}{2}, & t \in [0, t_\varphi] \\ \dfrac{\lambda_2 V_{\mathrm{dc2}}}{t_{\mathrm{stair2}}}(t - t_\varphi) - \dfrac{\lambda_2 V_{\mathrm{dc2}}}{2}, & t \in [t_\varphi, t_\varphi + t_{\mathrm{stair2}}] \\ \dfrac{\lambda_2 V_{\mathrm{dc2}}}{2}, & t \in \left[t_\varphi + t_{\mathrm{stair2}}, \dfrac{T_{\mathrm{ac}}}{2}\right] \end{cases} \tag{7b}$$

According to the waveform symmetry of v_{ac1} and v_{ac2} as shown in Fig. 4, we have

$$v_{\mathrm{ac1}}(t) = -v_{\mathrm{ac1}}\left(t - \frac{T_{\mathrm{ac}}}{2}\right), \quad t \in \left[\frac{T_{\mathrm{ac}}}{2}, T_{\mathrm{ac}}\right] \tag{8a}$$

$$v_{\mathrm{ac2}}(t) = -v_{\mathrm{ac2}}\left(t - \frac{T_{\mathrm{ac}}}{2}\right), \quad t \in \left[\frac{T_{\mathrm{ac}}}{2}, T_{\mathrm{ac}}\right]. \tag{8b}$$

According to (6) and (7), the expression of i_{pri} during [0, $T_{\mathrm{ac}}/2$] can be derived as (9), shown at the bottom of the page, where $M = KV_{\mathrm{dc2}}/V_{\mathrm{dc1}}$ is the *dc voltage conversion ratio*.

According to the waveform symmetry of i_{pri} as shown in Fig. 4, we have

$$i_{\mathrm{pri}}(t) = -i_{\mathrm{pri}}\left(t - \frac{T_{\mathrm{ac}}}{2}\right), \quad t \in \left[\frac{T_{\mathrm{ac}}}{2}, T_{\mathrm{ac}}\right]. \tag{10}$$

According to (9) and (10), the expressions of i_{pri} at $t = 0$, t_{stair1}, t_φ, and $t_\varphi + t_{\mathrm{stair2}}$ can be derived as

$$I_{\mathrm{pri}}(0) = \frac{V_{\mathrm{dc1}}}{4L_{\mathrm{eq}}}\left[-\frac{T_{\mathrm{ac}}}{2}(\lambda_1 - \lambda_2 M) + \lambda_1 t_{\mathrm{stair1}} - \lambda_2 M(2t_\varphi + t_{\mathrm{stair2}})\right] \tag{11a}$$

$$I_{\mathrm{pri}}(t_{\mathrm{stair1}}) = \frac{V_{\mathrm{dc1}}}{4L_{\mathrm{eq}}}\left[-\frac{T_{\mathrm{ac}}}{2}(\lambda_1 - \lambda_2 M) + \lambda_1 t_{\mathrm{stair1}} - \lambda_2 M(2t_\varphi - 2t_{\mathrm{stair1}} + t_{\mathrm{stair2}})\right] \tag{11b}$$

$$I_{\mathrm{pri}}(t_\varphi) = \frac{V_{\mathrm{dc1}}}{4L_{\mathrm{eq}}}\left[-\frac{T_{\mathrm{ac}}}{2}(\lambda_1 - \lambda_2 M) + \lambda_1 (2t_\varphi - t_{\mathrm{stair1}}) - \lambda_2 M t_{\mathrm{stair2}}\right] \tag{11c}$$

$$I_{\mathrm{pri}}(t_\varphi + t_{\mathrm{stair2}}) = \frac{V_{\mathrm{dc1}}}{4L_{\mathrm{eq}}}\left[-\frac{T_{\mathrm{ac}}}{2}(\lambda_1 - \lambda_2 M) + \lambda_1 (2t_\varphi - t_{\mathrm{stair1}} + 2t_{\mathrm{stair2}}) - \lambda_2 M t_{\mathrm{stair2}}\right]. \tag{11d}$$

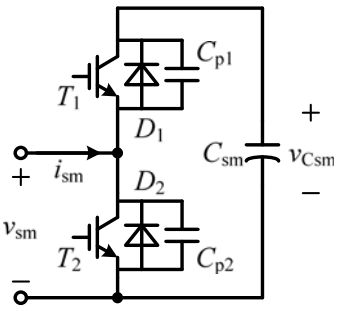

Fig. 5. HBSM with additional parallel capacitors.

According to Figs. 3(b) and 4, the active power of the QSW-IMDCC transferred from V_{dc1} to V_{dc2} can be calculated as

$$P = \frac{1}{T_{\mathrm{ac}}}\int_0^{T_{\mathrm{ac}}} v_{\mathrm{ac1}}(t)\, i_{\mathrm{pri}}(t)\, dt. \tag{12}$$

According to (7a), (8a), (9), (10), (11), and (12), when setting $t_{\mathrm{stair1}} = t_{\mathrm{stair2}} = t_{\mathrm{stair}}$, the expression of the transferred power can be derived as

$$P = \frac{\lambda_1\lambda_2 M V_{\mathrm{dc1}}^2}{2T_{\mathrm{ac}}L_{\mathrm{eq}}}\left[t_\varphi\left(\frac{T_{\mathrm{ac}}}{2} - t_\varphi\right) - \frac{t_{\mathrm{stair}}^2}{6}\right] = \frac{\lambda_1\lambda_2 M V_{\mathrm{dc1}}^2}{8f_{\mathrm{ac}}L_{\mathrm{eq}}}\left[D_\varphi(1 - D_\varphi) - \frac{D_{\mathrm{stair}}^2}{6}\right] \tag{13}$$

where $f_{ac} = 1/T_{ac}$ is the ac-link frequency and

$$D_\varphi = \frac{t_\varphi}{T_{\mathrm{ac}}/2}, D_{\mathrm{stair}} = \frac{t_{\mathrm{stair}}}{T_{\mathrm{ac}}/2}. \tag{14}$$

Then, with the power base $P_{\mathrm{base}} = V_{\mathrm{dc1}}^2/(8f_{\mathrm{ac}}L_{\mathrm{eq}})$, the normalized transferred power P^* is expressed as

$$P^* = \frac{P}{P_{\mathrm{base}}} = \lambda_1\lambda_2 M\left[D_\varphi(1 - D_\varphi) - \frac{D_{\mathrm{stair}}^2}{6}\right]. \tag{15}$$

It can be seen from (15) that the expression of the transferred power of the QSW-IMDCC is similar to that of the DAB dc/dc

$$i_{\mathrm{pri}}(t) = \begin{cases} \dfrac{V_{\mathrm{dc1}}}{2L_{\mathrm{eq}}}\left[\dfrac{\lambda_1}{t_{\mathrm{stair1}}}t^2 - (\lambda_1 - \lambda_2 M)t\right] + I_{\mathrm{pri}}(0), & t \in [0, t_{\mathrm{stair1}}] \\ \dfrac{V_{\mathrm{dc1}}}{2L_{\mathrm{eq}}}(\lambda_1 + \lambda_2 M)(t - t_{\mathrm{stair1}}) + I_{\mathrm{pri}}(t_{\mathrm{stair1}}), & t \in [t_{\mathrm{stair1}}, t_\varphi] \\ \dfrac{V_{\mathrm{dc1}}}{2L_{\mathrm{eq}}}\left[-\dfrac{\lambda_2 M}{t_{\mathrm{stair2}}}(t - t_\varphi)^2 + (\lambda_1 + \lambda_2 M)(t - t_\varphi)\right] + I_{\mathrm{pri}}(t_\varphi), & t \in [t_\varphi, t_\varphi + t_{\mathrm{stair2}}] \\ \dfrac{V_{\mathrm{dc1}}}{2L_{\mathrm{eq}}}(\lambda_1 - \lambda_2 M)[t - (t_\varphi + t_{\mathrm{stair2}})] + I_{\mathrm{pri}}(t_\varphi + t_{\mathrm{stair2}}), & t \in \left[t_\varphi + t_{\mathrm{stair2}}, \frac{T_{\mathrm{ac}}}{2}\right] \end{cases} \tag{9}$$

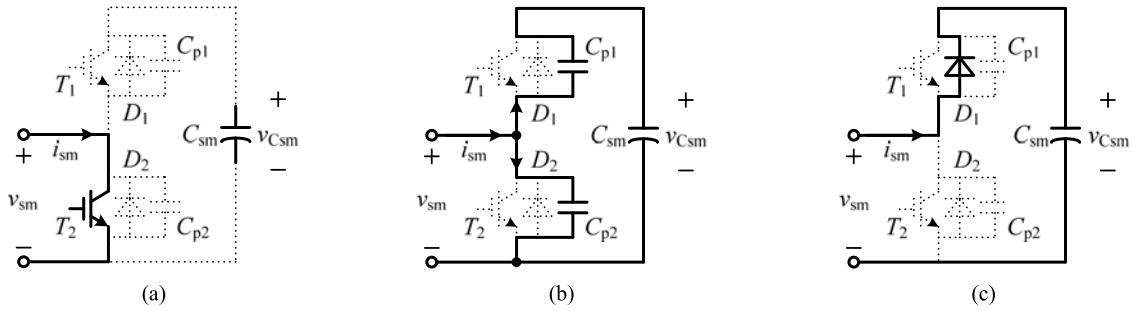

Fig. 6. ZVS operation of the switches in an HBSM during the transition from *bypassed* state to *inserted* state. (a) *Bypassed* state. (b) T_2 is turned off. (c) D_1 is conducting, providing zero-voltage turn-on condition for T_1.

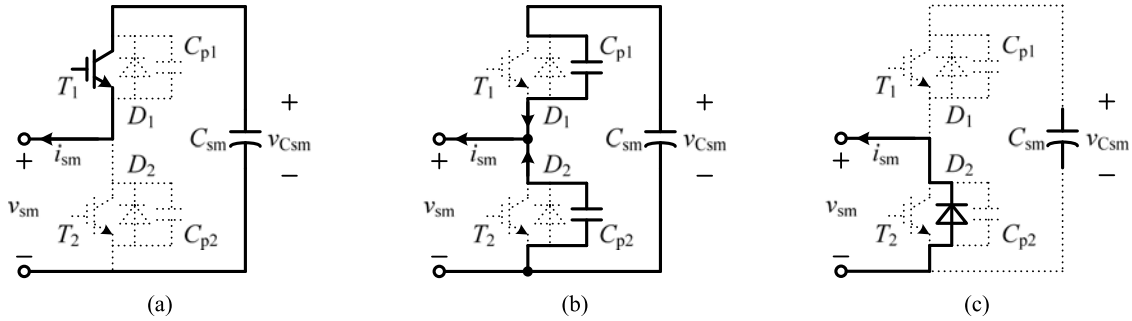

Fig. 7. ZVS operation of the switches in an HBSM during the transition from *inserted* state to *bypassed* state. (a) *Inserted* state. (b) T_1 is turned off. (c) D_2 is conducting, providing zero-voltage turn-on condition for T_2.

converter [9], except for the coefficients λ_1 and λ_2 and the negative term "$-D_{\rm stair}^2/6$" in the square bracket. The negative term degrades the power transfer capability of the QSW-IMDCC, since the voltage changing transitions reduce the dc voltage utilization ratios of the QSWs. Nevertheless, $D_{\rm stair}$ is usually very small compared with D_φ, thus the loss of the transferred power due to the negative term could be ignored. Since *M* is determined by the specifications of a designed system, the power transfer characteristics of the QSW-IMDCC are mainly determined by λ_1, λ_2, and D_φ. Larger λ_1 and λ_2 lead to larger P^* with the same D_φ, which indicates a higher power transfer capability. Besides, similar to the DAB dc/dc converter, D_φ should be no larger than 0.5 to guarantee a low reactive power.

IV. Soft-Switching Operation of the QSW-IMDCC

Actually, the arm currents in the QSW-IMDCC, as shown in Fig. 4, are suitable for soft-switching operation. Specifically, zero-voltage-switching (ZVS) can be achieved for the power switches, thus improving the system efficiency.

A. Requirements of ZVS for the Switches in an HBSM

For the purpose of achieving zero-voltage turn-off for the power switches, two capacitors are introduced to be connected in parallel with the two power switches in the HBSM, respectively [25], [26], as shown in Fig. 5. Note that the parallel capacitors C_{p1} and C_{p2} include the intrinsic capacitances of the power switches T_1 and T_2, respectively. The zero-voltage turn-on is achieved by using the arm current to discharge C_{p1} (or C_{p2}) before turning T_1 (or T_2) ON.

Fig. 6(a) shows the HBSM operating in *bypassed* state, where the submodule current i_{sm} flows through T_2. When T_2 is turned off, i_{sm} charges C_{p2} and discharges C_{p1}, as shown in Fig. 6(b). Since C_{p1} and C_{p2} limit the rising rate of the collector–emitter voltage of T_2, T_2 is zero-voltage turn-off. When C_{p1} is fully discharged, diode D_1 is forced to conduct, clamping the voltage of T_1 to be zero, as shown in Fig. 6(c). Thus, T_1 can be turned on with zero voltage. At this moment, the HBSM enters into *inserted* state. When the HBSM is operating in *bypassed* state, if i_{sm} flows through D_2, T_2 can be zero-voltage turn-off, but T_1 is hard turn-on, leading to sharp discharging of C_{p1} through T_1 and severe reverse recovery of D_2. Therefore, it can be concluded that when the HBSM transits from *bypassed* state to *inserted* state, i_{sm} must flow into the HBSM to guarantee the zero-voltage turn-off of T_2 and zero-voltage turn-on of T_1.

Fig. 7(a) shows the HBSM operating in *inserted* state, where the submodule current i_{sm} flows through T_1. When T_1 is turned off, $i_{\rm sm}$ charges C_{p1} and discharges C_{p2}, as shown in Fig. 7(b). Since C_{p1} and C_{p2} limit the rising rate of the collector–emitter voltage of T_1, T_1 is zero-voltage turn-off. When C_{p2} is fully discharged, diode D_2 is forced to conduct, clamping the voltage of T_2 to be zero, as shown in Fig. 7(c). Thus, T_2 can be turned on with zero voltage. At this moment, the HBSM enters into *bypassed* state. When the HBSM is operating in *inserted* state, if i_{sm} flows through D_1, T_1 can be zero-voltage turn-off, but T_2 is hard turn-on, leading to sharp discharging of C_{p2} through T_2 and severe reverse recovery of D_1. Therefore, it can be

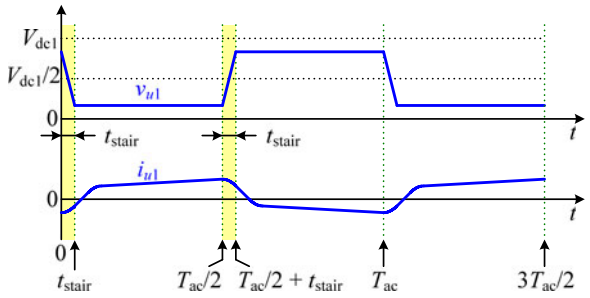

Fig. 8. Waveforms of v_{u1} and i_{u1}.

concluded that when the HBSM transits from *inserted* state to *bypassed* state, i_{sm} must flow out of the HBSM to guarantee the zero-voltage turn-off of T_1 and zero-voltage turn-on of T_2.

B. Full ZVS Condition for Each Arm

In order to derive the full-ZVS condition for each arm, V_{dc1}-side upper arm is taken as an example. For the convenience of illustration, the waveforms of the chain-link terminal voltage v_{u1} and the arm current i_{u1} shown in Fig. 3 are redrawn in Fig. 8. As mentioned in Section II, during the voltage rising transition $[T_{\mathrm{ac}}/2, T_{\mathrm{ac}}/2 + t_{\mathrm{stair}}]$ of v_{u1}, the HBSMs in V_{dc1}-side upper arm is inserted one by one. In order to realize ZVS for all the switches in the HBSMs to be inserted, according to the previous analysis, the arm current i_{u1} should always flow into the HBSMs. That is, $i_{u1} \geq 0$ should be ensured during the whole transition. As shown in Fig. 8, i_{u1} decreases during the time interval $[T_{\mathrm{ac}}/2, T_{\mathrm{ac}}/2 + t_{\mathrm{stair}}]$, so it is required that

$$I_{u1}\left(\frac{T_{\mathrm{ac}}}{2} + t_{\mathrm{stair}}\right) \geq 0. \tag{16}$$

According to (3) and (4), $i_{u1} = i_{\mathrm{pri}}/2 + i_{\mathrm{cir1}} = i_{\mathrm{pri}}/2 + P/V_{\mathrm{dc1}}$. Then, according to (10), (11b), and (13), we have

$$\begin{aligned} &I_{u1}\left(\frac{T_{\mathrm{ac}}}{2} + t_{\mathrm{stair}}\right) = \\ &\frac{V_{\mathrm{dc1}}}{8L_{\mathrm{eq}}}\left[\frac{T_{\mathrm{ac}}}{2}\left(\lambda_1 - \lambda_2 M\right) - \lambda_1 t_{\mathrm{stair}} + \lambda_2 M\left(2t_\varphi - t_{\mathrm{stair}}\right)\right] \\ &+\frac{\lambda_1\lambda_2 M V_{\mathrm{dc1}}}{2T_{\mathrm{ac}}L_{\mathrm{eq}}}\left[t_\varphi\left(\frac{T_{\mathrm{ac}}}{2} - t_\varphi\right) - \frac{t_{\mathrm{stair}}^2}{6}\right]. \end{aligned} \tag{17}$$

According to (14), (15), (16), and (17), we have

$$P^* \leq P_{\mathrm{B\_1r}}\left(\lambda_1, \lambda_2, D_{\mathrm{stair}}, D_\varphi\right) \tag{18}$$

where $P_{B_1 r}(\lambda_1, \lambda_2, D_{\mathrm{stair}}, D_\varphi)$ is the power boundary function and expressed as follows: see (19) shown at the bottom of the next page.

Inequality (18) is defined as the *full-ZVS condition* for V_{dc1}-side upper arm during the voltage rising transition of v_{u1}. For given λ_1, λ_2, and D_{stair}, when D_φ and P^* of the QSW-IMDCC satisfy (19), all switches in V_{dc1}-side upper arm are able to achieve ZVS during the voltage rising transition of v_{u1}. Similarly, the full-ZVS condition for V_{dc1}-side lower arm during the voltage rising transition of v_{l1} can be derived and it is the same as (19). Consequently, (19) is the full-ZVS condition for both arms at V_{dc1} side during the voltage rising transitions.

As mentioned in Section II, during the voltage falling transition $[0, t_{\mathrm{stair}}]$, the HBSMs are bypassed one by one. According to the previous analysis, in order to realize ZVS for all the switches in V_{dc1}-side upper arm, the arm current i_{u1} should always flow out of the HBSMs. That is, $i_{u1} \leq 0$ should be ensured during this transition. As shown in Fig. 8, i_{u1} increases during the time interval $[0, t_{\mathrm{stair}}]$, so it is required that

$$I_{u1}\left(t_{\mathrm{stair}}\right) \leq 0. \tag{20}$$

According to (3) and (4), $i_{u1} = i_{\mathrm{pri}}/2 + i_{cir1} = i_{\mathrm{pri}}/2 + P/V_{\mathrm{dc1}}$. Then, according to (11b) and (13), we have

$$\begin{aligned} &I_{u1}\left(t_{\mathrm{stair}}\right) \\ &= -\frac{V_{\mathrm{dc1}}}{8L_{\mathrm{eq}}}\left[\frac{T_{\mathrm{ac}}}{2}\left(\lambda_1 - \lambda_2 M\right) - \lambda_1 t_{\mathrm{stair}} + \lambda_2 M\right. \\ &\left.\left(2t_\varphi - t_{\mathrm{stair}}\right)\right] + \frac{\lambda_1\lambda_2 M V_{\mathrm{dc1}}}{2T_{\mathrm{ac}}L_{\mathrm{eq}}}\left[t_\varphi\left(\frac{T_{\mathrm{ac}}}{2} - t_\varphi\right)\right. \\ &\left. - \frac{t_{\mathrm{stair}}^2}{6}\right]. \end{aligned} \tag{21}$$

According to (14), (15), (20), and (21), we have

$$\begin{aligned} P^* &\leq P_{\mathrm{B\_1f}}\left(\lambda_1, \lambda_2, D_{\mathrm{stair}}, D_\varphi\right) \\ &= \frac{\lambda_1^2\left(1 - D_{\mathrm{stair}}\right)\left[D_\varphi\left(1 - D_\varphi\right) - \frac{D_{\mathrm{stair}}^2}{6}\right]}{1 + D_{\mathrm{stair}} - \frac{\lambda_1}{3}D_{\mathrm{stair}}^2 - 2\left(1 - \lambda_1\right)D_\varphi - 2\lambda_1 D_\varphi^2}. \end{aligned} \tag{22}$$

Inequality (22) is the full-ZVS condition for V_{dc1}-side upper arm during the voltage falling transition of v_{u1}. Similarly, the full-ZVS condition for V_{dc1}-side lower arm during the voltage falling transition of v_{l1} can be derived and it is the same as (22). Consequently, (22) is the full-ZVS condition for both arms at V_{dc1} side during the voltage falling transitions.

Similarly, the full-ZVS condition for V_{dc2}-side arms during the voltage rising transitions can be derived as

$$\begin{aligned} P^* &\geq P_{\mathrm{B\_2r}}\left(\lambda_1, \lambda_2, D_{\mathrm{stair}}, D_\varphi\right) \\ &= \frac{\lambda_1^2}{1 - D_{\mathrm{stair}}}\left[1 + D_{\mathrm{stair}} - \frac{\lambda_2}{3}D_{\mathrm{stair}}^2 - 2\left(1 - \lambda_2\right)D_\varphi - 2\lambda_2 D_\varphi^2\right] \\ &\cdot\left[D_\varphi\left(1 - D_\varphi\right) - \frac{D_{\mathrm{stair}}^2}{6}\right] \end{aligned} \tag{23}$$

while the full-ZVS condition for V_{dc2}-side arms during the voltage falling transitions can be derived as

$$\begin{aligned} P^* &\geq P_{\mathrm{B\_2f}}\left(\lambda_1,\ \lambda_2,\ D_{\mathrm{stair}},\ D_\varphi\right) \\ &= \frac{\lambda_1^2}{1 - D_{\mathrm{stair}}}\left[1 + D_{\mathrm{stair}} + \frac{\lambda_2}{3}D_{\mathrm{stair}}^2 - 2\left(1 + \lambda_2\right)D_\varphi + 2\lambda_2 D_\varphi^2\right] \\ &\cdot\left[D_\varphi\left(1 - D_\varphi\right) - \frac{D_{\mathrm{stair}}^2}{6}\right]. \end{aligned} \tag{24}$$

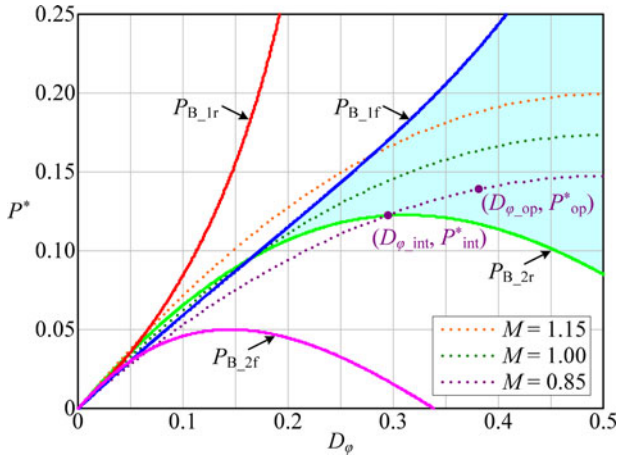

Fig. 9. Curves of the four boundary functions and a family of $P^* - D_\varphi$ curves with M as the parameter, where $\lambda_1 = \lambda_2 = 10/12$ and $D_{\text{stair}} = 0.05$.

C. Complete-ZVS Region

According to (19), (22), (23), and (24), the curves of the four power boundary functions (P_{B_1r}, P_{B_1f}, P_{B_2r}, and P_{B_1f}) with respect to D_φ are depicted in Fig. 9 with solid lines, where $\lambda_1 = \lambda_2 = 10/12$ and $D_{\text{stair}} = 0.05$ as an example. As shown in Fig. 9, the $P^* - D_\varphi$ plane is divided into several regions by the four solid curves. The shaded region, which is surrounded by P_{B_1f} and P_{B_2r}, is the *complete-ZVS region*, where all the four arms of the QSW-IMDCC can realize full-ZVS.

According to (15), a family of $P^* - D_\varphi$ curves with different M are depicted in Fig. 9 with dotted lines. For a certain M, the system operation point moves along the corresponding $P^* - D_\varphi$ curve, depending on the required transferred power. Take $M = 0.85$ as an example, the intersection of the $P^* - D_\varphi$ curve and the border of the complete-ZVS region is $(D_{\varphi\_\text{int}}, P^*_{\text{int}})$ while the system operation point on this $P^* - D_\varphi$ curve is $(D_{\varphi\_\text{op}}, P^*_{\text{op}})$. When $D_{\varphi\_\text{op}} \geq D_{\varphi\_\text{int}}$ (thus $P^*_{\text{op}} \geq P^*_{\text{int}}$), the system will operate inside the complete-ZVS region. Thus, it can be concluded that a smaller D_{φ_int} will lead to a larger control range of the output power with complete-ZVS. As shown in Fig. 9, M greatly affects D_{φ_int}. In order to obtain a small D_{φ_int}, M should be determined in such a way that the corresponding $P^* - D_\varphi$ curve goes through the intersection of $P_{B_1 f}$ and $P_{B_2 r}$. This imposes constraints on the design of the transformer turns ratio K.

According to (22) and (23), it can be verified that when λ_1, λ_2, and D_φ are determined, $P_{B_1 f}$ increases with decreasing D_{stair} while $P_{B_2 r}$ decreases with decreasing D_{stair}. Therefore, a smaller D_{stair} will lead to a larger complete-ZVS region, which will facilitate the soft-switching operation of the QSW-IMDCC.

In practice, the realization of ZVS for a power switch is related not only to the switch current direction but also to the value of its parallel capacitor. For example, the upper switch T_1 of the HBSM shown in Fig. 5 has a parallel capacitor C_{p1}. As shown in Fig. 6, after the lower switch T_2 is turned off, the switch current of T_1 will discharge C_{p1}. In order to guarantee the zero-voltage turn-on of T_1, it should be satisfied that

$$C_{\text{p1}} < \frac{i_{\text{turnon}} t_{\text{dead}}}{v_{\text{Csm}}} \tag{25}$$

where i_{turnon} is the switch current of T_1 during the turn-on process, t_{dead} is the dead-time between the turn-off of T_2 and the turn-on of T_1, and v_{Csm} is the energy-storage capacitor voltage. On the other hand, as shown in Fig. 7, if the switch current flows through T_1, then T_1 can be zero-voltage turn-off. In order to guarantee a sufficient zero-voltage turn-off, it should be satisfied that

$$C_{\text{p1}} > \frac{i_{\text{turnoff}} t_{\text{turnoff}}}{v_{\text{Csm}}} \tag{26}$$

where i_{turnoff} is the switch current of T_1 during the turn-off process and t_{turnoff} is the desired time for the collector–emitter voltage of T_1 to rise from zero to v_{Csm}. The value of the switch parallel capacitor can be designed based on (25) and (26).

V. Capacitor Voltage-Balancing Control Strategy

The capacitor voltages of the HBSMs in each arm should be well balanced to guarantee a normal operation. A capacitor voltage-balancing control strategy is proposed in this section to achieve this goal in the QSW-IMDCC.

The submodule capacitor voltage-balancing control for each arm of the QSW-IMDCC can be derived in a similar way, so V_{dc1}-side upper arm can be taken as an example. In normal operation, the sum of the capacitor voltages of the N_1 HBSMs in this arm are approximately V_{dc1}. Therefore, as long as the N_1 capacitor voltages are controlled to be balanced among each other (i.e., the difference between any two capacitor voltages is controlled to be within an acceptable range) dynamically, each capacitor voltage will be limited around V_{dc1}/N_1, thus achieving the goal.

As mentioned in Section II, V_{dc1}-side voltage amplitude ratio λ_1 is ranged from 0 to 1. Fig. 10(a) shows the waveforms of v_{u1} and i_{u1} when $\lambda_1 = 1$, where the voltage changing transitions of v_{u1} are ignored for simplification. During the first half-period $(0, T_{\text{ac}}/2)$, $v_{u1} = 0$, which means that all the N_1 HBSMs are *bypassed*. Thus, the capacitor voltages of these HBSMs remain unchanged. During the second half-period $(T_{\text{ac}}/2, T_{\text{ac}})$, $v_{u1} =$

$$P_{\text{B\_1r}}(\lambda_1, \lambda_2, D_{\text{stair}}, D_\varphi) = \begin{cases} \dfrac{\lambda_1^2(1-D_{\text{stair}})\left[D_\varphi(1-D_\varphi) - \frac{D_{\text{stair}}^2}{6}\right]}{1 + D_{\text{stair}} + \frac{\lambda_1}{3}D_{\text{stair}}^2 - 2(1+\lambda_1)D_\varphi + 2\lambda_1 D_\varphi^2}, & D_\varphi < \frac{1}{2\lambda_1}\left[1 + \lambda_1 - \sqrt{(1+\lambda_1)^2 - 2\lambda_1\left(1 + D_{\text{stair}} + \frac{\lambda_1}{3}D_{\text{stair}}^2\right)}\right] \\ +\infty, & D_\varphi \geq \frac{1}{2\lambda_1}\left[1 + \lambda_1 - \sqrt{(1+\lambda_1)^2 - 2\lambda_1\left(1 + D_{\text{stair}} + \frac{\lambda_1}{3}D_{\text{stair}}^2\right)}\right] \end{cases} \tag{19}$$

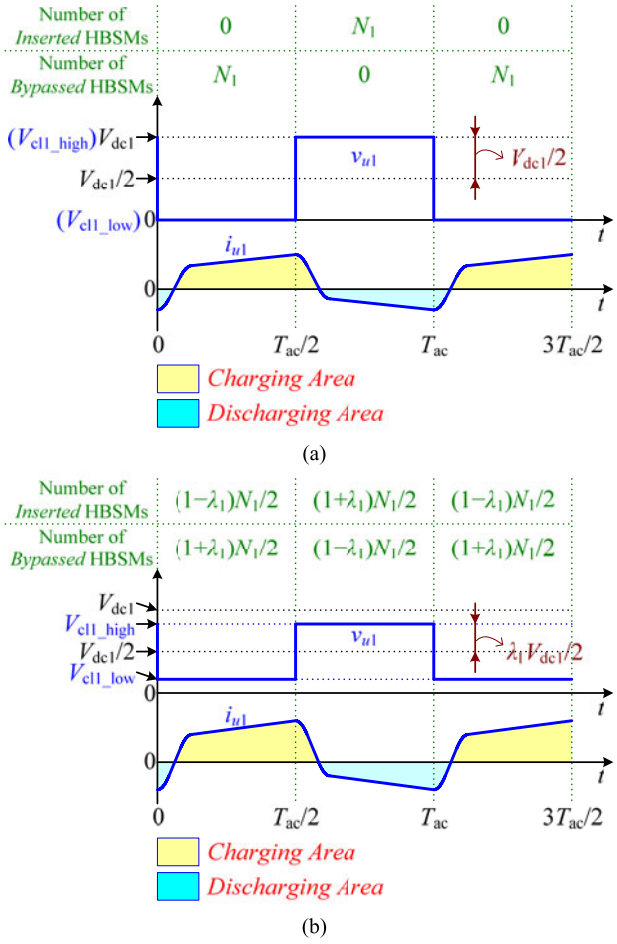

Fig. 10. Waveforms of v_{u1} and i_{u1}, where the voltage-changing transitions of v_{u1} are ignored. (a) $\lambda_1 = 1$. (b) $\lambda_1 < 1$.

V_{dc1}, which means that all the N_1 HBSMs are *inserted*. Thus, the capacitors of these HBSMs will be charged or discharged by i_{u1} when $i_{u1} > 0$ or $i_{u1} < 0$, respectively. Since the charging and discharging areas of i_{u1} over $[T_{\mathrm{ac}}/2, T_{\mathrm{ac}}]$ are usually not equal, the capacitor voltages of these HBSMs will be increased or decreased over this half-period. As a result, when considering multiple adjacent periods, these capacitor voltages will be totally unbalanced. Therefore, in order to ensure the balancing of the capacitor voltages of these HBSMs, λ_1 should be smaller than 1.

Fig. 10(b) shows the waveforms of v_{u1} and i_{u1} when $\lambda_1 < 1$. According to (3), (4), (9), (11), and (13), the integral of i_{u1} over the first half-period $[0, T_{ac}/2]$ can be calculated as

$$\begin{aligned}&\int_0^{T_{\mathrm{ac}}/2} i_{u1}(t)\,dt\\ &= \int_0^{T_{\mathrm{ac}}/2}\left[\frac{i_{\mathrm{pri}}(t)}{2}+i_{\mathrm{cir1}}(t)\right]dt = \int_0^{T_{\mathrm{ac}}/2}\left[\frac{i_{\mathrm{pri}}(t)}{2}+\frac{P}{V_{\mathrm{dc1}}}\right]dt\\ &\approx \frac{(1+\lambda_1)\lambda_2 M V_{\mathrm{dc1}}}{4L_{\mathrm{eq}}}\cdot t_\varphi\left(\frac{T_{\mathrm{ac}}}{2}-t_\varphi\right).\end{aligned} \tag{27}$$

As mentioned in Section III, D_φ is not larger than 0.5, and according to (14), $t_\varphi = D_\varphi \cdot T_{ac}/2$. So t_φ is no longer than $T_{\mathrm{ac}}/4$. Thus, according to (27), there is

$$\int_0^{T_{\mathrm{ac}}/2} i_{u1}(t)\,dt > 0. \tag{28}$$

Similarly, the integral of i_{u1} over the second half-period $[T_{\mathrm{ac}}/2, T_{\mathrm{ac}}]$ can be calculated as

$$\int_{T_{\mathrm{ac}}/2}^{T_{\mathrm{ac}}} i_{u1}(t)\,dt \approx \frac{V_{\mathrm{dc1}}}{4L_{\mathrm{eq}}}\cdot(\lambda_1-1)\lambda_2 M\cdot t_\varphi\left(\frac{T_{\mathrm{ac}}}{2}-t_\varphi\right). \tag{29}$$

Since t_φ is not larger than $T_{\mathrm{ac}}/4$ and $\lambda_1 < 1$, there is

$$\int_{T_{\mathrm{ac}}/2}^{T_{\mathrm{ac}}} i_{u1}(t)\,dt < 0. \tag{30}$$

As shown in Fig. 10(b), shortly before $t = 0$, v_{u1} equals $V_{cl1_{\mathrm{high}}} = (1+\lambda_1)V_{\mathrm{dc1}}/2$. Since the capacitor voltages of the HBSMs in this arm are about equal to V_{dc1}/N_1 if well balanced, there are $(1+\lambda_1)N_1/2$ HBSMs operating in *inserted* state and $(1-\lambda_1)N_1/2$ HBSMs in *bypassed* state. At $t = 0$, v_{u1} decreases from $V_{cl1_{\mathrm{high}}}$ to $V_{cl1_{\mathrm{low}}} = (1-\lambda_1)V_{\mathrm{dc1}}/2$, which means $\lambda_1 N_1$ HBSMs are changed from *inserted* state to *bypassed* state. As a result, during the half-period $(0, T_{\mathrm{ac}}/2)$, there are $(1-\lambda_1)N_1/2$ HBSMs in *inserted* state and $(1+\lambda_1)N_1/2$ HBSMs in *bypassed* state. According to (28), over the half-period $(0, T_{\mathrm{ac}}/2)$, the charging area of i_{u1} is larger than the discharging area, so the capacitor voltages of the $(1-\lambda_1)N_1/2$ HBSMs which are in the *inserted* state will have a net increase over this half-period. Thus, in order to balance the capacitor voltages, the $\lambda_1 N_1$ HBSMs with the highest voltages among the $(1+\lambda_1)V_{\mathrm{dc1}}/2$ HBSMs which are in *inserted* state shortly before $t = 0$ should be bypassed at $t = 0$ to avoid being charged.

As shown in Fig. 10(b), shortly before $t = T_{\mathrm{ac}}/2$, v_{u1} equals $V_{cl1_{\mathrm{low}}} = (1-\lambda_1)V_{\mathrm{dc1}}/2$. Since the capacitor voltages of the HBSMs in this arm are about equal to V_{dc1}/N_1 if well balanced, there are $(1-\lambda_1)N_1/2$ HBSMs in *inserted* state and $(1+\lambda_1)N_1/2$ HBSMs in *bypassed* state. At $t = T_{\mathrm{ac}}/2$, v_{u1} increases from $V_{cl1_{\mathrm{low}}}$ to $V_{cl1_{\mathrm{high}}} = (1+\lambda_1)V_{\mathrm{dc1}}/2$, which means that $\lambda_1 N_1$ HBSMs are changed from *bypassed* state to *inserted* state. As a result, during the half-period $(T_{\mathrm{ac}}/2, T_{\mathrm{ac}})$, there are $(1+\lambda_1)N_1/2$ HBSMs in *inserted* state and $(1-\lambda_1)N_1/2$ HBSMs in *bypassed* state. According to (22), over the half-period $(T_{\mathrm{ac}}/2, T_{\mathrm{ac}})$, the charging area of i_{u1} is smaller than the discharging area, so the capacitor voltages of the $(1+\lambda_1)N_1/2$ HBSMs which are in *inserted* state will have a net decrease over this half-period. Thus, in order to balance the capacitor voltages, the $\lambda_1 N_1$ HBSMs with the highest voltages among the $(1+\lambda_1)V_{\mathrm{dc1}}/2$ HBSMs which are in *bypassed* state shortly before $t = T_{\mathrm{ac}}/2$ should be inserted at $t = T_{\mathrm{ac}}/2$ for being charged.

It can be seen from Fig. 10 that within an ac-link period T_{ac}, there are $(1+\lambda_1)N_1/2$ HBSMs whose capacitor voltages will have a net decrease over the second half-period $(T_{\mathrm{ac}}/2, T_{\mathrm{ac}})$ but only $(1-\lambda_1)N_1/2$ HBSMs whose capacitor voltages will have a net increase over the first half-period $(0, T_{\mathrm{ac}}/2)$. Thus, for a certain HBSM, the possibility to have a net increase in its capacitor

voltage over a certain period, $\xi_{\rm inc1}$, is approximately equal to $[(1-\lambda_1)N_1/2]/N_1 = (1-\lambda_1)/2$ while the possibility to have a net decrease over a certain period, $\xi_{\rm dec1}$, is approximately equal to $[(1+\lambda_1)N_1/2]/N_1 = (1+\lambda_1)/2$. It is obvious that $\xi_{\rm inc1}$ is smaller than $\xi_{\rm dec1}$. This indicates that before the capacitor voltage of this HBSM gets the opportunity to have a net increase over a certain period, it will continue to have net decreases over $N_{\rm period1}$ periods, where $N_{\rm period1}$ is approximately equal to the ratio of $\xi_{\rm dec1}$ to $\xi_{\rm inc1}$, that is

$$N_{\rm period1} \approx \frac{\xi_{\rm dec1}}{\xi_{\rm inc1}} = \frac{1+\lambda_1}{1-\lambda_1}. \tag{31}$$

As a consequence, the capacitor voltage balancing of a certain HBSM is achieved every $(1+N_{\rm period1})$ ac-link periods. This means that with the same ac-link frequency, the values of the submodule capacitors in the proposed capacitor voltage-balancing control strategy will be a bit larger than those in the existing strategies [18]–[20], whose voltage balancing is usually achieved every ac-link period.

Apparently, the value of λ_1 will affect the capacitor voltage balancing of the HBSMs in $V_{\rm dc1}$-side arms. If properly reducing the value of λ_1, the value of $N_{\rm period1}$ will decrease according to (31), thus speeding up the capacitor voltage-balancing process. By doing so, the value of the HBSM capacitors could be reduced under the same voltage ripple limitation, thus lowering the system volume.

The approaches to implement capacitor voltage-balancing control for the other arms can be derived in the same way.

It is worth noting that the arm current sensors, which are necessary in the existing capacitor voltage-balancing control strategies to obtain the direction information of the currents [19]–[22], [27], [28], are not required in the proposed strategy, thus reducing the cost.

VI. Simulation Results

The IMDCC shown in Fig. 1(a) has been simulated in MATLAB/Simulink, where the proposed soft-switching operation scheme and capacitor voltage-balancing strategy are adopted. Table I lists the specifications and parameters of the main components of the QSW-IMDCC. The power is assumed to transfer from $V_{\rm dc1}$ side to $V_{\rm dc2}$ side, and the load at $V_{\rm dc2}$ side is a passive load. The voltage closed-loop control for regulating the output voltage $v_{\rm dc2}$ is incorporated. $v_{\rm dc2}$ is measured and then compared with the reference value $V_{\rm dc2_{ref}}$. The voltage error is sent to a proportional-integral regulator, producing the phase shift D_φ between the corresponding chain-link terminal voltages v_{u1} and v_{u2} (or v_{l1} and v_{l2}).

Fig. 11 shows the waveform of $v_{\rm dc2}$ during the start-up of the QSW-IMDCC. As seen, $v_{\rm dc2}$ goes into steady state after about 0.04 s and has an overshoot of 34%. Fig. 12 shows the steady-state simulation waveforms of the QSW-IMDCC at the rated power, from which we can see that v_{u1} has a square waveform expect for the voltage changing transitions which appear to be oblique lines approximately. Fig. 13 shows the voltage-changing transitions of v_{u1}. As seen in Fig. 13(a), there are $\lambda_1 N_1 = 10$ staircases in the voltage rising transition of v_{u1} since the

TABLE I
Simulation Parameters

Parameter	Symbol	Value
Rated input dc voltage	V_{dc1N}	800 kV
Rated output dc voltage	V_{dc2N}	160 kV
Rated active power	P_N	320 MW
V_{dc1}-side submodule number per arm	N_1	12
V_{dc2}-side submodule number per arm	N_2	12
V_{dc1}-side submodule energy-storage capacitor	C_{sm1}	0.1 mF
V_{dc2}-side submodule energy-storage capacitor	C_{sm2}	2.0 mF
Parallel capacitor of $V_{\rm dc1}$-side switch	C_{p_1}	4.7 nF
Parallel capacitor of $V_{\rm dc2}$-side switch	C_{p_2}	150 nF
Transformer turns ratio	K	5
V_{dc1}-side arm inductor	L_{arm1}	8 mH
V_{dc2}-side arm inductor	L_{arm2}	1.2 mH
The additional inductor plus the leakage inductor	$L_{add}+L_\sigma$	20.5 mH
Rated duty ratio of the shifted phase	$D_{\varphi N}$	0.3
AC-link frequency	f_{ac}	1 kHz
V_{dc1}-side voltage amplitude ratio	λ_1	10/12
V_{dc2}-side voltage amplitude ratio	λ_2	10/12
Voltage-changing transition duty ratio	$D_{\rm stair}$	0.05

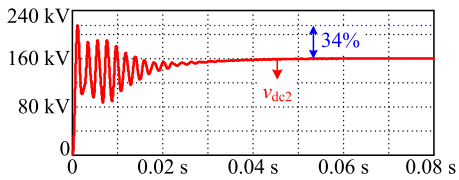

Fig. 11. Waveform of $v_{\rm dc2}$ during the start-up of the QSW-IMDCC.

HBSMs are inserted one by one during this transition. v_{u1} does not change sharply even at the rising edges because the parallel capacitors of the switches reduce the terminal voltage rising rate of an HBSM during the transition from *bypassed* state to *inserted* state. As seen in Fig. 13(b), the voltage falling transition of v_{u1} appears to be a smooth oblique line and has no staircases because the arm current i_{u1} is very small during this transition, which makes the charging and discharging of the switch parallel capacitors slow. As a result, the *dv/dt* of v_{u1} is reduced significantly.

The previous illustration is focused on v_{u1}. Actually, all the waveforms in Fig. 12 are in agreement with the corresponding ideal waveforms which can be drawn based on the parameters in Table I and the equations in Sections II and III, thus verifying the theoretical analysis in Sections II and III.

Fig. 14 shows the gate–emitter voltage v_{GE}, collector–emitter voltage v_{CE}, and collector current i_{CE} of the lower switch T_2 in the first HBSM in $V_{\rm dc1}$-side upper arm when the QSW-IMDCC operates at the rated power. As shown in Table I, D_φ equals 0.3 at this moment. Then, according to Fig. 9, with $M=1$ and $D_\varphi = 0.3$, the operation point of the QSW-IMDCC is below $P_{B_1 r}$ and $P_{B_1 f}$, which means that the full-ZVS conditions (18) and (22) are satisfied for T_2. Thus, T_2 can be zero-voltage turn-on or turn-off, which has been verified by Fig. 14. As seen from Fig. 14(a), before T_2 is turned on, v_{CE} has fallen to zero and i_{CE} flows through the antiparallel diode D_2. Thus, T_2 is zero-voltage turn-on. As seen from Fig. 14(b), v_{CE} increases with

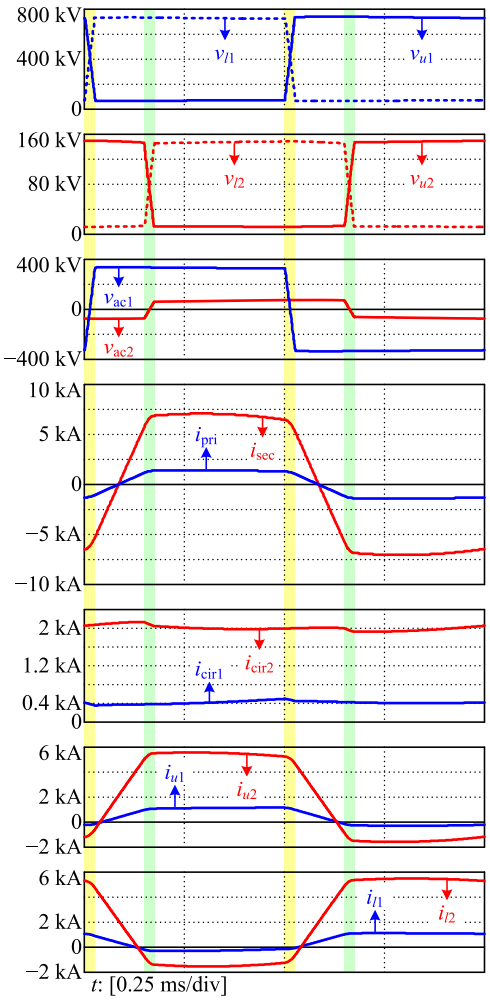

Fig. 12. Steady-state simulation waveforms of the QSW-IMDCC at the rated power.

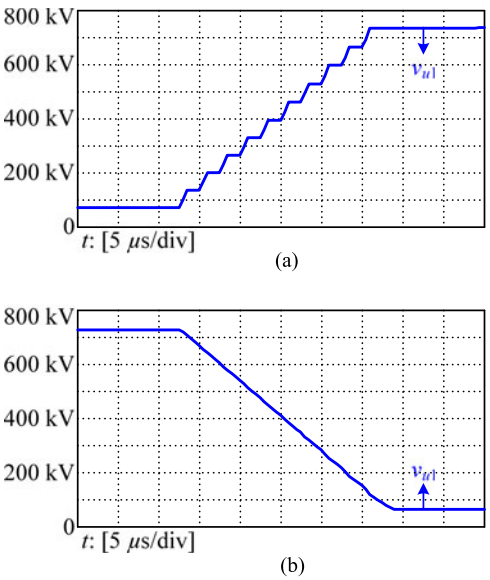

Fig. 13. Voltage-changing transitions of v_{u1}. (a) Rising transition. (b) Falling transition.

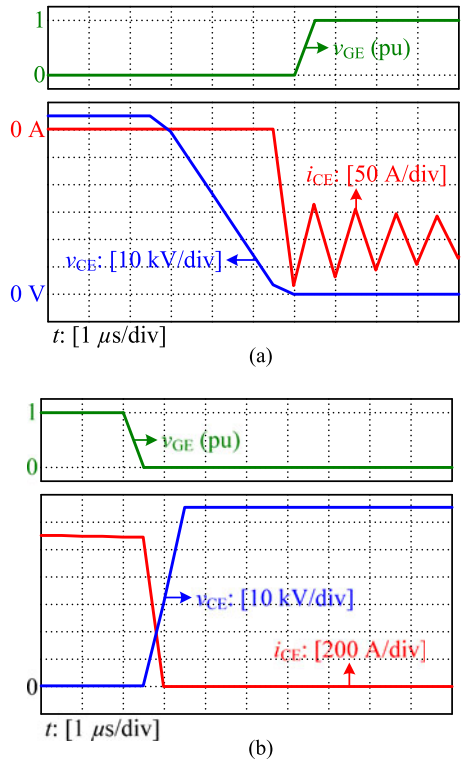

Fig. 14. v_{GE}, v_{CE}, and i_{CE} of T_2 in the first HBSM in V_{dc1}-side upper arm at the rated power. (a) Turn-on of T_2. (b) Turn-off of T_2.

a reduced rising rate when T_2 is turned off, thus achieving a nearly zero-voltage turn-off.

Fig. 15 shows v_{GE}, v_{CE}, and i_{CE} of the same switch T_2 when the QSW-IMDCC operates at half of the rated power. It can be calculated from (15) that D_φ is about 0.12 at this moment. Then, according to Fig. 9, with $M = 1$ and $D_\varphi = 0.12$, the operation point of the QSW-IMDCC is below $P_{B_1 r}$ but above $P_{B_1 f}$, which means that the full-ZVS condition (18) is satisfied for T_2 but (22) is not. Since T_2 is turned off during the voltage rising transitions and turned on during the voltage falling transitions, it can be concluded that T_2 can be zero-voltage turn-off but cannot be zero-voltage turn-on, which has been verified by Fig. 15. As seen from Fig. 15(a), when T_2 is turned on, v_{CE} is larger than zero. Thus, T_2 is not zero-voltage turn-on. As seen from Fig. 15(b), v_{CE} rises slowly when T_2 is turned off, thus achieving a nearly zero-voltage turn-off.

In conclusion, the simulation waveforms in Figs. 14 and 15 are in agreement with the theoretical analysis in Section IV. Similar study can be applied to other switches, and the conclusion is the same.

Fig. 16(a) shows the capacitor voltage waveforms of the 12 HBSMs in V_{dc1}-side upper arm. As seen, all the capacitor voltages are well balanced and basically fluctuate within 95–105% of the reference value (66.7 kV), which proves that the capacitor voltage-balancing control strategy is effective. Fig. 16(b) shows the capacitor voltage waveform of one of the HBSMs as an example. As seen, before the capacitor voltage has a net increase

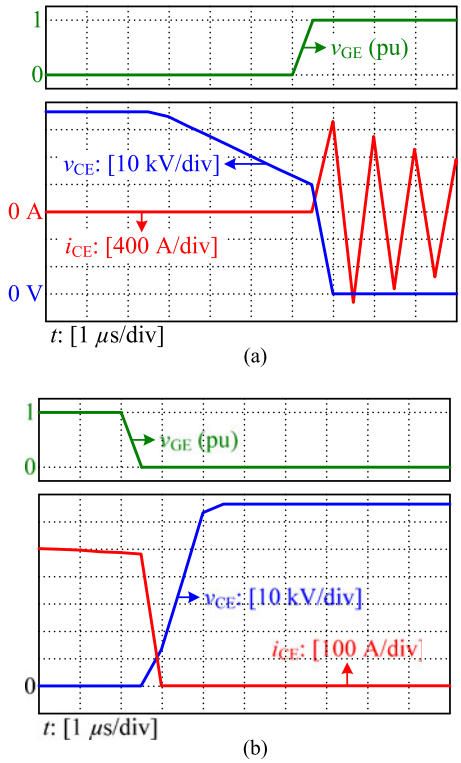

Fig. 15. v_{GE}, v_{CE}, and i_{CE} of T_2 in the first HBSM in V_{dc1}-side upper arm at half of the rated power. (a) Turn-on of T_2. (b) Turn-off of T_2.

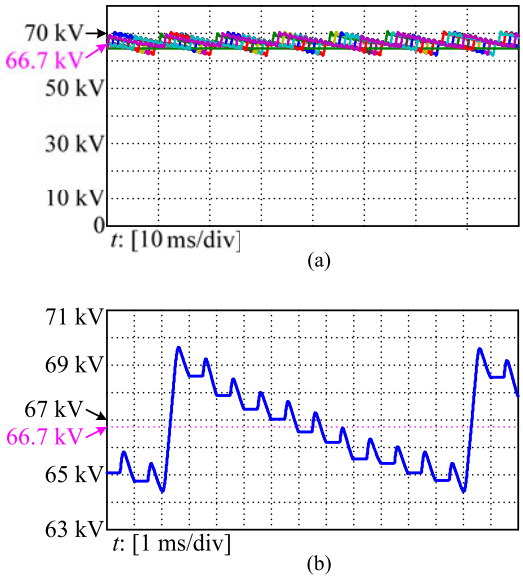

Fig. 16. Capacitor voltage waveforms of the 12 HBSMs in V_{dc1}-side upper arm. (a) All of the capacitor voltages. (b) One of the capacitor voltages.

over a certain period, it continues to have net decreases over the previous ten periods, which approximately verifies (31).

As mentioned in Section I, the IMDCC has dc fault blocking capability. Fig. 17 shows the waveforms of v_{ac1}, v_{ac2}, the output dc current i_{dc2}, and the input dc current i_{dc1} when a V_{dc2}-side dc short-circuit fault occurs at $t = 0.1$ s. Since all the switches

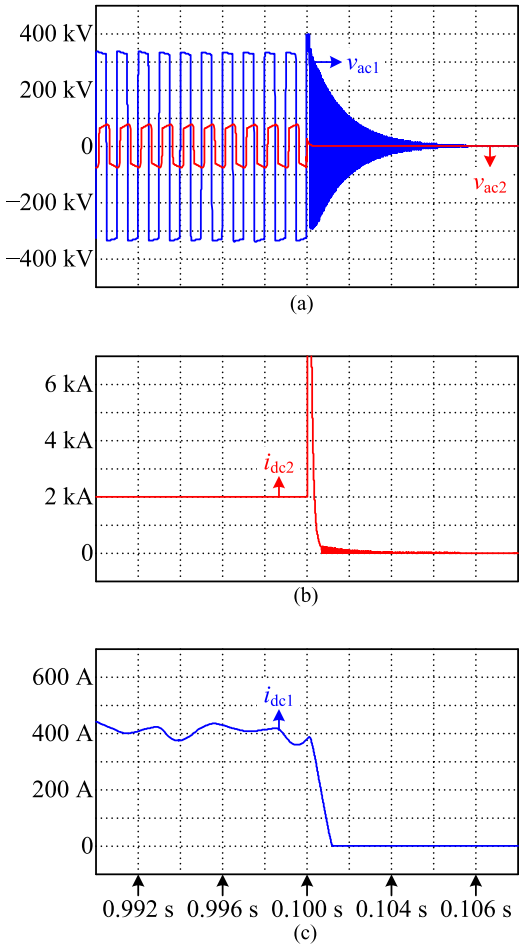

Fig. 17. Waveforms of v_{ac1}, v_{ac2}, i_{dc2}, and i_{dc1} responding to a V_{dc2}-side dc short-circuit fault. (a) v_{ac1} and v_{ac2}. (b) i_{dc2}. (c) i_{dc1}.

in the IMDCC are forced to be turned off when a fault current (i.e., 1.5 p.u.) is sensed, the HBSMs are rejected from the power conversion. Thus, the equivalent ac voltage sources v_{ac1} and v_{ac2} attenuate to zero after the dc fault as shown in Fig. 17(a). Since the fault side only absorbs energy, V_{dc2}-side arm currents are always positive and flow through the antiparallel diodes of the lower switches of the HBSMs, clamping the terminal voltages of V_{dc2}-side chain-links to zero. Thus, v_{ac2} decreases to zero rapidly. In contrast, V_{dc1}-side arm currents are alternating, making the parallel capacitors of the HBSM switches oscillate with the arm inductors, the additional inductor, and the transformer leakage inductor. Thus, v_{ac1} oscillates around zero with a gradually decreasing amplitude.

As seen from Fig. 17(b), the output dc current i_{dc2} rises sharply when the dc fault occurs, but reduces to zero after only one ac-link period (1 ms) since all the switches in the IMDCC are forced to be turned off. Thus, the fault current is successfully limited before causing more damage. As seen from Fig. 17(c), the input dc current i_{dc1} does not rise sharply but attenuates to zero rapidly after the dc fault occurs, which implies that the fault has been successfully blocked and not propagated from the fault side to the healthy side.

VII. Conclusion

This paper proposes a soft-switching operation scheme for the IMDCC with a high ac-link frequency. In this scheme, a QSW modulation method is employed. The chain-links in the QSW-IMDCC utilize voltage-changing transitions to reduce the *dv*/*dt* of their terminal voltages. The chain-link terminal voltages are QSWs with their voltage rising and falling transitions intentionally arranged to be staircase shaped. During the voltage rising (or falling) transition of a chain-link terminal voltage, the HBSMs in the corresponding arm are inserted (or bypassed) one by one. By doing so, the height of each stair is limited to one submodule capacitor voltage, thus reducing the *dv*/*dt*. Besides, in the QSW-IMDCC, each of the two arms in the same phase will conduct half of the transformer current, and each arm current will also contain a circulating component. With such arm currents, soft switching can be achieved for the power switches, so the QSW-IMDCC can suffer less switching loss and thus have a higher efficiency. Moreover, a capacitor voltage-balancing control strategy is proposed in Section V. The core of this strategy is to properly select the HBSMs which are to be inserted or bypassed during the voltage-changing transitions. It is worth noting that this strategy does not need any arm current sensors, thus reducing the cost. Finally, the proposed soft-switching operation scheme and capacitor voltage-balancing control strategy are verified by the simulation results.

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