Reliability Analysis and Redundancy Configuration of MMC With Hybrid Submodule Topologies

Jianzhong Xu, *Member, IEEE*, Penghao Zhao, and Chengyong Zhao, *Member, IEEE*

***Abstract*—Modular multilevel converter (MMC) has become the most promising converter technology for high-voltage direct current (HVdc) transmission systems. MMC submodule (SM) topologies with dc fault ride-through capabilities are emerging which are suitable for overhead line applications. The hybrid SM design of each converter arm can get the compromise of higher capability of handling dc fault and lower capital investments and losses. In this paper, the initial hybrid SM numbers design method for supporting the dc-link voltage and riding-through dc faults and the optimized hybrid SM redundancy configuration strategy for effectively increasing the reliability of MMC are proposed and calculated. In contrast with the previously proposed redundancy configuration for MMC with the single SM topology, this approach solves the curvature of three-dimensional surface to calculate the recommended redundant hybrid SM numbers which takes both the semiconductor device utilization rate and the reliability of MMC into consideration.**

***Index Terms*—Hybrid submodule (SM), modular multilevel converter (MMC), redundancy configuration, reliability analysis, three-dimensional (3-D) surface.**

I. Introduction

MODULAR multilevel converter-based high-voltage direct current (MMC-HVdc) transmission is gaining in popularity as a dc power transmission option [1]–[4]. Compared with the conventional two- and three-level voltage-sourced converters (VSC), the MMC topology offers more advantages such as [1], [2]:

1) its modular design permits easier scalability to any desired voltage and power levels simply by including a larger or smaller number of modules;
2) output voltage waveform with negligible ripple content which eliminates the need for ac filters;
3) no common dc-link capacitor is required;
4) lower switching losses which leads to high efficiency.

In future, the widespread use of the MMC-HVdc transmission is anticipated [5]. However, the lack of the dc fault ride-through capability imposes major restrictions on half-bridge MMC (H-MMC) used in overhead line (OHL) transmission fields.

The dc circuit breakers (DCCB) are supposed to be the best choice for the use of H-MMC in large-scale dc grid. However, high-voltage and large-current DCCBs are not yet put into practical applications [6]. The alternative choice under this situation is to use the MMC topologies with built-in dc fault handling capability, mainly including the full-bridge MMC, the clamp-double MMC, and the MMC using hybrid converter arm design which contains no less than two different submodule (SM) topologies and at least one of them can interrupt the dc-side short-circuit fault current.

In 2010, ALSTOM proposed hybrid multilevel converter topologies at CIGRE [7], and the hybrid converters combine the characteristics of two-level VSC and MMC. The hybrid cascaded multilevel converter (HCMC) and alternate-arm multilevel converter (AAMC) are two specific topologies of these hybrid converters which can ride-through severe dc fault. However, HCMC and AAMC are in relation to the press-packed series technology of insulated gate bipolar transistor (IGBT), while in this paper, only the universal three-phase symmetrical MMC topology and the different SM configurations are discussed.

Qin *et al.* [8] proposed two new SM topologies as well as a hybrid design methodology using the proposed SMs to embed the dc fault handling capability into MMC. For large-scale dc grid with multiple MMC converters, hundreds of SMs in each phase arm should be equipped with a certain number of redundant SMs to increase the operation reliability of the HVdc system. However, Qin *et al.* [8] considered the topology design only and did not include the reliability analysis and redundancy configurations of the hybrid MMC.

In the previous research, Zhao *et al.* proposed the dc fault ride-through capability index (DFRTI) [9] for the purpose of evaluating the dc fault current suppressing capability of the MMC using different SM topologies, and the DFRTI index will be a basis of this paper to design the initial hybrid SM numbers and the redundancy configuration.

The authors also proposed an effective reliability analysis method for calculating the SM redundancy configuration of the MMC with single SM topology in [10]. Similarly, MMC with hybrid SM topologies should guarantee the basic dc fault ride-through capability and high operation reliability at the same time. However, more redundant SMs will bring higher reliability as well as higher capital investments and losses. To save cost, it is important to evaluate the redundancy efficiency of a single semiconductor device, and this is defined as the semiconductor utilization rate of IGBTs which will be introduced in later

Manuscript received April 8, 2015; accepted June 3, 2015. Date of publication June 12, 2015; date of current version November 30, 2015. This work was supported in part by the National Natural Science Foundation of China under Grant 51177042 and the National High Technology Research and Development Program of China (863 Program) under Grant 2013AA050105, and in part by the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources (LAPS15017) and the Fundamental Research Funds for the Central Universities (2015QN04). Recommended for publication by Associate Editor M. A. Perez.

The authors are with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing 102206, China (e-mail: xujianzhong@ncepu.edu.cn; zhao_penghao@outlook.com; chengyongzhao@ncepu.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2444877

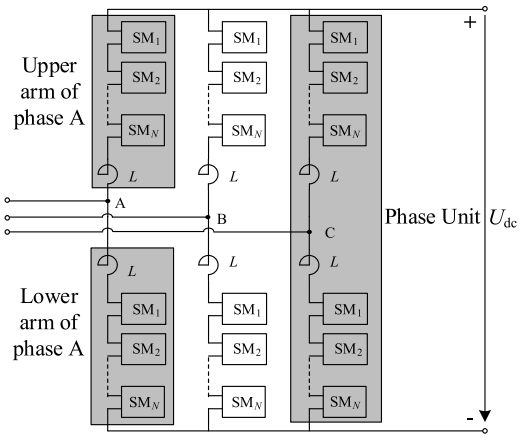

Fig. 1. Schematic diagram of a three-phase MMC.

sections. The authors have studied the dc fault ride-through capability and reliability analysis of the MMC with single SM topology and achieved certain results. This paper will further extend the previous research to the MMC with hybrid SM topologies and propose the corresponding reliability and redundancy configuration method of hybrid MMC followed by the recommended redundant number of SMs for engineering design.

The rest of this paper is organized as follows. Section II introduces the topologies of MMC and several SMs. Section III studies the initial critical SM number configuration of hybrid MMC. Section IV presents the reliability analysis and redundancy configuration method. Section V verifies the proposed approach. Section VI provides some discussions and Section VII concludes this paper.

II. MMC AND SM TOPOLOGIES

This section introduces the MMC topology and different types of SM structures, including those which have the ability to ride-through severe dc-side fault. Latter section will show how these SMs are effectively and economically configured to interrupt the short-circuit currents and increase the reliability of MMC. The fully detailed MMC model shown in Fig. 1 is comprised of three phase units and each unit consists of upper and lower phase arms. Each phase arm includes N identical SMs and an arm reactor L. The controller shown in [11] is used to suppress the circulating second harmonic current among the phase units.

The SMs are the basic building blocks of MMC, Fig. 2, respectively, represents the half-bridge SM (HBSM) [12], the full-bridge SM (FBSM) [13], the clamp double SM (CDSM) [14], the clamp single SM (CSSM) [15], and the improved hybrid SM (IHSM) [16]. All SMs are comprised of IGBTs, diodes, and dc storage capacitors. Note that Fig. 2 also shows the fault current paths (see dotted lines in Fig. 2) after the IGBTs are blocked (shadow areas), which are the preparations for the later initial SM numbers design in the hybrid MMC.

In Fig. 2, except the HBSM, all the other four SM topologies permit the MMC to ride-through the dc fault simply by blocking all the valves after the dc fault detected.

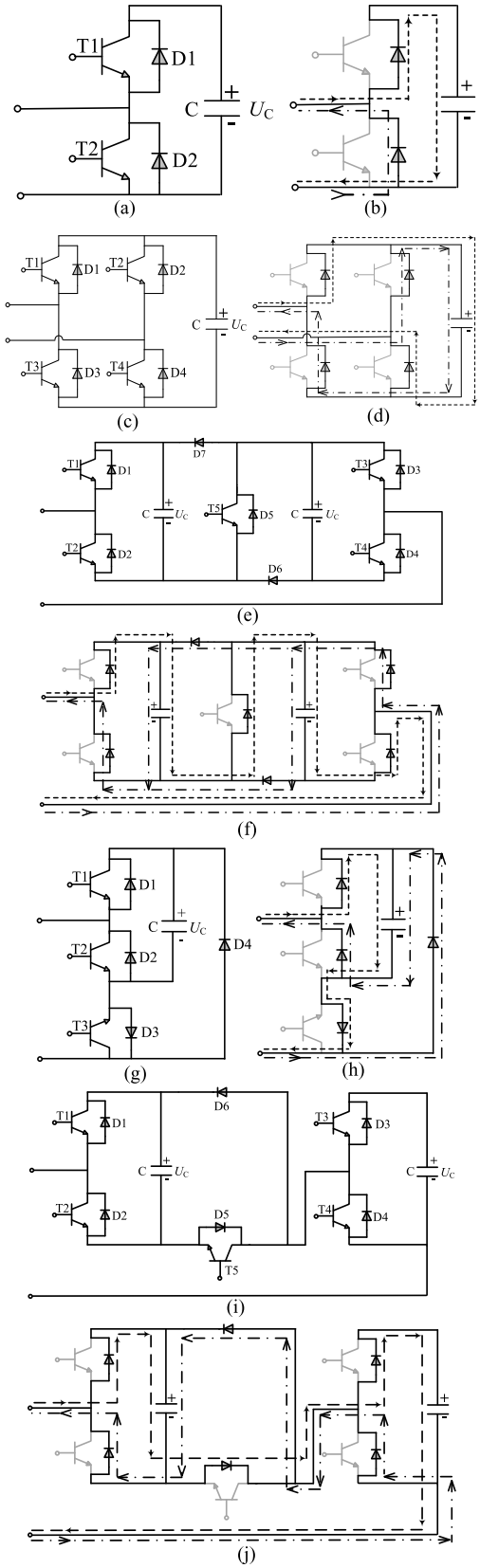

Fig. 2. Structures and fault current paths of SMs. (a) Structure of HBSM. (b) Fault current path of HBSM. (c) Structure of FBSM. (d) Fault current path of FBSM. (e) Structure of CDSM. (f) Fault current path of CDSM. (g) Structure of CSSM. (h) Fault current path of CSSM. (i) Structure of IHSM. (j) Fault current path of IHSM.

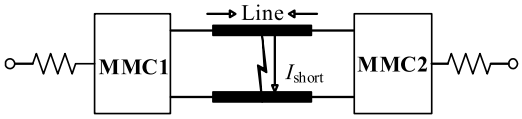

Fig. 3. Diagram of dc fault in the MMC-HVdc system.

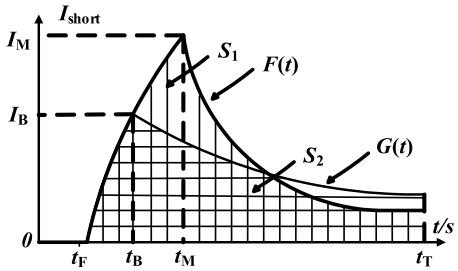

Fig. 4. Principle diagram of DFRTI.

Previously, the DFTRI was proposed to evaluate the dc fault current clearing capabilities of MMC [9]. DFRTI is defined as (1) and illustrated in Figs. 3 and 4

$$\text{DFRTI} = \frac{S_1}{S_2} = \frac{\int_{t_F}^{t_T} F(t)dt}{\int_{t_F}^{t_T} G(t)dt}. \tag{1}$$

In (1) and Figs. 3 and 4, the following symbols are defined:

I_{short}: the instantaneous dc pole-to-pole short-circuit current shown in Fig. 3;

t_F: the time when dc fault occurred;

t_B: the time when MMCs are blocked;

I_B: the value of I_{short} at t_B;

F(*t*): I_{short} curve under dc fault without blocking MMCs;

G(*t*): I_{short} curve under dc fault with MMCs blocked at t_B;

S_1: area under curve *F*(*t*) from t_F to t_T shown in Fig. 4;

S_2: area under curve G(*t*) from t_F to t_T shown in Fig. 4;

I_M: the maximum value of I_{short};

t_M: the time when I_{short} reaches its maximum value;

t_T: the time when 3-phase ac breakers are tripped.

Using the simulation data, DFRTI values of MMCs with different SM topologies can be obtained by numerical integration, and the comparison results are as follows:

$$\begin{aligned}\text{DFRTI}\,(\text{FBSM}) &= \text{DFRTI}\,(\text{CSSM}) > \text{DFRTI}\,(\text{CDSM}) \\ &= \text{DFRTI}\,(\text{IHSM}) \gg \text{DFRTI}\,(\text{HBSM}).\end{aligned}$$

The results above show the dc fault blocking capabilities of the five different SMs, which corresponds with the analysis of the fault current paths illustrated in Fig. 2.

For each SM, the required device numbers are, respectively, shown in Table I, note that this is not the final required device number comparison under the same dc-link voltage because CDSM and IHSM undertake twice of the dc capacitor voltage as compared with the HBSM, FBSM, and CSSM.

From the DFRTI index and device number comparisons above, CSSM and CDSM seem to be the relatively promising choices for the OHL MMC-HVdc transmission systems. HBSM-based MMC-HVdc cannot ride-through dc faults. Hence, the expensive underground or undersea cables are required. However, CSSM uses 50% more IGBTs and CDSM uses 25% more IGBTs compared with HBSM.

TABLE I
DEVICE NUMBER OF SMS

SM type	IGBT	Diode	Capacitor
HBSM	2	2	1
FBSM	4	4	1
CDSM	5	7	2
CSSM	3	4	1
IHSM	5	6	2

Therefore, the hybrid MMCs with different SM topologies are emerging as shown in [17]–[19], and normally the HBSM is selected as the fundamental SM topology to support the dc-link voltage and the other SMs with higher DFRTI values are responsible for cutting off the dc fault currents.

In this paper, two hybrid MMC topologies are considered; the first topology is the hybrid of HBSM and CSSM, and the second topology is the hybrid of HBSM and CDSM. Next section will calculate the initial critical number ratio of the two SM topologies in the hybrid MMC and later section will show the proposed reliability analysis and redundancy configuration methods, which are the main contributions of this paper.

III. INITIAL CRITICAL MODULE NUMBER CONFIGURATION IN THE HYBRID MMC

Section II introduces several SM topologies of the MMC; hence, based on the combination of these topologies, hybrid MMC may have many different variants. To reduce the investments, hybrid MMC with HBSM and another SM topology should be the first priority. Meantime, it is necessary to block the MMC after dc fault occurs, so the second SM topology should possess the dc fault ride-through capability. To guarantee the dc fault handling capability of the hybrid MMC, the least number of SMs with higher DFRTI should be constrained. It is worth noting that the various SM topologies have identical steady-state characteristic, hence the function of supporting the entire dc-link voltage can be simply calculated by adding all inserted SM capacitor voltages together.

As described previously, the first hybrid MMC (defined as hybrid MMC1) in this paper is composed of HBSM and CSSM, and the short-circuit-current path of hybrid MMC1 under blocked state is shown in Fig. 5.

The numbers of the HBSMs and CSSMs in the same arm are N_{H} and N_{CS}, respectively. The SM capacitor voltage U_{C}, dc-link voltage U_{dc}, and ac voltage have the following relationship, in which *m* is the modulation ratio ($m < 1$), and U_{ph} and U_{L} are the phase and line-to-line voltage amplitudes of the secondary side of the transformer. Since this is the initial critical

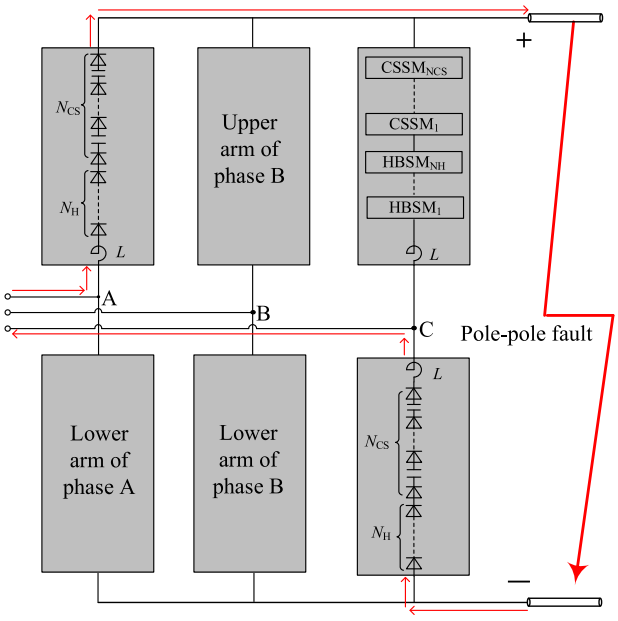

Fig. 5. Arm current path of the hybrid MMC1 under blocked state.

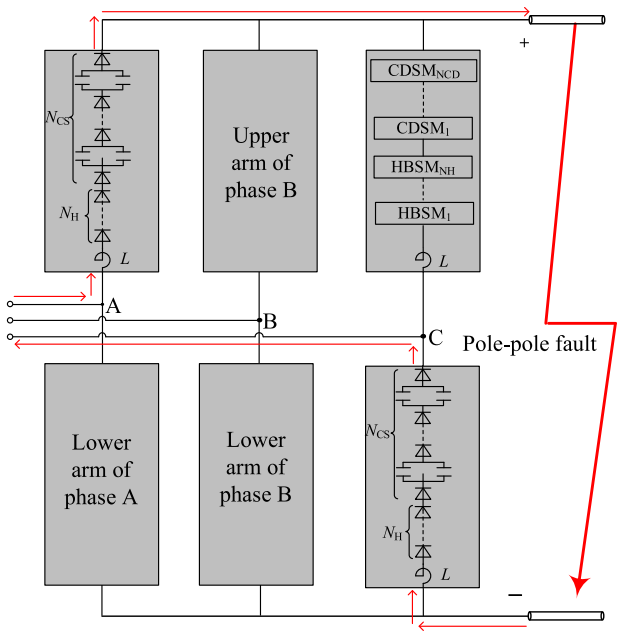

Fig. 6. Arm current path of the hybrid MMC2 under blocked state.

SM number design, the redundant SMs are ignored

$$\begin{cases} U_{\rm dc} = (N_{\rm H} + N_{\rm CS})U_{\rm C} \\ U_{\rm ph} = \frac{1}{2}mU_{\rm dc} = \frac{1}{2}m(N_{\rm H} + N_{\rm CS})U_{\rm C} \\ U_L = \sqrt{3}U_{\rm ph} = \frac{\sqrt{3}}{2}m(N_{\rm H} + N_{\rm CS})U_{\rm C}. \end{cases} \tag{2}$$

As shown in Table I, the CSSMs require more IGBTs than HBSMs; hence, to find the minimum ratio of CSSM in the phase arm, it is necessary to study the worst dc fault scenario of the MMC-HVdc system, which is the pole-to-pole short-circuit fault [9]. For hybrid MMC1 with HBSM and CSSM, only CSSM can cut off the fault current, as can be seen from Fig. 2. In Fig. 5, fault current flows between upper arm and lower arm of two different phase units, and taking the upper arm of phase A and lower arm of phase C as an example, there are two $N_{\rm CS}$ capacitors connected in series to withstand the peak value of the line-to-line ac voltage. To guarantee the dc fault ride-through capability of the hybrid MMC1, the number of CSSM in an arm should meet the requirement as

$$2N_{\rm CS}U_{\rm C} \geq U_L. \tag{3}$$

Substituting (2) into (3), we obtain

$$\left\lceil \frac{\sqrt{3}}{4}m \right\rceil \leq \frac{N_{\rm CS}}{N_{\rm H} + N_{\rm CS}} \leq 1. \tag{4}$$

$\lceil {\rm X} \rceil$ is the ceiling function. The value of m is usually between 0.85 and 0.9 in normal operation. To insure that the hybrid MMC1 can cut off dc fault currents in all circumstances, $m = 1$ is selected. Thus, the minimum proportion of $N_{\rm CS}$ in an arm is 0.43 approximately, and the above analysis can be applied to the hybrid MMC with HBSM and FBSM as well.

As for CDSM, it is different from FBSM and CSSM. It can be seen from Fig. 2 that a CDSM is equivalent to two HBSMs under the steady-state operation. While under a blocked state, its two capacitors are in paralleled connection. Therefore, the effective clamped voltage of the two capacitors in one CDSM is still $U_{\rm C}$, as shown in Fig. 6. Similarly, the SM capacitor voltage Uc, dc-link voltage $U_{\rm dc}$ and ac voltage have the following relationship:

$$\begin{cases} U_{\rm dc} = (N_{\rm H} + 2N_{\rm CD})U_{\rm C} \\ U_{\rm ph} = \frac{1}{2}mU_{\rm dc} = \frac{1}{2}m(N_{\rm H} + 2N_{\rm CD})U_{\rm C} \\ U_L = \sqrt{3}U_{\rm ph} = \frac{\sqrt{3}}{2}m(N_{\rm H} + 2N_{\rm CD})U_{\rm C}. \end{cases} \tag{5}$$

The total voltage of the capacitors under blocked state in the arm current path is 2 $N_{\rm CD}U_{\rm C}$. To cut off the dc fault current, the total voltage of capacitors in hybrid MMC2 should satisfy

$$2N_{\rm CD}U_{\rm C} \geq U_L. \tag{6}$$

The proportion of $N_{\rm CD}$ in an arm can be concluded from (5) and (6), as

$$\left\lceil \frac{\sqrt{3}m}{4 - \sqrt{3}m} \right\rceil \leq \frac{N_{\rm CD}}{N_{\rm H} + N_{\rm CD}} \leq 1. \tag{7}$$

To ensure the dc fault ride-through capability, $m = 1$ is selected. In this case, the minimum proportion of $N_{\rm CD}$ is 0.76 approximately.

Once the proportion of the number of CSSM or CDSM in the hybrid MMC is obtained, the initial critical SM number is determined, which can ensure the basic dc fault ride-through capability of the hybrid MMC. However, the final number of the SMs will be decided in latter section considering the SM redundancy configuration schemes.

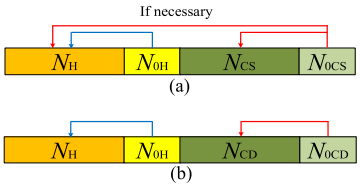

Fig. 7. Number of SMs in an arm of the hybrid MMC. (a) Hybrid MMC1 with HBSM and CSSM. (b) Hybrid MMC2 with HBSM and CDSM.

IV. Reliability Analysis and Redundancy Configuration

For an MMC equipped with redundant SMs, the redundant SMs can substitute those faulted SMs as long as the number of faulted SMs is not more than the number of redundant SMs. However, the reliability analysis and redundancy configuration of a hybrid MMC is more complicated than an MMC with a single SM topology. As in some cases, the redundant SMs with higher DFRTI (i.e., CSSM) can be used to substitute the faulted HBSM, and this is not the case for CDSM, since it has two capacitors in each SM. Similarly, the redundant HBSMs cannot be used to substitute the faulted CSSM or CDSM to guarantee the dc faults handling capability of the hybrid MMC, as shown in Fig. 7.

Because of the symmetry of MMC, reliability of an arm can represent the reliability of the MMC to some extent. This section will mainly focus on the analysis of the reliability of the hybrid MMCs and provide the entire framework of the analysis procedures.

In Fig. 7, $N_{\rm H}$, $N_{\rm CS}$, and $N_{\rm CD}$ are the initial critical numbers of HBSM, CSSM, and CDSM, respectively, under steady state, as previously illustrated in Section III. $N_{0\rm H}$, $N_{0\rm CS}$, and $N_{0\rm CD}$ are the corresponding redundant numbers of HBSM, CSSM, and CDSM, respectively. Fig. 7(a) represents the hybrid MMC1 with HBSM and CSSM, in which the red arrow means that redundant CSSMs can substitute the faulted HBSMs and CSSMs, the blue arrow means that redundant HBSMs can only substitute faulted HBSMs. Fig. 7(b) shows the hybrid MMC2 with HBSM and CDSM, in which the red arrow means redundant CDSMs can only substitute the faulted CDSMs and the blue arrow means redundant HBSMs can only substitute the faulted HBSMs.

A. Reliability Analysis of Hybrid MMC

All the SM topologies of MMCs are mainly composed of several IGBTs, diodes, and capacitors (ignoring the protective switches). Hence, the reliability of MMC, which can be defined as continuously reliable working in a certain time period, is mainly decided by these devices. If the reliabilities of IGBT, diode, and capacitor are defined as R_I, R_D, and R_C, respectively, according to the number of devices shown in Table I, reliabilities of HBSM, CSSM, and CDSM can be calculated as

$$R_{\rm H} = R_I^2 R_D^2 R_C \tag{8}$$

$$R_{\rm CS} = R_I^3 R_D^4 R_C \tag{9}$$

$$R_{\rm CD} = R_I^5 R_D^7 R_C^2. \tag{10}$$

If the numbers of the faulted HBSMs and CSSMs in an arm are $i_{\rm H}$ and $i_{\rm CS}$, respectively, as described previously, the calculation of the MMC reliability should include the following two parts:

1) $i_{\rm H}$ is not more than $N_{\rm H}$, while $i_{\rm CS}$ is not more than $N_{\rm CS}$, the reliability of the hybrid MMC1 is R_1, which is shown in (11), and in this situation, there is no substitution between HBSM and CSSM. Therefore, the maximum of faulted CSSMs is only limited by the redundant number of CSSMs

$$R_1 = \sum_{i_{\rm H}=0}^{N_{0\rm H}} \left[\sum_{i_{\rm CS}=0}^{N_{0\rm CS}} C_{N_{\rm H}+N_{0\rm H}}^{i_{\rm H}} (1-R_{\rm H})^{i_{\rm H}} R_{\rm H}^{N_{\rm H}+N_{0\rm H}-i_{\rm H}} \times C_{N_{\rm CS}+N_{0\rm CS}}^{i_{\rm CS}} (1-R_{\rm CS})^{i_{\rm CS}} R_{\rm CS}^{N_{\rm CS}+N_{0\rm CS}-i_{\rm CS}} \right] \tag{11}$$

2) $i_{\rm H}$ is more than $N_{\rm H}$, and in this case $i_{\rm CS}$ must be not more than $N_{\rm H} + N_{\rm CS} - i_{\rm H}$, the reliability of hybrid MMC1 is R_2, as shown in (12). While in this case, the maximum of faulted CSSMs is limited because $i_{\rm H}$ is greater than $N_{\rm H}$ and some redundant CSSMs are used to substitute faulted HBSMs

$$R_2 = \sum_{i_{\rm H}=N_{0\rm H}+1}^{N_{0\rm H}+N_{0\rm CS}} \left[\sum_{i_{\rm CS}=0}^{N_{0\rm H}+N_{0\rm CS}-i_{\rm H}} C_{N_{\rm H}+N_{0\rm H}}^{i_{\rm H}} (1-R_{\rm H})^{i_{\rm H}} \times R_{\rm H}^{N_{\rm H}+N_{0\rm H}-i_{\rm H}} C_{N_{\rm CS}+N_{0\rm CS}}^{i_{\rm CS}} (1-R_{\rm CS})^{i_{\rm CS}} \times R_{\rm CS}^{N_{\rm CS}+N_{0\rm CS}-i_{\rm CS}} \right]. \tag{12}$$

Therefore, the overall reliability of the hybrid MMC1 can be obtained by adding (11) and (12), as

$$R_{\rm MMC1} = R_1 + R_2. \tag{13}$$

For hybrid MMC2 with HBSM and CDSM, CDSM is equivalent to two HBSMs under steady state, and there are no substitutions between redundant HBSMs and CDSMs. Hence, the reliability of the hybrid MMC2 can be directly obtained by (14), in which $i_{\rm H}$ and $i_{\rm CD}$ are the numbers of the faulted HBSMs and CDSMs in the hybrid MMC arm, respectively

$$R_{\rm MMC2} = \sum_{i_{\rm H}=0}^{N_{0\rm H}} \left[\sum_{i_{\rm CD}=0}^{N_{0\rm CD}} C_{N_{\rm H}+N_{0\rm H}}^{i_{\rm H}} (1-R_{\rm H})^{i_{\rm H}} R_{\rm H}^{N_{\rm H}+N_{0\rm H}-i_{\rm H}} \times C_{N_{\rm CD}+N_{0\rm CD}}^{i_{\rm CS}} (1-R_{\rm CD})^{i_{\rm CD}} R_{\rm CD}^{N_{\rm CD}+N_{0\rm CD}-i_{\rm CD}} \right]. \tag{14}$$

In this section, the possible substitution between SMs with different dc fault blocking capabilities is addressed, which is the major point of concern when deducing the reliability equations and actually it does make the equations relatively complicated. The reliabilities of the hybrid MMCs increase with the number of redundant SMs growing and the changing rates of the three-dimensional (3-D) curves can be calculated by first-order differences and further the critical points of the redundancy configurations can be obtained for optimal selection.

B. First-Order Difference of the Reliability of the Hybrid MMC

For hybrid MMC1 with HBSM and CSSM, to simplify the calculation, values of R_{MMC1} are put into matrix R_{M1}. The elements in R_{M1} are shown in (15), where $N_{0\mathrm{H}m}$ and $N_{0\mathrm{CS}m}$ are the maximum values of $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$

$$R_{\mathrm{M1}}(i,j) = R_{\mathrm{MMC1}}|_{N_{0\mathrm{H}}=j-1,N_{0\mathrm{CS}}=i-1} \quad (i=1,2,\ldots,N_{0\mathrm{CSm}}+1, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}+1). \tag{15}$$

For hybrid MMC1, to reveal the mathematical rules of R_{MMC1} changing with $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$, it is necessary to calculate the first-order differences of $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$ separately. For discrete data, first-order difference can represent the changing rate of R_{MMC1} to $N_{0\mathrm{H}}$ and $N_{0\mathrm{C}}$ approximately. Specifically, when the $N_{0\mathrm{H}}$ ($N_{0\mathrm{CS}}$) is fixed, the first-order difference of $N_{0\mathrm{CS}}(N_{0\mathrm{H}})$ is calculated. Because $N_{0\mathrm{H}}$ ($N_{0\mathrm{CS}}$) has many values, for ease of calculation, the first-order difference of $N_{0\mathrm{H}}$ ($N_{0\mathrm{CS}}$) is put into a matrix *D* as well.

Note that the first-order difference method used in this paper is backward difference. The matrices of first-order differences of $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$ are D_{H} and D_{CS}, respectively. Calculation formulas of D_{H} and D_{CS} are

$$D_{\mathrm{H}}(i,j) = R_{M1}(i,j+1) - R_{M1}(i,j) \quad (i=1,2,\ldots,N_{0\mathrm{CSm}}+1, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}) \tag{16}$$

$$D_{\mathrm{CS}}(i,j) = R_{M1}(i+1,j) - R_{M1}(i,j) \quad (i=1,2,\ldots,N_{0\mathrm{CSm}}, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}+1). \tag{17}$$

It is easy to understand that the value of R_{MMC1} increases with $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$ growing, however the changing rate of R_{MMC1} varies. Hence, there should be a critical point and if $N_{0\mathrm{H}}$ or $N_{0\mathrm{CS}}$ is larger than the threshold value, the changing rate of R_{MMC1} becomes fairly small, and it is of great importance to find these critical points. A threshold value *t* is set and the method to select the critical points is

$$D_{\mathrm{H}}(i,j) \geq \mathrm{t} \text{ and } D_{\mathrm{H}}(i,j+1) < t \quad (i=1,2,\ldots,N_{0\mathrm{CSm}}, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}-1) \tag{18}$$

$$D_{\mathrm{CS}}(i,j) \geq \mathrm{t} \text{ and } D_{\mathrm{CS}}(i+1,j) < t \quad (i=1,2,\ldots,N_{0\mathrm{CSm}}-1, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}). \tag{19}$$

Similarly, the reliability matrix R_{M2} of hybrid MMC2 with HBSM and CDSM is shown in (20), in which $N_{0\mathrm{H}m}$ and $N_{0\mathrm{CD}m}$ are the maximum values of $N_{0\mathrm{H}}$ and $N_{0\mathrm{CD}}$

$$R_{M2}(i,j) = R_{\mathrm{MMC2}}|_{N_{0\mathrm{H}}=j-1,N_{0\mathrm{CD}}=i-1} \quad (i=1,2,\ldots,N_{0\mathrm{CDm}}+1, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}+1). \tag{20}$$

For hybrid MMC2, D_{H} and D_{CD} are

$$D_{\mathrm{H}}(i,j) = R_{M2}(i,j+1) - R_{M2}(i,j) \quad (i=1,2,\ldots,N_{0\mathrm{CDm}}+1, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}) \tag{21}$$

$$D_{\mathrm{CD}}(i,j) = R_{M2}(i+1,j) - R_{M2}(i,j) \quad (i=1,2,\ldots,N_{0\mathrm{CDm}}, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}+1). \tag{22}$$

The rules for selecting the critical points of redundant SM numbers are

$$D_{\mathrm{H}}(i,j) \geq t \text{ and } D_{\mathrm{H}}(i,j+1) < t \quad (i=1,2,\ldots,N_{0\mathrm{CDm}}, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}-1) \tag{23}$$

$$D_{\mathrm{CS}}(i,j) \geq t \text{ and } D_{\mathrm{CS}}(i+1,j) < t \quad (i=1,2,\ldots,N_{0\mathrm{CSm}}-1, \qquad j=1,2,\ldots,N_{0\mathrm{Hm}}). \tag{24}$$

C. Optimal SM Redundancy Configuration of the Hybrid MMC

As for the optimal redundancy configuration of the hybrid MMC, the individual device utilization ratio should be considered to ensure that each redundant SM provides the largest reliability increase to the hybrid MMC. For this purpose, this paper also considers the economic factor and proposes the redundancy efficiency of the IGBTs in the redundant SMs.

For hybrid MMC1, similar to the reliability analysis, the effective number of IGBT in redundant SMs is calculated in (25)–(27). In fact, in (27), *Q* is mathematical expectation of the effective number of IGBT in redundant SMs. The definition of the IGBT utilization rate in redundant SMs is shown in (28)

$$Q_1 = \sum_{i_{\mathrm{H}}=0}^{N_{0\mathrm{H}}} \left[\sum_{i_{\mathrm{CS}}=0}^{N_{0\mathrm{CS}}} (2i_{\mathrm{H}}+3i_{\mathrm{CS}}) C_{N_{\mathrm{H}}+N_{0\mathrm{H}}}^{i_{\mathrm{H}}} (1-R_{\mathrm{H}})^{i_{\mathrm{H}}} \times R_{\mathrm{H}}^{N_{\mathrm{H}}+N_{0\mathrm{H}}-i_{\mathrm{H}}} C_{N_{\mathrm{CS}}+N_{0\mathrm{CS}}}^{i_{\mathrm{CS}}} (1-R_{\mathrm{CS}})^{i_{\mathrm{CS}}} \times R_{\mathrm{CS}}^{N_{\mathrm{CS}}+N_{0\mathrm{CS}}-i_{\mathrm{CS}}} \right] \tag{25}$$

$$Q_2 = \sum_{i_{\mathrm{H}}=N_{0\mathrm{H}}+1}^{N_{0\mathrm{H}}+N_{0\mathrm{CS}}} \left[\sum_{i_{\mathrm{CS}}=0}^{N_{0\mathrm{H}}+N_{0\mathrm{CS}}-i_{\mathrm{H}}} (2i_{\mathrm{H}}+3i_{\mathrm{CS}}) C_{N_{\mathrm{H}}+N_{0\mathrm{H}}}^{i_{\mathrm{H}}} \times (1-R_{\mathrm{H}})^{i_{\mathrm{H}}} R_{\mathrm{H}}^{N_{\mathrm{H}}+N_{0\mathrm{H}}-i_{\mathrm{H}}} C_{N_{\mathrm{CS}}+N_{0\mathrm{CS}}}^{i_{\mathrm{CS}}} (1-R_{\mathrm{CS}})^{i_{\mathrm{CS}}} \times R_{\mathrm{CS}}^{N_{\mathrm{CS}}+N_{0\mathrm{CS}}-i_{\mathrm{CS}}} \right] \tag{26}$$

$$Q = Q_1 + Q_2 \tag{27}$$

$$\eta_1 = \frac{Q}{2N_{0\mathrm{H}}+3N_{0\mathrm{CS}}}. \tag{28}$$

For hybrid MMC2, there is no substitution between HBSM and CDSM, hence the effective number and utilization rate of IGBT in redundant SMs are shown in

$$Q = \sum_{i_{\mathrm{H}}=0}^{N_{0\mathrm{H}}} \left[\sum_{i_{\mathrm{CD}}=0}^{N_{0\mathrm{CD}}} (2i_{\mathrm{H}}+5i_{\mathrm{CD}}) C_{N_{\mathrm{H}}+N_{0\mathrm{H}}}^{i_{\mathrm{H}}} (1-R_{\mathrm{H}})^{i_{\mathrm{H}}} \times R_{\mathrm{H}}^{N_{\mathrm{H}}+N_{0\mathrm{H}}-i_{\mathrm{H}}} C_{N_{\mathrm{CD}}+N_{0\mathrm{CD}}}^{i_{\mathrm{CD}}} (1-R_{\mathrm{CD}})^{i_{\mathrm{CD}}} \times R_{\mathrm{CD}}^{N_{\mathrm{CD}}+N_{0\mathrm{CD}}-i_{\mathrm{CD}}} \right] \tag{29}$$

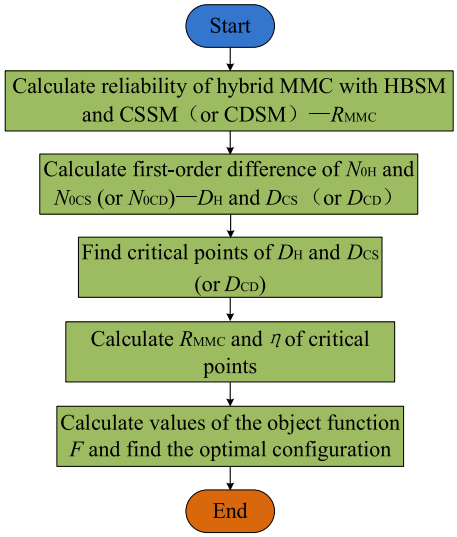

Fig. 8. Flowchart of the proposed optimal redundancy configuration of the hybrid MMC.

$$\eta_2 = \frac{Q}{2N_{0\mathrm{H}} + 5N_{0\mathrm{CD}}}. \tag{30}$$

In order to process the optimal design of the redundancy configuration, for both hybrid MMC1 and hybrid MMC2, the object function proposed in this paper is defined as

$$F = \omega_1 R_{\mathrm{MMC}} + \omega_2 \eta \tag{31}$$

in which both the MMC reliability and IGBT utilization rate are taken into consideration, and ω_1 and ω_2 are the weighting factors. Calculation of F uses the values of $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$ (or $N_{0\mathrm{CD}}$) obtained from (18) (or (23)) and (19) (or (24)). $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$ (or $N_{0\mathrm{CD}}$) referring to the maximum value of F are the optimal redundancy configuration of the hybrid MMC. The flowchart of the proposed optimal redundancy configuration of MMC with hybrid SM topologies is shown in Fig. 8.

Fig. 8 includes the main procedures of the proposed redundancy configuration method and will be validated step by step in later section using examples of both hybrid MMC1 and hybrid MMC2.

V. Validations

The previous section introduces the proposed method of calculating the optimal SM redundancy configuration of hybrid MMC. For more vivid expression, numerical examples are shown in this section. The calculation is accomplished in MATLAB.

A. Hybrid MMC1 With HBSM and CSSM

In this example, $N_{\mathrm{H}} = 220$, $N_{\mathrm{CS}} = 180$, and the proportion of N_{CS} in hybrid MMC1 is 0.45 (larger than 0.43, for the ease of calculation). This proportion can fulfil the requirement of cutting off dc fault currents. $N_{0\mathrm{H}}$ is selected not to be more than 20% of N_{H}, and $N_{0\mathrm{CS}}$ is not more than 20% of N_{CD}, which means $N_{0\mathrm{Hm}} = 44$ and $N_{0\mathrm{CSm}} = 36$. Assuming the values of

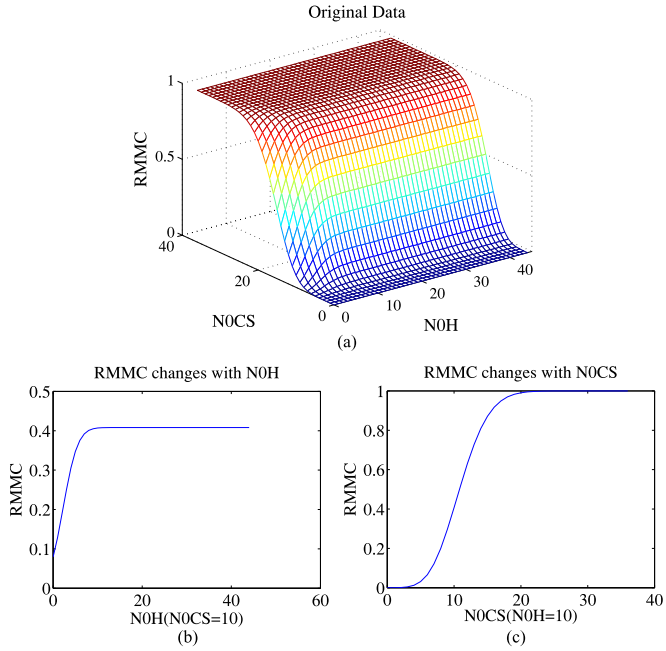

Fig. 9. Reliability of the hybrid MMC1. (a) R_{MMC1} changes with $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$. (b) R_{MMC1} changes with $N_{0\mathrm{H}}$. (c) R_{MMC1} changes with $N_{0\mathrm{CS}}$.

TABLE II
Reliability of the Hybrid MMC1

$N_{0\mathrm{CS}}$ \ $N_{0\mathrm{H}}$	11	12	13	14	15
11	0.5224	0.5227	0.5228	0.5228	0.5228
12	0.6320	0.6323	0.6324	0.6324	0.6324
13	0.7291	0.7294	0.7295	0.7295	0.7295
14	0.8095	0.8097	0.8098	0.8098	0.8098
15	0.8719	0.8721	0.8721	0.8722	0.8722

the reliabilities of the single IGBT, diode, and capacitor are known, then according to (8)–(10), the calculated values are $R_{\mathrm{H}} = 0.98$ and $R_{\mathrm{CS}} = 0.94$.

The first step is to calculate the reliability of the hybrid MMC1. Fig. 9 shows the 3-D surface of R_{MMC} changing with $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$, and part of the values of R_{MMC} are shown in Table II.

The results of the first-order differences of R_{MMC1} are shown in Fig. 10, D_{H} and D_{CS} are the first-order differences of $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$, some of the values of D_{H} and D_{CS} are shown in Tables III and IV.

From (18) and (19), many critical points are found, and some of them are presented in Table V.

Since both the MMC reliability and economic issues should be considered, without loss of generality, both ω_1 and ω_2 are set to be 0.5 in this example. It is worth noting that the values of $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$ correspond to the maximum F in (31). Therefore, using these data, the optimal hybrid SM redundancy configuration can be found, which is as follows.

Table VI shows the optimal redundant numbers of HBSMs and CSSMs, which are, respectively, 8 and 19 (with $N_{\mathrm{H}} =$

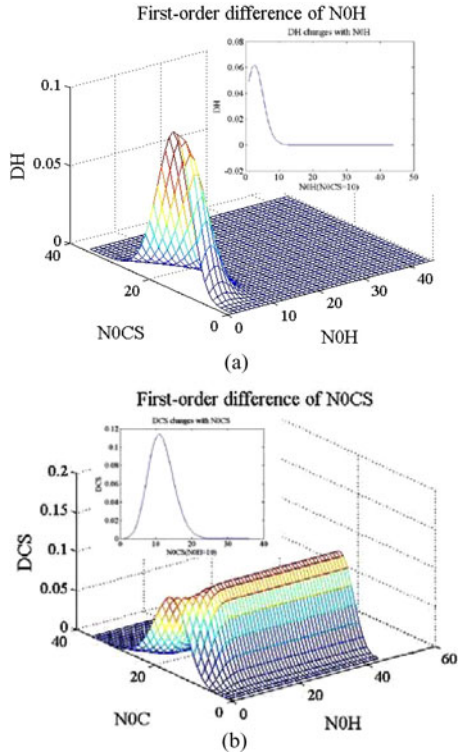

Fig. 10. First-order differences of $N_{0\mathrm{H}}$ and $N_{0\mathrm{CS}}$ (a) D_H (b) D_{CS}

TABLE III
FIRST-ORDER DIFFERENCE OF $N_{0\mathrm{H}}$

$N_{0\mathrm{CS}}$ \ $N_{0\mathrm{H}}$	4	5	6	7	8
11	0.0641	0.0480	0.0316	0.0185	0.0098
12	0.0693	0.0508	0.0329	0.0191	0.0010
13	0.0698	0.0501	0.0319	0.0182	0.0094
14	0.0660	0.0462	0.0290	0.0164	0.0084
15	0.0588	0.0403	0.0248	0.0138	0.0070

TABLE IV
FIRST-ORDER DIFFERENCE OF $N_{0\mathrm{CS}}$

$N_{0\mathrm{CS}}$ \ $N_{0\mathrm{H}}$	4	5	6	7	8
11	0.0995	0.1047	0.1075	0.1088	0.1093
12	0.1001	0.1007	0.0999	0.0989	0.0981
13	0.0948	0.0910	0.0872	0.0842	0.0823
14	0.0849	0.0777	0.0717	0.0675	0.0649
15	0.0722	0.0630	0.0558	0.0511	0.0483

220, $N_{\mathrm{CS}} = 180$, and SM reliabilities $R_{\mathrm{H}} = 0.98$ and $R_{\mathrm{CS}} = 0.94$). The reliability of the hybrid MMC1 is 0.9815, which is large enough for the normal operation of MMC, and $\eta = 0.5972$ indicates that more than 50% of the redundant IGBTs in hybrid MMC1 are effectively utilized to cut-off the dc short-circuit fault current.

TABLE V
CRITICAL POINTS FOR THE HYBRID MMC1

$N_{0\mathrm{H}}$	$N_{0\mathrm{CS}}$	R_{MMC1}	η_1	F
9	18	0.9691	0.5924	0.7808
8	19	0.9815	0.5972	0.7894
8	20	0.9898	0.5835	0.7866
7	21	0.9937	0.5814	0.7876
7	22	0.9967	0.5646	0.7807
6	23	0.9977	0.5603	0.7790
5	24	0.9981	0.5556	0.7768
4	25	0.9982	0.5507	0.7744

TABLE VI
OPTIMAL REDUNDANCY CONFIGURATION OF THE HYBRID MMC1

$N_{0\mathrm{H}}$	$N_{0\mathrm{CS}}$	R_{MMC1}	η_1	F
8	19	0.9815	0.5972	0.7894

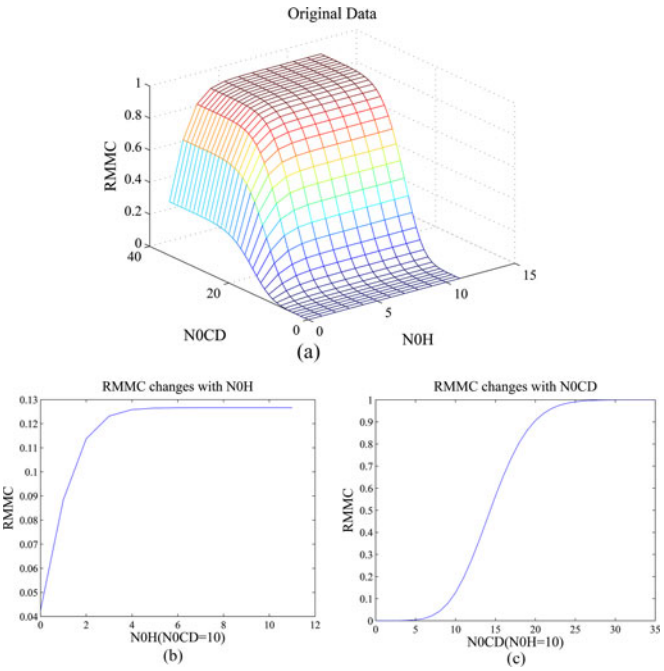

Fig. 11. Reliability of the hybrid MMC2. (a) R_{MMC2} changes with $N_{0\mathrm{H}}$ and $N_{0\mathrm{CD}}$. (b) R_{MMC2} changes with $N_{0\mathrm{H}}$. (c) R_{MMC2} changes with $N_{0\mathrm{CD}}$.

B. Hybrid MMC2 With HBSM and CDSM

To make the two scenarios of hybrid MMC1 and MMC2 more comparable, the hybrid converters are assumed to have the same dc-link voltage, hence in this example, $N_{\mathrm{H}} = 54$, $N_{\mathrm{CD}} = 173$, and the proportion of N_{CD} in an arm is approximately 0.76. This proportion can fulfil the requirement of cutting off the dc fault currents. $N_{0\mathrm{H}}$ is not more than 20% of N_{H}, while $N_{0\mathrm{CS}}$ is not more than 20% of N_{CD}, which means $N_{0\mathrm{Hm}} = 11$ and $N_{0\mathrm{CSm}} = 35$ (maximum values). Also, assume the values of $R_{\mathrm{H}} = 0.98$ and $R_{\mathrm{CD}} = 0.92$. According to Fig. 8, the first step is to calculate the reliability of the hybrid MMC2. Fig. 11 shows the

TABLE VII
RELIABILITY OF THE HYBRID MMC2

N_{0CD} \ N_{0H} / R_{MMC2}	7	8	9	10	11
7	0.0212	0.0212	0.0212	0.0212	0.0212
8	0.0425	0.0425	0.0425	0.0425	0.0425
9	0.0768	0.0768	0.0768	0.0768	0.0768
10	0.1266	0.1266	0.1266	0.1266	0.1266
11	0.1930	0.1930	0.1930	0.1930	0.1930

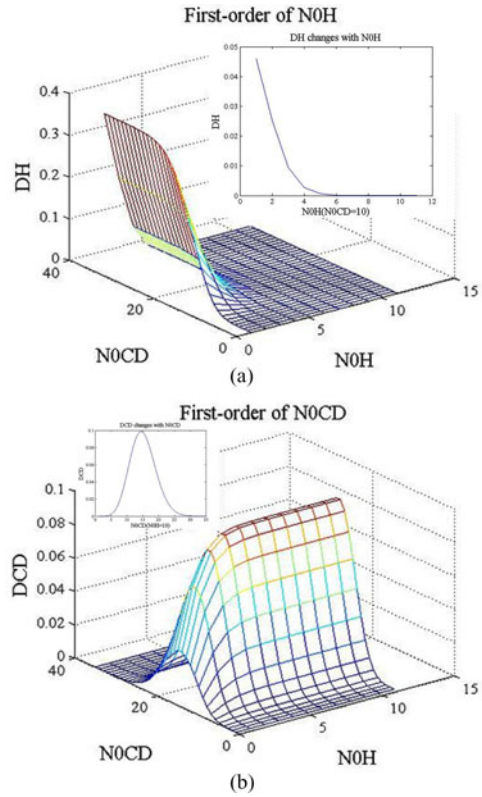

Fig. 12. First-order differences of N_{0H} and N_{0CD} (a) D_H (b) D_{CD}

TABLE VIII
FIRST-ORDER DIFFERENCE OF N_{0H}

N_{0CD} \ N_{0H} / D_H	0	1	2	3	4
11	0.2381	0.1309	0.0489	0.0139	0.0032
12	0.2679	0.1473	0.0550	0.0157	0.0036
13	0.2930	0.1612	0.0602	0.0171	0.0040
14	0.3133	0.1723	0.0643	0.0183	0.0043
15	0.3288	0.1808	0.0675	0.0192	0.0045

3-D surface of R_{MMC} changing with N_{0H} and N_{0CD}, and some values of R_{MMC} are shown in Table VII.

The results of the first-order differences of N_{0H} and N_{0CS} of R_{MMC2} are shown in Fig. 12, and some values of D_H and D_{CS} are shown in Tables VIII and IX.

Based on (23) and (24), there are also many critical points, and some of them are presented in Table X.

TABLE IX
FIRST-ORDER DIFFERENCE OF N_{0CD}

N_{0CD} \ N_{0H} / D_{CD}	6	7	8	9	10
6	0.0118	0.0118	0.0118	0.0118	0.0118
7	0.0213	0.0213	0.0213	0.0213	0.0213
8	0.0342	0.0343	0.0343	0.0343	0.0343
9	0.0499	0.0499	0.0499	0.0499	0.0499
10	0.0664	0.0664	0.0664	0.0664	0.0664

TABLE X
CRITICAL POINTS FOR THE HYBRID MMC2

N_{0H}	N_{0CD}	R_{MMC2}	η_2	F
4	28	0.9924	0.2465	0.6195
5	28	0.9974	0.3249	0.6611
6	28	0.9983	0.3827	0.6905
7	28	0.9985	0.4186	0.7085
8	28	0.9985	0.4367	0.7176
9	28	0.9985	0.4434	0.7210
10	28	0.9985	0.4437	0.7211
11	28	0.9985	0.4408	0.7196

TABLE XI
OPTIMAL REDUNDANCY CONFIGURATION OF THE HYBRID MMC2

N_{0H}	N_{0CD}	R_{MMC2}	η_2	F
10	28	0.9985	0.4437	0.7211

Using these data, and based on (31), set $\omega_1 = \omega_1 = 0.5$, then the optimal SM redundancy configuration can be obtained, which is shown in Table XI.

Table XI indicates that for $N_H = 54$ and $N_{CD} = 173$, hybrid MMC2 requires much more redundant CDSMs as compared with the number of redundant CSSMs in hybrid MMC1, that is because there are more IGBTs and diodes in CDSM which leads to lower SM reliability and the dc fault blocking capability of the single CDSM (with two capacitors inside) is only the same as the single CSSM (only one capacitor inside), i.e., *DFRTI* (CSSM) $>$ *DFRTI* (CDSM). Even R_{MMC} is fairly satisfying with the value of 0.9985, its IGBT utilization rate is only 0.4437 which is much smaller than that in hybrid MMC1. Therefore, the hybrid MMC1 with HBSM and CSSM is supposed to be a preferable converter topology for the use in future OHL-based HVdc system.

VI. DISCUSSION

The reliability of the hybrid MMC increases with the number of the redundant SMs growing. However, this leads to higher complexity of the control system and larger investments. Therefore, it is reasonable to believe that there is a compromise (tradeoff) between the enough high reliability and relatively low investments, and there should be an optimal hybrid SM redundancy configuration by considering both of the converter reliability and the utilization rates of IGBTs. Because IGBTs are the most expensive devices in converter parts of the MMC-HVdc

systems, they are supposed to be representing the investments of the hybrid MMCs in a certain way.

When severe dc pole to pole short-circuit fault occurs, simply by blocking all the IGBTs in hybrid MMCs, the healthy redundant SMs with dc fault ride-through capability can enhance the ability of the hybrid MMC when cutting off the fault currents (the faulted SMs are bypassed and can no longer be inserted into the fault current path). In addition, the SMs with higher DFRTI is possible to substitute the HBSMs if the number of the faulted HBSMs is more than the redundant SMs which is supposed to increase the reliability of hybrid MMC in normal operations.

VII. Conclusion

This paper analyzed the initial proportions of the different SM topologies in hybrid MMCs on the precondition of handling the dc pole-to-pole short-circuit fault currents. Beginning from the initial SM configuration, this paper also proposes the approach to calculate the optimal SM redundancy configuration of the hybrid MMCs, in which the reliability of hybrid MMC and the utilization rate of IGBTs are considered.

Two hybrid MMCs which are respectively composed of HBSM working with CSSM, and HBSM working with CDSM are considered. The flowchart of the optimal SM number design is provided for the engineers of this field which is supposed to calculate the recommended values of the redundant SMs of hybrid MMCs, not only suitable for the two examples presented in this paper but also any multilevel converters with different SM topologies. Meanwhile, given the same reliability values of the IGBTs, diodes, and capacitors, calculation results show that the hybrid MMC1 is more economical and has greater application potentials than hybrid MMC2 if taking both dc fault ride-through capability and device utilization rate into consideration.

Acknowledgment

The authors would like to thank Prof. R. Iravani from the University of Toronto for providing many useful suggestions.

References

[1] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[2] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. F. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.

[3] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[4] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[5] J. Xu, C. Zhao, W. Liu, and C. Guo, "Accelerated model of modular multilevel converters in PSCAD/EMTDC," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 129–136, Jan. 2013.

[6] J. Xu, A. M. Gole, and C. Zhao, "The use of averaged-value model of modular multilevel converter in dc grid," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 519–528, Apr. 2015.

[7] D. R. Trainer, C. C. Davidson, C. D. M. Oates, N. M. Macleod, D. R. Critchley, and R. W. Crookes, "A new hybrid voltage sourced converter for hvdc power transmission," presented at the CIGRE Meeting, Paris, France, 2010, p. B4_111.

[8] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for hvdc systems based on various submodule circuits," *IEEE Trans Power Del.*, vol. 30, no. 1, pp. 385–394, Feb. 2015.

[9] C. Zhao, J. Xu, and T. Li, "DC faults ride-through capability analysis of Full-Bridge MMC-MTDC System," *Sci. China Technol. Sci.*, vol. 56, no. 1, pp. 253–261, Jan. 2013.

[10] C. Wang, C. Zhao, and J. Xu, "A method of calculating sub-module redundancy configurations in modular multilevel converters," *Autom. Electr. Power Syst.*, vol. 37, no. 16, pp. 103–107, Aug. 2013.

[11] R. Picas, J. Pou, S. Ceballos, J. Zaragoza, G. Konstantinou, and V. Agelidis, "Optimal injection of harmonics in circulating currents of modular multilevel converters for capacitor voltage ripple minimization," in *Proc. IEEE ECCE Asia Downunder*, 2013, pp. 318–324.

[12] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Tech. Conf.*, 2003, pp. 3–6.

[13] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-Bus-applications," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 502–507.

[14] R. Marquardt, "Modular multilevel converter topologies with DC-short circuit current limitation," in *Proc. IEEE 8th Int. Power Electron. ECCA Asia Conf.*, 2011, pp. 1425–1431.

[15] P. Zhao, C. Wang, J. Xu *et al.* "A sub-module topology of MMC with DC fault ride-through capability," *Power Syst. Technol.*, vol. 38, no. 12, pp. 3441–3446, Dec. 2014.

[16] J. Zhang, C. Zhao, L. Guo, "Simulation analysis on submodule topology of modular multilevel converter," *Autom. Electr. Power Syst.*, vol. 39, no. 2, pp. 106–111, Jan. 2015.

[17] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1137–1146, Mar. 2015.

[18] R. Zeng, L. Xu, L. Yao, and J. Morrow, "Pre-charging and DC fault ride-through of hybrid mmc based hvdc systems," *IEEE Trans. Power Del.*, vol. 30, no. 3, pp. 1298–1306, Jun. 2015.

[19] R. Li, G. Adam, D. Holliday, J. Fletcher, and B. Williams, "Hybrid cascaded modular multilevel converter with dc fault ride-through capability for hvdc transmission system," *IEEE Trans. Power Del.*, (Early Access).

Jianzhong Xu (M'14) was born in Shanxi, China. He received the B.S. and Ph.D. degrees from North China Electric Power University (NCEPU), Beijing, China, in 2009 and 2014, respectively.

He is currently a Lecturer at the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, NCEPU. From 2012 to 2013, he was a Visiting Scholar of the University of Manitoba, Winnipeg, MB, Canada. His research interests include HVdc and flexible ac transmission systems.

Penghao Zhao was born in Henan, China. He received the B.S. degree from North China Electric Power University, Beijing, China, in 2013, where he is currently working toward the M.A. degree in power system and its automation.

His research interest includes HVdc.

Chengyong Zhao (M'05) was born in Zhejiang, China. He received the B.S., M.S., and Ph.D. degrees in power system and its automation from North China Electric Power University (NCEPU), Beijing, China, in 1988, 1993, and 2001, respectively.

He is currently a Professor and the Deputy Director of the New Energy Power Grid Institute in the Electrical and Electronic Engineering School of NCEPU. His research interests include HVdc and flexible ac transmission systems.