Reconfigurable Periodic Bifrequency DPWM With Custom Harmonic Reduction in DC–DC Converters

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***Abstract*—Majority of spectral spreading techniques employ chaos-based pulsewidth-modulation (PWM) schemes in a switching dc–dc converter, in which neither dynamic performance nor ripple parameter can be correctly predicted so as for efficiency. Periodic frequency modulation using a triangular carrier wave can achieve custom spectral spreading and harmonic reduction. This paper proposes a periodic bifrequency digital PWM (BF-DPWM) technique in a dc–dc converter, which uses two discrete frequencies f_1 and f_2 as guided by a modulating signal $f_{\rm m}$. Fourier analysis shows that f_1 and f_2 do not exist; however, they contribute to power spectrum of $f_{\rm m}$. This method achieves considerable harmonic reduction and improved DPWM resolution with an insignificant ripple impact, compared to a dither-based periodic modulation scheme. Design guidelines using simulation study are presented. A buck converter prototype has been made, and different control schemes are implemented using a field-programmable gate array device. Test results show that the BF-DPWM has insignificant impacts on transient performance. Finally, the proposed scheme is extended to the triangular-wave modulation scheme, which results in further harmonic reduction.**

***Index Terms*—Bi-frequency modulation, conducted EMI, DC-DC converters, digital pulse width modulator, periodic modulation.**

I. Introduction

SWITCH-MODE power supplies, beside offering several performance and efficiency benefits, suffer from electromagnetic interference (EMI) issues because of fast switching currents and voltages in them [1]–[3]. These may cause interference with nearby devices and also the input power lines [4]. Thus, EMI reduction is an important concern in all modern electronic equipments, as evidenced by the presence of many regulations [5], [6]. These link electromagnetic compatibility with the ability to meet the interfering power spectrum under a threshold level. The use of passive EMI filters and shielding are standard practices for EMI reduction [7]; however, bulky passive power circuit components increase size, cost, and losses. Also they eventually limit the input current slew rate, which results in poor transient performance.

Beside passive EMI filters, switching frequency modulation techniques enable spectral spreading for further EMI reduction [8]. Majority of spectral spreading techniques employ randomized switching frequency modulation [9]–[11] or chaos-based pulsewidth-modulation (PWM) [12]–[16] schemes in a switching dc–dc converter. However, it is difficult to analytically predict ripple parameters so as for efficiency. The programmable pulsewidth modulator was proposed in [17], which uses (offline) optimized timing parameters. Variable switching frequency operation was proposed in [18]. Periodic frequency modulation techniques can achieve spectral spreading and harmonic reduction [19]–[22] with predictable ripple parameters. Spectral spreading using a sinusoidal modulation profile was applied to switching power converters by F. Lin and D. Y. Chen [19]. Frequency modulation using a triangular periodic carrier wave can result in custom spectral spreading [20]–[22]. A periodic bifrequency modulation scheme was introduced in [23], in which time periods are generated using variable frequency approaches, such constant on-time and constant-off time control. This requires separate hardware resources in digital implementation and a variable frequency operation makes it difficult to predict discrete frequencies as the operating point changes. Moreover, impacts on closed-loop stability and dynamic performance have not been reported.

This paper proposes a bifrequency digital PWM (BF-DPWM) technique in a dc–dc converter. This uses two discrete frequencies f_1 and f_2 under a periodic modulation and achieves considerable harmonic reduction [24]. This also improves the voltage resolution with an insignificant ripple impact, compared to a dither-based periodic modulation scheme [25]. Discrete-time models are used for stability analysis and design guidelines are presented. A buck converter prototype was made, and different control schemes are implemented using a field-programmable gate array (FPGA) device. This method is extended to the triangular-wave modulation scheme for further harmonic reduction.

This paper is organized as follows. Section II presents the proposed periodic BF-DPWM technique. Power spectral density is analyzed in Section III. Section IV presents design and simulation study of the proposed scheme. Section V demonstrates performance improvement using test results using a synchronous buck converter. Section VI presents the concluding remarks.

II. Proposed Periodic BF-DPWM

A. Voltage-mode Periodic BF-DPWM

Fig. 1 shows the schematic diagram of a dc–dc buck converter governed by the voltage-mode BF-DPWM. Primarily this consists of 1) a "periodic modulator" block and 2) a "BF-DPWM" block. The former consists of a free-running counter, which gets

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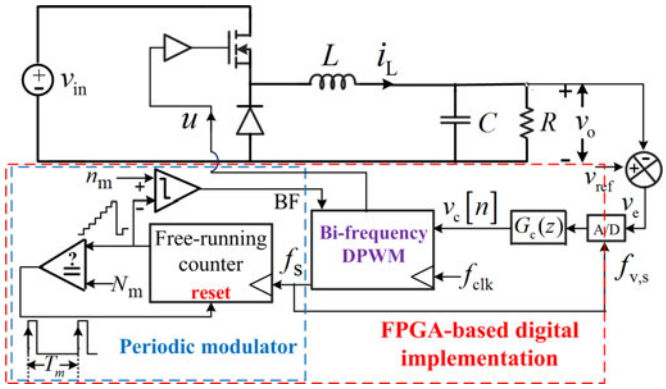

Fig. 1. Schematic diagram of a synchronous buck converter governed by the proposed voltage-mode BF-DPWM scheme.

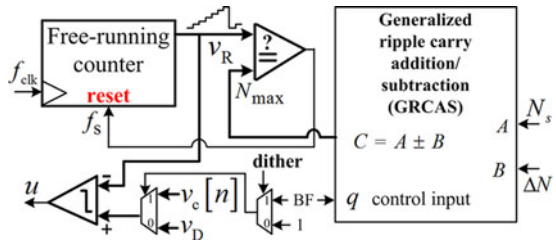

Fig. 2. Internal architecture of the proposed BF-DPWM (in Fig. 1): $t_{\rm clk}$ indicates the controller clock; N_s indicates the counting limit to generate the nominal time period $T = (N_s + 1)\, t_{\rm clk}$; ΔN represents a variable parameter to generate a bifrequency operation.

incremented at the rising edge of the switching clock $f_{\rm s}$. The counter is reset if the counting value reaches the upper limit $N_{\rm m}$. The "BF" control signal is set to "logic 1" as long as the counting value is smaller than $n_{\rm m}$. Thus, for a given set of the parameters $n_{\rm m}$ and $N_{\rm m}$ (where $n_{\rm m} < N_{\rm m}$), the "BF" signal generates a periodic pulse that decides the occurrence of the periodic bifrequency operation. Fig. 2 shows the internal architecture of the "BF-DPWM," which uses a generalized ripple-carry adder/subtractor (GRCAS) with the "BF" signal as the control input "q." If "$q = 0$," the GRCAS adds two data inputs and generates the output $N_{\rm max} = N_s + \Delta N$; otherwise, the output becomes $N_{\rm max} = N_s - \Delta N$. The counter set-value N_s is related to the nominal switching period as $T = (N_s + 1)\, t_{\rm clk}$. If the "dither" control signal is set to "logic 0," the upper-limit $N_{\rm max}$ of the free-running counter in Fig. 2 periodically varies between $N_s \pm \Delta N$ depending on the status of the "BF" signal. For a nonzero ΔN (where $\Delta N < N_s$), this generates two discrete time periods with $T_1 = (N_s - \Delta N + 1)\, t_{\rm clk}$ and $T_2 = (N_s + \Delta N + 1)\, t_{\rm clk}$, which appear periodically with synchronism of the modulating "BF" signal. The time period of modulating period can be written as $T_m = [n_m T_1 + (N_m - n_m)\, T_2]$. Fig. 2 shows that the duty ratio under the BF-DPWM scheme is generated using the closed-loop digital voltage controller. Thus, it is reasonable to assume that the effective steady-state duty ratio D_k (where $k \in \{1, 2\}$) for an active time period T_k under a bifrequency operation remains the same as that using the fixed-frequency voltage-mode DPWM, i.e., $D_k = D$. With $n_m = N$ and $N_m = 2N$, the periodic bifrequency operation is shown in Fig. 3 with respective on-times $t_1 = DT_1$ and $t_2 = DT_2$.

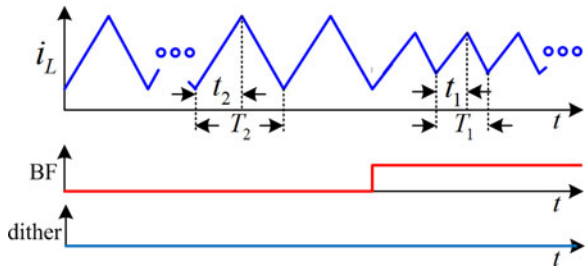

Fig. 3. Control waveforms under a BF-DPWM scheme.

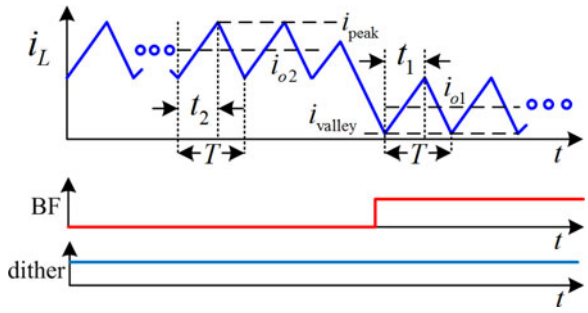

Fig. 4. Control waveforms under a dither-based DPWM scheme.

B. Dither-Based Periodic Modulation

By setting the "dither" command to "logic 1" and considering $\Delta N = 0$ in Fig. 2, the proposed BF-DPWM block can be reconfigured to a periodic dither-based modulation. This considers a fixed time period T throughout, however, uses two discrete duty ratios depending on the status of the "BF" signal. For "BF = logic 0," the gate pulse u is generated by an open-loop configuration using a set value $v_{\rm D}$; otherwise, the closed-loop voltage controller generates u. Using a periodic modulation with $n_m = N$ and $N_m = 2N$, it is reasonable to consider $D - \Delta D$ and $D + \Delta D$ as the respective steady-state duty ratios under open-loop and closed-loop configurations. Thus from Fig. 4, $t_{1,2} = (D \mp \Delta D)\, T$ and $T_{1,2} = T$. Also ΔD can be customized by suitably adjusting v_D.

C. Voltage-mode Bifrequency Periodic Triangular Modulation

1) Classical Triangular Modulation: With a little modification of the proposed scheme in Fig. 2, an approximate periodic triangular modulation (PTM) technique (in [22]) can be realized. In a conventional voltage-mode PTM scheme, the upper value of the periodic sawtooth waveform is periodically modulated. This indicates that the switching period (T) linearly increases with time over a finite number of cycles; thereafter, T linearly decreases over the same number of cycles. Such linear changes in T can be easily implemented using a digital platform [20]. This paper considers a much simplified, rather an approximate approach. By setting "dither = logic 0" and $\Delta N = 0$ in Fig. 2, the counter upper-limit $N_{\rm max}$ is incremented (at the rising edge of the running switching clock $f_{\rm s}$) over Δn number of successive cycles, starting with the set value $N_{\rm s}$. Thereafter, $N_{\rm max}$ is decremented over the same number of cycles. This can be easily implemented using an increment/decrement counter as shown in

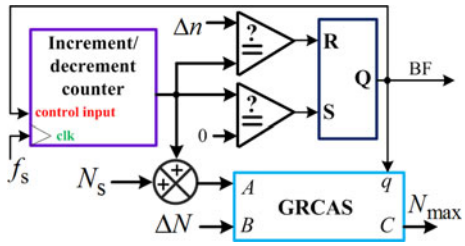

Fig. 5. Internal architecture of the proposed BF-DPWM (in Fig. 1) with triangular modulation: Δn generates periodic triangular modulation.

Fig. 5, in which the "control input" command decides whether to increment or to decrement. If "control input = logic 1," the counter starts incrementing at the rising edge of the switching signal f_s. The time period of f_s periodically varies with $N_{\max}$. After the counter reaches Δn, the "control input" is set to logic 0, and the counter starts decrementing. For $\Delta n \ll N_s$, this represents a triangular modulation scheme with an approximate rate $1/(N_s t_{\rm clk})$ Hz/V. For a reasonably large value of Δn, this would represent a periodic exponential modulation scheme.

2) Bifrequency Triangular Modulation: In this bifrequency periodic triangular modulation, two discrete rates of change of frequency are considered as shown in Fig. 5. While the "BF" command is set to logic 1, the counter starts incrementing at the rising edge of f_s so as for $N_{\max}$ with a base value $N_s - \Delta N$ as generated by the GRCAS. However, for "BF = logic 0," $N_{\max}$ is decremented with a base value $N_s + \Delta N$. Thus, this results in two discrete rates of change of frequency as $1/[(N_s \mp \Delta N)t_{\rm clk}]$ Hz/V. This represents a periodic bifrequency triangular modulation, and later, it will be shown using test results that this can further reduce power level of the harmonic contents, compared to a conventional PTM.

III. Power Spectral Density: A Comparative Study

The power spectral density (PSD) of the signal under test provides levels of power spectrum of a periodic signal at its different harmonic contents. For example, the PSD of the input current reflects the measure of the conducted EMI, while the PSD of the output voltage provides the measure of the radiated EMI. However, it is cumbersome to analytically formulate the PSD of either of the aforementioned signals, which need to be evaluated using numerical methods. To provide analytical insights of the PSD under different periodic modulation schemes, Fourier series is rather applied on the control signal u in this paper.

A. PSD Under Conventional DPWM

Consider a buck converter in Fig. 1 under the conventional voltage-mode DPWM, i.e., $\Delta N = 0$ and "dither = logic 0" in Fig. 2. With a stable steady-state operation, the effective modulating frequency is same as the converter switching frequency, irrespective of the values of n_m and N_m. Thus, Fourier coefficients can be obtained for the control signal u over the periodic interval T as follows:

$$u(t) = \sum_{k=-\infty}^{\infty} c_k e^{j2\pi k f_s t},\ c_k = \frac{1}{T}\left[\int_0^{DT} 1 \times e^{-j2\pi k f_s t} dt\right] \tag{1}$$

where $f_s = 1/T$ and D indicates the steady-state duty ratio. Thus, the PSD of u under the fixed-frequency DPWM becomes

$$\begin{aligned} |c_k|^2 &= c_k * c_{-k} = \left(\frac{1}{2\pi k}\right)^2 \left(e^{-j2\pi kD} - 1\right)\left(e^{j2\pi kD} - 1\right) \\ &= D^2 \mathrm{sinc}^2(\pi k D). \end{aligned} \tag{2}$$

B. PSD Under Periodic Modulation

Consider a periodic modulation scheme with $n_m = N$ and $N_m = 2N$ (in Fig. 2). For the BF-DPWM shown in Fig. 3, two discrete time periods $T_1 = T - \Delta T$ and $T_2 = T + \Delta T$ (where T is the nominal time period) with their respective on-time durations as t_1 and t_2. The modulating time period is

$$T_m = N(T_1 + T_2) = 2NT = 1/f_m. \tag{3}$$

Thus, the Fourier series representation of u becomes

$$u(t) = \sum_{k=-\infty}^{\infty} c_k e^{j2\pi k f_m t} \quad \text{with} \quad 1/f_m = 2NT. \tag{4}$$

The Fourier series coefficient can be derived over T_m as

$$c_k = \frac{1}{T_m}\left(I_1 + e^{-j2\pi k f_m N T_1} \times I_2\right) \tag{5}$$

$$\text{where} \quad I_r = \underbrace{\sum_{i=0}^{N-1} \left(e^{-j2\pi k f_m T_r}\right)^i}_{I_{r1}} \times \underbrace{\int_0^{t_r} e^{-j2\pi k f_m t} dt}_{I_{r2}} \tag{6}$$

where $r \in \{1, 2\}$; I_{r1} and I_{r2} can be derived as

$$\begin{aligned} I_{r2} &= \frac{jT_m}{2\pi k} \times \left(e^{-j2\pi k f_m t_r} - 1\right) \\ I_{r1} &= \frac{1 - e^{-j2\pi k f_m N T_r}}{1 - e^{-j2\pi k f_m T_r}} = e^{-j\pi k f_m (N-1) T_r} \times f_r(k) \\ f_r(k) &= \frac{\sin(\pi k f_m N T_r)}{\sin(\pi k f_m T_r)}. \end{aligned} \tag{7}$$

For a periodic signal, $|c_k|^2$ (with $c_k^* = c_{-k}$) represents the PSD of u, which can be derived using (3)–(7), as

$$|c_k|^2 = \left(\frac{1}{2\pi k}\right)^2 \left[|a|^2 f_1^2 + |b|^2 f_2^2 + (ab^* + a^* b) f_1 f_2\right] \tag{8}$$

where the expressions of $f_1(k)$ and $f_2(k)$ are given in (7), and

$$\begin{aligned} a &= \left(e^{-j2\pi k f_m t_1} - 1\right) \times e^{-j\pi k f_m (N-1) T_1} \\ b &= \left(e^{-j2\pi k f_m t_2} - 1\right) \times e^{-j\pi k f_m [2NT_1 + (N-1)T_2]}. \end{aligned} \tag{9}$$

The aforementioned equations can be further simplified as follows:

$$|c_k|^2 = \left(\frac{1}{\pi k}\right)^2 \left[x_1^2 + x_2^2 + 2x_1x_2\cos\theta\right]$$
$$x_r = \sin(\pi k f_m t_r) \times f_r(k)$$
$$\theta = \frac{\pi k}{2NT}\left[2NT + (T_1 - T_2) - (t_1 - t_2)\right]. \quad (10)$$

Referring to Figs. 3 and 4, it is reasonable to assume that $2NT \gg (T_1 - T_2) - (t_1 - t_2)$; thus, $\cos\theta \approx \cos(\pi k) = (-1)^k$. With this assumption, (10) can be simplified as

$$|c_k|^2 = \left(\frac{1}{\pi k}\right)^2 \left[x_1 + (-1)^k x_2\right]^2. \quad (11)$$

This shows that the PSD of the control input does not contain any frequency related to time periods T_1 or T_2; however, harmonic contents are functions of their relative difference.

1) PSD Under Dither-Based Modulation: From Fig. 4, timing parameters for a dither-based periodic modulation scheme under the voltage-mode DPWM controller become

$$T_1 = T_2 = T, \;\; t_1 = (D - \Delta D)T, \;\; t_2 = (D + \Delta D)T \quad (12)$$

where D indicates the steady-state duty ratio using the fixed-frequency voltage-mode DPWM controller. A difference in duty ratio, ΔD can be achieved through a suitable choice of $v_{\rm D}$ (in Fig. 2) as discussed in Section II-A. Using (10)–(12), the PSD of u under the periodic dither-based modulation can be derived for odd integer values of k, as follows:

$$\left|c_{(2k+1)}\right|^2 = \left[\frac{2\sin\left[\frac{\pi(2k+1)\Delta D}{2N}\right] \times \cos\left[\frac{\pi(2k+1)D}{2N}\right]}{\pi(2k+1) \times \sin\left[\frac{\pi(2k+1)}{2N}\right]}\right]^2. \quad (13)$$

Similarly, the PSD of u can be derived for even k as follows:

$$|c_{2k}|^2 = \left[\frac{\sin(\pi kD/N) \times \cos(\pi k\Delta D/N) \times \sin(\pi k)}{\pi k \times \sin(\pi k/N)}\right]^2. \quad (14)$$

Since $\sin(\pi k) = 0$, the aforementioned equation shows that $|c_{2k}|^2 = 0$ for even values of k. However, for k being an integral multiple of $2N$, the PSD of u, $|c_{2Nk}|^2$ in (14) can be shown to be

$$|c_{2Nk}|^2 = D^2 \times \cos^2(\pi k\Delta D) \times \mathrm{sinc}^2(\pi kD). \quad (15)$$

Since $T_m = 2N \times T$, the PSD, $|c_{2Nk}|^2$, of the gate signal u using a dither-based modulation would accordingly modify the PSD, $|c_k|^2$, using the fixed-frequency DPWM in (2).

2) PSD Under Bifrequency Modulation: From Fig. 3, timing parameters for a periodic bifrequency modulation scheme under the voltage-mode DPWM controller become

$$t_1 = DT_1, \; t_2 = DT_2, \; T_1 = T - \Delta T, \; T_2 = T + \Delta T_2 \quad (16)$$

where D indicates the steady-state duty ratio using the fixed-frequency voltage-mode DPWM controller. A difference in time period ΔT can be achieved through a suitable choice of ΔN (in Fig. 2) as discussed in Section II-B. Using (10), (11), and (16), the PSD of u under the periodic bifrequency modulation can be derived for both odd and even integer values of k. The PSD expressions are cumbersome, hence, they are not presented in this paper. However, the PSD expression of u can be simplified, for k being an integral multiple of $2N$, as

$$|c_{2Nk}|^2 = \left[\frac{\sin(\pi kNx) \times \sin(\pi kD) \times \cos(\pi kDx)}{\pi kN \times \sin(\pi kx)}\right]^2 \quad (17)$$

where $x = \Delta T/T = \Delta N/N_s$. The frequency resolution Δf under the BF-DWPM becomes $\Delta f = f/2N$. This means that a considerably large N improves frequency resolution, thus improving the spectral distribution. Under this consideration, it is reasonable to approximate Nx in (17) as

$$Nx \approx m \pm x \;\Rightarrow\; |\sin(\pi kNx)| \approx |\sin(\pi kx)| \;\text{ for } m \in I^+. \quad (18)$$

Using (18), the PSD of u in (17) can be approximated as

$$|c_{2Nk}|^2 \approx D^2 \times \cos^2(\pi kD\Delta T/T) \times \mathrm{sinc}^2(\pi kD). \quad (19)$$

It is not necessary for N to be very large in order to arrive an approximation as given in (18). In fact, (19) is perfectly valid for $N = 1$, and the analytical PSD expression in (11) can be graphically plotted for arbitrary integer values of N and k .

C. Custom Harmonic Reduction

It is important to investigate the impact of both the periodic modulation schemes on the harmonic contents of the unmodulated DPWM scheme. Since $T_m = 2NT$, it is reasonable to compute the PSD $|c_{2Nk}|^2$ for both the periodic modulation schemes in order to quantify the relative spectral attenuation (or harmonic reduction) over the unmodulated DPWM. Using (2), (15), and (19), the relative PSD can be written as

$$\frac{|c_{2Nk}|^2_{\rm PSD-dither}}{|c_k|^2_{\rm PSD-DPWM}} = \cos^2(\pi k\Delta D) \quad (20)$$

$$\frac{|c_{2Nk}|^2_{\rm PSD-BF-DPWM}}{|c_k|^2_{\rm PSD-DPWM}} = \cos^2[(\pi kD) \times (\Delta T/T)] \quad (21)$$

$$\frac{|c_{2Nk}|^2_{\rm PSD-BF-DPWM}}{|c_k|^2_{\rm PSD-dither}} = \frac{\cos^2[(\pi kD) \times (\Delta T/T)]}{\cos^2[(\pi kD) \times (\Delta D/D)]}. \quad (22)$$

From (20)–(22), it is clear that the dc (at $k = 0$) PSD component of the gate signal u under the unmodulated DPWM scheme remains unaffected by either of the periodic modulation schemes. This indicates that the steady-state duty-ratio D or more generally the operating point using the fixed-frequency DPWM is preserved in the average sense. Further, (20) and (21) show that the PSD under the unmodulated DPWM scheme will be attenuated at fundamental and harmonic components using both the periodic modulation schemes, and the fold of attenuation increases with k. Although $|c_{2Nk}|^2$ in (22) appears to be the same for both the periodic modulation schemes with $\Delta D/D = \Delta T/T$, the BF-DPWM is expected to further reduce the harmonic contents using (17). Moreover, impacts on steady-state ripple parameters need to be analyzed.

The PSD expressions in (20)–(22) provide analytical justifications of harmonic reduction using different periodic modulation schemes. However, this study uses Fourier series coefficient that

can be analytically derived for a continuous-time periodic signal. For numerical as well as experimental study of the power spectrum, the Fourier transform is rather applied because the periodic signal often needs to sampled at a uniform rate, which is much higher than the Nyquist rate [26]. Fourier transform can be derived using Fourier coefficient as follows:

$$X(\omega) = \sum_{k=-\infty}^{\infty} (2\pi c_k)\, \delta(\omega - k\omega_0); \quad \omega_0 = 2\pi f_{\rm m}. \tag{23}$$

Then, the Discrete Fourier transform can be obtained and the fast Fourier transform (FFT) algorithm can be used to quantify the power spectrum for numerical and experiment studies.

IV. Analysis and Design of the Proposed Scheme

A. Steady-State Ripple Characterization

The expressions of the steady-state inductor current and voltage ripple parameters under the fixed-frequency DPWM can be derived following [27] with $T_{1,2} = T$ and $t_{1,2} = DT$. The steady-state current ripple Δi_L can be written as

$$\Delta i_L = \frac{(v_{\rm in} - v_o)\, DT}{L} = \frac{v_{\rm in}\,(1-D)\, DT}{L}. \tag{24}$$

1) Current Ripple Under a Dither-Based Modulation: With $T_{1,2} = T$, Fig. 4 shows two steady-state duty ratios $D - \Delta D$ and $D + \Delta D$ (for the nominal duty-ratio D) using the dither-based DPWM. Thus, two steady-state output voltages v_{o1} and v_{o2} (with the respective load currents i_{o1} and i_{o2} for the load resistance R) will appear periodically, which are written as

$$\begin{aligned} v_{o1} &= (D - \Delta D)\, v_{\rm in}, \quad i_{o1} = v_{o1}/R \\ v_{o2} &= (D + \Delta D)\, v_{\rm in}, \quad i_{o2} = v_{o2}/R. \end{aligned} \tag{25}$$

Using (24) and (25), two steady-state ripple currents become

$$\begin{aligned} \Delta i_{L1} &= \frac{(D - \Delta D)\,(1 - D + \Delta D)\, T v_{\rm in}}{L} \\ \Delta i_{L2} &= \frac{(D + \Delta D)\,(1 - D - \Delta D)\, T v_{\rm in}}{L}. \end{aligned} \tag{26}$$

Using (25) and (26), the peak current ($i_{\rm peak} = i_{o2} + \Delta i_{L2}/2$) and the valley current ($i_{\rm valley} = i_{o1} - \Delta i_{L1}/2$) in Fig. 4 are

$$\begin{aligned} i_{\rm peak} &= (D + \Delta D) \times \left[\frac{v_{\rm in}}{R} + \frac{T v_{\rm in}\,(1 - D - \Delta D)}{2L}\right] \\ i_{\rm valley} &= (D - \Delta D) \times \left[\frac{v_{\rm in}}{R} - \frac{T v_{\rm in}\,(1 - D + \Delta D)}{2L}\right]. \end{aligned} \tag{27}$$

Thus, the peak-to-peak inductor current ripple becomes

$$\Delta i_{L,d} = i_{\rm peak} - i_{\rm valley} = \Delta i_L + \left(\frac{2}{R} - \frac{T\Delta D}{L}\right)\frac{\Delta D}{D} v_{\rm ref} \tag{28}$$

where Δi_L indicates the nominal current ripple in (24) using the DPWM technique. The aforementioned expression shows that the inductor ripple is considerably affected by a dither-based periodic modulation scheme, particularly at higher load current conditions (for smaller R). Similarly, the output voltage ripple can be analytically derived. Various dither-based scheme are discussed in [30] to minimize ripple parameters, and the proposed theoretical framework can be extended to investigate their impacts on spectral characteristics.

2) Current Ripple Under the Proposed Bifrequency DPWM: From Fig. 3, the steady-state duty ratio using the BF-DPWM remains the same as that of the fixed-frequency DPWM. Moreover, the peak-to-peak current is simply the largest current ripple related to the time period $T + \Delta T$, which is written as

$$\Delta i_{L,\text{BF-DPWM}} = \Delta i_L \times \left(1 + \frac{\Delta T}{T}\right). \tag{29}$$

The aforementioned expression shows that the current ripple linearly increases with the percentage change in time period $\Delta T/T$. Moreover, it is independent of load current. This implies that even though the percentage change equally affects the harmonic reduction in (22), the ripple parameters are significantly affected by the dither-based modulation in (28), compared to that in (29) using the proposed BF-DPWM.

B. Duty-Ratio Resolution Under BF-DPWM

The duty-ratio resolution in a conventional voltage-mode DPWM is limited to $\Delta d = 1/(N_s + 1)$. For a periodic dither-based modulation with $T_m = 2NT$, Δd can be improved by

$$\Delta d_{\rm dither} = \frac{1}{2N} \times \frac{1}{(N_s + 1)} = \frac{1}{2N} \times \Delta d. \tag{30}$$

For the same T_m, the duty-ratio resolution $\Delta d_{\rm BF}$ using the proposed periodic BF-DPWM can be improved as

$$\Delta d_{\rm BF} = \frac{1}{2N}\frac{1}{(N_s + \Delta N + 1)} = \left(1 + \frac{\Delta T}{T}\right)^{-1} \times \Delta d_{\rm dither}. \tag{31}$$

Thus, the proposed BF-DPWM can further improve the duty-ratio resolution using the dither-based modulation scheme with an insignificant impact on ripple parameter, as given in (29).

C. Design of the Discrete-Time Compensator

The compensator design under voltage mode control is well studied [27]. This uses state-space averaging followed by linearization around an operating point to derive various transfer functions. An equivalent hold concept can be used to accurately derive such transfer functions for a DPWM dc–dc converter [28]. Thereafter, a discrete-time voltage controller $G_{\rm c}(z)$ in Fig. 1 can be directly designed in the digital domain [29]. A similar compensator design method can be directly applied for the proposed BF-DPWM, as the closed-loop remains active throughout. A discrete-time proportional-integral (PI) controller is considered in this paper, as follows:

$$v_{\rm c}[n] = k_{\rm p} v_{\rm e}[n] + u_{\rm I}[n] \tag{32}$$

where $u_{\rm I}[n] = u_{\rm I}[n-1] + k_{\rm i} v_{\rm e}[n]$, $v_{\rm e}[n] = (v_{\rm ref} - v_{\rm n})$; $k_{\rm p}$ and $k_{\rm i}$ indicate proportional and integral gains in discrete domain. However, $G_c(z)$ may be a lag/lead or a type-3 compensator, and the design steps in [29] would be equally applicable.

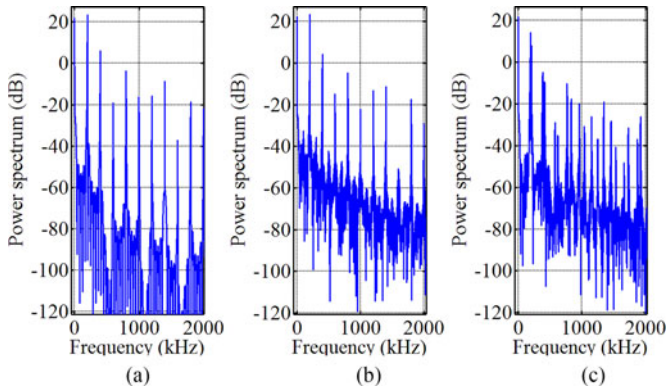

Fig. 6. Power spectrum computed based on simulation results using the FFT algorithm for $N = 35$ at $v_{\rm in} = 9$ V and $R = 1.7\,\Omega$ (a) DPWM (b) Dither (c) Bi-frequency DPWM.

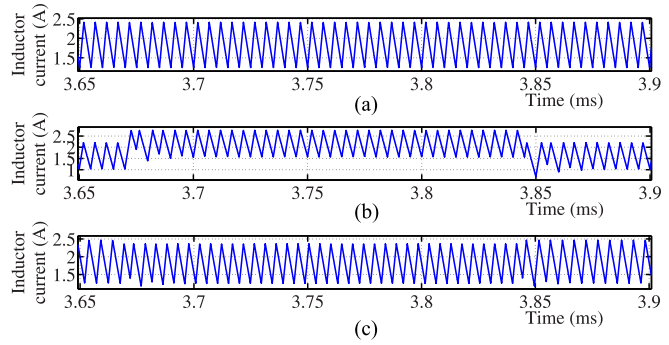

Fig. 7. Inductor current ripple using the (a) fixed-frequency DPWM, (b) dither-based DPWM, and (c) BF-DPWM for $N = 35$ at $v_{\rm in} = 9$ V and $R = 1.7\,\Omega$.

D. Simulation Results and Discussion

The nominal parameter set considered for simulation study is as follows: $T = 5\ \mu$s, $L = 9\ \mu$H, $C = 470\ \mu$F, $R \in [0.3\ \Omega, 5\ \Omega]$, $v_{\rm in} = 9$ V, and $v_{\rm ref} = 3.3$ V. The PI controller parameters in (32) are taken to be $k_p = 50$ and $k_i = 0.9$ and the frequency of the controller clock $f_{\rm clk} = 100$ MHz.

Using the aforementioned parameter set, Fig. 6 shows the power spectrum of the switched node voltage, which was obtained numerically using the FFT algorithm. This shows that for a nominal switching frequency of 200 kHz, the higher harmonic contents can be reduced using both the dither-based technique and the proposed BF-DPWM compared to that using the fixed-frequency DPWM technique.

Fig. 7 shows that the (peak-to-peak) inductor current ripples are (a) 1.1612 A using the fixed-frequency DPWM, (b) 1.55 A using the dither-based DPWM for $\Delta D/D = 10\%$, and (c) 1.277 A using the BF-DPWM for $\Delta T/T = 10\%$, whereas the calculated ripple parameters using (24), (28), and (29) are found to be 1.1616, 1.562, and 1.28 A, respectively. This shows that while a dither-based DPWM technique attenuates the spectral speaks similar to the proposed BF-DPWM scheme, it considerably increases the ripple parameters. The current ripple is expected to increase further at higher load current conditions or for a smaller value of the load resistance R.

V. Hardware Implementation

A buck converter prototype is made and different digital controllers are implemented using an FPGA device. The same parameter set in Section IV-D is considered for experimental investigation. For the prototype signal conditioning circuits, an 8-bit pipeline ADC (AD9280) is considered to sample the output voltage with the same rate of the switching clock f_s.

A. Measured Power Spectrum Using FFT and Steady-State Current Ripple: A Comparative Study

Fig. 8 shows a comparative study of the measured power spectrum of the switch node voltage of a buck converter using the FFT algorithm. The measured power spectrum (FFT) using different modulation techniques are more or less consistent with the simulated power spectrum as shown in Fig. 6. However, there are some mismatches, particularly for second and also for a few higher harmonic contents. This can be attributed to the practical parasitics, such as dc resistance of the inductor, ESR of the capacitor, finite slew rates of the MOSFETs as well as the drivers. These would cause a deviation in the steady-state duty ratio and also inject a few extra frequency components, which have not been included in the simulation as well as in the analytical studies.

Fig. 9 shows the measured inductor current ripples of (a) 1.59 A using the dither-based modulation scheme (with $\Delta D/D = 10\%$) and (b) 1.29 A using the BF-DPWM (with $\Delta T/T = 10\%$). The ripple parameters are consistent with the simulation results in Fig. 7 as well as with the analytical derivations in (28) and (29). This also shows that the current ripple considerably increases using the dither-based modulation compared to the proposed scheme for a similar percentage increase for the respective modulating parameters.

B. Harmonic Reduction Using Triangular Modulation Schemes

Figs. 10 and 11 show the measured power spectrum (using a Tektronix made mixed-domain-oscilloscope MDO4054-3) using different triangular modulation schemes. For each figure, the bottom half displays the power spectrum of the switch node voltage (related to the spectrum analyzer channel) and the top half displays time domain waveforms with following axis properties: From the top, Ch 1 (1 A/div), Ch 2 (50 mV/div), and Ch 3 (5 V/div) indicate the inductor current, the ac coupled output voltage, and the gate signal, respectively.

Fig. 10 shows that the spectral peaks can be band limited and flat using a periodic triangular modulation scheme in [20], [22]. With $\Delta N/N_s$=5%, the proposed periodic bifrequency modulation can further reduce the harmonic contents of the fixed-frequency DPWM as shown in Fig. 11. The ripple parameters using the proposed scheme are also comparable with the conventional triangular modulation scheme.

C. Load Transient Performance

For a slower controller bandwidth of $1/20^{\rm th}$ of the switching frequency f_s, Fig. 12 shows the load transient performance using

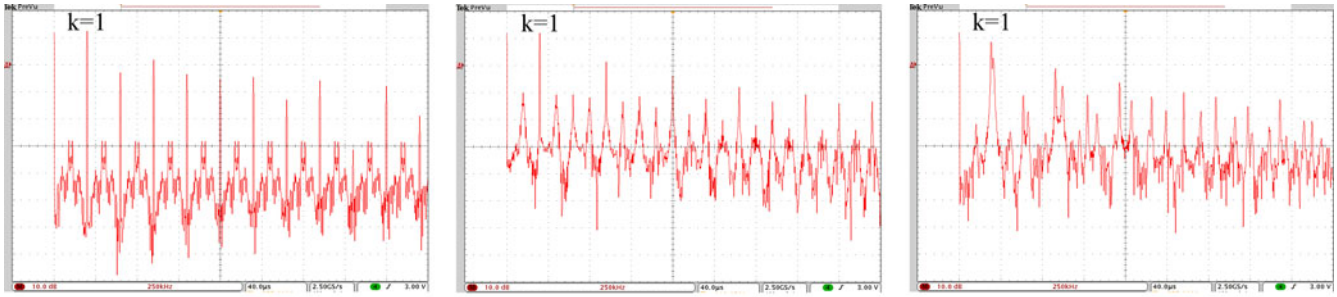

Fig. 8. Measured power spectrum in a synchronous buck converter using different modulation schemes with $N = 35$ at $v_{\rm in} = 9$ V and $R = 1.7\,\Omega$: For each figure, x-axis indicates the power spectrum (FFT) of the switch node voltage with 10 dB/div and y-axis indicates the frequency with 250 kHz/div.

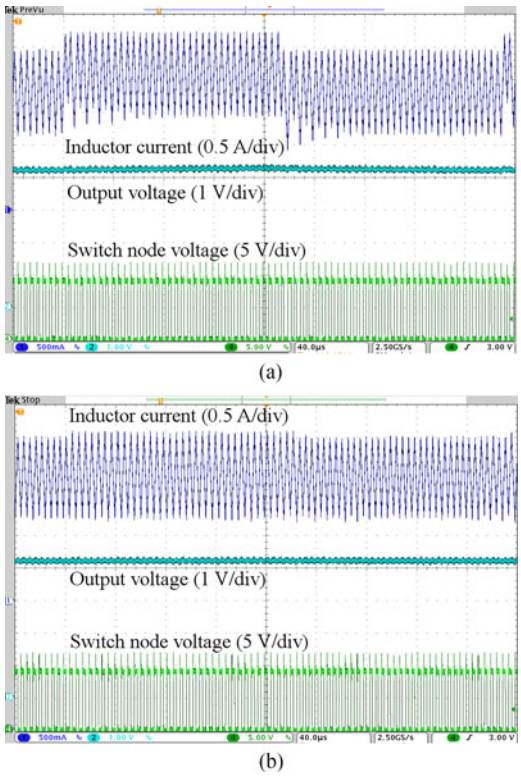

Fig. 9. Measured inductor current ripple in a synchronous buck converter for $N = 35$ at $v_{\rm in} = 9$ V and $R = 1.7\,\Omega$ (a) Dither-based modulation (b) Bi-frequency pulse width modulation.

different modulation schemes in a synchronous buck converter. This results in nearly 220-μs settling time (or 44 switching cycles) and 80-mV voltage undershoot using the fixed-frequency DPWM for a step change in load current from 2 to 4.7 A at 9-V input. Moreover, the transient performance is closely retained using the proposed BF-DPWM for different modulation parameters as indicated in the respective captions.

Using the load current feed forward and different PI controller gains, Fig. 13 confirms a fast load transient recovery using the fixed-frequency DPWM. This results in nearly 10-μs settling time (or 2 switching cycles) and 40-mV voltage undershoot for a step change in load current from 0.7 to 3.2 A. Also the proposed BF-DPWM closely retains the transient performance, even using different modulation parameters.

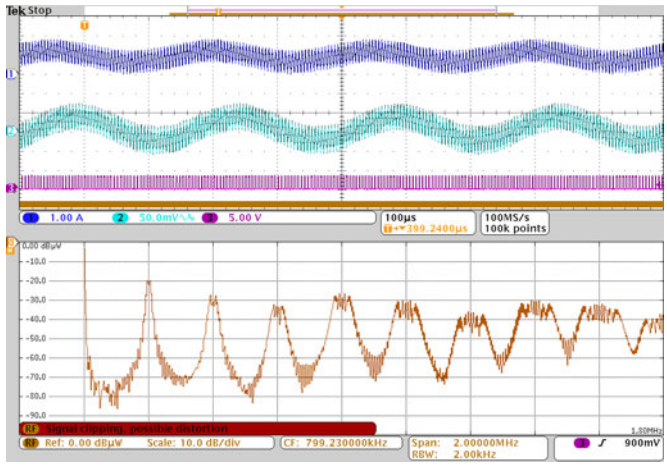

Fig. 10. Power spectrum of the switched node voltage of a synchronous buck converter at $v_{\rm in} = 9$ V and $R = 4.5\,\Omega$ under a triangular-wave modulation with $\Delta n = 50$: Time scale -100 μs/div.

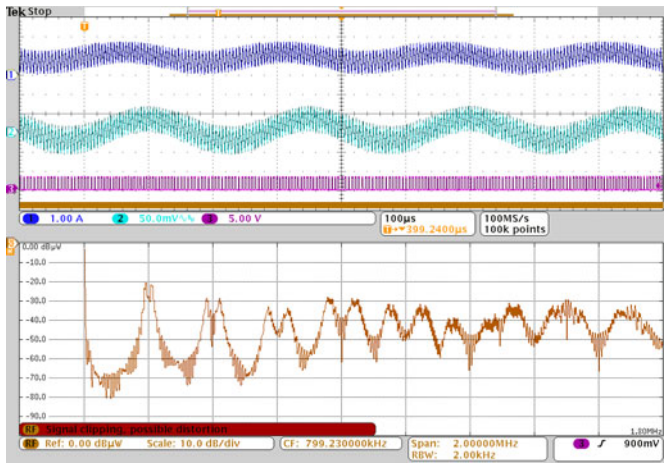

Fig. 11. PSD of the switched node voltage of a synchronous buck converter at $v_{\rm in} = 9$ V and $R = 4.5\,\Omega$ under a triangular-wave modulation with $\Delta n = 50$ and $\Delta N/N_s$ was taken as 5%: Time scale -100 μs/div.

The aforementioned study shows that the proposed modulation scheme has almost no impact on the load transient performance, irrespective of the transient step size as well as the controller bandwidth. The BF-DPWM only attempts to

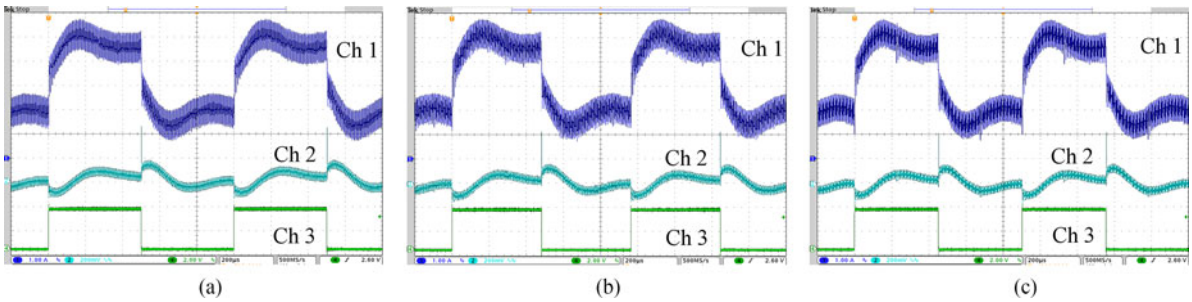

Fig. 12. Transient response of a buck converter for a step change in load current from 2 to 4.7 A, and back with $k_p = 50$ and $k_i = 0.9$: (a) Fixed-frequency DPWM, (b) BF-DPWM with $\Delta T/T = 4\%$ and $N = 10$, and (c) BF-DPWM with $\Delta T/T = 10\%$ and $N = 25$: For each figure, Ch 1, Ch 2, and Ch 3 indicate the inductor current (1 A/div), ac coupled output voltage (0.2 V/div), and step command (2 V/div), respectively, with time scale 0.2 ms/div.

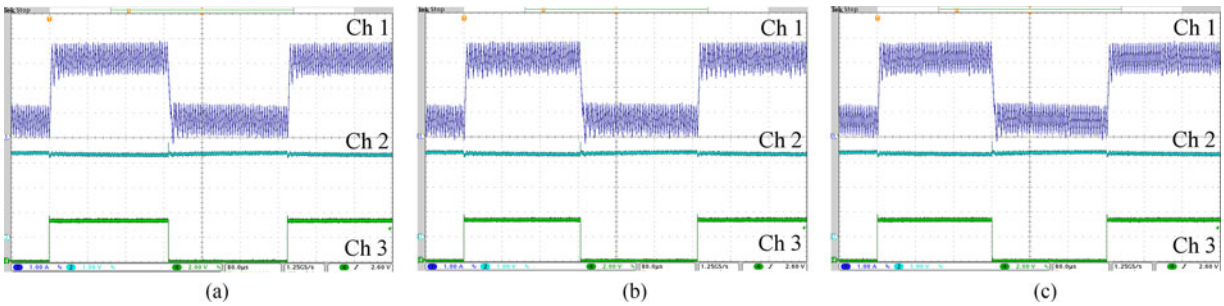

Fig. 13. Load transient response with load current feed-forward in a buck converter for a step change from 0.7 to 3.2 A, and back with $k_p = 60$ and $k_i = 0.3$: (a) Fixed-frequency DPWM, (b) BF-DPWM ($\Delta T/T = 4\%$ and $N = 10$), and (c) BF-DPWM ($\Delta T/T = 10\%$ and $N = 25$): For each figure, Ch 1, Ch 2, and Ch 3 indicate the inductor current (1 A/div), output voltage (1 V/div), and step command (2 V/div), respectively, with time scale 80 μs/div.

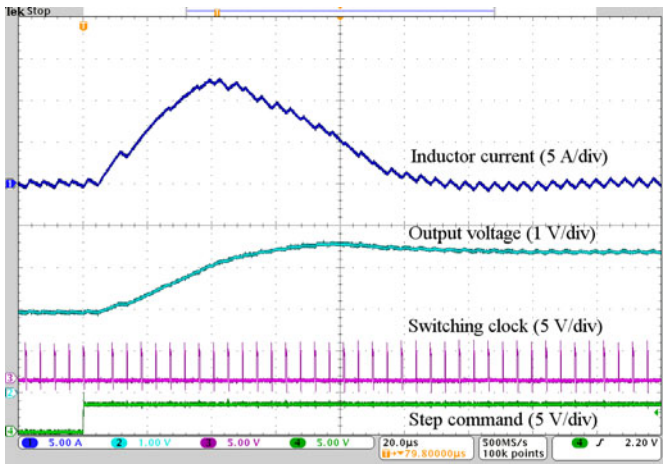

Fig. 14. Reference (step) transient performance in a synchronous buck converter using the conventional DPWM with $T = 5\ \mu$s: Time scale $-20\ \mu$s/div.

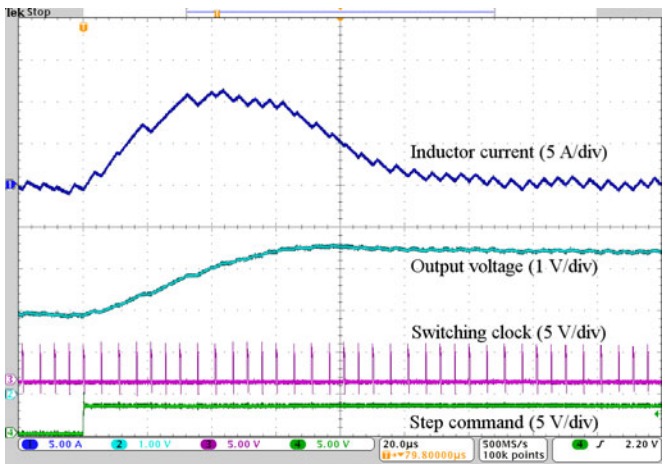

Fig. 15. Reference (step) transient performance in a synchronous buck converter using the proposed BF-DPWM with $N = 3$ and $\Delta N/N_s$=10%: Time scale $-20\ \mu$s/div.

periodically modulate the operating frequency, while the voltage controller remains the same as the fixed-frequency DPWM.

D. Reference Tracking Performance

Fig. 14 shows the transient performance in a synchronous buck converter using the conventional voltage-mode DPWM for a step change in reference voltage from 2 to 3.4 V at $R = 10\,\Omega$. This results in 200-mV voltage overshoot, 12-A inductor overshoot, and 0.1-ms settling time. Fig. 15 shows the transient performance in a synchronous buck converter using the proposed BF-DPWM under the same test conditions as aforementioned with $N = 3$ and $\Delta T/T$=10%. The figures show that the reference tracking performance using the proposed BF-DPWM remains more or less the same as that using the classical fixed-frequency DPWM. Even the use of a higher controller bandwidth would have an insignificant performance impact using the proposed BF-DPWM scheme; however, the peak inductor current is expected to significantly increase.

Thus, the proposed BF-DPWM technique seems to have an insignificant impact on transient performance for a change in load current and/or reference voltage.

VI. Conclusion

In this paper, a periodic BF-DPWM technique was proposed in a dc–dc converter. This would require two discrete frequencies f_1 and f_2 and a modulating signal f_m. The proposed BF-DPWM would achieve considerable harmonic reduction and improved DPWM resolution with an insignificant ripple impact. A buck converter prototype was made, and different control schemes were implemented using an FPGA device. Test results demonstrate that the BF-DPWM has insignificant impacts on transient performance. The proposed scheme was extended to the triangular-wave modulation scheme for further harmonic reduction.

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