Improved Power-Quality-Based Welding Power Supply With Overcurrent Handling Capability

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***Abstract*—This paper proposes a power-factor-corrected canonical switching cell (CSC) converter-based switched-mode power supply for arc-welding applications. In the proposed arc-welding power supply (AWPS), CSC converter operating in discontinuous inductor current mode (DICM) is used to attain inherent power factor correction. The DICM operation substantially reduces the complexity of the control and effectively regulates the dc-link voltage. At the back end, a pulsewidth-modulated (PWM) isolated full bridge dc–dc converter is used to provide a high-frequency isolation, which is mandatory for the arc-welding process. A dual-loop control scheme is utilized to incorporate overcurrent protection and to regulate dc voltage at the output making it suitable for arc-welding applications. Test results are presented to confirm the viability of the proposed AWPS. The performance of the proposed AWPS is evaluated on the basis of total harmonic distortion (THD) of the supply current, power factor, dynamic response, and voltage regulation to prove its effectiveness.**

***Index Terms*—Arc-welding power supply (AWPS), canonical switching cell (CSC) converter, power quality (PQ), total harmonic distortion (THD).**

I. Introduction

ARC-WELDING is considered as one of the most principal ways of welding. However, the weld quality, technical and economic characteristics of arc-welding machine are mainly dependent on its power supply [1], [2]. There are two types of power supplies for arc-welding: arc-welding power supply (AWPSs) with dc output; AWPS with ac output. The first type provides constant polarity current and voltage, leading to high arc stability and a smoother welding output as compared to the second one. Conversely, ac welding power supply yields a combination of negative and positive current, which works satisfactorily mainly for welding aluminum or its alloys only [3].

For decades, conventional dc AWPS employed an uncontrolled diode bridge rectifier (DBR) followed by a bulky dc-link capacitor at the front end and an inverter along with the rectifier for ac–dc conversion at the load end. Fig. 1 presents the measured power quality (PQ) indices for the conventional dc AWPS including parameters like total harmonic distortion (THD) of current, power factor (PF), displacement power factor (DPF) at the input ac mains. As depicted from the obtained results, extremely low PF and large harmonic currents generated by the conventional AWPS are prime issues as they can lead to increased losses in the utility systems.

(a) (b) (c)

Fig. 1. Measured PQ indices of the conventional AWPS (with DBR) at rated load with supply voltage as 220 V. (a) Conventional AWPS input voltage and current; (b) input power and PF; (c) harmonic spectrum of input current.

With the advent of power electronic devices, active power factor correction (PFC) technique has been extensively utilized to comply with stringent regulations of international PQ standards [4]. In an effort to improve the PQ of the switched-mode power supplies (SMPSs), several ac–dc converters are reported in [5]–[7]. Casanueva *et al.* [8] have proposed a boost converter as the front end converter to improve the input PF of an AWPS. Nevertheless, the boost converters suffer from some major drawbacks such as high start-up inrush current and lack of current limiting during overload conditions; these two factors violate primary requirements of an AWPS. While designing a dc power supply for arc-welding applications, the major concern is to develop an SMPS that is able to regulate the output voltage as well as the output current during a welding process to obtain high-quality weld. On the other hand, for welding applications, where the output voltage is much lower than the input supply voltage, a buck-type PFC converter is needed. Klumpner and Corbridge [9] have proposed a two-stage SMPS for arc-welding application having a buck converter at the input stage where the PQ issues have not been addressed. In case of buck converter, the input current is discontinuous in nature, this necessitates the use of large passive filter at the buck converter input [10]–[13]. Consequently, the overall cost and size of the SMPS go up. So, buck converter is not recommended for the front end of an AWPS. Buck–boost converters, like zeta converter, exhibit discontinuous input current resulting in high EMI and other difficulties in implementation [14]–[17]. So, emphasis is on the development of SMPSs having boost–buck converters like Cuk converter and SEPIC to achieve PF correction at the utility interface [18]–[21]. The use of boost–buck converters at the front end ensures a continuous input current. However, Cuk converter and SEPIC employ two inductors and capacitors, making them large and inefficient. Hwu and Yau [22] have explored the buck–boost operation of a KY converter, which has four switches, two

Manuscript received December 10, 2014; revised May 6, 2015; accepted June 26, 2015. Date of publication July 10, 2015; date of current version November 30, 2015. Recommended for publication by Associate Editor T. Shimizu.

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Digital Object Identifier 10.1109/TPEL.2015.2454994

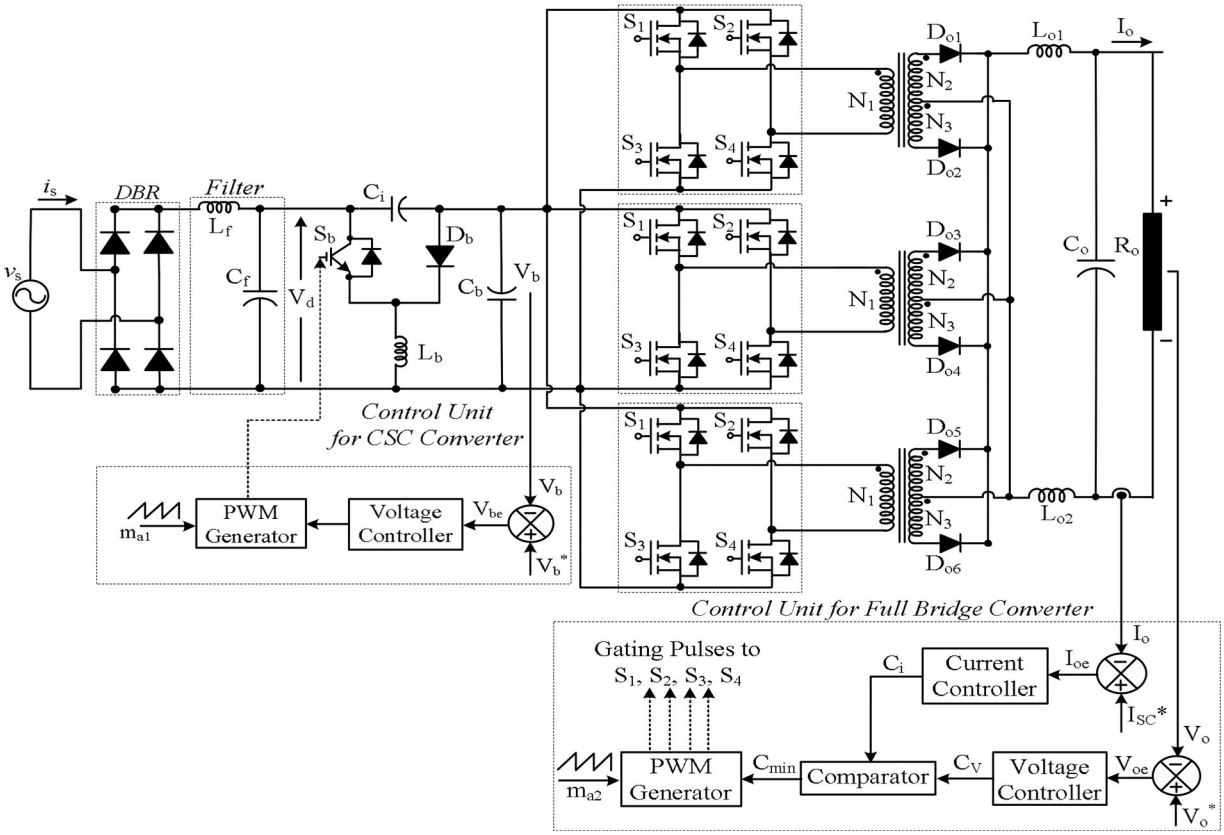

Fig. 2. Configuration of CSC converter and isolated FB converter-based AWPS.

capacitors, an inductor, and a diode. Employing a large number of semiconductor devices makes it an inappropriate solution apart from compromising on reliability.

In this paper, a CSC converter is proposed as a front converter to deal with the PQ issues associated with an AWPS. Moreover, an effort has been put forward to incorporate overcurrent withstand capability in the proposed AWPS, which is very important for achieving high-quality weld. CSC converter allows one to overcome the shortcomings of aforementioned buck–boost converters by having less number of input devices, nonpulsating input current, etc. [23]–[26]. Additionally, the DICM operation results in inherent PFC and fast dc-link voltage regulation using a single-loop voltage feedback controller [27]. Besides, power switch is turned on at zero current and the freewheeling diode is turned off at zero current reducing the switching losses. The CSC converter is followed by full-bridge (FB) converters, which provide high-frequency isolation desired for safe welding operation [28], [29]. The FB converters are used to emulate the conventional welding power supply. Three FB converter modules are connected in parallel to incorporate the power expandability feature depending on the current rating of the power supply. The major contribution of this paper is twofold: 1) input PQ improvement by using CSC converter at the front end, and 2) voltage regulation and overcurrent limiting at the output end by using FB converters. The AWPSs that are currently available in the market are devoid of power factor correction and input PQ improvement. AWPS stands out as a special entity as compared to other power supplies because overcurrent limiting capability is mandatory for welding applications. The proposed AWPS is integrated with the overcurrent limiting capability as increased load current may lead to burn through the welds and more spatter generation. Limiting the current during the welding process also avoids spatter generation and improves weld bead appearance. The theoretical analysis and operation of the proposed AWPS is presented in the following sections. The power supply for welding applications has been designed to attain satisfactory control properties so that weld quality is good. Finally, a prototype of the proposed AWPS is developed to illustrate its efficacy over a wide line/load range. Test results are presented to demonstrate the viability of the proposed AWPS.

II. Proposed CSC Converter-Based AWPS

The system configuration of the proposed PF-corrected AWPS is presented in Fig. 2. In this section, the DBR is followed by CSC converter, which acts as a preregulator to achieve PFC at the utility interface. The DICM operation of the CSC converter minimizes the turn-on switching losses of the power switches and enhances the reverse recovery of the output diodes significantly. The CSC converter converts the rectified input ac mains voltage into an intermediate regulated dc voltage. The controlled output of the CSC converter is fed to the FB converters, which provide the desired dc arc voltage suitable for the welding load. The FB converters are designed to operate in continuous conduction mode (CCM). The proposed topology

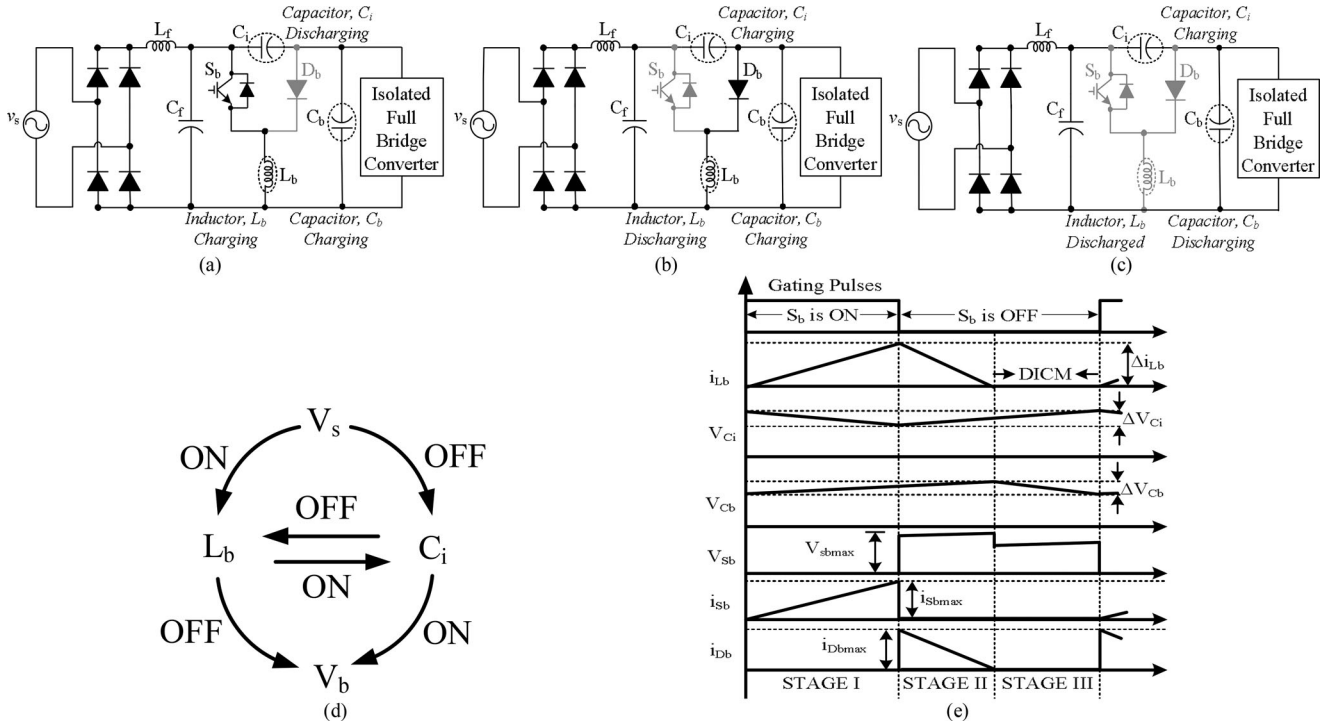

Fig. 3. Operation of CSC converter: (a) Stage I, (b) Stage II, (c) Stage III, (d) energy transfer in one switching period, and (e) waveforms during one switching period.

is designed taking into account the important properties of arc-welding process like constant output dc voltage, output dc arc current regulation during overload, and reduced input current harmonics over wide line/load range. Individual control loops are designed for both the converters (CSC and FB) to optimize their functions. The efficient control of AWPS facilitates fast dynamic response, which enables to achieve high-quality weld.

III. Operation of Proposed CSC Converter-Based AWPS

In this section, the operating principle of both the converters is discussed in detail. The following assumptions are made to simplify the analysis of the proposed AWPS:

1) all semiconductor devices are considered to be ideal;
2) all semiconductor devices are considered to be ideal;
3) the capacitors C_b and C_o are considered to be large enough to maintain the output voltages V_b and V_o as constants without any ripple during one switching period;
4) the supply voltage v_s is considered to be a constant during one switching frequency (f_s) cycle as $f_s >> f$, the line frequency.

A. Operating Modes of CSC Converter

The operating principle of the CSC converter is analogous to the conventional Cuk converter although Cuk converter uses two inductors in place of a single inductor for the CSC converter. The operation of CSC converter is presented in Fig. 3. The rectified output of the DBR is given to the CSC converter. For DICM operation, there are three intermediate operating stages of the CSC converter for every switching cycle, which are described as follows:

Stage I: During this stage, the switch S_b conducts while the diode D_b is reverse biased as shown in Fig. 3(a). In this interval, the power is transferred from the supply as well as from the intermediate capacitor C_i to the inductor L_b as presented in Fig. 3(d). Therefore the intermediate capacitor C_i discharges through the inductor L_b and dc-link capacitor C_b causing the voltage across the intermediate capacitor to decrease. The value of intermediate capacitor C_i must be large enough to maintain its voltage continuous during this period.

Stage II: This stage begins when the switch is turned off leading to the conduction of diode D_b. As shown in Fig. 3(b), the energy stored in inductor L_b is released to intermediate capacitor C_i and dc-link capacitor C_b. Thus, the current through the inductor L_b starts decreasing while the voltage across the intermediate capacitor C_i begins to increase. The voltage across the dc-link capacitor V_b also continues to increase.

Stage III: This stage is illustrated in Fig. 3(c). When the current through the inductor L_b becomes zero, the converter enters into DICM as shown in Fig. 3(e). The intermediate capacitor C_i continues to get charged from the supply. As the diode is reverse-biased, I_b is provided by discharging of the dc-link capacitor C_b. Hence, the dc-link voltage decreases during this period. The energy transfer process for CSC converter during one complete switching period is shown in Fig. 3(d). The current through the inductor L_b remains zero until switch S_b is triggered again to restart the switching cycle as shown in Fig. 3(e).

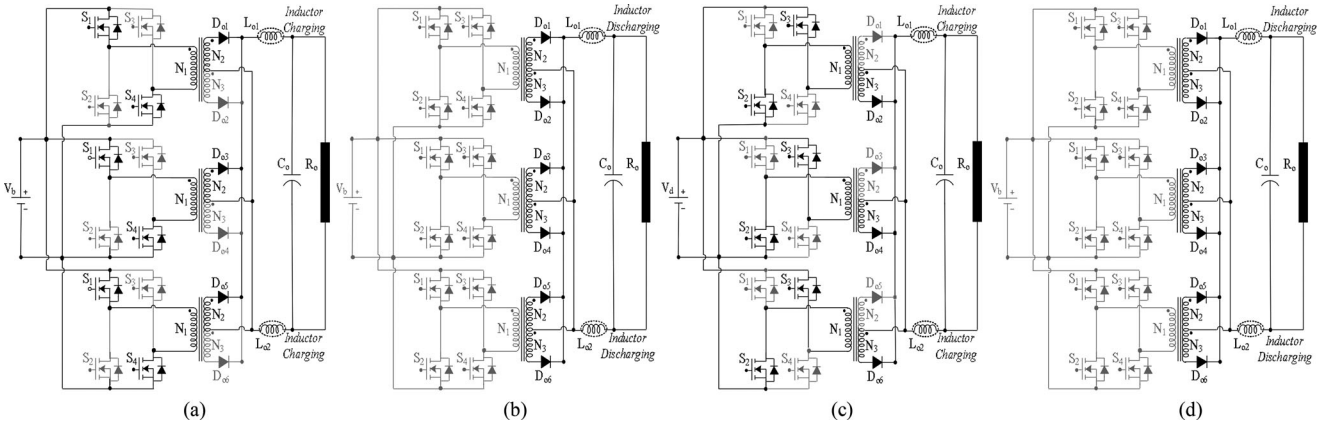

Fig. 4. Operation of FB buck converter: (a) Stage I, (b) Stage II, (c) Stage III, and (d) Stage IV.

B. Operating Modes of FB Converter

The controlled output of CSC converter is fed to the FB buck converter to step down the dc-link voltage to the desired level. Three FB converters are connected in parallel so that device rating can be reduced and also scaling up the power rating is easy. Referring to Fig. 4, the FB converters operate in CCM whose operating stages are described as follows:

Stage I: This stage is initiated when the switches S_1 and S_4 are turned on and the dc-link voltage V_b is applied across the primary winding of the high-frequency transformers (HFTs) as shown in Fig. 4(a). The diodes D_{o1}, D_{o3}, and D_{o5} become forward biased, and the energy is stored in the output inductors L_{o1} and L_{o2}. This results in an increased inductor current while the output filter capacitor C_o discharges through the welding load.

Stage II: During this stage, S_1, S_2, S_3, and S_4 are switched off while all the output diodes ($D_{o1}, D_{o2}, D_{o3}, D_{o4}$, D_{o5}, and D_{o6}) freewheel the energy stored in the output inductors L_{o1} and L_{o2}. This stage is presented in Fig. 4(b). The inductors release its stored energy to the output capacitor C_{o} and welding load; thus, the output inductor current starts decreasing linearly.

Stage III: Analogous to Stage I, switch pair S_2 and S_3 conducts to transfer the energy to output inductors, as shown in Fig. 4(c). Diodes D_{o1}, D_{o3}, and D_{o5} remain open during this interval. However, the output capacitor C_o discharges through the welding load.

Stage IV: Likewise, Stages II and IV are similar, as shown in Fig. 4(d), as none of the switch pairs conduct, and again the output rectifier diodes ($D_{o1}, D_{o2}, D_{o3}, D_{o4}, D_{o5},$ and D_{o6}) act as freewheeling diodes. The output inductors release their stored energy charging the output capacitor C_o. This stage terminates when the switches S_1 and S_4 are switched on again and the operating modes repeat in each switching cycle.

IV. Design of Proposed CSC Converter-Based AWPS

A 1.5 kW (P_{in}) AWPS is designed, simulated, and experimentally investigated to illustrate its efficacy for welding applications. The switching frequency of both the converters is much higher as compared to the line frequency. So, the supply voltage v_s is assumed to be constant during one switching cycle to derive the necessary component design.

A. Design of Input Filter

The output of DBR is fed to the *L–C* filter to suppress the higher order harmonics in the input current [30]. The value of maximum capacitance for achieving low harmonic content in the input current is calculated as

$$C_{\max} = \frac{I_m \tan\theta}{2 \times \pi \times f_L \times V_m} \tag{1}$$

where V_m and I_m are the peak input ac voltage and current, respectively, and f_L is the fundamental frequency. The maximum capacitance is estimated as 0.4 μF. θ is considered as 1° for achieving a high PF. A 220 nF filter capacitor C_f is selected in the development of the prototype. To obtain low harmonic distortion at the input ac mains, the filter inductor is expressed as

$$L_f = \frac{1}{4 \times \pi^2 \times f_c^2 \times C_f} \tag{2}$$

where f_c is the cutoff frequency, which is considered to be 3 kHz. A filter inductor of 2.8 mH is selected for hardware development.

B. Design of CSC Converter

The CSC converter is designed to provide a dc-link voltage V_b of 360 V at a constant switching frequency of 30 kHz. The inductor L_b operates in DICM; so current through L_b becomes discontinuous. But, the voltage across the intermediate capacitor C_i remains continuous during a switching period. For the supply voltage (v_s) of 220 V, the rectified output of DBR (V_d) is expressed as

$$V_d = \frac{2\sqrt{2}v_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} \approx 198\,\mathrm{V}. \tag{3}$$

The output voltage V_b of CSC converter is given by

$$V_b = \frac{D_b}{1 - D_b} V_d \tag{4}$$

where D_b represents the duty ratio for the switch S_b.

The nominal value of duty ratio in DICM operation is obtained as

$$D_{bn} = \sqrt{2} M \sqrt{K_a} \tag{5}$$

$$\text{where } M = \frac{V_b}{V_m} = \frac{360}{311} = 1.157 \tag{6}$$

and K_a is the conduction parameter.

For DICM operation

$$K_a < \frac{1}{2(M + |\sin \omega t|)^2}. \tag{7}$$

For the CSC converter to be in DICM for the complete line cycle of supply voltage, conduction parameter is given as

$$K_a|_{\omega t = 90^\circ} < \frac{1}{2(M+1)^2} < 0.107. \tag{8}$$

Substituting these values in (5), the value of duty ratio, D_{bn} for DICM operation of CSC converter, $D_{bn} = 0.271$.

1) Design of Input Inductors (L_b): The input inductor of the CSC converter is designed such that the inductor current becomes discontinuous during every switching period. The critical value of L_b is

$$L_{bc} = \frac{V_d D_{bn}}{2 f_{sb} I_d} = \frac{198 \times 0.271}{2 \times 30000 \times 6.13} = 145.89\ \mu\text{H} \tag{9}$$

where f_{sb} is the switching frequency of the CSC converter. In order to ensure DICM operation of the inductor, L_b must be less than L_{bc}. Hence, the selected value of inductor L_b is 90 μH.

2) Design of Intermediate Capacitor (C_i): The intermediate capacitor C_i is designed for permissible voltage ripple ΔV_{C_i} across it such that the voltage V_{C_i} remains continuous during the complete switching period. Therefore, the voltage ripple is taken as 10% of V_{C_i}

$$C_i = \frac{V_b D_{bn}}{\Delta V_{C_i} f_{sb} R_b} = \frac{P_i D_{bn}}{\Delta V_{C_i} f_{sb} V_b} = \frac{1500 \times 0.271}{56 \times 30\,000 \times 360} = 0.672\ \mu\text{F}. \tag{10}$$

The selected value of intermediate capacitor C_i is 0.66 μF.

3) Design of DC-Link Capacitor (C_b): The value of capacitor C_b mainly depends upon the acceptable voltage ripple ΔV_b in the dc-link voltage. Considering the output ripple voltage to be 5% of the dc-link voltage, its value can be calculated as

$$C_b = \frac{P_o}{2\pi f_L V_b \Delta V_b} = \frac{1500}{2 \times \pi \times 50 \times 360 \times 18} = 736.8\ \mu\text{F} \tag{11}$$

where f_L is the line frequency, i.e., 50 Hz and ΔV_b is the output voltage ripple. To reduce the output voltage ripple, the output capacitor is chosen as 940 μF.

C. Design of FB Buck Converter

The FB buck converters connected in modular arrangement, form the second stage of the proposed AWPS and provide HF isolation to the power supply. In this way, modularity is achieved in the system therefore the devices used in each of them can be of lower power rating. The output of the CSC converter acts as the input to the isolated FB buck converter operating at a switching frequency of 100 kHz. The FB converters signify the conventional welding power supply. For sake of simplicity, single module of FB converter is considered during analysis.

1) Design of Turns Ratio of HFT: For an isolated FB buck converter, the net change in the inductor current is zero over one switching cycle. Therefore, the output to input voltage ratio can be represented as

$$\left\{ V_d \left(\frac{N_2}{N_1} \right) - V_o \right\} \left(\frac{t_{\text{on}}}{T_s} \right) - \left\{ V_o \left(\frac{t_{\text{off}}}{T_s} \right) \right\} = 0 \tag{12}$$

where $T_s = 1/f_s$ denotes the switching period of FB converter. The duty cycle, D_f for rated output voltage V_o is expressed as

$$D_f = \frac{V_o}{2V_d} \left(\frac{N_1}{N_2} \right). \tag{13}$$

The FB buck converter is designed to operate in CCM; so by rearranging the aforementioned equation, the turns ratio is calculated to achieve an output voltage of 60 V

$$\left(\frac{N_1}{N_2} \right) = \frac{2 D_f V_d}{V_o} = \frac{2 \times 0.4 \times 360}{60} = 4.8 \tag{14}$$

2) Design of Output Inductors (L_{o1} and L_{o2}): The value of output inductors L_{o1} and L_{o2} must be large enough such that the currents through them remain continuous over one switching period. If the permissible ripple current is Δi_{L_o} (10% of I_o), then the value of output inductors ($L_{o1} = L_{o2}$) can be calculated as

$$L_{o1} = \frac{V_o\,(0.5 - D_f)}{f_s(\Delta i_{Lo1})} = \frac{60 \times (0.5 - 0.4)}{100\,000 \times 5} = 12\ \mu H \tag{15}$$

To ensure CCM operation of the inductor, the selected value of $L_o = 15$ μH.

3) Design of Output Capacitor (C_o): The output capacitor C_o is intended to mitigate the output voltage ripple. The voltage ripple on output capacitor C_o is calculated as

$$\Delta V_o = \frac{V_o\,(1 - 2D_f)}{32 f_s^2 L_{o1} C_o}. \tag{16}$$

Considering the voltage ripple to be 10% of V_o, the output capacitor value is estimated as

$$C_o = \frac{V_o\,(1 - D_f)}{8 f_s^2 L_{o1} (\Delta V_o)} = \frac{60 \times (1 - 0.4)}{8 \times 100\,000^2 \times 15 \times 10^{-6} \times 6} \cong 5\ \mu\text{F}. \tag{17}$$

The aforementioned calculated design values, along with the specifications of the components utilized in the prototype of proposed AWPS, are tabulated in Table I.

TABLE I
DESIGN SPECIFICATIONS FOR CSC CONVERTER-BASED AWPS

Component		Calculated Value	Selected Value
CSC Converter	Inductor, L_b	145.89 μH	90 μH
	Intermediate capacitor, C_i	0.672 μF	0.66 μF
	DC-link capacitor, C_b	736.8 μF	940 μF
FB Buck Converter	Turns ratio, N_1/N_2	4.8	5
	Inductors, L_{o1} and L_{o2}	12 μH	15 μH
	Capacitor, C_o	5 μF	7 μF

V. CONTROL OF PROPOSED CSC CONVERTER-BASED AWPS

The proposed PFC AWPS is developed using two different individual controllers dedicated to each converter stage. Simple voltage follower approach is adopted for CSC converter to achieve PFC at the utility interface. However, dual-loop control scheme is utilized in FB converter. A brief description of both the control schemes is given in the following sections.

A. Control of CSC Converter

The voltage follower approach is employed for DICM operation of the CSC converter. The DICM operation of inductor L_b helps in achieving PFC inherently by implementing the single voltage feedback control loop. The voltage controller loop regulates the dc-link voltage V_b despite any variations in CSC converter's output current I_b and supply voltage v_s. In this approach, the dc-link voltage is taken as a feedback and then compared with the reference voltage V_b^*. Correspondingly, the generated voltage error signal, V_{be} at any *n*th instant is expressed as

$$V_{be}(n) = V_b^*(n) - V_b(n). \tag{18}$$

Thereafter, this voltage error signal is given to a proportional and integral (PI) controller to ensure a controlled output V_{cv}

$$\begin{aligned} V_{cv}(n) &= V_{cv}(n-1) + k_{pv}\{V_{be}(n) - V_{be}(n-1)\} \\ &\quad + k_{iv}V_{be}(n) \end{aligned} \tag{19}$$

where k_{pv} and k_{iv} denote the proportional and integral gains of the PI voltage controller respectively.

Finally, the output of voltage controller is compared with a high-frequency saw-tooth waveform m_{a1} to derive pulses to fire the device in the CSC converter

$$\begin{aligned} &\text{If } m_{a1}(t) < V_{\rm cv}(t), \text{ then } S_b = 1; \\ &\text{if } m_{a1}(t) \geq V_{cv}(t), \text{ then } S_b = 0 \end{aligned} \tag{20}$$

where 1 and 0 represent the on and off switching states of power switch S_b respectively.

B. Control of FB Buck Converter

The FB converter controller is intended to deliver a constant dc voltage at the output. In addition, it must also limit the output current during overload conditions, which ensures high-quality weld bead over a wide load range. The current limit is an essential criterion, which must be integrated to make the SMPS suitable for arc-welding applications. In order to satisfy the important prerequisite of AWPS, dual-loop control scheme is adopted. In this technique, apart from sensing the output voltage, output current is also taken as a feedback. The voltage loop is used to regulate the output voltage, while the current loop restricts the output load current during overload conditions. The output voltage V_o is sensed and then compared with the reference voltage V_o^* to generate the voltage error signal, V_{oe}. This error signal is processed by the PI voltage controller to maintain a constant voltage at the output. The output of the PI voltage controller is expressed as

$$\begin{aligned} C_V(k) &= C_V(k-1) + k'_{pv}\{V_{oe}(k) - V_{oe}(k-1)\} \\ &\quad + k'_{iv}V_{oe}(k) \end{aligned} \tag{21}$$

where k'_{pv} and k'_{iv} are the proportional and integral gains of the voltage controller, respectively.

On the other hand, the output current I_o is taken as a feedback signal and compared with the output current limit $I_{\rm SC}$. The current controller mainly constitutes a PI controller, which processes the error signal to restrict the output current within the desired limits

$$C_i(k) = C_i(k-1) + k'_{pi}\{I_e(k) - I_e(k-1)\} + k'_{ii}I_e(k) \tag{22}$$

where k'_{pi} and k'_{ii} represent the proportional and integral gain constants of the current controller, respectively. Afterward, the comparator compares the outputs of both PI controllers, and whichever is found to be lower, it is fed to the pulsewidth-modulated (PWM) generator to generate the gating pulses. So, the duty cycle of FB converter power switches is amended conforming to the changes in the output dc voltage and the welding current.

VI. EXPERIMENTAL VALIDATION OF PROPOSED AWPS

To corroborate the operating principle and viability of the proposed AWPS, a prototype is developed, using the specifications listed in Table I. A digital signal processor (DSP) TI-TMS320F2812 is employed to implement the controllers and the performance of proposed CSC converter-based AWPS is evaluated. Test results are recorded and discussed in the following sections.

A. Steady-State Performance

The steady-state performance of the proposed AWPS at rated load and at 220 V supply voltage showing the supply voltage (v_s), supply current (i_s), output voltage (V_o), and output current (I_o) is illustrated in Fig. 5(a). The intermediate results are presented in Fig. 5(b), including CSC converter dc-link voltage (V_b) and current (I_b). The output voltage is regulated to 60 V, while dc-link voltage is maintained at 360 V. The voltage-follower approach ensures that the input current is sinusoidal and is in phase with the input voltage. In Fig. 5(c), the DICM operation of the CSC inductor is shown. It is also evident from the obtained results that the voltage across the intermediate capacitor remains continuous. The voltage and current stresses for switch

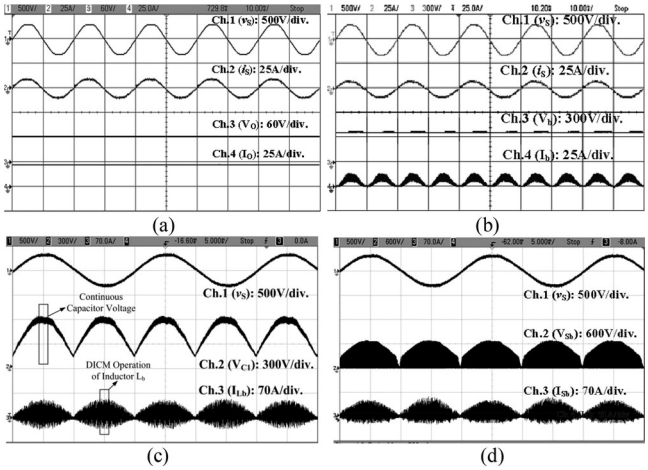

Fig. 5. Steady-state performance of proposed converter at rated load and 220 V (rms) supply voltage. (a) Waveforms of v_s, i_s, V_o, and I_o; (b) waveforms of v_s, i_s, V_b, and I_b; (c) waveforms of v_s, V_{C1}, and I_{Lb} demonstrating DICM; (d) waveforms of voltage and current stress of switch S_b.

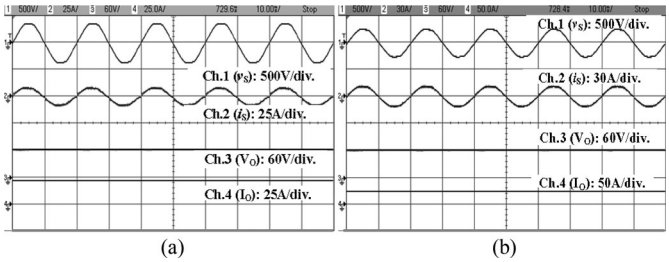

Fig. 6. Test results under supply voltage variations: (a) waveforms of v_s, i_s, V_o, and I_o at rated load and at $v_s = 260$ V. (b) Waveforms of v_s, i_s, V_o, and I_o at rated load and at $v_s = 182$ V.

S_b are shown in Fig. 5(d). The peak voltage and current stresses for switch S_b are 680 V and 45 A, respectively.

B. Dynamic Performance Under Supply Voltage Variation

The performance of the proposed power supply is also investigated at varying supply voltages. Fig. 6(a) and (b) shows the performance of CSC converter-based AWPS on varying the supply voltage from 260 to 182 V (rms). It can be perceived from these test results that the controller regulates the output voltage and dc-link voltage to their rated values. The input current is adjusted in accordance with the supply voltage such that converter draws almost the same rated power. Furthermore, the input current remains sinusoidal in nature throughout the wide range of supply voltage.

C. Dynamic Performance Under Light-Load Condition

Apart from the supply voltage variations, the performance of the proposed AWPS is also verified during light-load conditions. To illustrate the efficacy of the proposed AWPS under light-load conditions, the load is suddenly varied as shown in Fig. 7(a). It can be observed that the output current is reduced suddenly following the reduction in load while a constant dc voltage is

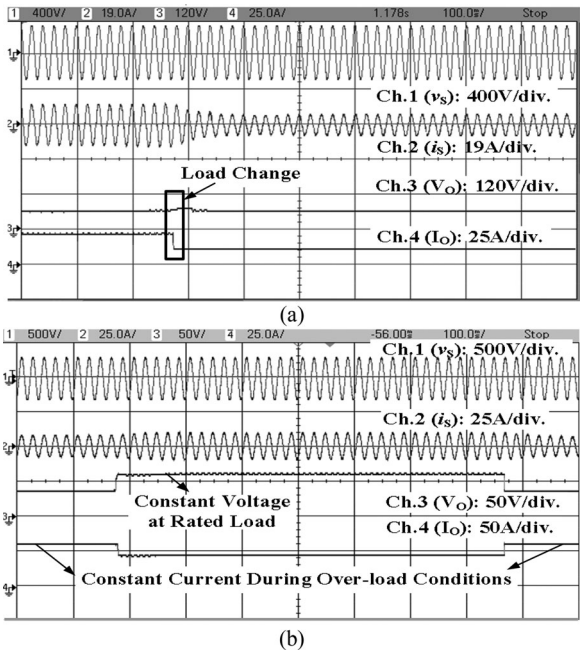

Fig. 7. (a) Waveforms of v_s, i_s, V_o, and I_o under load variations; (b) waveforms of v_s, i_s, V_o, and I_o under overload condition.

maintained at the output. The supply current is still found to be in phase with the supply voltage.

D. Dynamic Performance Under Overload

The welding load current plays a significant role on the stability of the arc-welding process. To make the proposed power supply viable for welding applications, it is mandatory that it should work efficiently even during overload conditions. Therefore, the behavior of the developed prototype is also studied when the load is increased beyond its rated value as shown in Fig. 7(b). The proposed AWPS is designed with the maximum output current limit (I_{SC}) set at 30A, which can be adjusted as per the requirement while designing the dual-loop controller. Referring to Fig. 7(b), the dual-loop controller efficiently limits the output current to 30A even when the load is increased beyond its rated value by adjusting the output voltage suitably. As C_i becomes less than C_v, the duty cycle of the switches is now determined by the value of C_i instead of C_v. Therefore, whenever the load is increased beyond a certain limit such that the output current becomes greater than 30A the controller switches from constant voltage to constant current and successfully maintains constant current at the output. In this way, by limiting the output current, a good weld appearance can be achieved with reduced spatter.

E. Improved PQ of the Proposed AWPS

The performance of the proposed AWPS at different power levels is presented in Table II. It can be clearly seen that the PF remains close to unity with an efficiency greater than 86% throughout the wide load range. The performance parameters such as apparent power (*S*), active power (*P*), reactive power

TABLE II
PERFORMANCE OF PFC-CSC CONVERTER-BASED AWPS AT DIFFERENT POWER LEVELS

Input Power, $P_{\rm in}$ (kW)	Output Power, P_o (kW)	Efficiency, η (%)	THD of I_s (%)	I_s (A)	PF	DPF
0.75	0.65	86.3	6.7	3.53	0.99	1.0
0.90	0.79	87.5	5.6	4.22	1.0	1.0
1.05	0.93	88.1	5.0	4.76	1.0	1.0
1.20	1.06	88.4	4.3	5.45	1.0	1.0
1.35	1.20	89.2	3.9	6.15	1.0	1.0
1.51	1.34	88.7	3.4	6.88	1.0	1.0

TABLE III
COMPARISON OF NONISOLATED BUCK–BOOST CONVERTERS

Schemes → Attributes ↓	Cuk	SEPIC	Zeta	CSC (Proposed)
No. of Components	6	6	6	5
EMI	Medium	Medium	High	Medium
Cost	Medium	Medium	High	Low
Size	Medium	Medium	High	Low
Switch current stress	Medium	Medium	High	Low
PFC	Good	Good	Good	Excellent

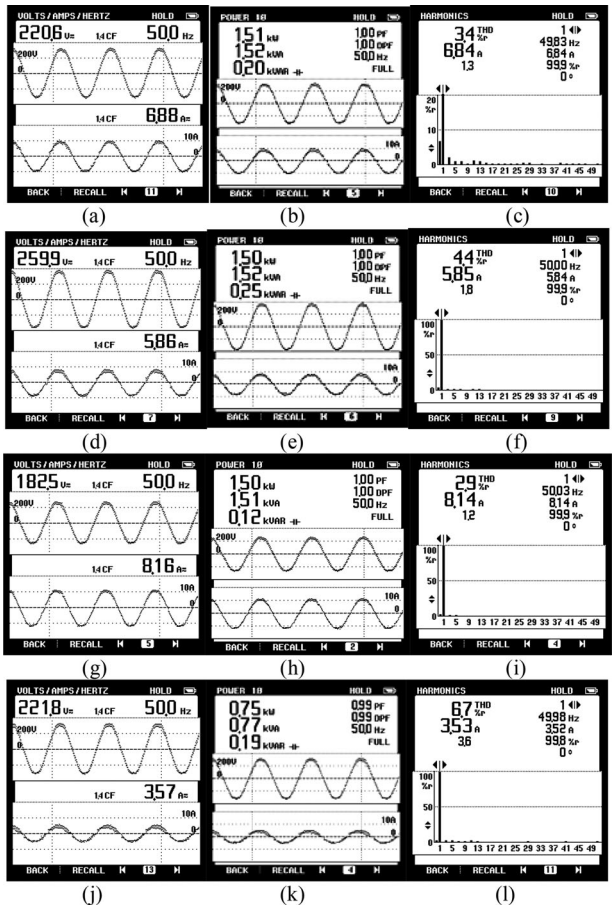

Fig. 8. PQ indices and performance parameters (v_s, i_s, P, Q, S, PF, DPF, CF, and THD of i_s of proposed PFC-CSC converter-based AWPS; (a)–(c) at rated load and v_s at 220 V; (d)–(f) at rated load and v_s at 260 V; (g)–(i) at rated load and v_s at 182 V; and (j)–(l) at light-load and v_s at 220 V.

(Q), supply voltage (v_s), supply current (i_s) at different line/load conditions are presented in Fig. 8. Various PQ indices such as PF, DPF, and THD for wide range of line/load conditions are also demonstrated in Fig. 8. It is evident from test results that CSC converter works as an excellent PFC preregulator during variable loads and supply voltages, thereby validating the improved PQ of the proposed AWPS. The PF and DPF are found to be approaching unity. The THD of input current is also quite low, making it adhere to the stringent standards specified by IEC61000-3-2.

F. Comparative Analysis With Conventional AWPS

A comparative assessment of the proposed PFC-CSC converter-based AWPS with the conventional AWPS is carried out to validate the suitability of the proposed power supply for welding application as shown in Fig. 9. The conventional AWPS mainly has a DBR followed by FB buck converter without any PFC at the front stage. A comparison on the basis of THD of supply current is presented in Fig. 9(a).

It is evident that input current THD in conventional AWPS is greater than 70% whereas in the proposed AWPS it is less than 7%. The efficiencies of both the AWPS are also compared as shown in Fig. 9(b), which depicts the superiority of the proposed power supply clearly. The losses associated with the proposed AWPS are always less as compared to the conventional AWPS attaining a higher efficiency over a wide operating range. From Fig. 9(c), it is evident that the PF remains close to unity in the proposed AWPS whereas a very low PF varying from 0.60 to 0.65 is achieved for conventional AWPS. High input current THD and low PF make the conventional AWPS violate international PQ standards. On the basis of the observed PQ indices and efficiency, it can be said that the proposed CSC converter-based SMPS performs much better than the conventional AWPS and emerges out as a viable solution for arc-welding applications.

G. Comparative Analysis With Buck–Boost Converters

From the obtained test results, it is evident that the input current is a sinusoidal unity PF current. However, in other buck–boost or boost–buck converters like zeta, Cuk, and SEPIC, the input current waveform becomes a little more distorted because of the fact that the input inductor in these converters are connected directly across the input dc supply voltage through a switch that causes a rapid current build-up in the inductor. When the switch is turned off, especially when the converter is operating in DICM, the current has to decay rapidly, making the input current get distorted. A brief comparison of nonisolated buck–boost converters operating in DICM mode has been presented in Table III. The proposed front end CSC converter requires less number of components. The CSC converter also has minimum EMI issues, cost, switch stress and provides excellent PFC at the ac mains making it the best choice for arc-welding applications.

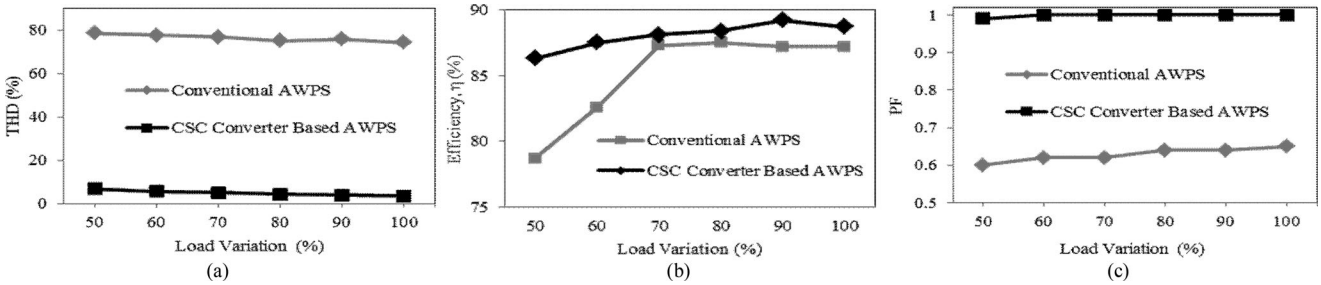

Fig. 9. Comparative analysis of (a) THD of supply current at ac mains (b) efficiency, and (c) PF variation with input power for the conventional and the proposed CSC converter-based AWPS.

VII. Conclusion

A PFC-CSC converter-based AWPS has been analyzed, designed, and implemented to illustrate its improved performance with regard to PQ at input ac mains. A simple voltage follower approach has been utilized to integrate the DICM operation of the CSC converter. Considering wide range of load and supply voltage variations as it is seen realistically in a welding power supply, it is found that DICM operation leads to inherent PFC at the utility interface. From the obtained results, it is evident that the proposed AWPS has performed exceedingly well in the wide operational range. The supply current THD is found to be well within the allowable limits of IEC 61000-3-2 standard [4]. The dual-loop controller for FB converters has effectively maintained a constant dc voltage at the output and also efficiently limits the output current during overload conditions. This reduces spatter generation and thus enhances the quality of the weld. The proposed AWPS takes care of this overcurrent handling requirement very well simultaneously maintaining the voltage at a constant value when the load is light. The results presented have shown that both objectives have been achieved successfully. Altogether, the proposed welding power supply has shown satisfactory performance and it has confirmed its proficiency and suitability for arc welding applications.

References

[1] J.-M. Wang and S.-T. Wu, "A novel inverter for arc welding machines," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1431–1439, Mar. 2015.

[2] J.-M. Wang, S.-T. Wu, S.-C. Yen, and H.-J. Chiu, "A simple inverter for arc-welding machines with current doubler rectifier," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5278–5281, Nov. 2011.

[3] K. Weman, *Welding Process Handbook*. Cambridge, MA, USA: Woodhead, 2003, pp. 13–25.

[4] *Limits for Harmonic Current Emissions*, International Electro Technical Commission Standard 61000-3-2, 2004.

[5] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[6] M. M. Jovanovic and J. Yungtaek, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications—An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.

[7] O. Gracia, J. A. Cobos, R. Prieto, and J. Uceda, "Single phase power factor correction: A survey," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749–755, May 2003.

[8] R. Casanueva, F. J. Azcondo, F. J. Diáaz, and C. Branas, "TIG welding machines," *IEEE Ind. Appl. Mag.*, vol. 17, no. 5, pp. 53–58, Sep./Oct. 2011.

[9] C. Klumpner and M. Corbridge, "A two-stage power converter for welding applications with increased efficiency and reduced filtering," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2008, pp. 251–256.

[10] V. Grigore and J. Kyyra, "High power factor rectifier based on buck converter operating in discontinuous capacitor voltage mode," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1241–1249, Nov. 2000.

[11] R. Oruganti and M. Palaniapan, "Inductor voltage control of buck-type single-phase ac–dc converter," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 411–416, Mar. 2000.

[12] S.-K. Ki and D. D.-C. Lu, "A high step-down transformerless single-stage single-switch AC/DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 36–45, Jan. 2013.

[13] J. P. R. Balestero, F. L. Tofoli, G. V. Torrico-Bascope, and F. J. M. de Seixas, "A dc–dc converter based on the three-state switching cell for high current and voltage step-down applications," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 398–407, Jan. 2013.

[14] M. A. Al-Saffar, E. H. Ismail, and A. J. Sabzali, "Integrated buck–boost–quadratic buck PFC rectifier for universal input applications," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2886–2896, Dec. 2009.

[15] E. Niculescu, M. C. Niculescu, and D. M. Purcaru, "Modelling the PWM zeta converter in discontinuous conduction mode," in *Proc. MELECON*, 2008, pp. 651–657.

[16] B. Singh, M. Agrawal, and S. Dwivedi, "Analysis, design and implementation of a single-phase power-factor corrected ac-dc zeta converter with high frequency isolation," *J. Electr. Eng. Technol.*, vol. 3, no. 2, pp. 243–253, 2008.

[17] S. Singh, B. Singh, B. Gurumoorthy, and V. Bist, "Power factor corrected zeta converter based improved power quality switched mode power supply," *IEEE Trans. Ind. Electron.*, Early Access, Mar. 2015.

[18] V. Bist and B. Singh, "PFC Cuk converter-fed BLDC motor drive," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 871–887, Feb. 2015.

[19] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode sepic and cuk power factor preregulators: Analysis and design," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 630–637, Oct. 1997.

[20] C. G. Bianchin, R. Gules, A. A. Badin, and E. F. R. Romaneli, "High-power-factor rectifier using the modified SEPIC converter operating in discontinuous conduction mode," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4349–4364, Mar. 2015.

[21] P. F. de Melo, R. Gules, E. F. R. Romaneli, and R. C. Annunziato, "A modified SEPIC converter for high power factor rectifier and universal input voltage applications," *IEEE Trans. Power Electron.*, vol. 25, no. 2, Feb. 2010.

[22] K. I. Hwu and Y. T. Yau, "Two types of KY buck–boost converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2970–2980, Aug. 2009.

[23] O. Sago, K. Matsui, H. Mori, I. Yamamoto, M. Matsuo, I. Fujimatsu, Y. Watanabe, and K. Ando, "An optimum single phase PFC circuit using CSC converter," in *Proc. 30th IEEE-IECON Conf.*, Nov. 2–6, 2004, vol. 3, pp. 2684–2689.

[24] B. Williams, "Generation and analysis of canonical switching cell dc to dc converters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 329–346, Jan. 2014.

[25] K. Matsui, I. Yamamoto, T. Kishi, M. Hasegawa, H. Mori, and F. Ueda, "A comparison of various buck–boost converters and their application

to PFC," in *Proc. 28th IEEE-IECON Conf.,* Nov. 5–8, 2002, vol. 1, pp. 30–36.
[26] Y. Ando, K. Matsui, and M. Hasegawa, "Discussions on various chopper circuits for power factor corrections," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2013, pp. 1–6.
[27] J. Sun, D. M. Mitchell, M. F. Greuel, P. T. Krein, and M. R. Bass, "Averaged modeling of PWM converters operating in discontinuous conduction mode," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 482–492, Jul. 2001.
[28] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive study of single-phase ac-dc power factor corrected converters with high-frequency isolation," *IEEE Trans. Ind. Informat.*, vol. 7, no. 4, pp. 540–556, Nov. 2011.
[29] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics, Converter, Application and Design*, 3rd ed. Hoboken, NJ, USA: Wiley, 2002.
[30] V. Vlatkovic, D. Borojevic, and F. C. Lee, "Input filter design for power factor correction circuits," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 199–205, Jan. 2005.

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