

Fault-Decoupled Instantaneous Frequency and Phase Angle Estimation for Three-Phase Grid-Connected Inverters

G. De Donato, *Member, IEEE*, G. Scelba, *Member, IEEE*, G. Borocci, *Member, IEEE*,
F. Giulii Capponi, *Member, IEEE*, and G. Scarcella, *Member, IEEE*

Abstract—Frequency and phase angle estimation is a key aspect for grid-connected inverters that are required to guarantee low-voltage fault-ride-through capability. Over the past two decades, a number of estimation algorithms have been proposed, mostly based on the well-known phase-locked loop (PLL). It has been demonstrated that standard PLLs do not perform correctly in abnormal grid conditions, due to the oscillations produced in the frequency and phase angle estimates by the voltage harmonics. This paper introduces a new, general approach to harmonic decoupling and presents a highly intuitive and simple scheme, applying it to an $\alpha\beta$ -PLL; compensation of any desired number of harmonic components is possible. Two implementations of this decoupling scheme are presented. It is shown that the performances of the resulting fault-decoupled PLLs are comparable with those of other advanced frequency and phase angle estimation structures.

Index Terms—Estimation algorithm, fault ride through, frequency, grid connection, harmonics, phase angle, phase-locked loop (PLL).

I. INTRODUCTION

THREE-PHASE, grid-connected inverters require a precise measurement of the instantaneous grid voltages at the point of common coupling (PCC), in order to maintain synchronization and to be able to control instantaneous power flow. These measurements are then used to obtain estimates of the frequency and phase angle of the positive-sequence component of the grid voltage, which are required by the current controller, [1]. Many national grid codes have been recently updated to require low-voltage fault ride through capability from grid-connected inverters. For example, in the event of a voltage sag, the Italian grid code CEI-021, [2], prescribes that the inverter must not disconnect for at least 200 ms, and up to 400 ms if the sag is less than 60% of the rated voltage. During the fault, it is also required that the inverter provides voltage support to the grid, aiding positive-sequence voltage recovery and negative-sequence voltage reduction, [3]. In all of the published control algorithms, it

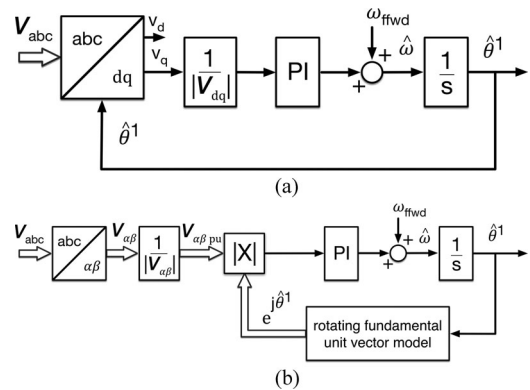


Fig. 1. Basic PLLs for frequency and phase angle estimation. (a) SRF-PLL. (b) $\alpha\beta$ -PLL.

is of fundamental importance that the frequency and phase angle estimation algorithm maintain correct tracking even during a fault occurrence.

A number of frequency and phase angle estimation algorithms have been proposed over the past two decades; the well-known phase-locked loop (PLL), [4]–[5], which has been used in telecommunications in a variety of applications for the past 80 years, is at the core of most of these techniques. In particular, the synchronous reference frame PLL (SRF-PLL) first proposed by Kaura and Blasko in 1996, [6], has become the most widely used PLL for grid-connected converters. In the SRF-PLL, shown in Fig. 1(a), a three phase to synchronous reference frame transformation acts as the phase detector; a PI regulator, acting as the loop filter, estimates the frequency, which is then integrated to obtain the estimated phase angle. Another basic PLL, shown in Fig. 1(b), is the $\alpha\beta$ -PLL, in which the vector product between the measured and estimated stationary reference frame voltage vectors acts as the phase detector. Both the SRF-PLL and the $\alpha\beta$ -PLL operate correctly when the measured voltages form a positive sequence. However, they both have deficiencies when operating in distorted grids, since the negative-sequence and the higher order harmonic components cause oscillations in both the steady state frequency and phase angle estimates, [6]–[7]. A significant improvement in performance has been obtained with the decoupled double synchronous reference frame (DDSRF) PLL [8], in which a decoupling network removes, at steady state, the negative-sequence component from the input to the SRF-PLL. A different

Manuscript received January 30, 2015; revised April 12, 2015; accepted June 12, 2015. Date of publication June 16, 2015; date of current version November 30, 2015. Recommended for publication by Associate Editor R. Burgos

G. De Donato, G. Borocci, and F. Giulii Capponi are with the Department of Astronautical, Electrical, and Energetic Engineering, University of Rome “La Sapienza,” 00184 Rome, Italy (e-mail: giulio.dedonato@uniroma1.it; gabriele.borocci@uniroma1.it; fabio.giulicapponi@uniroma1.it).

G. Scelba and G. Scarcella are with the Department of Electrical, Electronic, and Computer Engineering, University of Catania, 95127 Catania, Italy (e-mail: giacomo.scelba@dieei.unict.it; giuseppe.scarcella@dieei.unict.it).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2015.2445797

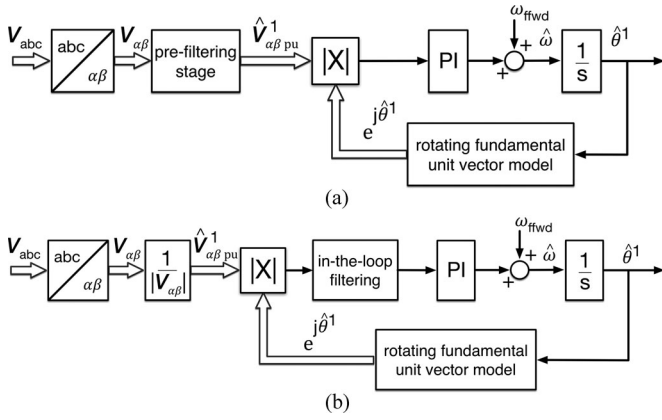


Fig. 2. Advanced PLL structures. (a) Prefiltered PLL. (b) In-the-loop filtered PLL.

implementation of the decoupling network is proposed in [9], leading to the multiple reference frame PLL. In [10], negative-sequence decoupling is applied to the $\alpha\beta$ -PLL, which is shown to have reduced overshoot in the frequency and phase angle estimates compared to the SRF-PLL. In [11], the same authors extend the decoupling network for the $\alpha\beta$ -PLL to harmonic components, while in [12] they propose an adaptive algorithm that is able to modify the parameters of the PI regulator in the $\alpha\beta$ -PLL, in order to keep the frequency estimate within the prescribed limits during fault transients. Since these decoupling networks do not modify the structure of the PLL loop, they can generally be interpreted as a prefiltering stage for the PLL input, as shown in Fig. 2(a). Here, without loss of generality, the prefiltering is applied to an $\alpha\beta$ -PLL.

A significant number of prefiltering methods that are alternative to decoupling networks can be found in the literature; all use frequency-adaptive filtering techniques. In [13], a positive-sequence component detector based on a dual-second-order generalized integrator (DSOGI) is proposed; the positive-sequence component is then fed to a PLL, giving rise to a DSOGI-PLL. The positive-sequence detector acts as a frequency-adaptive notch filter (ANF), in order to remove the negative-sequence component even in the event of frequency variations. In [14], a bandpass synchronous reference frame moving average filter (MAF) is used to extract the positive-sequence component and then feed it to an SRF-PLL. Other methods rely on the use of frequency-adaptive complex-coefficient filters (CCFs), [15]–[18]. As an alternative to CCFs, it is possible to use the generalized delayed signal cancellation, [19]. In this case, the prefiltering is achieved by a number of cascaded complex transformations that each removes a certain number of vector harmonic components; also in this case, the output is fed to an SRF-PLL.

As an alternative to prefiltering, in-the-loop filtering has also been explored in many contributions. The general idea is shown in Fig. 2(b). An additional filter of some kind is placed in cascade with the PI regulator in order to eliminate the undesired oscillations produced by the negative sequence and harmonic

components. For example, the authors in [20] propose the use of adaptive frequency notch filters within an $\alpha\beta$ -PLL, [21] explores the use of a fourth-order observer within an SRF-PLL (SOAP-PLL), and [22] performs a review of PLLs that use in-the-loop MAFs.

Apart from the previously described developments in PLL techniques, other estimators have been developed in the last decade to allow detection of the positive-sequence voltage frequency and phase angle. Among them, the most significant are the SOGI frequency locked loop (SOGI-FLL) [23], the three-phase ANF [24], and the enhanced PLL [25]–[26]. These techniques are all very similar from a mathematical point of view and behave basically as frequency-adaptive second-order band-pass filters, [26]. In [23], multiple SOGIs are tuned at harmonic frequencies, giving rise to the MSOGI-FLL.

This paper focuses on improving existent PLL techniques. In particular, it studies a new approach to decoupling, compared to the ones that have been proposed to date in the PLL literature. The scheme that will be described is general, highly intuitive, and allows compensating any number of harmonic components; its implementation can be achieved in a number of ways. Two of these, applied to an $\alpha\beta$ -PLL, will be described here: one is based on the previously described decoupling networks, while the other is based on multisynchronous reference frame filtering, a technique that has already been applied successfully in active filter current control, [27]–[29]. The proposed scheme stems from the work of the authors carried out on single-phase PLLs, [30], and on speed and position estimation for ac drives with low-resolution position sensors, [31]. The dynamic performances of the resulting fault-decoupled PLLs will be analyzed for specific grid faults with superimposed harmonic distortion. Conversely, the dynamic performance of the control loop of grid-connected inverters using these PLLs is out of the scope of this paper and will be the subject of future investigation.

II. HARMONIC DECOUPLING STRATEGIES

Ideally, a decoupling algorithm should remove all of the unwanted harmonic components from the measured voltages, in order to keep the PLL locked to fundamental harmonic, positive-sequence component at all times. Although decoupling can be performed in any reference frame, in this paper, it will be carried out in the stationary reference frame since it will be applied to an $\alpha\beta$ -PLL. Thus, one can define a decoupling voltage vector $V_{\alpha\beta dec}$ as

$$V_{\alpha\beta dec} = V_{\alpha\beta} - V_{\alpha\beta}^1 = V_{\alpha\beta}^{-1} + \sum_{h=\pm 3, \pm 5, \dots}^{\infty} V_{\alpha\beta}^h \quad (1)$$

where $V_{\alpha\beta}$ is the measured stationary reference frame voltage vector, $V_{\alpha\beta}^1$ is the rotating fundamental harmonic, positive-sequence vector, $V_{\alpha\beta}^{-1}$ is the rotating fundamental harmonic, negative-sequence vector, and $V_{\alpha\beta}^h$ is the generic rotating h th order harmonic voltage vector. Equation (1) is written for the most generic case of an unbalanced voltage at a PCC with nonlinear loads, where nonzero-sequence voltage harmonics

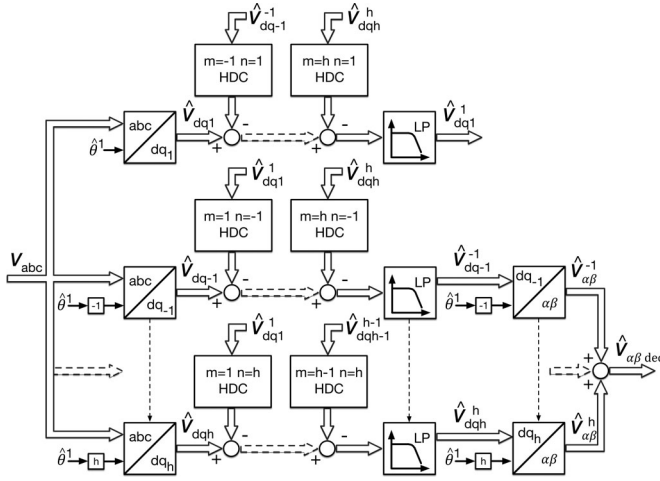


Fig. 3. MDC algorithm.

appear at all odd multiples of the fundamental frequency f_e , [20].

An *a priori* knowledge of $\hat{V}_{\alpha\beta dec}$ is not possible, however, it can be estimated by using properly formed algorithms. The following sections describe two possible ways to obtain this. Both algorithms are based on the fact that a reference frame transformation of the voltage vector to any harmonic frequency hf_e produces a frequency shift of the entire voltage spectrum. The voltage component at that frequency becomes stationary, while all the other harmonic components will be rotating, albeit at different speeds compared to the stationary reference frame; these rotating components can be either decoupled, as in the algorithm presented in Section II-A, or filtered, as in the algorithm presented in Section II-B, in order to produce an estimate $\hat{V}_{\alpha\beta}^h$ of the voltage component at hf_e . By replicating this approach, it is possible to estimate any number of harmonic components, which are then transformed back to the stationary reference frame and added up to produce the desired $\hat{V}_{\alpha\beta dec}$. It should be noticed that all of the reference frame transformations use the phase angle estimate $\hat{\theta}^1$ coming from the $\alpha\beta$ -PLL; thus, both of these approaches can be seen as a number of frequency-adaptive bandpass filters working in parallel.

A. MDC Algorithm

Fig. 3 shows the block diagram of the multiharmonic decoupling cell (MDC) algorithm. This is essentially an extension of the DDSRF algorithm presented in [8] and is mathematically equivalent to the algorithm described in [9]. The difference with what has been presented previously is that here the algorithm is used to calculate $\hat{V}_{\alpha\beta dec}$, while in [9] the algorithm is used to calculate $\hat{V}_{\alpha\beta}^1$, which is then fed to the PLL. The harmonic decoupling cells (HDCs) that are visible in Fig. 3 are structured according to the general definition given in [8]; m indicates the harmonic order of the component that is being decoupled, while n indicates the harmonic order of the frequency at which the decoupling is taking place. A first-order low-pass filter is cascaded

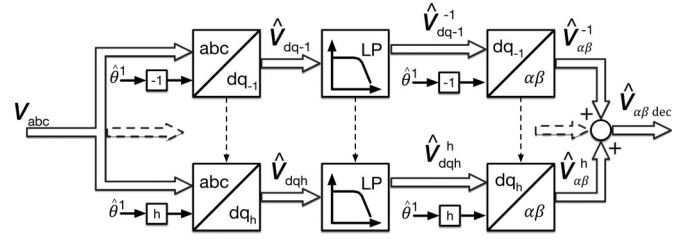


Fig. 4. MSF algorithm.

with the HDCs to attenuate any residual, undecoupled harmonic components: following the indications in [8], the low-pass filters are tuned for a 35-Hz bandwidth. Each estimated harmonic component is subsequently used to decouple its influence through the HDCs in the other reference frames.

With h being the number of harmonic components that are estimated, it can be easily seen that this algorithm requires the use of $(h^2 + h)$ HDCs and $2h$ reference frame transformations. Furthermore, extending the algorithm to decouple a new harmonic requires a significant amount of modifications, so the MDC algorithm is not modular.

B. MSF Algorithm

Fig. 4 shows the block diagram of the multiharmonic SRF filtering (MSF) algorithm. The basic idea is to apply only low-pass filtering after each reference frame transformation, instead of decoupling each harmonic and then applying light filtering, as done above. It has been decided to use Butterworth filters due to their straightforward tuning. The filter order is determined by the spectral separation between the various harmonics. For example, assuming balanced (or lightly unbalanced) voltage harmonics, the significant harmonic orders present in the spectrum are $h = +1, -1, -5, +7, -11$, etc. The closest harmonic to $\hat{V}_{\alpha\beta}^{-1}$ is $\hat{V}_{\alpha\beta}^1$, i.e., spectrally separated by $2f_e$. In this case, a sixth-order filter, with a cutoff frequency around 25 Hz, successfully removes the effect of $\hat{V}_{\alpha\beta}^1$ and all other harmonic components from $\hat{V}_{\alpha\beta}^{-1}$. The calculation of $\hat{V}_{\alpha\beta}^{-1}$ has the heaviest filtering requirement, since the other harmonic components have a wider spectral separation. For example, the closest harmonic component to $\hat{V}_{\alpha\beta}^{-5}$ is $\hat{V}_{\alpha\beta}^{-1}$, spectrally separated by $4f_e$; in this case, a fifth-order filter with a cutoff frequency around 40 Hz is sufficient to obtain a good estimate. This filter order can also be kept for the calculation of the remaining components, or even further relaxed, since the spectral separation increases to $6f_e$, for $|h| > 5$. On the other hand, if the voltage harmonics are heavily unbalanced, the harmonic orders present in the spectrum are $+1, -1, -3, -3, +5, -5$, etc. Thus, each harmonic component is always spectrally separated by $2f_e$ from its closest neighbor and sixth-order filters are required throughout.

From a computational point of view, this algorithm requires h filters and $2h$ reference frame transformations. Furthermore, extending the algorithm to decouple a new harmonic requires no

TABLE I
TYPE-E FAULT DETAILS

f_c	50 Hz
$V_{\text{pre-fault}}^1$	$340 \angle 0^\circ$ V
Zero-sequence voltage	$46.47 \angle 0^\circ$ V
V_{fault}^1	$246.47 \angle 0^\circ$ V
V_{fault}^{-1}	$46.47 \angle 0^\circ$ V
V_{fault}^7	$50 \angle -30^\circ$ V

modification of the existing structure. Thus, the MSF algorithm is completely modular.

C. Performance Evaluation of the Decoupling Algorithms

In order to compare the performances of the two decoupling algorithms and to understand their underlying limitations, simulations have been performed for a type-E fault, [32], with a superimposed positive-sequence, seventh-harmonic voltage. The details of the fault are shown in Table I, expressed in terms of the actual voltage components. A zero-sequence voltage is also present in this type of fault, although it does not appear in the harmonic spectrum of $V_{\alpha\beta}$.

In this analysis, the reference frame transformations in both algorithms are performed assuming perfect phase angle estimation; this has been done to allow an analysis of the decoupling algorithms only, without the effect of the PLL dynamics. Without any loss of generality in the results, both algorithms have been implemented to estimate $V_{\alpha\beta}^{-1}$, $V_{\alpha\beta}^{-5}$, $V_{\alpha\beta}^7$, and $V_{\alpha\beta}^{-11}$. Fig. 5(a) shows the grid voltages during the fault, while Fig. 5(b) shows the amplitudes of $\hat{V}_{\alpha\beta}^{-1}$ according to the MDC and MSF algorithms. The MSF estimate is significantly slower than its MDC counterpart, both in the rise and settling times, due to its sixth-order filtering requirements. On the other hand, Fig. 5(c) shows the amplitudes of $\hat{V}_{\alpha\beta}^{-5}$; transient decoupling errors can be noticed for the MDC estimate, while the MSF estimate is far less sensitive, as a consequence of its strongly filtered nature; similar waveforms are also obtained for $\hat{V}_{\alpha\beta}^{-11}$. Finally, Fig. 5(d) shows the amplitudes of $\hat{V}_{\alpha\beta}^7$. Compared to $\hat{V}_{\alpha\beta}^{-1}$, the MSF estimate is significantly quicker, due to the fact that the LPF filter has a lower order and a higher cutoff frequency; nonetheless, the MDC estimate remains the quicker of the two. As expected, both algorithms estimate the harmonic components correctly at steady state.

From the above, it is evident that the MDC algorithm has a faster response compared to the MSF algorithm, however, it is more sensible to transient decoupling errors.

III. FAULT-DECOUPLED $\alpha\beta$ -PLL

The $\alpha\beta$ -PLL can easily incorporate any of the above decoupling algorithms, as shown in Fig. 6, resulting in a fault-decoupled $\alpha\beta$ -PLL. Here, $\hat{V}_{\alpha\beta\text{dec}}$ is subtracted from $V_{\alpha\beta}$, in order to obtain $\hat{V}_{\alpha\beta}^{-1}$, which constitutes the input to the PLL. The PLL can be tuned by applying small-signal analysis, [4]. If the decoupling algorithm's influence on the dynamics is sufficiently

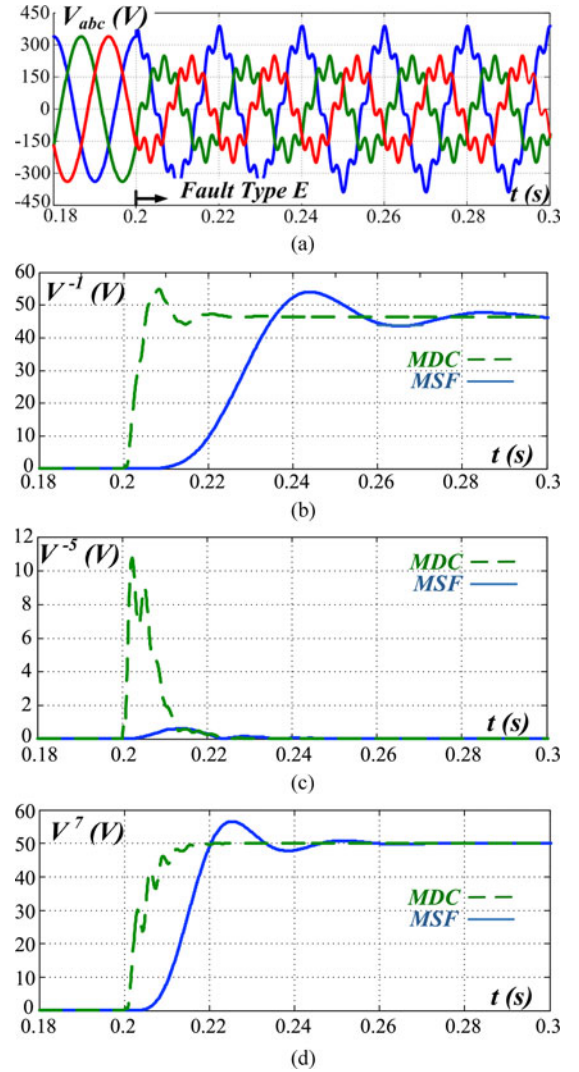


Fig. 5. Decoupling algorithm behavior following a type-E fault. (a) phase voltage waveforms. (b) Amplitude of $\hat{V}_{\alpha\beta}^{-1}$. (c) Amplitude of $\hat{V}_{\alpha\beta}^{-5}$. (d) Amplitude of $\hat{V}_{\alpha\beta}^7$.

small, this leads to the well-known closed loop transfer function between the estimated and input phase angles

$$\frac{\hat{\theta}^1}{\theta^1} = \frac{K_p s + K_i}{s^2 + K_p s + K_i}. \quad (2)$$

Equation (2) is a second-order transfer function with one zero and two poles. The PI regulator gains can be selected by performing classical root locus analysis.

In the $\alpha\beta$ -PLL that is used in this study, the only difference with respect to the PLLs shown in Figs. 1 and 2 is that the feedforward signal is summed at the output of the integral path of the PI regulator. This is done to obtain an “unenanced” frequency estimate $\hat{\omega}_{unenh}$ which is inherently more filtered than the “enhanced” frequency estimate $\hat{\omega}_{enh}$. This different filtering property is evident by comparing the closed loop transfer

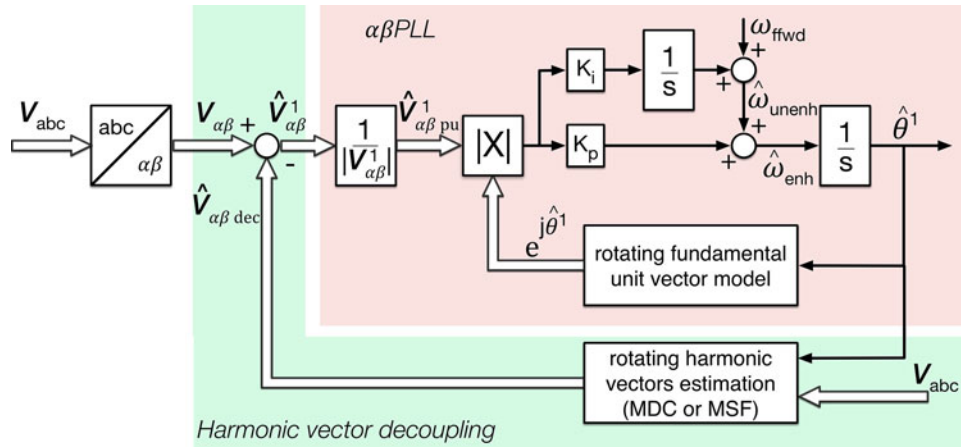


Fig. 6. General structure of a fault-decoupled $\alpha\beta$ -PLL.

functions between these estimates and the actual frequency

$$\frac{\hat{\omega}_{enh}}{\omega} = \frac{K_p s + K_i}{s^2 + K_p s + K_i} \quad (3)$$

$$\frac{\hat{\omega}_{unenh}}{\omega} = \frac{K_i}{s^2 + K_p s + K_i}. \quad (4)$$

Since (4) has no closed loop zero, it will have stronger high-frequency filtering properties than (3).

One important type of transient operation that should be used to validate the tuning of the PLL is the phase jump. This occurs frequently in the event of a fault due to modifications in the grid impedances. A simulation has been performed to show the performance of the PLL following a 30° phase jump. The PI gains have been set to $K_p = 304$ and $K_i = 19108$, i.e., the open-loop zero is placed at -10 Hz and the two closed loop poles are placed at -14 and -34 Hz on the real axis. In order to analyze the dynamic behaviors, PLLs with MDC decoupling (MDC-PLL), with MSF decoupling (MSF-PLL) and without decoupling have all been simulated. The algorithms decouple the same set of harmonics that was used in Section II-C. Fig. 7(a) shows a comparison of the phase angle estimation error; it can be seen that apart from residual errors introduced by the decoupling algorithms, the phase angle transient is quite similar for all three cases and converges rapidly. Fig. 7(b) shows the enhanced frequency estimates: in this case, the initial frequency step in all three estimates is very large; furthermore, decoupling errors cause significant oscillations on the estimates of both the MDC- and MSF-PLL, compared to the PLL without decoupling. Fig. 7(c) shows the unenhanced frequency estimates: here, it can be seen that the drop in the estimated frequency is much lower due to the previously described dynamic properties; furthermore, the transient is very similar for all three PLLs. This allows concluding that the unenhanced estimate should be preferred over the enhanced estimate and will be used in the rest of this paper for frequency estimation. Furthermore, these results prove that an initial tuning of the PLL can be performed without taking the decoupling structures into account.

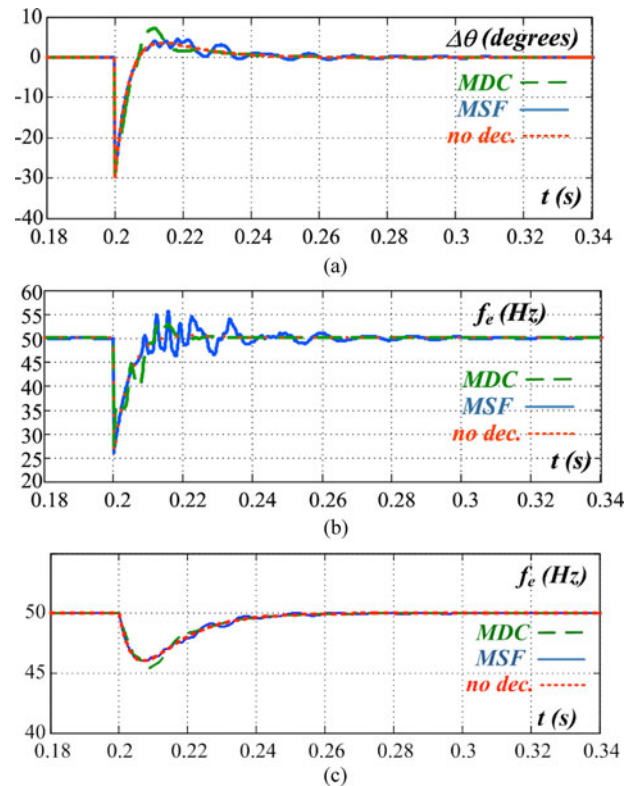


Fig. 7. Estimates following a 30° phase jump for the $\alpha\beta$ -PLL with MDC decoupling, MSF decoupling, and no decoupling. (a) Phase angle. (b) Enhanced frequency. (c) Unenhanced frequency.

IV. COMPARATIVE ANALYSIS

The MDC- and MSF-PLLs have been evaluated through simulation with MATLAB-Simulink. The comparative analysis that follows has been split into two sections for clarity. The first section shows the performances of the PLLs subjected to two consecutive faults. The second section shows the results of comparisons with two other state-of-the-art estimators, namely the MSOGI-FLL, [23], and the SOAP-PLL,

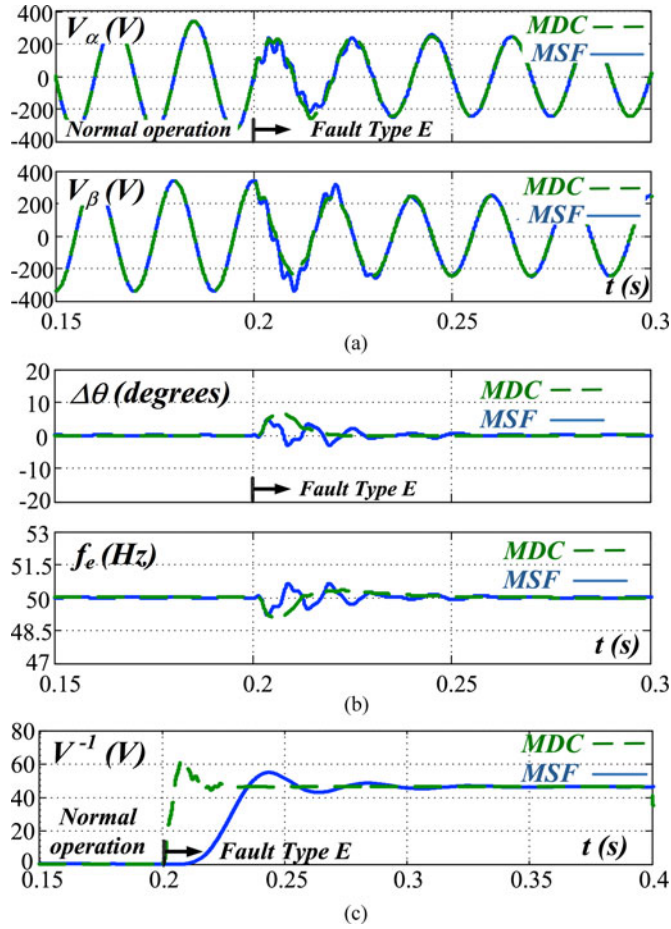


Fig. 8. Performance of the MDC- and MSF-PLLs during a type-E fault. (a) \hat{V}_α^{-1} and \hat{V}_β^{-1} components. (b) Phase angle estimation errors and frequency estimates. (c) Amplitude of $\hat{V}_{\alpha\beta}^{-1}$.

[21]. The MSOGI-FLL is taken as an example of an algorithm that is inherently able to estimate and decouple multiple harmonic components; conversely, the SOAP-PLL is taken as an example of an algorithm that is not inherently able to estimate multiple harmonics, but with appropriate in-the-loop filtering can effectively reduce the influence of the harmonic components on frequency and phase angle estimation. In order to allow a fair evaluation, the PI gains of the MDC- and MSF-PLLs have been set to the values used in [21] for all the simulations performed in this section, i.e., $K_p = 251.3$ and $K_i = 15791.4$; this corresponds to placing the open-loop zero at -10 Hz and the closed-loop poles coincident at -20 Hz on the real axis. The MSOGI-FLL is tuned as in [23].

A. Comparisons Between the MDC- and MSF-PLLs

The first fault that the PLLs are subjected to is an augmented version of a type-E fault described in Table I. This is a particular type of voltage sag that occurs in the event of a double line to ground fault. In addition, a seventh-harmonic component has been added during the fault. Fig. 8 shows the performance of the two PLLs during the fault. Fig. 8(a) shows the \hat{V}_α^{-1} and \hat{V}_β^{-1} com-

TABLE II
TYPE-F FAULT DETAILS

f_e	50 Hz
$V_{pre-fault}^1$	$340 \angle 0^\circ$ V
Zero-sequence voltage	0 V
V_{fault}^1	$193.14 \angle 0^\circ$ V
V_{fault}^{-1}	$73.14 \angle 180^\circ$ V
V_{fault}^{-5}	$20 \angle 45^\circ$ V
V_{fault}^{-7}	$50 \angle -30^\circ$ V

TABLE III
FAULT DETAILS

f_e	45 Hz
$V_{pre-fault}^1$	$340 \angle 0^\circ$ V
Zero-sequence voltage	0 V
V_{fault}^1	$170 \angle -30^\circ$ V
V_{fault}^{-1}	$85 \angle 110^\circ$ V
V_{fault}^{-5}	$102 \angle -10^\circ$ V
V_{fault}^{-7}	$68 \angle -0^\circ$ V
V_{fault}^{-11}	$68 \angle -0^\circ$ V

ponents of the decoupled voltage vector $\hat{V}_{\alpha\beta}^{-1}$. It can be seen that within about 1.5 cycles, the waveforms recover their sinusoidal shape, indicating that correct decoupling has been achieved for both PLLs. Fig. 8(b) shows the phase angle estimation errors and the frequency estimates. The maximum phase angle error is about 7° for the MDC-PLL and 5° for the MSF-PLL, while the fluctuations in the frequency estimates are at all times less than 1 Hz. Fig. 8(c) shows the estimated amplitudes of the fundamental harmonic, negative-sequence component. By comparing it with Fig. 5(b), it can be seen that the PLL dynamics cause a slight increase in the overshoot of the MDC-PLL estimate, but not of the MSF-PLL estimate.

The second fault is a type-F fault described in Table II. This fault is more demanding than the first, since the two faulty phase voltages undergo phase jumps in addition to a variation in their amplitudes. This causes the fundamental harmonic, negative sequence to be phase shifted by 180° with respect to the previous case. This fault type has been augmented as well with fifth- and seventh-harmonic components, as shown in Fig. 9(a). Fig. 9(b)–(d) shows the performance of the PLLs. With respect to the previous fault, the tracking performance is altered, especially for the MSF-PLL. Fig. 9(b) shows how \hat{V}_α^{-1} and \hat{V}_β^{-1} are strongly distorted during the transient, which this time lasts for a full two cycles. The phase angle and frequency estimation errors shown in Fig. 9(c) increase considerably due to the large decoupling errors shown in Fig. 9(d). However, the algorithm maintains correct tracking and converges to correct steady-state estimates. The MDC-PLL is evidently the quicker of the two to regain proper tracking, since it is able to estimate $\hat{V}_{\alpha\beta}^{-1}$ correctly in a shorter amount of time.

B. Comparison With State-of-the-Art Estimation Algorithms

The comparison between the two fault-decoupled PLLs and the MSOGI-FLL, and the SOAP-PLL has been performed on the basis of the fault conditions shown in Table III. This test is

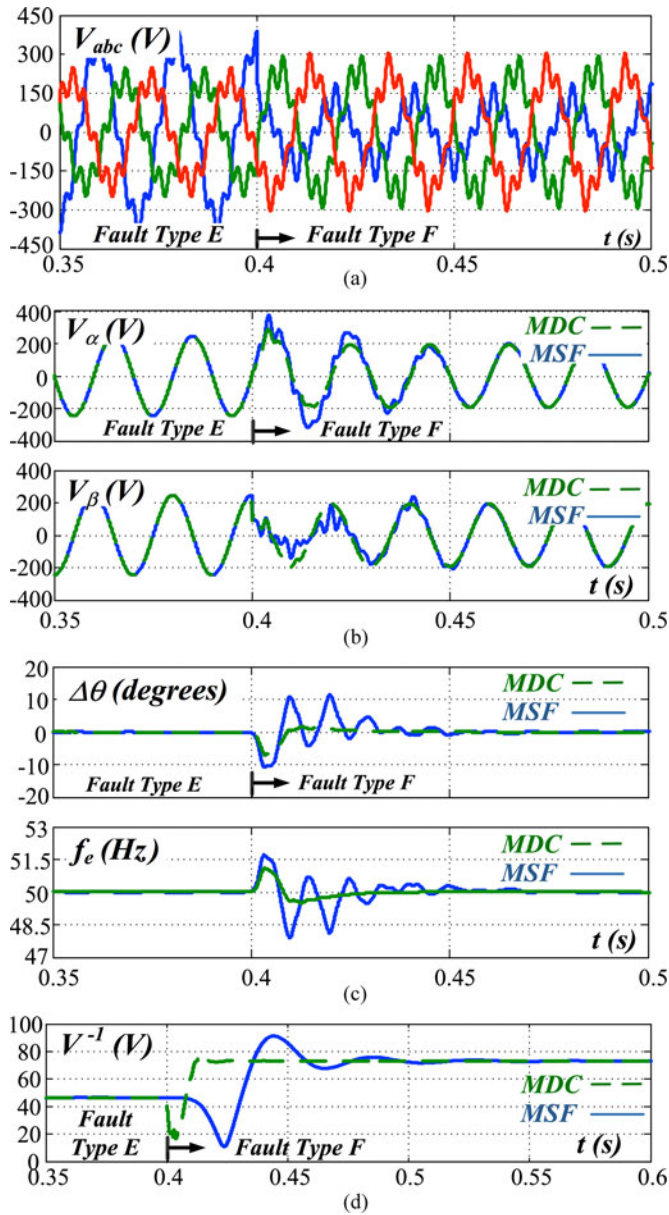


Fig. 9. Performance of the MDC- and MSF-PLLs during a type-F fault. (a) Phase voltage waveforms. (b) \hat{V}_α^{-1} and \hat{V}_β^{-1} components. (c) phase angle estimation errors and frequency estimates. (d) Amplitude of $\hat{V}_{\alpha,\beta}^{-1}$.

extremely demanding, since simultaneous frequency and phase jumps are present, together with fifth-, seventh-, and eleventh-harmonic components. The voltage waveforms are shown in Fig. 10(a). Fig. 10(b) shows the phase angle estimation errors for all the above algorithms during the fault. The MDC-PLL and MSOGI-FLL have similar transients; the MSF-PLL has a somewhat longer settling time, while the SOAP-PLL has the largest overshoots and a settling time similar to the MSF-PLL. At steady state, the MSOGI-FLL, MSF-PLL, and MDC-PLLs all have practically zero estimation error, while the SOAP-PLL has residual ripple. Fig. 10(c) shows the estimated frequency for the four algorithms. The MDC-PLL has the quickest response; the other three algorithms require about two cycles to reach

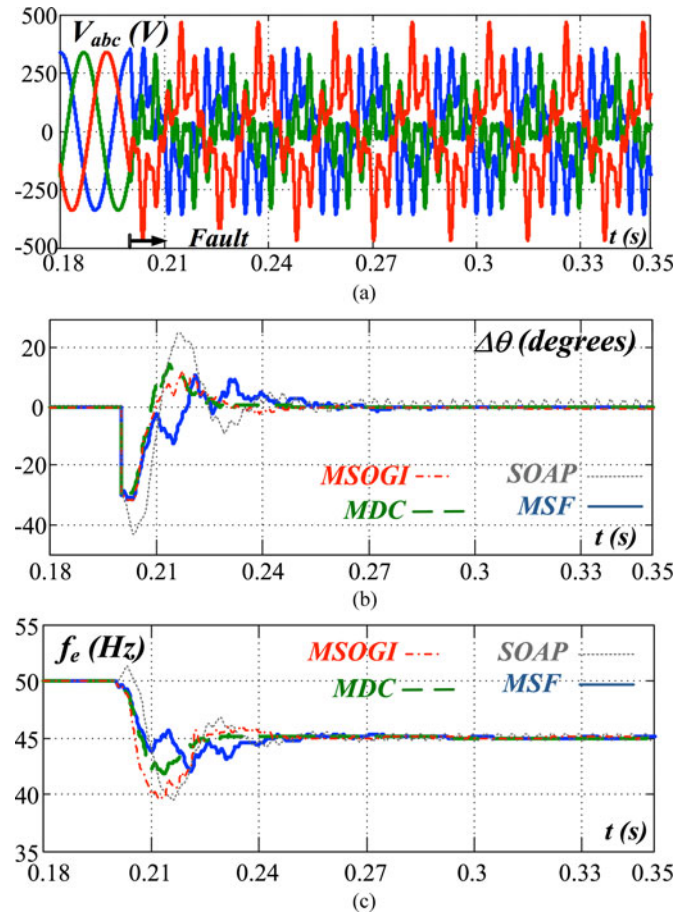


Fig. 10. Performance comparison between MDC-PLL, MSF-PLL, MSOGI-FLL, and SOAP-PLL. (a) Phase voltage waveforms. (b) Phase angle estimation errors. (c) Frequency estimates.

steady state. The MSOGI-FLL and SOAP-PLL have larger frequency errors compared to the MDC- and MSF-PLLs.

Fig. 11 shows the estimated amplitudes of the harmonic components, only for the three algorithms that perform these calculations. The transients are highly distorted, but the main characteristics of the MDC- and MSF-PLLs are confirmed: the former is faster but subjected to higher decoupling errors, while the latter is slower, leading to more filtered estimates. The MSOGI-FLL has a somewhat intermediate dynamic response.

C. Digital Implementation

The two fault-decoupled PLLs have been implemented digitally on a 32-bit, floating point, 150-MHz TI Delfino F28335. Fig. 12 shows the block diagram of the digital implementation. A 10-kHz sampling frequency was chosen and the PI parameters were calculated in order to be consistent with the above simulations. The s-domain zeros and poles were mapped to the z-domain according to $z = e^{sT_s}$, with T_s being the sampling time. Thus, the s-domain open-loop zero at -10 Hz maps to $z = 0.9937$ and the two coincident s-domain closed-loop poles at -20 Hz map to $z = 0.9875$. To achieve this, the PI gains are set to $K_p = 249$ and $K_i = 15692.5$. By comparing these gains with

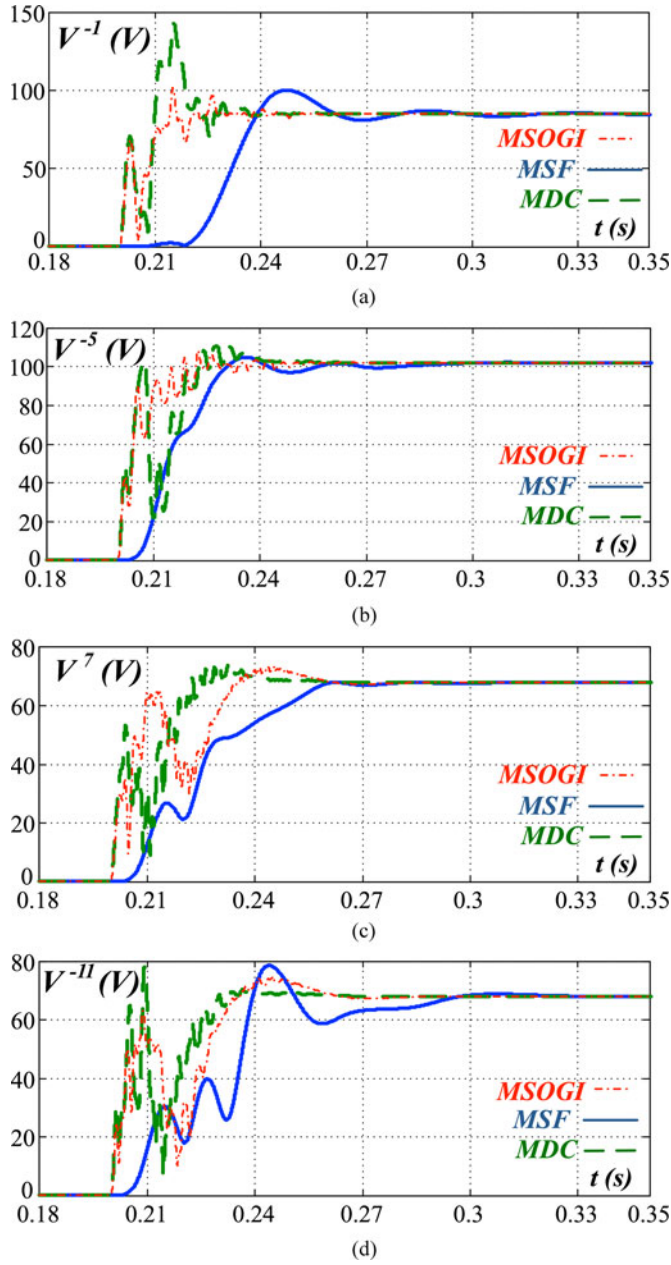


Fig. 11. Performance comparison between MDC-PLL, MSF-PLL, MSOGI-PLL: (a) Amplitude of $\hat{V}_{\alpha\beta}^{-1}$. (b) Amplitude of $\hat{V}_{\alpha\beta}^{-5}$. (c) Amplitude of $\hat{V}_{\alpha\beta}^{-7}$. (d) Amplitude of $\hat{V}_{\alpha\beta}^{-11}$.

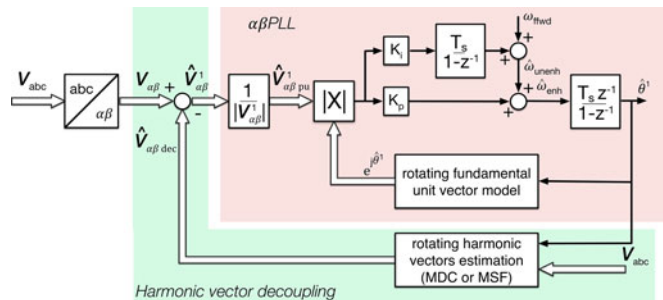


Fig. 12. Digital implementation of the fault-decoupled $\alpha\beta$ -PLL.

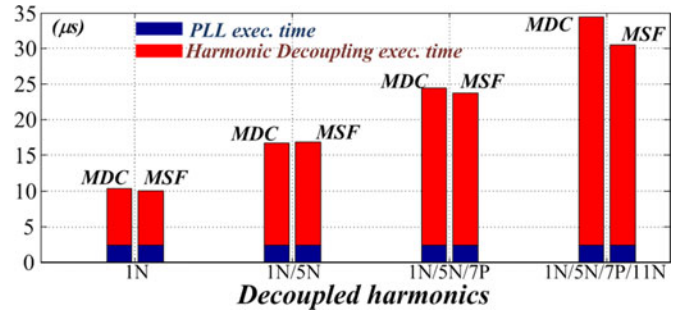


Fig. 13. Execution times of the MDC-PLL and MSF-PLL as a function of the number of decoupled harmonics

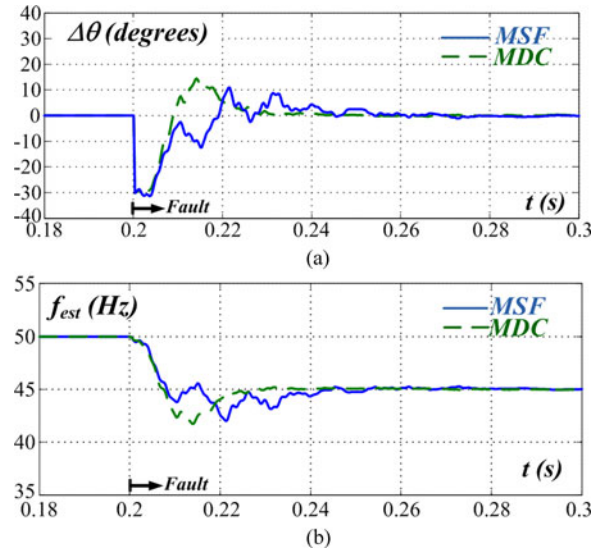


Fig. 14. Digital implementation of MDC-PLL and MSF-PLL. (a) Phase angle estimation error. (b) Unenhanced frequency estimates.

the s -domain counterparts given at the beginning of Section IV, it can be seen that they are very similar. Thus, as long as the sampling frequency is sufficiently high, it is also possible to use the s -domain gains without affecting the dynamic performance of the PLL significantly.

The PLLs were coded in C. The execution time required by the MDC-PLL and MSF-PLL depends on the number of decoupled harmonics. This is shown in Fig. 13 and is equal to the sum of the execution time required by the $\alpha\beta$ -PLL and by the harmonic decoupling. The first contribution, in blue, is constant and equal to $2.4 \mu\text{s}$, while the second contribution, in red, depends on the algorithm. As the number of decoupled harmonics increases, the MDC-PLL requires progressively more total execution time due to the higher degree of complexity of the algorithm: for instance, in case of four decoupled harmonics, the total execution time is equal to $30.6 \mu\text{s}$ for the MSF-PLL and $34.5 \mu\text{s}$ for the MDC-PLL. For a larger amount of decoupled harmonics, this difference will increase even further. It should be stated that no optimization of the code was used, except for the use of look-up tables for the trigonometric functions. It is expected that, by using processor-specific code optimization, the

execution times of the harmonic decoupling strategies should decrease considerably. Nonetheless, the present implementations of both algorithms are sufficiently fast to be implemented within the control systems of modern grid-connected inverters with PWM switching frequencies up to 15 kHz.

Both algorithms were tested for the fault case of Table III. Fig. 14(a) shows the unenhanced frequency estimation, while Fig. 14(b) shows the phase angle estimation error. No appreciable difference in behavior is visible with respect to the simulation results shown in Fig. 10.

V. CONCLUSION

This contribution has introduced a general approach to harmonic decoupling in PLLs for grid-connected inverters and has presented a highly intuitive and simple scheme, applying it to an $\alpha\beta$ -PLL. Two implementations of this decoupling scheme have been described: the MDC algorithm and the MSF algorithm. Key conclusions can be summarized as follows:

- 1) The MDC algorithm requires less filtering, is quicker than the MSF algorithm, but it is not modular;
- 2) The MSF algorithm relies on heavy filtering, thus is slower; on the other hand it is modular;
- 3) as long as the decoupling algorithm's influence on the dynamics is sufficiently small, fault-decoupled PLLs can be easily tuned by using (2)-(4);
- 4) simulations have allowed to evaluate the performances of the fault-decoupled PLLs and it has been shown that they are comparable to those of other advanced frequency and phase angle estimation structures;
- 5) digital implementation on a 32-bit floating point microcontroller has shown that the MDC-PLL requires progressively more total execution time compared to the MSF-PLL as the number of decoupled harmonics increases. However, both algorithms are sufficiently fast to be implemented within the control system of modern grid-connected inverters.

REFERENCES

- [1] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 654–664, Mar. 2009.
- [2] *Reference Technical Rules for the Connection of Active and Passive Users to the LV Electrical Utilities*, CEI-0-21 Standard, Dec. 2013.
- [3] X. Guo, X. Zhang, B. Wang, W. Wu, and J. M. Guerrero, "Asymmetrical grid fault ride-through strategy of three-phase grid-connected inverter considering network impedance impact in low-voltage grid," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1064–1068, Mar. 2014.
- [4] F. M. Gardner, *Phase-lock Techniques*, 3rd ed. New York, NY, USA: Wiley, 2005.
- [5] A. J. Viterbi, "Acquisition and tracking behavior of phase-locked loops," in *Proc. Symp. Active Networks Feedback Syst.*, Apr. 1960, pp. 583–619.
- [6] V. Kaura and V. Blasko, "Operation of phase locked loop system under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 58–63, Jan./Feb. 1997.
- [7] S.-K. Chung, "A phase tracking system for three phase utility interface inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 431–438, May 2000.
- [8] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584–592, Mar. 2007.
- [9] P. Xiao, K. A. Corzine, and G. K. Venayagamoorthy, "Multiple reference frame-based control of three-phase PWM boost rectifiers under unbalanced and distorted input conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2006–2017, Jul. 2008.
- [10] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "A new hybrid PLL for interconnecting renewable energy systems to the grid," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2709–2719, Nov./Dec. 2013.
- [11] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "Synchronization of grid-connected renewable energy sources under highly distorted voltages and unbalanced grid faults," in *Proc. IEEE 39th Annu. Conf. Ind. Electron. Soc.*, Nov. 2013, pp. 1887–1892.
- [12] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "An adaptive phase-locked loop algorithm for faster fault ride through performance of inter-connected renewable energy sources," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 2619–2626.
- [13] P. Rodriguez, R. Teodorescu, I. Candela, A.V. Timbus, M. Liserre, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–7.
- [14] E. Robles, S. Ceballos, J. Pou, J. L. Martin, J. Zaragoza, and P. Ibanez, "Variable-frequency grid-sequence detector based on a quasi-ideal low-pass filter stage and a phase locked loop," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2552–2563, Oct. 2010.
- [15] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194–1204, Apr. 2011.
- [16] C. Blanco, D. Reigosa, F. Briz, J. M. Guerrero, and P. Garcia, "Grid synchronization of three-phase converters using cascaded complex vector filter PLL" in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2012, pp. 196–203.
- [17] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 765–778, Feb. 2013.
- [18] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Performance improvement of a prefiltered synchronous-reference-frame PLL by using a PID-type loop filter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3469–3479, Jul. 2014.
- [19] F. A. S. Neves, H. E. P. de Souza, M. C. Cavalcanti, F. Bradaschia, and E. J. Bueno, "Digital filters for fast harmonic sequence component separation of unbalanced and distorted three-phase signals," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3847–3859, Oct. 2012.
- [20] C. Blanco, D. Reigosa, F. Briz, and J.M. Guerrero, "Synchronization in highly distorted three-phase grids using selective notch filters" in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 2641–2648.
- [21] Y. Park, S.-K. Sul, W.-C. Kim, and H.-Y. Lee, "Phase-locked loop based on an observer for grid synchronization," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1256–1265, Mar./Apr. 2014.
- [22] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750–2763, Jun. 2014.
- [23] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2011.
- [24] D. Yazdani, M. Mojiri, A. Bakhshai, and G. Joos, "A fast and accurate synchronization technique for extraction of symmetrical components," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 674–683, Mar. 2009.
- [25] M. Karimi-Ghartemani, S. A. Khajehodini, P. K. Jain, and A. Bakhshai, "Problems of startup and phase jumps in PLL systems," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1830–1838, Apr. 2012.
- [26] M. Karimi-Ghartemani, "Linear and pseudolinear enhanced phase-locked loop (EPLL) structures," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1464–1474, Mar. 2014.
- [27] P. Mattavelli, "A closed-loop selective harmonic compensation for active filters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 1, pp. 81–89, Jan./Feb. 2001.
- [28] M. J. Newman, D. N. Zmood, and D.G. Holmes, "Stationary frame harmonic reference generation for active filter systems," *IEEE Trans. Ind. Appl.*, vol. 38, no. 6, pp. 1591–1599, Nov./Dec. 2002.
- [29] V. M. Moreno, M. Liserre, A. Pigazo, and A. Dell'Aquila, "A comparative analysis of real time algorithms for power signal decomposition in multiple

synchronous reference frames," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1280–1289, Jul. 2007.

- [30] M. Cacciato, G. Scarcella, G. Scelba, and L. Finocchiaro, "Multi-reference frame based PLL for single phase systems in voltage distorted grids" in *Proc. 16th Eur. Conf. Power Electron. Appl.*, Sep. 2014, pp. 1–8.
- [31] G. Scelba, G. De Donato, G. Scarcella, F. Giulii Capponi, and F. Bonaccorso, "Fault tolerant rotor position and velocity estimation using binary Hall-effect sensors for low cost vector control drives," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 1629–1636, Sep./Oct. 2014.
- [32] M. H. J. Bollen and I. Y. H. Gu, *Signal Processing of Power Quality Disturbances*, 1st ed. New York, NY, USA: Wiley, 2006.



Giulio De Donato (S'05, M'08) was born in Cork, Ireland, in 1978. He received the M.S. and Ph.D. degrees in electrical engineering from the University of Rome "La Sapienza," Rome, Italy, in 2003 and 2007, respectively.

He was a Research Associate with the Department of Electrical Engineering, University of Rome "La Sapienza," from 2007 to 2008; from 2008 to 2010 he was an Assistant Professor with the same Department and, since 2010, he has held the same position with the Department of Astronautical, Electrical and

Energetic Engineering. His current research interests include digital control of brushless drives and analysis and design of permanent magnet machines.

Prof. De Donato is a Registered Professional Engineer in Italy and is a Member of the IEEE Industry Applications, the IEEE Industrial Electronics, and the IEEE Power Electronics Societies. He is a Member of the IEEE IAS Industrial Drives Committee, IAS Electric Machines Committee and IES Electrical Machines Committee. He received the 2014 First Prize Paper Award from the IAS Industrial Drives Committee.



Giacomo Scelba (S'04, M'07) received the M.S. and Ph.D. degrees in electrical engineering from the University of Catania, Catania, Italy, in 2002 and 2005, respectively.

In 2004, he was a Visiting Student at Rockwell Automation Standard Drives Development, Mayfield Heights, OH, USA. He is currently an Assistant Professor at the Department of Electrical, Electronic and Computer Engineering, University of Catania. His current research interests include sensorless control, digital signal processing, ac drive control technologies, fault tolerant control solutions devoted to multiphase and multidrive AC systems, and control techniques for renewable energy systems.

Prof. Scelba is a Registered Professional Engineer in Italy and is a Member of the IEEE Industry Applications, the IEEE Industrial Electronics and the IEEE Power Electronics Societies. He received the 2014 First Prize Paper Award from the IAS Industrial Drives Committee.



Gabriele Borocci (S'11–M'14) was born in Rome, Italy, in 1987. He received the B.S and M.S. degrees in electrical engineering, in 2009 and 2012, respectively, from the University of Rome "La Sapienza," Rome, Italy, where he is currently working toward the Ph.D. degree in Electrical Engineering.

His research interests include advanced control of electrical drives, power electronics, and optimization of electrical drives for energy savings.

Mr. Borocci is a Registered Professional Engineer in Italy and a Member of the IEEE Industry

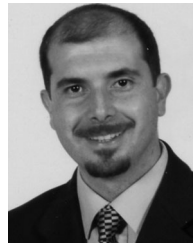
Applications Society.



Fabio Giulii Capponi (M'98) received the M.S. and Ph.D. degrees in electrical engineering from the University of Rome "La Sapienza," Rome, Italy, in 1994 and 1998, respectively.

From 1996 to 2010, he was with the Department of Electrical Engineering, University of Rome "La Sapienza," and, since 2010, he has been with the Department of Astronautical, Electrical and Energetic Engineering as an Assistant Professor. During 2003 and 2004, he was a Visiting Scholar at the Wisconsin Electrical Machines and Power Electronics Consortium, University of Wisconsin, MD, USA. He is author or coauthor of more than 60 technical published papers. His current research interests include permanent magnet motor drives and digital control systems design for unconventional power converter topologies.

Prof. Capponi is a Registered Professional Engineer in Italy and is Member of the IEEE Industry Applications, the IEEE Industrial Electronics, and the IEEE Power Electronics Societies. He is a Member of the IEEE IAS Industrial Drives Committee, Electric Machines Committee, and Transportation Systems Committee. He received the 2014 First Prize Paper Award from the IAS Industrial Drives Committee. He is currently serving as an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS.



Giuseppe Scarcella (S'98, M'99) received the M.S. and Ph.D. degrees in electrical engineering from the University of Catania, Catania, Italy, in 1995 and 1999, respectively.

In 1995, he received an SGS Thomson (now ST Microelectronics) Research Grant. In 1998, he spent a period at the University of Wisconsin, MD, USA, working on "sensorless control of electrical drives." In 1999, he joined the Department of Electrical, Electronic, and Systems Engineering, University of Catania, as a Temporary Researcher. In 2001, he obtained a permanent position as Assistant Professor, in the same department, where, since 2005, he has been an Associate Professor in the areas of power electronics, electrical machines and drives. He is the author of more than 130 technical papers published on journals and proceedings of national and international conferences and holds several international patents. His current research interests include sensorless control of electrical machines, advanced control, digital modulation techniques, efficiency optimization techniques, and electromagnetic compatibility.

Prof. Scarcella is a Member of the IEEE Industry Applications Society. He received the 1998 Third Prize Paper Award and the 2014 First Prize Paper Award from the IAS Industrial Drives Committee, and the IEEE TRANSACTIONS ON POWER ELECTRONICS Best Paper Award in 2000. He is currently serving as an Associate Editor in IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS.