Electrothermal Multiscale Modeling and Simulation Concepts for Power Electronics

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***Abstract*—This paper presents a finite-element-based simulation methodology to improve on multiscale modeling and analysis limitations of power electronics development. The method utilizes homogenization and nonmatching grid concepts to offer a high degree of flexibility and reduce computational effort. The applied homogenization method provides effective material properties to realize full-chip modeling performance without the need to model geometric details. The concept of nonmatching grids allows the inclusion of a subregion with substantially finer mesh than its surrounding regions. This allows the flexible integration of micrometer scale geometries with a high degree of detail within the full-chip model. Both concepts are thoroughly introduced and an application to a state-of-the-art power electronics semiconductor technology is presented. This paper focuses on electrothermal interaction and is experimentally verified on a dedicated test structure. The presented results provide electrothermal insights in current power electronic technologies and emphasize their potential to further improve the robustness and reliability of next generation technologies.**

***Index Terms*—Electrothermal effects, finite-element (FE) methods, heat transfer, multiscale modeling, power semiconductor devices, thermal characterization.**

I. Introduction

In the past, the minimum chip area of power semiconductor devices was mainly determined by on-resistance and current transport requirements. Today's power electronic technologies, however, are primarily limited by thermal management. Over the last decades, continues advances in process technologies, consecutive shrinking of transistor features as well as the integration of additional digital logic (e.g., protective circuit concepts) lead to very high power densities. Even though state-of-the-art silicon technologies can operate at extreme power densities of more than $1300\ \mathrm{W \cdot mm^{-1}}$ [1], the resulting peak temperatures and large temperature gradients are posing enormous design challenges. It is well understood in the literature that thermally triggered stress events are the driving forces regarding device robustness and reliability [2]–[4]. Peak junction temperature is the dominant parameter triggering thermal destructive events, thus defining the device's robustness [5]. Temperature distribution and in particular temperature gradients in the device's multimaterial stack are identified as one of the root causes for fatigue phenomena [6], limiting the device's lifetime performance [7], [8].

Consequently, the performance of experimental and numerical thermal characterization methods are a key factor to improve and optimize the design of technology, device structure, and circuitry. Supported by accurate geometric information as well as measured material parameters available from the fabrication process, numerical characterization methods can provided detailed three-dimensional (3D) temperature distribution and heat flow analysis with high accuracy [9]. Even though finite element (FE) simulations are widely utilized to study heat-transfer problems in power electronics, existing modeling and simulation approaches are limited by the multiscale nature of modern power semiconductors. This is exemplarily shown in Fig. 1 for a contemporary trench metal oxide semiconductor field effect transistor (MOSFET) semiconductor technology.

For a thermal analysis of such a technology, some details are negligible. The thermal impact of very thin silicon dioxide layers [e.g., gate oxides visible in the trench structure of Fig. 1(c)] or various barrier layers (e.g., about 20-nm thick titanium diffusion barriers) is minute. Including these simplification to the model, the smallest layer dimensions of the thermally relevant structures are in the order of 10^{-7} m. The silicon die is usually enclosed in plastic package and glued or soldered to a printed circuit board (PCB). Typical dimensions of the latter are in the range of 10^{-2} m. The presence of five orders of magnitude of relevant thermal details inhibits an effective analysis.

In addition, scale separation is found in high aspect-ratio layers. For instance, the top metallization of a power semiconductor typically features a layer spawning of the entire active area (i.e., one or few $\mathrm{mm^2}$) while measuring only few micrometer in thickness. The adequate 3D modeling of the unit cell shown in Fig. 1(c) (cube with a side length of about $6.2\ \mu\mathrm{m}$) requires around 100 000 FEs according to [10]. A typical power device consists of several thousands of single transistor cells, thus a simulation of the entire power device exceeds even today's advanced computer capabilities. The standard FE method is, therefore, a nonoptimal choice for analyzing multiscale problems.

In the literature, a typical approach to overcome multiscale limitations is to simplify complex layer structures, for example, by means of compact or lumped models [11]–[13]. Lumped

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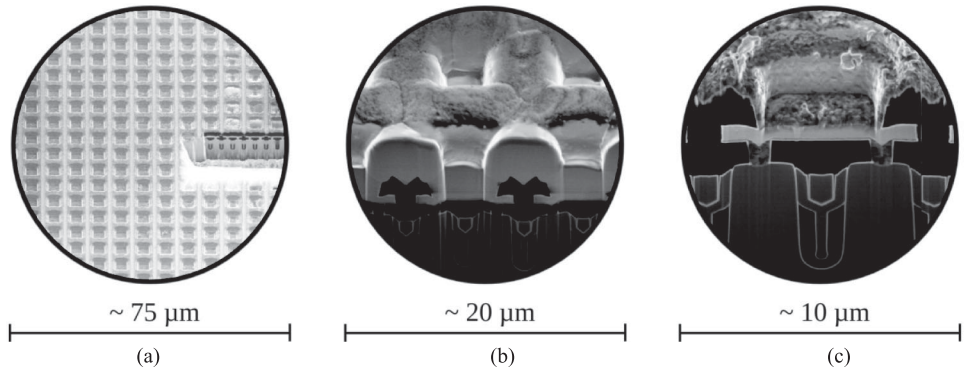

Fig. 1. Three FIB images at different scales demonstrating the periodic (a) yet heterogeneous (b), (c) structure of a state-of-the-art trench MOSFET technology.

models can be used to approximate the spatial dependences of the problem as an equivalent thermal resistor-capacitor (RC) network [14]–[17]. Each RC section represents a spherical heat conduction path and approximates the thermal impedance. The geometry is then represented by the connectivity of the approximated thermal impedance. In order to improve spatial details, advanced simulation concepts use, e.g., finite difference method (FDM) or finite volume method (FVM) to discretize regions of interest and model them with traditional equivalent thermal networks or Fourier series thermal models. Dedicated simulation examples applied to electrothermal power electronics applications are [18]–[22]. The research field of effective, yet accurate modeling is very active, demonstrating the inherit difficulty of trading-off simulation time and accuracy. Recently, Evans *et al.*, applied concepts of *model order reduction* to FDM methods [23].

Notwithstanding the good results of existing, sophisticated compact modeling methods, an accurate FE modeling approach is a prerequisite for thermomechanical reliability investigations where the full spatial distribution of the temperature field is required (e.g., [24]). In this paper, an finite element-based electrothermal simulation approach is presented to overcome current limitations of the classical FE method. The implementation of homogenization methods in combination with nonmatching grid concepts provide full-chip temperature distribution with high spatial resolution for selected regions.

Homogenization: Homogenization methods provide effective (i.e., spatially or temporally averaged) material properties for regions with complex heterogeneous structures. The methods have primarily been advanced by material researchers [25], especially in the domain of composite engineering and advanced alloys. In this field, the macroscopic response of a material highly depends on its microscopic composition and orientation. Current homogenization research focuses mainly on multiphysics (i.e., thermomechanical, electrothermal, piezoelectric) problems as well as higher order homogenization concepts [26], [27]. These paradigms are more and more applied to a wide range of engineering disciplines. Mu *et al.*, used an iterative FE approach to calculate effective parameters of core-loss in complicated magnetic structures [28]. *System-level* simulations (e.g., hybrid power systems [29]) heavily rely on meaningful averaging to bring down simulation time. Our focus lies within aiding the development of high-power semiconductor devices and their effective thermal analysis. Power electronic devices often consist of parallel transistor cells, which give rise to periodic structures. The approach presented in this paper is specifically designed to use these periodicities for the calculation of effective material parameters.

Nonmatching grids: Nonmatching grid methods remove the strong requirement of compatible elements in the standard FE method and allow incompatible meshes on the subdomain boundaries. By meshing the subdomains independently, the flexibility of finding the optimal discretization in each of them is increased. In regions of broken periodicity, e.g., a sensor structure interrupting the periodic arrangement of transistor cells, homogenized results can vastly differ from reality [30]. In addition, once a microscopic structure is replaced by an averaged layer, the local information cannot easily be retrieved unless more sophisticated methods are applied (e.g., [25]). The approach presented in this paper supports full-chip multiphysics simulations of power electronics devices. It provides detailed temperature distribution and heat flow results of heterogeneous regions of interest. For example, known point-of-failure locations can be modeled in great detail and directly embedded in a full-chip simulation.

This paper is organized as follows: Background and theory to the electrothermal FE formulation are outlined in Section II. Next, the applied homogenization scheme is described in the first part of Section III. The second part of Section III provides details on the nonmatching grid technique. In Section IV, the two concepts are applied to the modeling of a power electronics test device in order to support an experimental validation. It includes a description of the test device and its multiscale properties as well as details on sensor calibration and FE model boundary conditions (BCs). Section V shows a comparison of experimental and simulated results. Finally, we conclude by summarizing the results and suggesting future applications.

II. Background and Theory

A. Physical Equations

The governing physical equations describing the thermal and electrical behavior are the *heat equation*

$$\rho c \frac{\partial T}{\partial t} - \nabla \cdot (\lambda \nabla T) = p_{\mathrm{V}} \tag{1}$$

the *charge continuity equation* in matter

$$\begin{aligned} \nabla \cdot \vec{j} &= 0 \\ \nabla \cdot (\gamma \nabla \phi) &= 0 \end{aligned} \tag{2}$$

and their corresponding initial and BCs. In (1), ρ is the density, c is the specific heat capacity, λ is the thermal conductivity, and T the temperature. Furthermore, pv represents the thermal power density, or heat generation rate per unit volume. In (2), $\vec{j}$ is the current density, γ is the electric conductivity, and ϕ is the electric potential. Note that we assume that the displacement current density $\vec{j}_D$ caused by polarization of bound charges in the dielectric can be neglected in our application. The temperature-dependent material parameters are ρ, c, λ, and γ. In addition, the conductivities λ and γ may depended on the direction of the flux ($\vec{q} = \tilde{\lambda} \nabla T$ or $\vec{j} = \tilde{\gamma} \nabla \phi$, respectively). In this case, a tilde (e.g., $\tilde{\lambda}$) distinguishes between anisotropic tensorial material parameters and scalar material parameters. The two equations are coupled by means of joule heating

$$\begin{aligned} p_V &= \vec{E} \cdot \vec{j} \\ &= (\nabla \phi) \cdot (\gamma \nabla \phi) \end{aligned} \tag{3}$$

where $\vec{E}$ is the irrotational electric field. The Dirichlet (essential or first-type) and Neumann (natural or second-type) BC for the heat equation are

$$T = T_e \text{ on } \Gamma_e \quad \text{and} \quad \lambda \frac{\partial T}{\partial \vec{n}} = \vec{q}_{\mathrm{n}} \text{ on } \Gamma_n. \tag{4}$$

A Dirichlet BC imposes the temperature T on the boundary Γ_e. A Neumann BC prescribes the heat flux $\vec{q}_n$ through the surface Γ_n with normal vector $\vec{n}$. This allows the inclusion of convective and radiative boundary conditions. The electrical boundary conditions are

$$\phi = \phi_e \text{ on } \Gamma_e \quad \text{and} \quad \gamma \frac{\partial \phi}{\partial \vec{n}} = \vec{j}_n \text{ on } \Gamma_n \tag{5}$$

used to impose the electric potential ϕ and current density $\vec{j}_n$, respectively.

B. Electrothermal FE formulation

The solution of the boundary-value problem by means of the FE method requires the transformation of the partial differential equations (1) and (2) and their BCs into the weak (variational) form.

These steps involve the multiplication with a suitable test function ω, integrating over the computational domain Ω and applying *Green's* integral theorem. For clarity, only the variational formulation of the heat equation (1) is shown for the case of homogeneous *Neumann* BCs, i.e., $\partial\Omega = \Gamma_n$ and $\vec{q}_n = 0$

$$\int_\Omega \omega \left(\rho c \frac{\partial T}{\partial t} \right) \mathrm{d}\Omega + \int_\Omega \lambda (\nabla \omega) \cdot \nabla T \, \mathrm{d}\Omega - \int_\Omega \omega p_V \, \mathrm{d}\Omega = 0. \tag{6}$$

The aforementioned equation can be discretized by the *Galerkin* method, in which the domain Ω is approximated by a mesh or discretization $\mathcal{T}_h$ with characteristic length scale h. Furthermore, $\omega \approx \omega^h$ and $T \approx T^h$ are approximated with piecewise polynomial functions defined on the elements of the mesh.

The resulting algebraic system of equations for (1) and (2) obtained after spatial and time discretization can be expressed in matrix form

$$\mathbf{M}(\underline{T}_{n+1}) \, \dot{\underline{T}}_{n+1} + \mathbf{K}^T(\underline{T}_{n+1}) \, \underline{T}_{n+1} = \underline{f}(\underline{\phi}_{n+1}, \underline{T}_{n+1}) \tag{7}$$

$$\mathbf{K}^\phi(\underline{T}_{n+1}) \, \underline{\phi}_{n+1} = \underline{g}_{n+1} \tag{8}$$

where $\mathbf{M}$ is the mass matrix, $\underline{f}_{n+1}$ is the load vector resulting from the last term in (6) and n denotes the time step counter. $\mathbf{K}^T$ and $\mathbf{K}^\phi$ are the stiffness matrices for the thermal and electrical problem, and $\underline{g}_{n+1}$ is the right-hand side of the electric problem due to the boundary conditions of (5). $\dot{\underline{T}}_{n+1}$, $\underline{T}_{n+1}$ and $\underline{\phi}_{n+1}$ are the algebraic vectors of the time derivative of temperature, the temperature itself and the electric potential defined on the nodes of the mesh. Time integration is performed with the backward Euler scheme [31]. Further details including a step-by-step derivation are outlined in [31]–[33].

For linear material parameters ρ, c, λ, and γ, i.e., no temperature dependence, the solution strategy for each time step i is simply as follows:

1) solve (8) with appropriate boundary and initial conditions;
2) calculate the joule heating term $\underline{f}_{n+1}$ using (3);
3) solve (7) using $\underline{f}_{n+1}$ with appropriate boundary and initial conditions.

In the case of temperature-dependent material parameters $\rho(T)$, $c(T)$, $\lambda(T)$, and $\gamma(T)$, an iterative solution scheme has to be applied as displayed in Fig. 2. Thereby, the inner iteration counter k for solving the nonlinear heat equation and the outer iteration counter i to control the overall convergence between the electrical and thermal equation is introduced. For each time step n, the following iterative solution scheme is performed:

1) Solve the *inhomogeneous* electric conduction (8) with given temperature $\underline{T}^i_{n+1}$ ($\underline{T}^0_{n+1} = \underline{T}_n$) to evaluate the electric conductivity $\gamma(T)$. As a result, we obtain the electric potential ϕ^i_{n+1}.
2) Calculate the temperature-dependent joule heating term $\underline{f}^i_{n+1}(\underline{\phi}^i_{n+1}, \underline{T}^i_{n+1})$ using (3).
3) Set $\underline{T}^k_{n+1} = T^i_{n+1}$ and iteratively solve the *nonlinear* heat equation (7)

$$\mathbf{M}(\underline{T}^k_{n+1}) \dot{\underline{T}}^{k+1}_{n+1} + \mathbf{K}^T(\underline{T}^k_{n+1}) \underline{T}^{k+1}_{n+1} = \underline{f}^k_{n+1}(\underline{\phi}^i_{n+1}, \underline{T}^k_{n+1}). \tag{9}$$

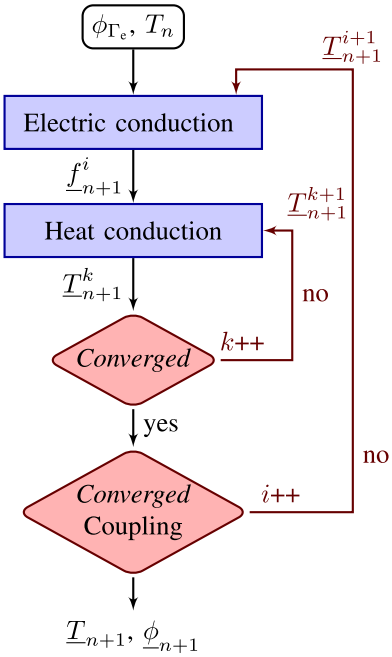

Fig. 2. Iterative convergence strategy for the coupled electrothermal problem for a single time step n. The load vector $\underline{f}^{i}_{n+1}$ of the nonlinear heat equation is calculated from the power density of the electric conduction. The inner iteration (k) is a *Fix-point* method for the nonlinear thermal problem. The outer iteration (i) ensures the convergence of the coupled problem.

For the convergence of the nonlinear heat equation, an incremental stopping criterion for the temperature

$$\frac{\left\|\underline{T}^{k+1}_{n+1} - \underline{T}^{k}_{n+1}\right\|_2}{\left\|\underline{T}^{k+1}_{n+1}\right\|_2} < 10^{-3} \tag{10}$$

and a residual-based stopping criterion

$$\frac{\left\|\underline{f}^{k+1}_{n+1} - \mathbf{M}(\underline{T}^{k+1}_{n+1})\dot{\underline{T}}^{k+1}_{n+1} - \mathbf{K}^{T}(\underline{T}^{k+1}_{n+1})\underline{T}^{k+1}_{n+1}\right\|_2}{\left\|\underline{f}^{k+1}_{n+1}\right\|_2} < 10^{-3} \tag{11}$$

is applied. Here, $\|\cdot\|_2$ is the L_2-norm and k the iteration counter. After convergence, we obtain $\underline{T}^{k+1}_{n+1}$.

4) Check for the convergence of the coupled systems, which is based on the change of the joule heating term between two subsequent outer iterations

$$\frac{\left\|\underline{f}^{i+1}_{n+1} - \underline{f}^{i}_{n+1}\right\|_2}{\left\|\underline{f}^{i+1}_{n+1}\right\|_2} < 10^{-3}\,. \tag{12}$$

If convergence is achieved, we set

$$\underline{T}_{n+1} := \underline{T}^{k+1}_{n+1}\,;\ \phi_{n+1} := \phi^{i}_{n+1} \tag{13}$$

else we set $\underline{T}^{i}_{n+1} = \underline{T}^{k+1}_{n+1}$, increase the outer iteration counter i by one and repeat steps 1 to 4.

Direct coupling of (1) and (2) is possible using a Newton scheme. However, the implementation presented in this study solves (1) and (2) sequentially as schematically outlined in Fig. 2. This approach is preferable here since only a small number of iterations is required for convergence.

Note that the electric conduction is a linear equation, i.e., nonlinear electric phenomena are not in the scope of this paper. For example, including the nonlinear electric behavior of an MOSFET in an FE domain requires additional work [34].

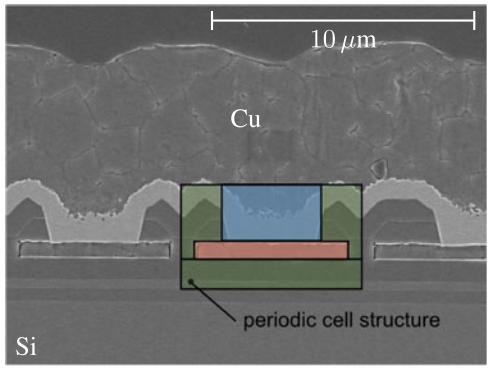

Fig. 3. SEM cross section across a test device. A periodic cell pattern is indicated schematically. On top of the periodic cell structure, the power metallization is visible.

III. Methodology

A. Homogenization concepts

The approach presented in this paper represents a simplified homogenization scheme dedicated to power electronic applications. It can be summarized as follows:

1) identification of a periodic cell structure;
2) 3D microscale FE modeling of selected cell structure;
3) solve heterogeneous static heat conduction problem based on an FE approach;
4) find analytical solution of the 3D boundary value problem and extract effective thermal conductivity;
5) determination of effective heat capacity based on direct and optimized approach;
6) run iterative FE scheme to accommodate material nonlinearities.

First, a suitable periodic cell structure is selected. The cross section shown in Fig. 3 obtained by scanning electron microscope (SEM) imaging shows a typical power technology metallization stack. One of the representative periodic cells is highlighted schematically. The cell structure in Fig. 3 represents an inter-metal dielectric (IMD) layer and is made of horizontal aluminum (Al) routing wires, vertical copper (Cu) via plugs and surrounding silicon dioxide (SiO_2).

Second, the periodic cell structure, a so-called unit cell, is modeled in detail [see Fig. 4(a)], including all main layers (e.g., Al, Cu and SiO_2). Please note, the detailed modeling of thin layers (e.g., diffusion barriers made of titanium) as well as specific layer shapes may be neglected in the thermal simulation regime. However, to provide correct mechanical simulation results including accurate strain or stress distribution an accurate modeling of layer combinations and their detailed shapes are inevitable. Accurate geometric dimensions may be obtained by failure analysis methods such as FIB and SEM (see Fig. 3).

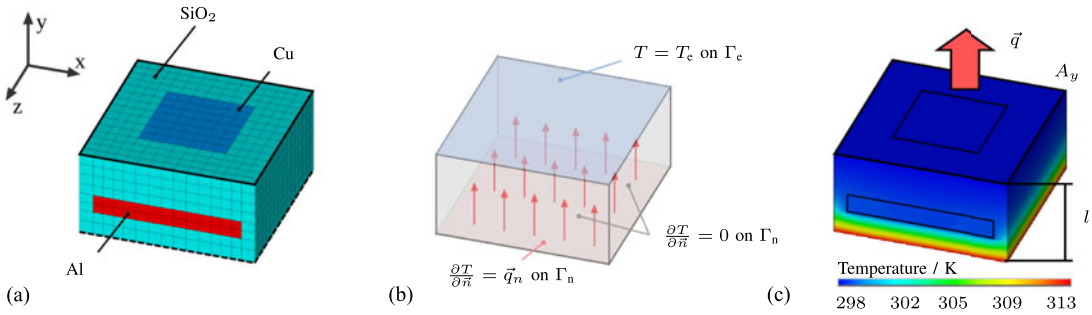

Fig. 4. Three steps of the homogenization approach shown for a unit cell. First, the microscale finite-element model of an example structure (cf., Fig. 3) showing the IMD layer structure of a representative power electronics technology. Second, a schematic view of the 3-D unit cell, which is simplified to a quasi 1-D boundary problem due to its corresponding boundary conditions. Third, the solution of static thermal FE simulation highlighting the quasi 1-D heat flow in y-directions.

Third, the 3D boundary value problem (BVP) of the unit cell is reduced to three one-dimensional (1D) BVPs in the three principal directions. For example, the 1D problem in y-direction is illustrated in Fig. 4(b). The heat flow through the unit cell is forced solely in y-direction by applying adiabatic (i.e., homogeneous Neumann) BCs to the four surrounding side walls. The top surface is held at a constant temperature T_e by applying an inhomogeneous Dirichlet BC. A constant heat flux $\vec{q} = P_s$ is forced to enter the domain at the bottom surface. The process is repeated analogously for the remaining principal directions x and z. In Fig. 4(c), the temperature distribution of the heterogeneously modeled unit cell is shown. This result is a solution of the *static heat equation* (i.e., (1) assuming $\partial T/\partial t = 0$) where the right-hand side is zero, thus solving a heat conduction problem (i.e., boundary value problem) in an FE scheme as outlined in Section II.

Fourth, assuming a homogeneous (i.e., effective material properties) unit cell the solution shown in Fig. 4(c) may be analytically solved with Fourier's conduction law. For the anisotropic and linear case (i.e., temperature independent), the 1D Fourier's law is

$$q_i = -\lambda_{ii}\frac{\mathrm{d}T}{\mathrm{d}i}, \qquad i \in \{x, y, z\} \tag{14}$$

where λ_{ii} is the effective thermal conductivity in one of the three directions x, y, and z. Providing the corresponding boundary conditions (T_e, $\vec{q}_i$), correct geometrical dimensions (l_i, A_i) as well as the temperature difference (ΔT) leads to a representative effective thermal conductivity ($\tilde{\lambda}_\mathrm{eff}$).

The heat flux density applied as inhomogeneous Neumann BC to the bottom of the unit cell (see Fig. 4) is

$$q_i = \frac{P}{A_i}, \qquad i \in \{x, y, z\} \tag{15}$$

where P is the power and A the surface area. The 1-D derivative of (14) can be written in a difference formulation as

$$\frac{\mathrm{d}T}{\mathrm{d}i} = \frac{T_\mathrm{sink} - T_\mathrm{source}}{i_\mathrm{sink} - i_\mathrm{source}} = \frac{\Delta T}{l_i}, \qquad i \in \{x, y, z\} \tag{16}$$

where ΔT represents the temperature difference between the source surface and the sink surface. The distance between the two surfaces is defined by l. Substituting (15) and (16) into (14) results in

$$\frac{P}{A_i} = -\lambda_{ii}\frac{\Delta T}{l_i}, \qquad i \in \{x, y, z\} \tag{17}$$

which is rearranged to

$$\lambda_{ii} = \frac{P l_i}{A_i \Delta T_i}, \qquad i \in \{x, y, z\}\,. \tag{18}$$

It should be noted that (18) is equivalent to the solution of a thermal RC network derived from a lumped model [12]. Applying (18) to unit cells in all three main directions provides the diagonal entries of the thermal conductivity tensor

$$\tilde{\lambda}_\mathrm{eff} = \begin{bmatrix} \lambda_{xx} & 0 & 0 \\ 0 & \lambda_{yy} & 0 \\ 0 & 0 & \lambda_{zz} \end{bmatrix}. \tag{19}$$

Fifth, the specific heat capacity c is required to perform transient FE simulations. The specific heat capacity is defined as

$$c = \frac{C_\mathrm{th}}{m} = \frac{C_\mathrm{th}}{\rho V} \tag{20}$$

where C_th is the heat capacity, m is the mass, ρ is density, and V is the corresponding volume. Basically, there are two ways to determine the effective thermal capacity. The straight forward approach simply uses a volume-weighted and mass-weighted approach, as presented in [10]. The mass-weighted effective specific heat is

$$c_\mathrm{eff} = \frac{\sum_{j=1}^{n} c_j m_j}{\sum_{j=1}^{n} m_j} \tag{21}$$

and the volume-weighted effective density is

$$\rho_\mathrm{eff} = \frac{\sum_{j=1}^{n} \rho_j V_j}{\sum_{j=1}^{n} V_j} \tag{22}$$

where n is the number of different materials present in the unit cell. Naturally, this averaging approach does not necessarily provide an optimized solution to a dynamic thermal

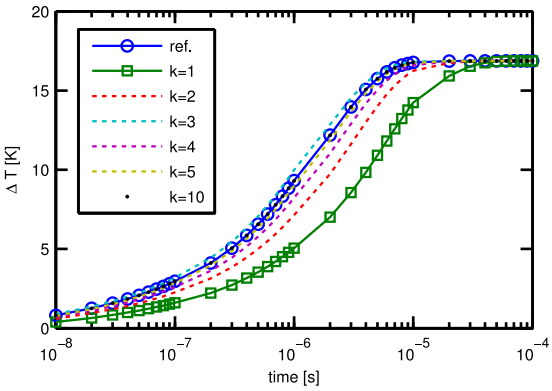

Fig. 5. Thermal step response of an unit cell. The temperature difference between the source and sink surface is shown during a transient heat event until the static regime is reached after about $10\ \mu$s.

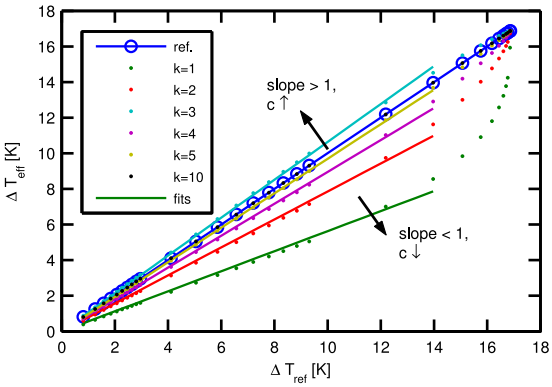

Fig. 6. Goodness of the fit is verified in a correlation plot. A slope of one indicates a perfect match in a linear case. The search algorithm is based on a simple root-finding method.

problem. Further improvements to the weighted material parameters are feasibly using an numerical simulation-based optimization method presented in the following.

In a numerical optimization scheme, the thermal step response obtained from the effective model simulation is compared to the reference step response from the detailed simulation model. The value of the heat capacity is then iteratively adapted to fit the reference response. In Fig. 5, the process of iterative alignment is shown for the first five iterations as well as the final iteration ($k = 10$). The step response input function is defined logarithmically from nanoseconds to milliseconds in order to cover for the relevant time constants in power electronic applications.

Fig. 5 details the optimizations scheme. The reference thermal response of the heterogeneous unit cell is the blue solid line with circle markers. The green line with square markers is the result of the first iteration $k = 1$, which is based on the effective unit cell. The thermal response of the first iteration does not adequately represent the reference curve for time scales shorter than 3×10^{-5} s. In this case, the specific heat capacity is too large. The value for the specific heat capacity in the next iteration is inferred from a correlation plot (see Fig. 6). By comparing the amplitude of the effective model to the amplitude of the reference model, the mismatch is easily identifiable. A straight

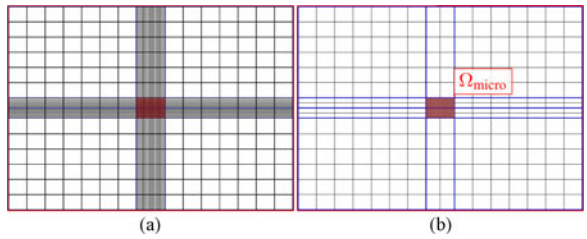

Fig. 7. Schematic representation of a conforming grid as well as a nonmatching gird.

line with a slope of 1 indicates a linear correlation between the two input data. If the slope is smaller than 1, c has to be reduced. On the contrary, if the slope is larger than 1, c has to be increased. This is basically a root-finding problem, which is solved with a *bisection* algorithm.

Depending on the actual problem, for most applications, the weighted heat capacities are sufficient. However, when proceeding toward higher power densities and shorter time constants, the numerical optimization approach offers additional flexibility to fit effective material properties to an application relevant dynamic behavior.

Sixth, the methods presented previously are correct for linear material properties. Inaccuracies due to temperature-dependent material properties (e.g., in silicon, silicon dioxide) are compensated in an iterative approach. The basic idea is to derive effective material parameters from a relatively small temperature rise, thus neglecting nonlinear deviations. In addition, temperature-dependent material properties are accounted for by varying the absolute ambient temperature. The remaining inaccuracy due to nonlinear material properties is directly related to the ambient temperature step size. Since this approach is implemented in a computational scheme, the absolute ambient temperature, and consequently, the introduced error can easily be adjusted to reach a satisfactory solution.

B. Nonmatching grids

In the regular FE method, the domain Ω is discretized in strictly *conforming elements*. Adjacent elements must share one edge (2-D) or one surface (3D). Furthermore, the element shape is required to pass quality measures, i.e., their shape must not be excessively distorted. This means, when passing from one characteristic length scale to another, a significant amount of lightly distorted elements must be utilized, reducing the flexibility of the standard method. These two limitations are the main obstacle in multiscale FE simulations, in which structures of different characteristic lengths need to be resolved.

The approach presented in this paper is based on the *Mortar* FE method [35]–[37], a nonmatching domain decomposition technique. Using the Mortar FE method, the discretization of the subdomain does not need to match on the interface Γ_{nm}. Fig. 7 displays a conforming (a) and nonmatching (b) discretization.

To transmit information between adjacent subdomains, the FE formulation is enhanced by *Lagrange* multipliers and the following conditions have to be fulfilled on the interface Γ_{nm}

between subdomain Ω_i and Ω_j:

$$u_i = u_j \tag{23a}$$

$$\vec{n}_i \lambda_i \nabla u_i = \vec{n}_j \lambda_j \nabla u_j. \tag{23b}$$

The first condition is enforced in a weak (integral) sense, as the point-wise equality of the standard FE method is not achievable on an incompatible interface. In the case of two adjacent subdomains Ω_1 and Ω_2, we arrive at

$$\int_{\Gamma_{\mathrm{nm}}} \mu \left(u_1 - u_2\right) \, \mathrm{d}\Gamma = 0 \tag{24}$$

where μ represents an appropriate test function. The second condition (23b) ensures the continuity of the flux across the interface, which is realized by Lagrange multipliers λ_M

$$\lambda_M = -\vec{n}_1 \lambda_1 \cdot \nabla u_1 = -\vec{n}_2 \lambda_2 \cdot \nabla u_2 \tag{25}$$

where $\vec{n}_i$ is the normal vector of Γ_{nm}.

Adding (24) and (25) to the FE formulation outlined in Section II results in

$$\begin{bmatrix} \mathbf{M}_{\mathrm{u}_1} & 0 & 0 \\ 0 & \mathbf{M}_{\mathrm{u}_1} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \underline{\dot{u}}_1 \\ \underline{\dot{u}}_2 \\ 0 \end{bmatrix} + \begin{bmatrix} \mathbf{K}_{\mathrm{u}_1} & 0 & \mathbf{D} \\ 0 & \mathbf{K}_{\mathrm{u}_2} & \mathbf{N} \\ \mathbf{D}^t & \mathbf{N}^t & 0 \end{bmatrix} \begin{bmatrix} \underline{u}_1 \\ \underline{u}_2 \\ \underline{\lambda}_{\mathrm{M}} \end{bmatrix} = \begin{bmatrix} \underline{f}_{\mathrm{u}_1} \\ \underline{f}_{\mathrm{u}_2} \\ 0 \end{bmatrix}. \tag{26}$$

The matrices $\mathbf{D}$ and $\mathbf{N}$ define the coupling between the domains connected by the interface Γ_{nm} and require special attention since intersections between the two domains have to be taken into account. It should be highlighted that, in addition to the thermal and electrical problem treated here, the Mortar method has been applied to the acoustic field [38], the piezoelectric coupling [39] and the mechanical-acoustic coupling[38]. We are using the Mortar method in the research code of [40]. Other methods known from the literature are Nitsche type mortaring [41] and the penalty formulation [42].

IV. Model Development

A. Test Device Description

An optical microscope image of the test chip fabricated specifically for this study is shown in Fig. 8. It's design is similar to that of a trench power MOSFET [1], but instead of an active transistor region, the test chip includes an embedded polysilicon layer acting as heating source (i.e., *polyheater*). It provides *in situ* heating based on Joule heating with well-defined power density and is used simultaneously as verification tool. The polyheater is a highly doped polycrystalline silicon layer, which can be used to, e.g., connect the gate terminal of a power MOSFET. It is inherently thermally stable due to its increasing resistance with higher temperatures (see Fig. 10) and allows high temperature experiments. Polysilicon *in situ* resistive heating structures are used for various applications of device characterizations [43], [44].

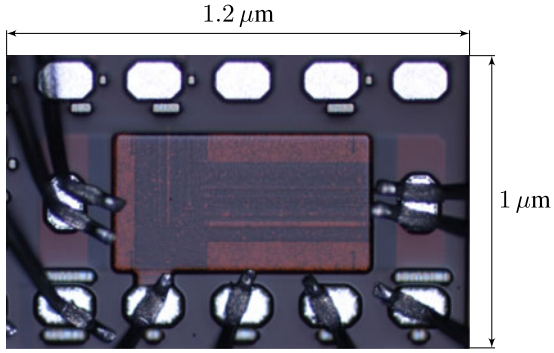

Fig. 8. Optical microscopic image of the test device (top view). The test device is specifically designed to verify electrothermal simulation results with experiments. A polysilicon layer is embedded as a well-defined heating source, simplifying the electrothermal coupling. Wire-bonds are used to connect the heating stage as well as enable *four-point* resistance measurements. Please notice two bonds per pad.

The test chip is based on a planarized rectangular heating geometry, where the polyheater is electrically isolated from the bottom silicon substrate by a relatively thick field oxide. The wafer thickness for this device is specified to $220 \pm 20\,\mu$m. A verification of the actual thickness by means of cross sectioning has not been performed. This study focuses on short pulses ($t < 500\,\mu$s), where modeling of the full substrate thickness is not necessary as the heat wave does not reach the bottom of the substrate. On the top side, the polyheater is isolated only by a thin gate oxide, except for small section on both sides, where it is electrically connected to the bond wires. On top of the gate oxide, the IMD layer is located. It consists of oxide layers, aluminum routing wires (*metal 1*), vertical via plugs and diffusion barriers as shown in Fig. 3. Furthermore, a thick copper layer is placed on top, acting as bond wire support and large heat capacity for fast thermal events (e.g., switching). It is, therefore, referred to as *power metallization* (PM). Finally, a layer of passivation is added. The layer stack and thicknesses are also indicated in the bottom plot of Fig. 13. The chip is assembled into a nonsealed ceramic package and wedge bonded with aluminum wires.

B. Multiscale Modeling Application

The test device presented in Figs. 8 and 9(a) includes a resistive metal temperature sensor [see Fig. 9(b)]. The sensor structure is fabricated using *metal 1* wires. In order to increase the sensitivity of the sensor, a meander structure is processed [see Fig. 9(b)], elevating the temperature-dependent signal. The meander structure's dimensions are $20 \times 30\,\mu$m with a minimum feature size of 500 nm for a single metal wire. *Force and sense* wires to support four-point probe measurement methods are routed directly to the probe's head [details visible in Fig. 9(b)]. The complex structure makes this device an ideal test object to study local temperature variations and gradients within the heterogeneous top metallization layer. The sensor structure is modeled in full detail and embedded in the full-chip model as shown in Fig. 9(a) and (c). The use of nonmatching grid interfaces allows the inclusion of a high degree of details in the

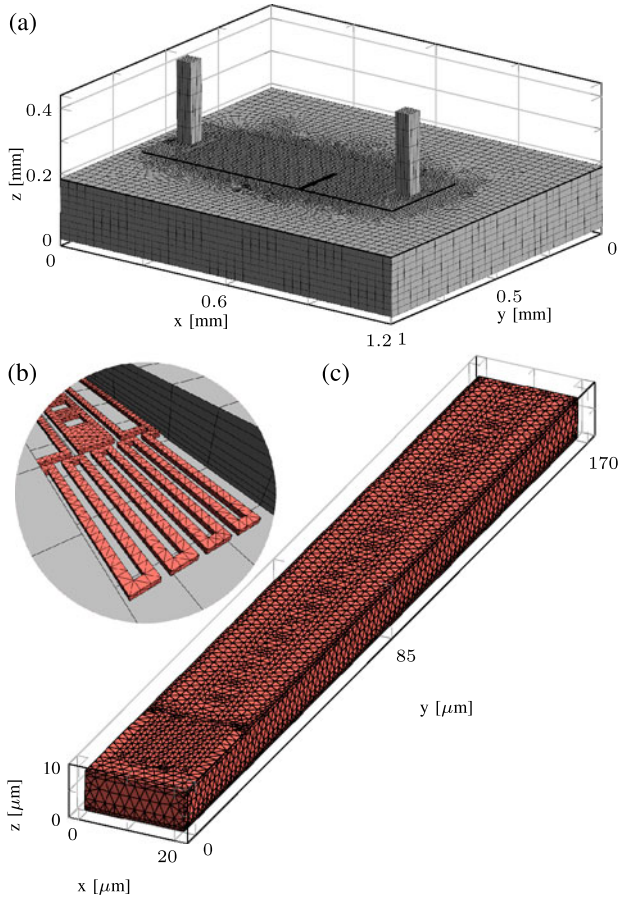

Fig. 9. Microscale sensor structure (c) is embedded into a full-chip microelectronic device model (a) using nonmatching grid technique (b).

micro model while the macromodel only resolves the coarse structure.

C. Sensor and Polyheater Calibration

In order to use the metal resistor structure as well as the polyheater as temperature sensing elements, a calibration procedure is required in advance to determine their temperature dependence. The temperature-dependent electrical resistance is measured by four-point probing in the temperature range of -60–$180\,^{\circ}\mathrm{C}$ with 20 K step size, limited by the laboratory equipment. The temperature is defined by a controlled airstream. During device operation even higher temperature values are expected, thus calibration results are extrapolated to an application sensor operating range. The metal resistor shows a linear behavior (experimentally verified up to 775 K in [45]) and can easily be extrapolated. The corresponding fitting parameters are given in Fig. 10. The temperature-dependent electrical resistance of the polycrystalline silicon layer is modeled with a power law

$$R(T) = a + bT^c \tag{27}$$

where a, b, and c are the corresponding fitting parameters. Since the exact geometry of the structure is known, it is possible to calculate the electrical resistivity of the fabricated polycrystalline silicon layer. Measurement results and fitting parameters are

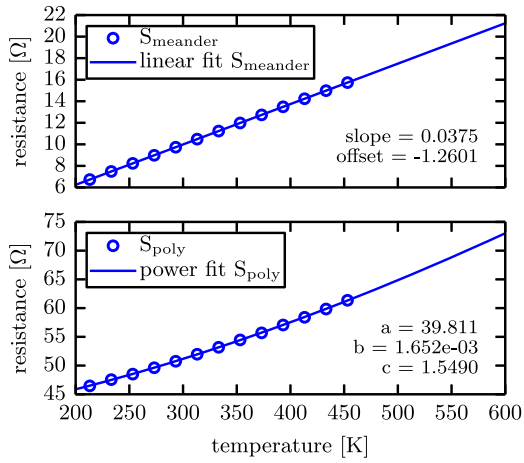

Fig. 10. Sensor temperature calibration curves. The resistive metal wire sensor shows a linear temperature dependence. The polycrystalline silicon layer exhibits a power law trend.

available in Fig. 10. Similar results for comparable polycrystalline silicon structures have been reported before [43], [46].

D. FE Simulation and Boundary Conditions

1) Material Parameter: Material parameters used for the FE simulation are either taken from the literature (summarized in Appendix), determined experimentally (see Section IV-C) or numerically optimized (see Section III-A). The thermal properties of highly doped bulk silicon are significantly lower compared to standard silicon according to [47] and [48]. Literature data were verified in advance by reference measurements on unprocessed raw wafers. Ideal material interface conditions are assumed here, i.e., imperfect contacts or defects are not taken into account.

2) Load and boundary conditions: A Dirichlet BC is applied on the backside of the model representing an ideal heat sink at $25\,^{\circ}\mathrm{C}$; see Fig. 12. The surrounding of the model is set to homogeneous Neumann BCs (i.e., adiabatic / isolating surfaces). Convective and radiative losses may be neglected considering small areas in combination with short times scales. A representative stress conditions of 100-μs pulse duration and approximately 60-V amplitude is applied (see voltage plot of Fig. 11). This 100-μs stress condition represents a typical application scenario during switching operations.

V. Results and Discussions

The coupled electrothermal simulation yields the electric potential $\phi(\vec{x}, t)$ and temperature field $T(\vec{x}, t)$. We are mainly interested in the temperatures reached in specific locations, but use the electric results for principal verification with measured quantities. Material parameters used in the simulation are given in the Tables I–VI.

A. Electrical Verification

The measured electrical current is shown in the lower plot Fig. 11 (solid line). In order to compare it to the simulation, the current is derived from the electric potential ϕ on the top surface Γ_b of one of the wire bonds $I_{\mathrm{simu}} = \gamma \int_{\Gamma_b} \frac{\partial \phi}{\partial \vec{n}}\, \mathrm{d}\Gamma_b$. As

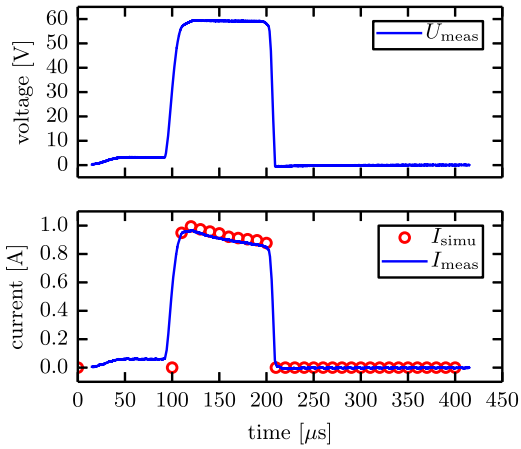

Fig. 11. Comparison of measured and simulated electrical signals. The voltage (upper plot) is applied to the packaged test device. The short pulse quickly heats up the polysilicon layer (cf., Fig. 15), thereby reducing its conductivity and the current. The matching of the experimental and simulated current curves ensures the correct power dissipation for the thermal analysis.

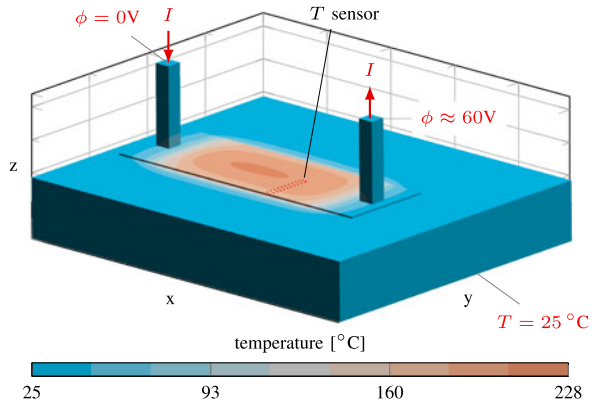

Fig. 12. Surface temperatures obtained at the end of the stress pulse ($t = 200\,\mu$s) by electrothermal FE simulation. The global temperature distribution is defined by larger geometrical structures such as power metallization and substrate layers. The heterogeneous sensor structure (schematically indicated) does not have a noticeable effect on the global temperature distribution.

can be seen in Fig. 11, measured and simulated current are in good agreement. Most importantly, the reduction in current that is caused by the temperature rise in the polysilicon layer is very well represented. The slightly lower measured current (approximately 4%) can be attributed to the existence of addition serial resistors, which are not covered by the simulation.

Please note, a match in electrical current ensures the correct power dissipation on the polysilicon heating stage, a prerequisite for accurate thermal results.

B. Global Heat Flow Analysis

In Fig. 12, the simulated surface temperature distribution of the test chip is shown at the end of the stress pulse ($t = 200\,\mu$s). Applied boundary conditions, large geometric entities such as silicon substrate, power metallization and homogenized layers are the main factors influencing the global temperature distribution. Microscopic structures like the in-depth modeled sensor

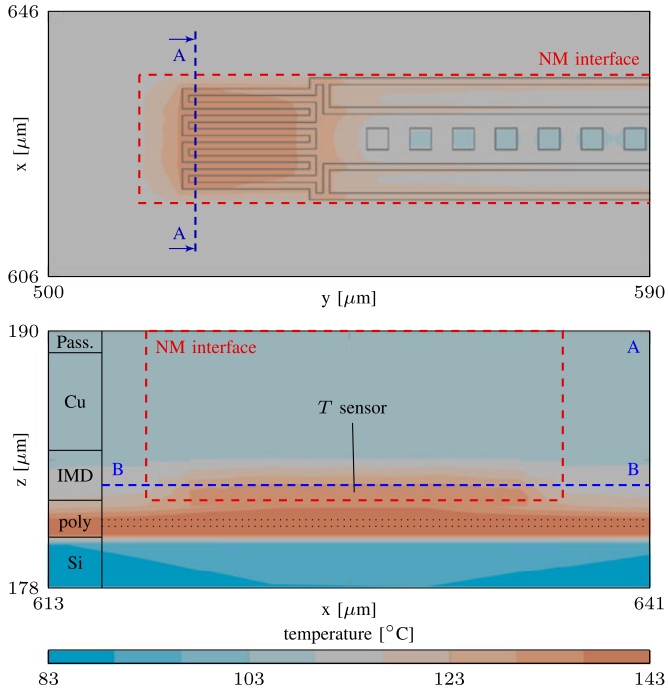

Fig. 13. Detailed temperature distribution from the embedded microscale sensor structure. The upper figure shows the temperature distribution extracted along the *B-B* cross section. A clear temperature hot spot is caused by the reduced thermal conductivity of the sensor structure at the time $t = 130\,\mu$s. The *A-A* cross section below shows the vertical heat spreading across the complex layer structure.

structure do not substantially affect the surface temperature distribution.

Surface temperature results may be compared to, e.g., infrared (IR) mapping methods as demonstrated in an earlier publication [46] and is done so routinely (see, e.g., also [20]). Alternatively, large scale temperatures may be compared using known temperature dependencies of, e.g., V_{GE} in an insulated-gate bipolar transistor insulated-gate bipolar transistor (IGBT) [22]. Our main interest lies in the verification of the *local* temperature at the sensor location, but we also use the measured voltage and current from Fig. 11 and the characterization curve of the polysilicon layer (27) to compare the average polysilicon layer temperature in Fig. 15. This comparison is discussed in detail later and gives sufficient confidence in the correct global temperature distribution to analyze the local temperature field.

C. Micromodel Heat Flow Analysis

In Fig. 13, the temperature distribution near the sensor structure is investigated in detail. The heterogeneous sensor structure is embedded in the homogenized full-chip model using non-matching (NM) grid interfaces (red dashed line). The temperature distribution shown in the upper plot of Fig. 13 indicates the formation of a temperature hot spot at the sensor location, critical for the device robustness. Increased temperatures close to the sensor meander region are caused by missing vertical and horizontal heat paths. It should be noted that the results plotted in Fig. 13 represent the worst case in terms of temperature inhomogeneity at the time 130 μs.

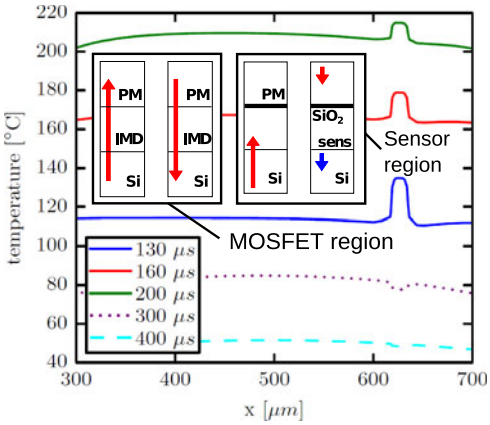

Fig. 14. Temperature profiles extracted from the path *B-B*, schematically highlighted in the cross section plot *A-A* of Fig. 13, for various time steps. The three solid lines represent the heating phase at the time steps 130, 160, and 200 μs. The dotted and dashed line show the corresponding temperature profile during the cool-down phase at the time steps 300 and 400 μs, respectively. The insets schematically show the direction and barriers of the flux during heating and cooling phase.

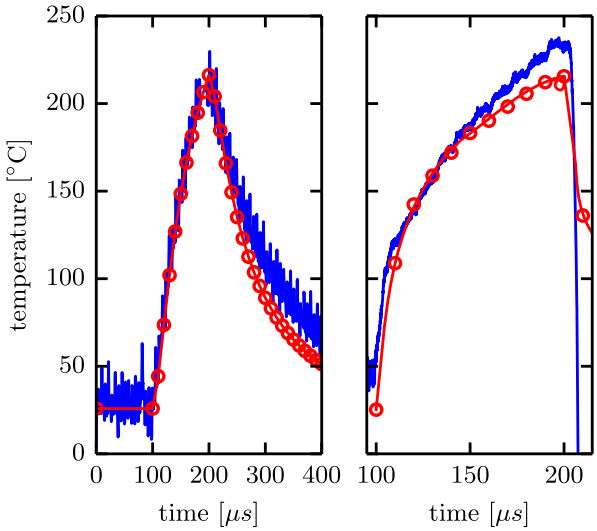

Fig. 15. Comparison of nonlinear electrothermal simulation results (round markers) with measurements (solid lines). On the left, results from the heterogeneous microscale meander structure are compared with calibrated resistive temperature measurements. On the right, the averaged polyheater temperature is shown. The experimental curve (solid) therein is calculated from a calibrated temperature model using measured heat-up pulse parameters.

In order to quantify the temporal evolution visible in the contour plot in more detail, horizontal line profiles (*B-B* path in the lower part of Fig. 13) are plotted for the sensor region in Fig. 14. The sensor shows a substantially higher temperature for the time steps 130, 160, and 200 μs before switch-off. Particularly strong temperature gradients occur at the sensor border where silicon dioxide layers are present to electrically isolate the passive sensor regions from the active device parts. This situation is shown in the insets of Fig. 14, where the direction of the flux is indicated by upward pointing arrows. In the sensor, the heat flux is severely inhibited by the SiO_2 layer on top, resulting in large temperature gradients at the interface, the driving forces regarding thermomechanical degradation.

After switch-off ($t > 200\,\mu$s), the direction of the flux is reversed and the system relaxes toward thermal equilibrium. The temperature inhomogeneity between sensor structure and surroundings is reduced (see exemplary time steps at 300 and 400 μs). The sensor temperature is slightly lower than the surrounding transistor region due to its insulation from the large heat reservoir on top (see insets in Fig. 14 with arrows pointing downward). The sensor is locally cooled by the flux through the substrate as indicated by the blue downward pointing arrow. To obtain such a level of detail in the transient thermal analysis, the presence of local details within the numerical model is inevitable.

D. Verification of Thermal Results

For the experimental verification, the meander sensor structure as well as the polyheater layer are used as resistive temperature sensing elements and compared with actual temperature results obtained by electrothermal FE simulation.

The results shown in the left graph of Fig. 15 compare the temperature at the resistive meander sensor during the 100 μs stress pulse and the subsequent cooling-down period. The rapid switch-off event at the end of the stress pulse at 200 μs causes oscillations on the sensor signal due to cable inductance. These switch-off oscillations of about 10 μs are, therefore, omitted from the solid measurement curve. The excellent agreement between measurements and simulations indicates: (a) modeling of the device and its sensor structure has been performed with sufficient details; (b) suitable material parameters have been used in the thermal simulation; and (c) the homogenization performed in the region just outside the sensor adequately accounts for the heterogeneous layer structure. The availability of the detailed model of the meander sensor structure makes it possible to analyze highly local temperature distribution at the sensor head. For example, the results shown in Fig. 15 (left) correspond to the average of the nodal values of the actual sensing metal structure. This approach properly reflects the resistive measurement principle where the temperature between the two sense fingers is also averaged (see Figs. 9 and 13, for geometrical details). Small deviations between measurements and simulations are noticeable during cool-down after about 250 μs. A possible explanation is that for short time constants, the heat flux is mainly distributed within the microscale sensor structure, a highly detailed model area where the highest accuracy is expected. For longer time constants, the heat flux propagates into the full-chip model with a limited model accuracy, resulting in limited accuracy.

The results presented in the right graph of Fig. 15 compare averaged polyheater temperatures between measurements and simulation for the 100 μs long heating pulse. The experimental temperature curve (solid blue line) is calculated from (27) and represents the temperature dependent resistance change of the polycrystalline silicon layer. As a result, no meaningful measurement data are available before switch-on ($t < 100\,\mu$s) and after switch-off ($t > 200\,\mu$s) because no current is applied to the polyheater. The differences between measurement and simulation are well below 10% and further confirm the validity of the thermal model.

VI. Conclusion and Outlook

We combined two approaches to overcome multiscale limitations for analyzing power electronic devices and applied them on a dedicated test chip structure. We used computational homogenization to derive and optimize effective material parameters for the complex heterogeneous interconnect stack, allowing us to reduce the effort modeling and bring down simulation time. We compensated the inevitable loss of local information in the microscale by modeling regions of interest in full detail and included them with a nonmatching grid technique into the FE simulation. The nonlinear coupled electrothermal multiscale simulation results are thoroughly discussed and good agreement is found when comparing them to experimental measurements.

Few approaches exist for nonmatching domain decomposition and we have used the *Mortar* FE method to couple micro- and macromodel. Its derivation results in physically consistent equations and inaccuracies are only caused by numerical integration along a common intersection grid. Inconveniently, we have sometimes observed highly irregular intersection element,s which can cause unphysical local variations in the temperature. We are, therefore, also investigating the use of the *Nitsche* technique [41], which should be more resilient due to the penalization of the jump on the interface.

The presented FE implementation offers a unique advantage over other electrothermal simulation concepts in that it provides the *local* and *global* temperature distribution. In particular, it enables subsequent mechanical simulations in which device degradation can be assessed in more sophisticated ways (e.g., metal fatigue, strain-rate-dependent yielding). We believe that through coupled electro-thermo-mechanical FE simulations our method can substantially contribute to the enhancements of robustness of new power electronic components.

We have applied the new method to a 3-D, transient electrothermal model bridging three orders of magnitude ($1\,\mu$m–$1\,$mm). Emerging *high electron mobility transistor* (HEMT) technologies may raise the requirement to even higher orders as the heat generation is concentrated in a very thin layer. This is demonstrated in [49], where results are limited to 2-D models due to computational constraints. However, 3-D analysis of Gallium-Nitride-based *HEMTs* may provide additional insights according to [50]. We believe our method can further contribute in removing analysis barriers in that domain as well, e.g., by using multiple, cascading interfaces or by improvements of the method itself.

APPENDIX

TABLE I
Electrical Properties of Dielectric Layers

Dielectrics (at T_a)	ρ_el [Ωm]	Ref.
SiO_2 (bulk)	$\geq 10^6$	[51]
SiO_2 (amorphous)	$\approx 10^{12} - 10^{14}$	[52]
polyimide (lateral)	$\geq 10^6$	[53]
polyimide (vertical)	$\geq 10^6$	[53]

TABLE II
Nonlinear Thermal Properties of Dielectric Layers Depending on Layer Thickness t

Silicon dioxide by Schafft [54]			
T [$^\circ$C]	λ (Bulk) [W/mK]	λ ($t = 2.74\,\mu$m)	λ ($t = 3.04\,\mu$m)
27	1.40	0.67	0.97
105	1.52	0.59	0.82
180	1.60	0.52	0.72
255	1.65	0.47	0.61

TABLE III
Electrical Properties of Metals

Metals (at T_a)	ρ_el [Ωm]	Ref.
aluminum	$2.7 \cdot 10^{-8}$	[55]
copper	$1.7 \cdot 10^{-8}$	[55]
tungsten	$5.65 \cdot 10^{-8}$	[55]

TABLE IV
Thermal Properties of Metals

Metals (at T_a)	ρ [kg/m^3]	c [J/kg$\cdot$K]	λ [W/mK]	Ref.
aluminum	2700	900	210	[55]
copper	8930	385	385	[55]
tungsten	19250	134	163.3	[55]

TABLE V
Nonlinear Thermal Properties of Silicon

T [$^\circ$C]	λ [W/mK]	c [J/kg$\cdot$K]
-50	241.5	587.6
0	170.9	723.4
77	122.0	761.0
127	102.5	781.0
177	88.0	799.1
227	76.7	815.7
327	60.5	845.3
427	49.5	871.1

TABLE VI
Effective Material Properties of the Inter-Metal Dielectric Region

Properties	IMD
ρ (volume weighted) [kg/m^3]	3137.15
c (mass weighted) [J/kgK]	581.78
λ_{xx} [W/mK]	5.30
λ_{yy} [W/mK]	4.63
λ_{zz} [W/mK]	51.67

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