Angular Modulation of Dual-Inverter Fed Open-End Motor for Electrical Vehicle Applications

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***Abstract*—In this paper, angular modulation index (AMI) implemented through a modified space vector modulation for the dual voltage source inverters (VSI) is proposed with the primarily aiming to reduce switching losses. The desired voltage across the load is synthesized by applying appropriate phase-angle displacement between space vector references. The proposed approach avoids the use of a dc/dc boost converter (which imposes loss and weight/price penalty to duplicate the dc-link voltage) and results to be particularly suitable for electrical/hybrid vehicle applications. Namely, the application of saving energy to keep driving has been identified as major concern. Hence, this work focuses on the strategy to enhance efficiency. The principles of the proposed controlling method and switching loss, which is reduced at least by 50%, are theoretically evaluated. This paper proposes a pioneering mathematical approach to correctly determine total harmonic distortion (THD) value of the voltage/current for the dual-VSI structure. Furthermore, simulation and experimental results prove that the proposed method insures benefits in terms of common-mode voltage, THD of the voltage, and switching loss reduction. The dual-VSI prototype supplying 1.5-kW induction motor is assembled in the laboratory to experimentally evaluate performance of the proposed method. Also, the simulation results carried out through MATLAB/Simulink environment are given to confirm performance of this easy-to-implement and high-efficient method.**

***Index Terms*—Angular modulation index (AMI), common-mode voltage (CMV), dual two-level inverter, electrical/hybrid vehicle, open-end motor, switching loss.**

I. Introduction

RECENTLY voltage source inverters (VSIs) have been widely used; as distributed generators, in order to improve power system characteristics [1], or as motor drives. Conventionally, in medium-/high-power motor-drive applications (especially in electrical/hybrid vehicles, tram, etc.), medium-voltage dc-source has been employed in order to respect battery safety concerns [2]. As a consequence, a boosting stage (i.e., a dc/dc converter) is required to link the dc-source and the VSI as illustrated in Fig. 1. The dc/dc converter, containing passive component, involves size/price penalty as well as degradation of the total efficiency of the system [3]. In conventional power stages, switching losses are further deteriorated by the presence of a dc/dc stage followed by the VSI stage, since the total efficiency is obtained by multiplying the efficiencies of the two power converters. The patent in [4] strives by allocating null time to that of nearby active space-vectors enhances VSI efficiency by around 4%.

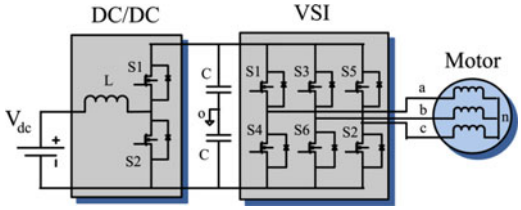

Fig. 1. Conventional conversion system applied in electrical vehicles.

The battery depth of discharge has an exponential relation with its lifetime expectancy as addressed in [5]. Due to the fact that these noncommon charging stations for novel generation vehicles are installed over constant/faraway distance, by discharging dc-source less while driving (seeking better efficiency), battery will life up more. The main challenges toward motor drive applications shown in Fig. 1 are their inherent weakness from bulky passive component, and more importantly, from efficiency point of view, exhausting battery rapidly [2], [3].

Recently, several multilevel VSI topologies have been introduced. Among them the most important ones can be sorted as: diode clamped [6], capacitor clamped [7], and cascaded converter [8]. All of these configurations suffer from complex look-up tables, region identifications, or unbalanced neutral-point feature [6]–[9]. Though the multilevel inverters are superior to conventional two-level inverters in term of level numbers of the output voltage, they still suffer from the common mode voltage (CMV) issues but with less severity [7].

The pioneering work of *Stemmler and Guggenbach* [10] shows that the open-end winding induction motor can be driven with dual VSI at either end by making six terminals of motor stator windings available. Through multilevel converters, the dual two-level VSI configuration has been of interest not only thanks to its independent easy controlling feature but also due to its simple power stage [11]. Furthermore, the dual-inverter topology benefits from no neutral-point fluctuations as well as reliability [12] and fault tolerance. Indeed, in case of fault at one inverter, the corresponding output terminals would be short circuited, and power would be provided by using another inverter as in a standard two-level VSI as presented in [13] and [14]. The dual-inverter structure inherently generates triple harmonic known as zero-sequence voltage (ZSV) [15]. Hence, arresting circulating zero-sequence currents in the motor phase windings is usually addressed using zero-sequence chokes in a single dc-source-driven dual inverter [10]. However, as discussed by the authors in [15]–[19], the ZSV and CMV issues affecting a

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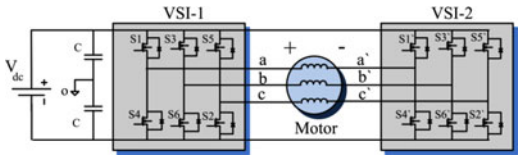

Fig. 2. Dual VSI fed open-end motor proposed for electrical vehicle.

dual VSI are highly suppressed by avoiding utilization of null vectors.

The proposed conversion system for hybrid/electrical vehicle applications is depicted in Fig. 2 with making use of dual VSI fed open-end motor instead of the boosting stage in order to reach the desired voltage [14]. In this paper, in order to achieve high efficiency as well as low CMV and ZSV values, modified space vector pulsewidth modulation, avoiding null vector utilization, is implemented. In particular, in order to adapt this modification in the dual-VSI structure, the approach proposed in this paper makes use of the concept of the Angular modulation index (AMI), which is based on phase-angle displacement between two VSI references. Authors in [20] adjusted angle between VSI connected to constant dc-source and floating capacitor (FC) bridge to control voltage level in FCs respecting the induction motor structure and its power factor variation. However, [20] suffers from lack of not only analytical principles but also total harmonic distortion (THD) and loss evaluation. This paper concentrates on efficiency issue as the main objective. Switching loss, which is theoretically mitigated by 50%–87%, is formulated respecting AMI and load power factor $\cos(\emptyset)$. Authors in [11] and [19] tried to analyze the output-voltage error and current ripple. However, due to the system complexity as well as the high number of possibilities, they eventually failed in achieving straightforward value or formula for THD. However, this paper introduces pioneering solution to accurately calculate THD value of the output voltage/current for the dual-VSI structure. This study currently is under patent procedure with number FR 15 50045 [21].

II. Decoupled Controlling Dual VSI

The power circuit configuration of the dual VSI supplying a three-phase open-end induction motor is depicted in Fig. 2. The hardware includes dual two-level inverters feeding both sides of open-end stator winding of an induction motor. Each VSI has the capability of independently synthesizing space vectors in $\alpha\beta$ asynchronous frame as

$$V^*_{i,x} = \sqrt{\frac{2}{3}} V_{\rm dc}\left(s_{a,i} + a s_{b,i} + a^2 s_{c,i}\right) \text{ where } a = e^{j\frac{2\pi}{3}} \quad (1)$$

where x (= 1 and 2) indicates VSI number and i (= from 1 to 2^3) represents the attainable switching combinations in a two-level VSI. In this equation, $V_{\rm dc}$ represents the dc-link voltage, and $s_{a,i}$, $s_{b,i}$, $s_{c,i}$ are the three-phase switching states. Either ON or OFF operation is represented by "+" or "−" in Fig. 3, respectively [22]. Where bottom switches operate complementary to top switches. Hence, each VSI produces 2^3 possible space vectors that build independent hexagon [23].

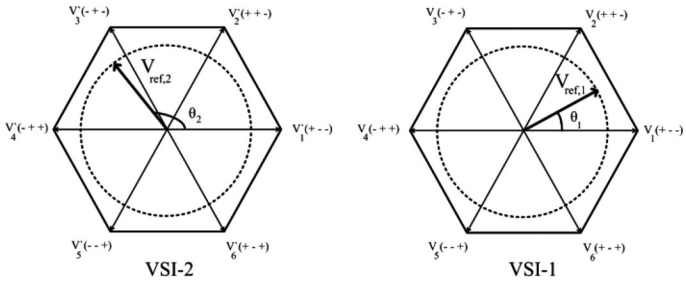

Fig. 3. Space vector diagram and references.

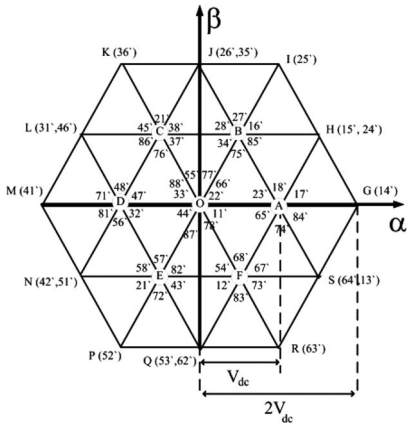

Fig. 4. Three-level space vector diagram for dual VSI.

In this paper, unlike previous concepts that force two references in dual VSI to be in opposite direction, two reference space vectors are constructed to take advantage of variable phase-angle displacement $\Delta\theta(=\theta_1-\theta_2)$. The space vectors obtained from (1) and space references for each VSI are shown in Fig. 3.

As defined in [19], the equivalent three-level space vectors for the dual VSI, as shown in Fig. 4, can be obtained from (1) as

$$V^*_{\rm comb} = V^*_{i,1} - V^*_{i,2}. \quad (2)$$

Thus, total possible switching combinations in dual VSI result in 64 ($2^3\times2^3$) space vectors spreading the $\alpha\beta$-frame over 19 space locations similar to the three-level VSI.

CMV, $v_{{\rm cmv},x}$, for the single VSI is represented based on instantaneous three-phase pole voltage ($v_{ao,x}$,$v_{bo,x}$, and $v_{co,x}$) as

$$v_{{\rm cmv},x} = \frac{1}{3}\left(v_{ao,x} + v_{bo,x} + v_{co,x}\right) \quad (3)$$

where x (= 1 and 2) represents inverter number. Finally, as defined in [15], ZSV, $v_{\rm zsv}$, for the dual inverter can be calculated as

$$v_{\rm zsv} = v_{{\rm cmv},1} - v_{{\rm cmv},2}. \quad (4)$$

Authors in [24] explained that one promising solution to completely eliminate ZSV would be synchronously applying $V_{\rm even}$ or $V_{\rm odd}$ at both sides of windings, where $V_{\rm even} \in \{V_2, V_4, V_6\}$ and $V_{\rm odd} \in \{V_1, V_3, V_5\}$.

TABLE I
ZSV FOR DUAL VSI

Number	Vector Combination	ZSV Level
1	**(8/7′)**	$-V_{\rm dc}$
2	**(8/4′),(8/6′),(8/2′),(5/7′), (3/7′), (1/7′)**	$-\frac{2V_{\rm dc}}{3}$
3	(8/5′), (8/3′), (5/4′), (3/4′), (8/1′), (5/2′), (3/6′), (3/2′), (4/7′), (1/4′), (1/6′), (1/2′), (6/7′), (2/7′), (5/6′)	$-\frac{V_{\rm dc}}{3}$
4	(8/8′), (5/5′), (5/3′), (3/5′), (3/3′), (4/4′), (5/1′), (3/1′), (4/6′), (4/2′), (1/5′), (1/3′), (6/4′), (2/4′), (1/1′), (6/6′), (6/2′), (2/6′), (2/2′), (7/7′)	0
5	(5/8′), (3/8′), (4/5′), (4/3′), (4/1′), (1/8′), (6/5′), (6/3′), (2/5′), (2/3′), (7/4′), (6/1′), (2/1′), (7/6′), (7/2′)	$\frac{V_{\rm dc}}{3}$
6	**(4/8′), (6/8′), (2/8′), (7/5′), (7/3′), (7/1′)**	$\frac{2V_{\rm dc}}{3}$
7	**(7/8′)**	$V_{\rm dc}$

TABLE II
CMV FOR DUAL VSI

Number	Vector Combination	CMV Level
1	**(8/8′)**	$-\frac{V_{\rm dc}}{2}$
2	**(1/8′), (3/8′), (5/8′), (8/1′), (8/3′), (8/5′)**	$-\frac{V_{\rm dc}}{3}$
3	(1/1′), (1/3′), (1/5′), (3/1′), (3/3′), (3/5′), (5/1′), (5/3′), (5/5′), (2/8′), (4/8′), (6/8′), (8/2′), (8/4′), (8/6′)	$-\frac{V_{\rm dc}}{6}$
4	(8/7′), (1/2′), (1/4′), (1/6′), (3/2′), (3/4′), (3/6′), (5/2′), (5/4′), (5/6′), (2/1′), (2/3′), (2/5′), (4/1′), (4/3′), (4/5′), (6/1′), (6/3′), (5/5′), (7/8′)	0
5	(2/2′), (2/4′), (2/6′), (4/2′), (4/4′), (4/6′), (6/2′), (6/4′), (6/6′), (1/7′), (3/7′), (5/7′), (7/1′), (7/3′), (7/5′)	$\frac{V_{\rm dc}}{6}$
6	**(2/7′), (4/7′), (6/7′), (7/2′), (7/4′), (7/6′)**	$\frac{V_{\rm dc}}{3}$
7	**(7/7′)**	$\frac{V_{\rm dc}}{2}$

Also, fed motor suffers from CMV issues like shaft voltage, ground currents, and bearing currents [19]. The CMV results from currents flowing in the paths provided by parasitic capacitors triggered by high switching frequencies of the VSI [25]. In a dual inverter, the CMV, $v_{\rm cmv}$, is defined as addressed in [26]

$$v_{\rm cmv} = \frac{1}{2}\left(v_{\rm cmv,1} + v_{\rm cmv,2}\right). \tag{5}$$

Each reference vector has possibilities to be constructed by selective vector groups as done in [14]–[19]. Assuming that the vectors applied at each interval by the first and second VSI are represented by (vector-1/vector-2') package, maximum ZSV can be produced by $(V_8/V_7{}')$ or $(V_7/V_8{}')$ pack, which leads to $\pm V_{\rm dc}$ (case 1 and 7 in Table I), or by $(V_{\rm even}/V_8{}')$, $(V_8/V_{\rm even}{}')$, $(V_{\rm odd}/V_7{}')$, and $(V_7/V_{\rm odd}{}')$, which lead to $\pm\frac{2V_{\rm dc}}{3}$ (case 2 and 6 in Table I), where V_7 and V_8, for both VSIs, are defined as $(+++)$ and $(---)$, respectively.

Using the same approach, maximum CMV is produced by using sets of $(V_7/V_7{}')$ or $(V_8/V_8{}')$, which lead to $\pm\frac{V_{\rm dc}}{2}$ (case 1 and 7 in Table II) or by $(V_{\rm odd}/V_8{}')$, $(V_8/V_{\rm odd}{}')$, $(V_{\rm even}/V_7{}')$ and $(V_7/V_{\rm even}{}')$, which lead to $\pm\frac{V_{\rm dc}}{3}$ (case 2 and 6 in Table II). Therefore, in order to decrease both the ZSV and the CMV, the use of null vectors in two VSIs should be avoided. So in the proposed method, in which active vectors are replaced by null ones, ZSV and CMV magnitude are limited to $\pm\frac{V_{\rm dc}}{3}$ and $\pm\frac{V_{\rm dc}}{6}$, respectively.

III. PROPOSED MODIFICATION AND MODULATION

In this section, principles of the proposed method are outlined from the standpoint of modulation, switching loss, and voltage/current THD. Percentage of switching losses not only is proportional to effective switching frequency, which is reduced by 66% in this paper, but also related to absolute magnitude of the output current while switching action.

In the first subsection, conventional space vector modulation (CSVM) is modified by avoiding null vector utilization to achieve switching loss and CMV mitigation. Hence, for each sector two phases are clamped to positive/negative dc rail. In the second subsection, concepts for synthesizing output voltage via adjusting phase-angle displacement between two reference vectors is formulated. Finally, losses and current/voltage THD for dual VSI is theoretically evaluated in the third and fourth subsection.

A. Modified CSVM

Modulation methods of dual-VSI fed open-end winding motor have been extensively researched with both carrier-based and space-vector-based PWMs. Application of CSVM results in 15% higher output voltage for a given dc bus voltage. Additionally, this leads to less harmonic content compared to the SPWM technique [27]. By projecting the reference vector on two nearby active vectors, the operating duty cycles are calculated as formulated in CSVM. By normalizing over the switching time interval, T_s, the duty cycle for each active vector can be expressed as: $\alpha_i = \frac{t_i}{T_s}$, where $i(=1$ to 6) denotes the sector number [28]. In order to fulfill the rest of the switching interval, α_0 $(=1-\alpha_i-\alpha_{i+1})$, null-vectors V_7 and V_8 are applied. Equation (6.a) and (6.b) express these duty cycles of active vectors, where modulation index M_i is defined as peak value of fundamental phase voltage, $V_{\rm peak}$, over that of square wave, $\frac{2V_{\rm dc}}{\pi}$

$$\alpha_i = \frac{2\sqrt{3}}{\pi} M_i \sin\left(i\frac{\pi}{3} - \theta\right) \tag{6.a}$$

$$\alpha_{i+1} = \frac{2\sqrt{3}}{\pi} M_i \sin\left(\theta - (i-1)\frac{\pi}{3}\right). \tag{6.b}$$

By equally dividing the null-vector duty cycle (α_0) into those of the two nearby active vectors, not only the CMV but also the effective switching frequency, which corresponds to switching losses, is suppressed. In fact, by applying just nearby active vectors, two legs are fixed to positive/negative dc rail, hence, just one leg is switched. By applying the previously discussed modifications, the modified duty cycles are expressed as

$$\alpha_{i(\rm new)} = \frac{1}{2} - \frac{3}{\pi} M_i \sin\left(\theta - \left(i - \frac{1}{2}\right)\frac{\pi}{3}\right) \tag{7.a}$$

$$\alpha_{i+1(\rm new)} = \frac{1}{2} + \frac{3}{\pi} M_i \sin\left(\theta - \left(i - \frac{1}{2}\right)\frac{\pi}{3}\right). \tag{7.b}$$

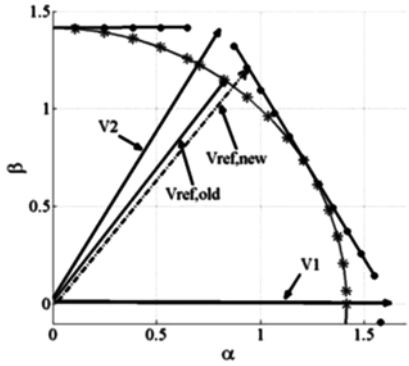

Fig. 5. Old and modified reference space vector for sector 1.

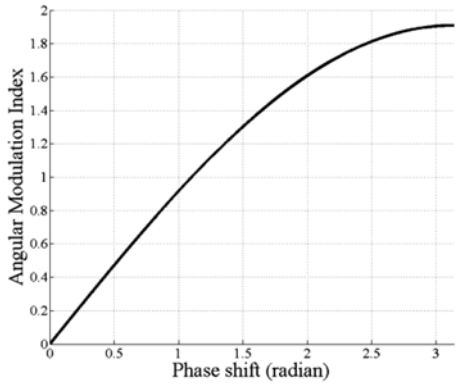

Fig. 6. AMI versus angle displacement.

Applying (7) instead of (6) into the controlling system, a new reference in the $\alpha\beta$-plane is achieved. The previously discussed modification transfers the original circular reference into a discontinuous-line reference at the surface of hexagon, as depicted in Fig. 5. After some algebra not reported here for the sake of brevity, the new reference voltage vector $\vec{V}_{\mathrm{ref,\,new}}$ is mathematically extracted as

$$\vec{V}_{ref,new} = \frac{\vec{V}_{i+1} + \vec{V}_i}{2} + (\alpha_{i+1} - \alpha_i)\,\frac{\vec{V}_{i+1} - \vec{V}_i}{2} \tag{8}$$

where $\vec{V}_i$ and $\vec{V}_{i+1}$ are two nearby space vectors, α_i and α_{i+1} are corresponding duty cycles extracted from CSVM by (6.a) and (6.b).

Fig. 5 shows that after applying the aforementioned modification, the VSI is forced to operate in the overmodulation region, where $\left(\frac{\sqrt{3}}{2} \approx \frac{\pi}{2\sqrt{3}}\right) \le M_i^{\mathrm{new}} \le \left(\frac{\pi}{6} + \frac{\sqrt{3}}{4} \approx \frac{3}{\pi}\right)$ with corresponding attainable voltage amplitude, V_{peak}, between $\left(\frac{\sqrt{3}}{\pi} \approx \frac{1}{\sqrt{3}}\right) V_{\mathrm{dc}}$ and $\left(\frac{1}{3} + \frac{\sqrt{3}}{2\pi} \approx \frac{6}{\pi^2}\right) V_{\mathrm{dc}}$ (the input voltage level is defined V_{dc}). In order to reach the highest possible output voltage levels for each VSI, a new modulation index $M_i^{\mathrm{new}} = \left(\frac{3}{\pi}\right)$ is desirable. As a consequence, tradeoff is formed here between number of commutations, which brings switching losses, and shrinking modulation index range. For instance, in the modified CSVM, the number of commutations within a switching interval is limited to two instead of six by applying symmetric sequence.

B. Proposed Angular Modulation

Previous papers have usually taken advantages of two opposite references $\Delta\theta = 180^\circ$ to yield desired output voltage [11]–[20]. However, in this paper, an AMI based on variable phase-angle displacement between two references is proposed, in order to minimize the commutation numbers while having full range modulation index. The open-end load requires the voltage across the two sides to be subtraction of the voltages produced by the first and second VSI, respecting virtual neutral point. However, note that each reference space vector can be separately built regardless of being in opposite direction, having $\Delta\theta(= \theta_1 - \theta_2)$.

The expressions in (9.a) and (9.b) specify the rotating fundamental space vectors, as shown in Fig. 3, where θ_x and $\vec{V}_{\mathrm{ref}x}$ are initial angle and magnitude of reference space vectors, respectively, and $x\ (= 1, 2)$

$$\vec{V}_{\mathrm{ref1}} = \vec{V}_{\mathrm{ref1}} \left(e^{j(\omega t + \theta_1)}\right) \tag{9.a}$$

$$\vec{V}_{\mathrm{ref2}} = \vec{V}_{\mathrm{ref2}} \left(e^{j(\omega t + \theta_2)}\right). \tag{9.b}$$

Assuming $\vec{V}_{\mathrm{ref1}} = \vec{V}_{\mathrm{ref2}}$ and making use of (9.a) and (9.b), the obtained voltage across the load can be cast as

$$\vec{V}_{\mathrm{ref}} = \vec{V}_{\mathrm{ref1}} - \vec{V}_{\mathrm{ref2}} = 2\vec{V}_{\mathrm{ref1}} \sin\left(\frac{\theta_1 - \theta_2}{2}\right) \left(e^{j(\omega t + \theta_t)}\right). \tag{10}$$

From (10) and due to $\vec{V}_{\mathrm{ref1}} = \frac{\sqrt{6}}{\pi} V_{\mathrm{dc}} M_i^{\mathrm{new}}$, AMI (11.a), which demonstrates nonlinear (sin-shaped) dependence on the phase shift, $\Delta\theta$, and initial phase angle, θ_t (11.b), can be extracted as

$$\mathrm{AMI} = \frac{\vec{V}_{\mathrm{ref}}}{\frac{\sqrt{6}}{\pi} V_{\mathrm{dc}}} = 2M_i^{\mathrm{new}} \sin\left(\frac{\theta_1 - \theta_2}{2}\right) \tag{11.a}$$

$$\theta_t = \frac{\pi}{2} + \frac{\theta_1 + \theta_2}{2}. \tag{11.b}$$

Fig. 6 shows the behavior of AMI versus phase shift $\Delta\theta(= \theta_1 - \theta_2)$ between two references. The proposed dual-VSI controlling scheme has the capability of having AMI up to twice $\left(2\left(\frac{3}{\pi}\right)\right)$ in comparison with maximum M_i of single VSI controlled by CSVM $\left(\frac{3}{\pi}\right)$. Hence, the voltage amplitude in the dual VSI controlled by AMI is function of angle displacement $\left(V_{\mathrm{peak}} = 2\left(\frac{6}{\pi^2}\right) V_{\mathrm{dc}} \sin\left(\frac{\theta_1 - \theta_2}{2}\right)\right)$ and can reach up to $2\left(\frac{6}{\pi^2}\right) V_{\mathrm{dc}}$. That means more dc-link voltage utilization as well as avoiding the need for an intermediate dc/dc conversion stage (in Fig. 1), suffering from low efficiency and massive passive components. Also for reaching the same desired output voltage, dual VSI requires less dc-link voltage level, thus imposing less voltage stress across the switches.

The desired output-voltage parameters, V_{peak} and θ_t, are conventionally demanded from the dual-VSI controller. In the proposed method, aforementioned parameters result in single

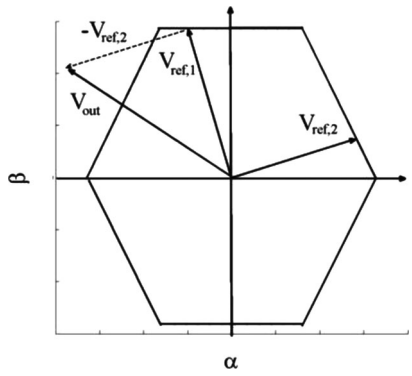

Fig. 7. Two reference space vectors and resulted voltage in $\alpha\beta$-plane.

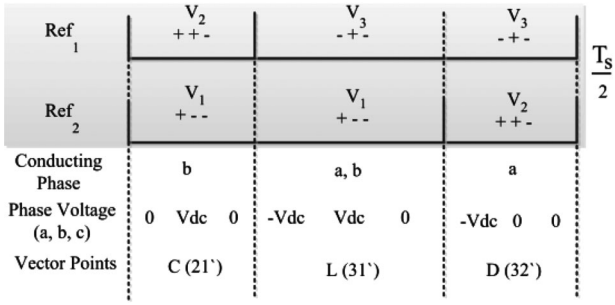

Fig. 8. Dual VSI features manipulated by AMI.

nonlinear equation as

$$V_{\text{peak}} = \frac{12V_{\text{dc}}}{\pi^2}\cos\left(\theta_t - \theta_1\right),\ \text{where}\ \theta_t - \theta_1 = \frac{\pi}{2} - \frac{\theta}{2}. \tag{11.c}$$

Hence, values of initial phase angles (θ_1 and θ_2) for both reference voltages can be calculated from (11.b) and (11.c) as

$$\begin{cases} \theta_1 = \theta_t - \cos^{-1}\left(\dfrac{\pi^2 V_{\text{peak}}}{12V_{\text{dc}}}\right) \\ \theta_2 = \theta_t - \pi + \cos^{-1}\left(\dfrac{\pi^2 V_{\text{peak}}}{12V_{\text{dc}}}\right). \end{cases} \tag{11.d}$$

As discussed in Section III-A, for each VSI, $M_i^{\text{new}} = \left(\frac{3}{\pi}\right)$ is reached. Eventually, by replacing instantaneous value of θ (which is $\omega t + \theta_1$ and $\omega t + \theta_2$ for the first and second VSI, respectively) in (7.a) and (7.b), operating duty cycles for nearby active vectors can be extracted, for each VSI.

For instance, the equivalent output voltage of dual VSI is shown in Fig. 7, at $t = 0$ and for $\theta_1 = 110^\circ$ and $\theta_2 = 20^\circ$. The system features in half of the switching interval, $\frac{T_s}{2}$, are elaborated such that VSI-2 reference space vector lies at sector 1 and VSI-1 is placed 90° leading at sector 2. Note that space vectors are implemented through symmetric sequence as: $V_i \rightarrow V_{i+1} \rightarrow V_i$.

The applied vectors are shown in Fig. 8, at which the $\frac{T_s}{2}$ is divided into three parts. Based on Fig. 7, VSI-1 switches active vectors of V_2 and V_3 and VSI-2 employs V_1 and V_2. Conducting phases, detected by $\left(s_{y,1} - s_{y,2}\right) i_y$, and dropped phase voltage, obtained by $\left(s_{y,1} - s_{y,2}\right) V_{\text{dc}}$, are explained, where $y = a,\ b,$ and c. Applied vector packages, *(Vector-1/Vector-2)*, in each subinterval correspond to vector points in three-level diagram of the dual VSI. For instance, set of (2/1′) is associated with point "*C*" in Fig. 4.

C. Switching Loss Evaluation

Based on the modified CSVM, each reference space vector is formed with just two nearby active vectors. Thus, at each sector, two legs are forced to be fixed while just one leg is modified. Current on phase "*a*" is modulated at sector 2 (where $V_2(++-)$ and $V_3(-+-)$ are implemented) and sector 5 (where $V_5(--+)$ and $V_6(+-+)$ are implemented), and found to be within $\pm 60^\circ$ of zero-crossing points in case of resistive load. So for this situation, sector 2 and 5 correspond to minimum absolute magnitude of the current which imposes minimum switching losses. This discussion involves the evaluation of the load power factor $\cos(\text{Ø})$ for the proposed method. By applying the same approach, current on phase "*b*" and "*c*" are switched at sectors 1, 4 and 3, 6, respectively.

In dual-VSI configuration, the voltage stress across switches is equal to dc-link voltage, V_{dc}, and the current stress is equal to following current. Thus, switching losses for one phase can be expressed in analogy to the single VSI modulated by CSVM addressed in [30] as

$$\begin{aligned} P_{\text{SW}} &= \frac{1}{2\pi}\int_0^{2\pi} E_{\text{SR}}\frac{\left|I_m\cos(\omega t)\right|.V_{\text{dc}}}{I_{\text{ref}}.V_{\text{ref}}} f_s d(\omega t) \\ &= \frac{2}{\pi}\frac{E_{\text{SR}}.I_m.f_s.V_{\text{dc}}}{I_{\text{ref}}.V_{\text{ref}}} \end{aligned} \tag{12}$$

where E_{SR}, V_{ref}, and I_{ref} are the reference parameters. The same mathematical approach is implemented for current on phase "a" of a single VSI modulated by modified CSVM to formulate losses, respecting balanced-load angle Ø as

$$P_{\text{SW}} = \frac{1}{2\pi}\left[\begin{aligned} &\int_{-\frac{2\pi}{3}}^{-\frac{\pi}{3}} E_{\text{SR}}\frac{\left|I_m\cos(\omega t - \text{Ø})\right|.V_{\text{dc}}}{I_{\text{ref}}.V_{\text{ref}}} f_s d(\omega t) + \\ &\int_{\pi/3}^{2\pi/3} E_{\text{SR}}\frac{\left|I_m\cos(\omega t - \text{Ø})\right|.V_{dc}}{I_{\text{ref}}.V_{\text{ref}}} f_s d(\omega t) \end{aligned}\right]. \tag{13}$$

After simplifications, power losses can be expressed as the function of the power factor as

$$P_{\text{SW}} = \frac{k}{\pi}\frac{E_{\text{SR}}.I_m.f_s.V_{\text{dc}}}{I_{\text{ref}}.V_{\text{ref}}} \tag{14.a}$$

$$k = \begin{cases} 2 - \sqrt{3}\left|\cos(\text{Ø})\right|, \left|\cos(\text{Ø})\right| \geq \dfrac{\sqrt{3}}{2} \\ \left|\sin(\text{Ø})\right|, \text{others}. \end{cases} \tag{14.b}$$

Equation (14.b) indicates that the highest loss percentage, $\frac{1}{\pi}$, can be obtained at full inductive/capacitive load situation. However, switching losses still reach 50% reduction ($\frac{2}{\pi}$ for CSVM in comparison with the highest value for modified CSVM $\frac{1}{\pi}$).

In dual-VSI circuit configuration, each VSI imposes individual switching loss related to the angle between the output current and corresponding reference voltage vector, Ø1 and Ø2

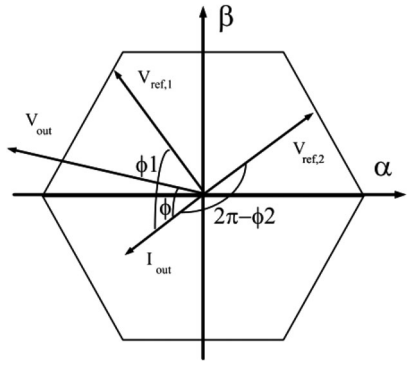

Fig. 9. Load angle definitions for dual VSI ($\phi 1$ and $\phi 2$).

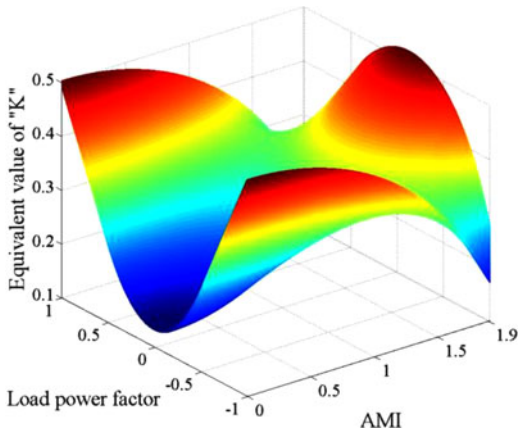

Fig. 10. Equivalent value of "*K*" versus AMI and load power factor.

(where $\emptyset 1$ and $\emptyset 2$ are extracted as: $\emptyset 1 = \frac{\pi}{2} + \emptyset - \frac{\theta_1 - \theta_2}{2}$ and $\emptyset 2 = \frac{\pi}{2} + \emptyset + \frac{\theta_1 - \theta_2}{2}$).

In Fig. 9, two space references ($V_{\mathrm{ref},1}$ and $V_{\mathrm{ref},2}$), desired voltage (V_{out}), load current (I_{out}), and load angle definitions ($\emptyset 1$ and $\emptyset 2$) are shown. The reference space vectors are in sectors 1 and 3, hence, the modulated currents on phase "*b*" and "*c*" produce switching losses.

Eventually, total switching losses, in dual-VSI structure, is equal to the sum of losses separately produced by each VSI. Therefore, from (14), this yields

$$P_{\mathrm{SW\_dual}} = \frac{2}{\pi}\left(\frac{k_1 + k_2}{4}\right)\frac{E_{\mathrm{SR}}.I_m.f_s.V_{\mathrm{dc}}}{I_{\mathrm{ref}}.V_{\mathrm{ref}}} \tag{15.a}$$

$$k_x = \begin{cases} 2 - \sqrt{3}\left|\cos\left(\emptyset_x\right)\right|, \left|\cos\left(\emptyset_x\right)\right| \geq \dfrac{\sqrt{3}}{2} \\ \left|\sin\left(\emptyset_x\right)\right|, \text{others} \end{cases} \tag{15.b}$$

where $x = 1, 2$ represents VSI number, respecting equivalent load angles ($\emptyset 1$ and $\emptyset 2$). Fig. 10 shows 3-D curve of equivalent $K(= \frac{k_1 + k_2}{4})$ for dual VSI operated by the proposed method versus AMI and load power factor $\cos(\emptyset)$. Switching losses are highly reduced by 50–86.6% in comparison with that of a single VSI modulated by CSVM. This 3-D curve indicates that three peaks in switching loss curve can happen when system operates either at low AMI (0) and high absolute power factor (± 1) or at high AMI ($2 \times \left(\frac{3}{\pi}\right)$) and low absolute power factor (0).

D. Voltage and Current THD Evaluation

In this subsection, theoretical assessments of voltage/current THD of the proposed method are derived. The Fourier series is used for analyzing phase voltage of each VSI (v_{ao} and $v_{a'o}$), respecting midpoint of dc source. For simplicity, the representation in the complex plane is applied as

$$\begin{cases} v_{ao}(\theta) = \displaystyle\sum_{n=-\infty}^{\infty} V_{n,1}^* e^{jn\theta} \\ V_{n,1}^* = \dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} \left(v_{ao}(\theta)\right) e^{-jn\theta} d\theta \end{cases} \tag{16.a}$$

$$\begin{cases} v_{a'o}(\theta) = \displaystyle\sum_{n=-\infty}^{\infty} V_{n,2}^* e^{jn\theta} \\ V_{n,2}^* = \dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} \left(v_{a'o}(\theta)\right) e^{-jn\theta} d\theta \end{cases} \tag{16.b}$$

where n denotes the integer numbers. The symmetric feature of the three-phase system allows reducing the integral calculus of $V_{n,1}^*$ and $V_{n,2}^*$ to just one sector (in this study, sector number 1), the obtained results being valid also for the other five sectors. This yields

$$V_{n,1}^* = \frac{1 - (-1)^n}{2\pi}\int_0^{\frac{\pi}{3}} \begin{pmatrix} v_{ao}(\theta) \\ -(-a)^n v_{bo}(\theta) \\ +(a)^{2n} v_{co}(\theta) \end{pmatrix} e^{-jn\theta} d\theta \tag{17.a}$$

$$V_{n,2}^* = \frac{1 - (-1)^n}{2\pi}\int_0^{\pi/3} \begin{pmatrix} v_{a'o}(\theta) \\ -(-a)^n v_{b'o}(\theta) \\ +(a)^{2n} v_{c'o}(\theta) \end{pmatrix} e^{-jn\theta} d\theta \tag{17.b}$$

where $a = e^{j2\pi/3}$. Simplifying (17), even harmonics are eliminated while odd ones are divided into: direct harmonic ranks ($6n + 1$), inverse harmonic ranks ($6n - 1$), and zero sequence harmonic ranks ($6n + 3$). By applying Clark transform, the Fourier coefficients for these ranks are given as

$$V_{6n+1,x}^* = \sqrt{\frac{3}{2}}\frac{1}{\pi}\int_0^{\pi/3} V_{i,x}^* e^{-j(6n+1)\theta} d\theta \tag{18.a}$$

$$V_{6n-1,x}^* = \sqrt{\frac{3}{2}}\frac{1}{\pi}\int_0^{\frac{\pi}{3}} \overline{V_{i,x}^*} e^{-j(6n-1)\theta} d\theta \tag{18.b}$$

$$V_{6n+3,x}^* = \frac{3}{\pi}\int_0^{\pi/3} v_{\mathrm{cmv},x} e^{-j(6n+3)\theta} d\theta \tag{18.c}$$

where $x = 1, 2$ denotes the VSI, and $V_{i,x}^*$ and $v_{\mathrm{cmv},x}$ are given by the (1) and (3), respectively. Values of $\overline{V_{i,x}^*}$, $V_{i,x}^*$, and $v_{\mathrm{cmv},x}$ for the first VSI controlled by the modified CSVM and with reference vector falling into the first sector are provided in Fig. 11

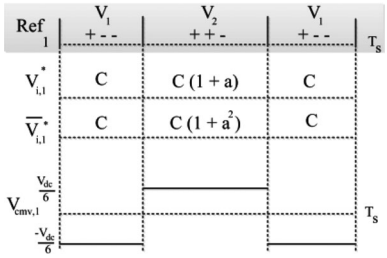

Fig. 11. $V^*_{i,1}$, $\overline{V^*_{i,1}}$, and $v_{\mathrm{cmv},1}$ for the first VSI at sector 1.

over one sampling interval, T_s, where the constant, C, is given by $\sqrt{\frac{2}{3}}V_{\mathrm{dc}}$.

By taking *K* samples over each sector, (18) is divided into *K* partial integrals for direct (19.a), inverse (19.b), and zero sequence (19.c) harmonic ranks as

$$V^*_{6n+1,x} = \frac{aV_{\mathrm{dc}}}{-j\pi\,(6n+1)}\left(a + \sum_{k=1}^{k=K}\begin{pmatrix} e^{-j(6n+1)\theta^B_{2,x}} \\ -e^{-j(6n+1)\theta^B_{1,x}}\end{pmatrix}\right) \tag{19.a}$$

$$V^*_{6n-1,x} = \frac{a^{-1}V_{\mathrm{dc}}}{-j\pi\,(6n-1)}\left(a^{-1} + \sum_{k=1}^{k=K}\begin{pmatrix} e^{-j(6n-1)\theta^B_{2,x}} \\ -e^{-j(6n-1)\theta^B_{1,x}}\end{pmatrix}\right) \tag{19.b}$$

$$V^*_{6n+3,x} = \frac{V_{\mathrm{dc}}}{-j\pi\,(6n+3)}\left(1 + \sum_{k=1}^{k=K}\begin{pmatrix} e^{-j(6n+3)\theta^B_{2,x}} \\ -e^{-j(6n+3)\theta^B_{1,x}}\end{pmatrix}\right) \tag{19.c}$$

where $\theta^B_{1,x}$ and $\theta^B_{2,x}$ for the first and the second VSI, respectively, are defined as

$$\theta^B_{2,x} = \frac{\pi}{3K}\left(k - \frac{1}{2} + \frac{\alpha_{2(\mathrm{new}),x}}{2}\right) \tag{20.a}$$

$$\theta^B_{1,x} = \frac{\pi}{3K}\left(k - \frac{1}{2} - \frac{\alpha_{2(\mathrm{new}),x}}{2}\right). \tag{20.b}$$

where k is an integer between *1* and *K*. In (20), $\alpha_{2(\mathrm{new}),1}$ and $\alpha_{2(\mathrm{new}),2}$ are brought from Section III-A [see (7.a)], and at the same M_i, can be expressed as

$$\alpha_{2(\mathrm{new}),1} = \alpha_{2(\mathrm{new}),2} = \frac{1}{2} + \frac{3}{\pi}M_i \sin\left(\left(k - \frac{1}{2}\right)\frac{\pi}{3K} - \frac{\pi}{6}\right). \tag{21}$$

The previously discussed expressions allow simplifying THD_V analysis for dual-VSI configuration avoiding complexity of the system as well as high number of possibilities. Dropped voltage across the load is expressed as the difference of the voltages synthesized by VSIs respecting predetermined phase-angle displacement, $\Delta\theta$, in which this concept also is valid for the Fourier coefficients as

$$V^*_{2n+1} = V^*_{2n+1,1} - V^*_{2n+1,2}e^{-j(2n+1)(\Delta\theta)} \tag{22}$$

where V^*_{2n+1} represents all harmonic ranks in (19) and $\Delta\theta$ should be expressed at the center of each sampling interval as: $\Delta\theta = \left(k' - \frac{1}{2}\right)\frac{\pi}{3K}$ and k' is an integer between *1* and *3K* to let the $\Delta\theta$ covers the whole range from 0 to π.

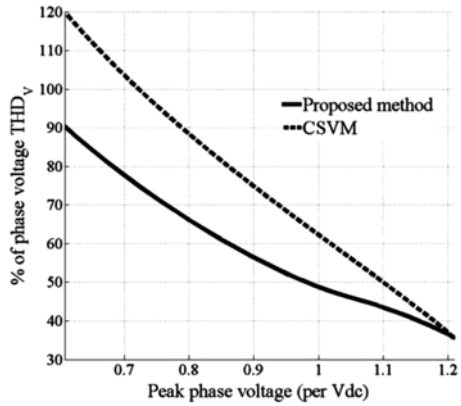

Fig. 12. THD_V of phase voltage in dual VSI versus V_{peak}.

From the formulation of output voltage harmonics in (22), the THD factor for voltage, THD_V, can be expressed as

$$\mathrm{THD}_V = \sqrt{2\sum_{n=1}^{\infty}\left|\frac{V^*_{2n+1}}{V^*_1}\right|^2}. \tag{23}$$

The expression of THD for current, THD_I, is derived from the expressions of current harmonics. Respecting current definition, ($I^*_{2n+1} = \frac{V^*_{2n+1}}{Z^*_{2n+1}}$), this is sufficient to take into account the harmonic impedance of the load, which is identified by resistive (*R*) and inductive (*L*) parameters. Since, harmonic impedance for the odd harmonics is given by

$$Z^*_{2n+1} = R + j\,(2n+1)\,L\omega. \tag{24}$$

The current harmonics can be written as

$$I^*_{2n+1} = \frac{V^*_{2n+1}}{R}\cos\left(\phi_{2n+1}\right)e^{j\phi_{2n+1}} \tag{25}$$

where $\phi_{2n+1} = \tan^{-1}\left((2n+1)\tan(\varnothing)\right)$. From these expressions, THD_I is expressed as

$$\mathrm{THD}_I = \sqrt{2\sum_{n=1}^{\infty}\left|\frac{I^*_{2n+1}}{I^*_1}\right|^2} = \sqrt{2\sum_{n=1}^{\infty}\left|\frac{V^*_{2n+1}}{V^*_1}\frac{cos\left(\phi_{2n+1}\right)}{cos\left(\phi\right)}\right|^2}. \tag{26}$$

Fig. 12 represents the THD_V, resulted from (23), for both CSVM and modified CSVM versus peak phase voltage (V_{peak}) for values between $\left(\frac{6}{\pi^2}\right)V_{\mathrm{dc}}$ and $2\left(\frac{6}{\pi^2}\right)V_{\mathrm{dc}}$. In Section IV, the reason of choosing this boundary is discussed. As an explicative example, Fig. 13 shows THD_I versus predetermined V_{peak} for $\cos(\phi) = \frac{\sqrt{3}}{2} = 0.866$.

IV. Simulation and Experimental Results

A prototype consisting of a dual three-phase two-level VSI produced by ARCEL, an open-end squirrel-cage medium-power induction motor coupled to a dc motor as shaft load, and rectifier as dc source are assembled in the laboratory as shown in Fig. 14. The proposed algorithm for the dual VSI is implemented in a full digital system by programming digital signal processor

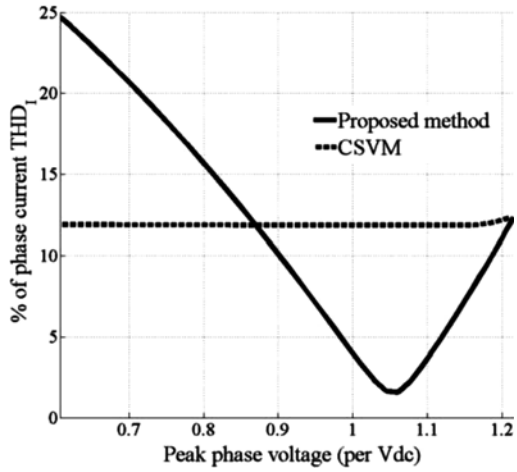

Fig. 13. THD_I of phase current in dual VSI versus V_{peak} at $\cos(\emptyset) = 0.866$.

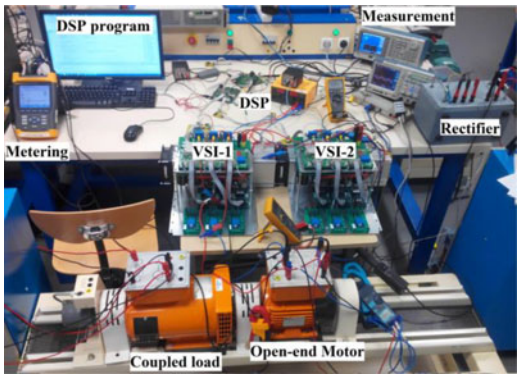

Fig. 14. Experimental setup.

(DSP), model RSF562TAADFH. Also, the simulation results are carried out based on the same system parameters through MATLAB/Simulink environment. The switching frequency f_s is chosen to take 27 samples within a sector (8.1 kHz). The dc-link voltage, labeled in Fig. 2 as V_{dc}, approximately equals to 270 V, and fundamental frequency f_o is set to 50 Hz.

In order to accurately compare THD of the phase voltage/current, which are resulted from MATLAB/Simulink (due to two independent definitions, AMI and M_i), the peak value of fundamental phase voltage V_{peak} is considered as x-axis in Figs. 15 and 16. These profiles are plotted for $\mathrm{AMI} > \left(\frac{3}{\pi}\right)$ or $M_i > \left(\frac{3}{2\pi}\right)$, which results in $V_{\mathrm{peak}} > \left(\frac{6}{\pi^2}\right) V_{\mathrm{dc}}$, in the proposed method or CSVM, respectively. Also, maximum peak phase voltage is limited to $V_{\mathrm{peak}} = 2\left(\frac{6}{\pi^2}\right) V_{\mathrm{dc}}$, wherein $\mathrm{AMI} = \left(\frac{6}{\pi}\right)$ or $M_i = \left(\frac{3}{\pi}\right)$.

The proposed method assures lower values for phase-voltage THD as shown in Fig. 15. Moreover, the current THD (see Fig. 16) has superior performance for relatively high values of V_{peak}. By comparing simulation results (see Figs. 15 and 16) with theoretical evaluations (see Figs. 12 and 13) in Section III-D, close agreement is observed.

THD_V is worsened in both methods, via generating low-amplitude voltage. Therefore, for $\mathrm{AMI} < \left(\frac{3}{\pi}\right)$, in which desired

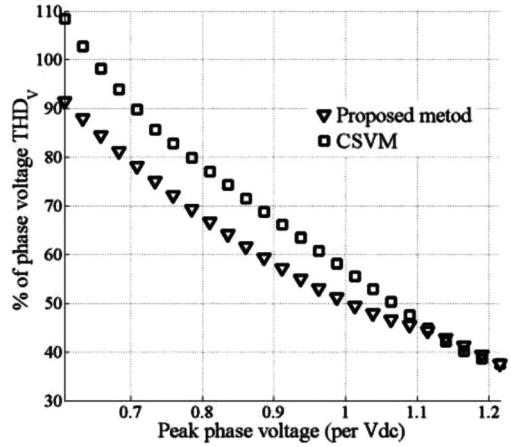

Fig. 15. THD_V of phase voltage in dual VSI versus V_{peak}.

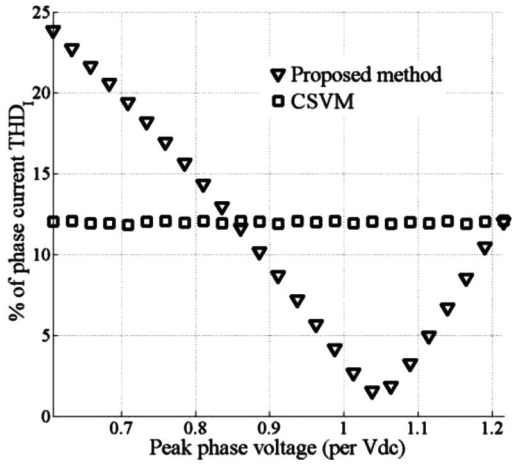

Fig. 16. THD_I of phase current in dual VSI versus V_{peak} at $\cos(\emptyset) = 0.866$.

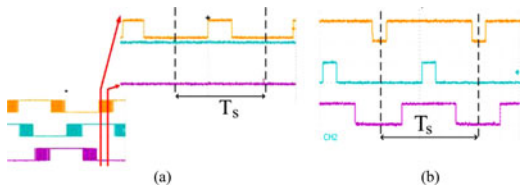

Fig. 17. Experimental results of controlling signals, where $T_s = \frac{1}{f_s}$. (a) Modified SVM. (b) CSVM.

voltage can be synthesized by operating one VSI, one of the VSIs should be clamped to positive/negative dc rail, while another is manipulated by CSVM.

Controlling signals for a VSI, employing CSVM and the modified CSVM, are illustrated in Fig. 17. As shown, in modified CSVM, effective switching frequency is reduced by 66%, which, consequently, brings lower switching losses.

One of the most important characteristics of power conversions is namely efficiency, especially for electrical/hybrid vehicle applications. This parameter is experimentally evaluated

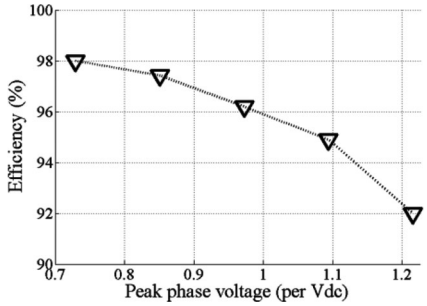

Fig. 18. Efficiency of the proposed method versus $V_{\rm peak}$.

for the proposed method with driving open-end squirrel-cage induction motor at nominal power, 1.5 kW. The same hardware (i.e., VSI, DSP, measurement devices, etc.) is employed for fairly comparing efficiency of the proposed method with that of CSVM, which is measured around 90%.

Fig. 18 shows efficiency of the proposed method versus $V_{\rm peak}$. As stated in Section III-C (see Fig. 10), the switching losses are averagely enhanced with increasing AMI, this leads to efficiency reduction as experimentally proved in Fig. 18. We used *FLUK 434 power quality analyzer* and *LEM LH1050* to measure input/output power. Note that error of these devices should be considered around 2–3%.

The ZSV, CMV, and low-order voltage feature of the proposed method is compared with those of CSVM, analyzed in [19] and [26]. The CMV and ZSV first of all are simulated through MATLAB/Simulink environment, and then, experimentally evaluated.

Fig. 19 shows the aforementioned features over one sampling interval. The CMV profile in the proposed method not only contains fewer voltage levels, 3 instead of 5 in CSVM, but also avoids attending the highest absolute CMV, $\pm\frac{V_{\rm dc}}{2} = \pm 135$ V, which appears in CSVM. Instantaneous ZSV profiles meet the same feature such as: voltage level and magnitude.

The top traces in Fig. 20(a) and (b) show ZSV, in which in both figures, voltage at point "1" equals to $\frac{V_{\rm dc}}{3}$. Also, CMV in Fig. 20(a), for dual VSI controlled with the proposed algorithm, contains $-\frac{V_{\rm dc}}{6}$ and $\frac{V_{\rm dc}}{6}$ at points "2" and "3," respectively. And finally, CMV in Fig. 20(b), for dual VSI modulated by CSVM, leads to $-\frac{V_{\rm dc}}{6}$, $\frac{V_{\rm dc}}{6}$, $-\frac{V_{\rm dc}}{2}$, $\frac{V_{\rm dc}}{2}$ at points "2," "3, "4," and "5," respectively. The CMV and ZSV are obtained from simulation (see Fig. 19) and experimental results (see Fig. 20) with values in Tables I and II are in a satisfactory agreement.

From MATLAB/Simulink environment, low-order phase-voltage THD for dual VSI controlled by the proposed method and CSVM is extracted as 5.68% and 20.71%, respectively. This eye-catching reduction can be observed by comparing Fig. 21 (a) and (b). Moreover, peak value of the fundamental phase voltage is calculated using an FFT analyzer block as 280 V, which is close to the value, 284 V, predicted by $V_{\rm peak} = {\rm AMI}\left(\frac{2}{\pi}\right)V_{\rm dc}$ at AMI = 1.654.

V. Conclusion

This paper deals with an AMI controlling method for dual-VSI configuration, while each VSI is modulated by the modified

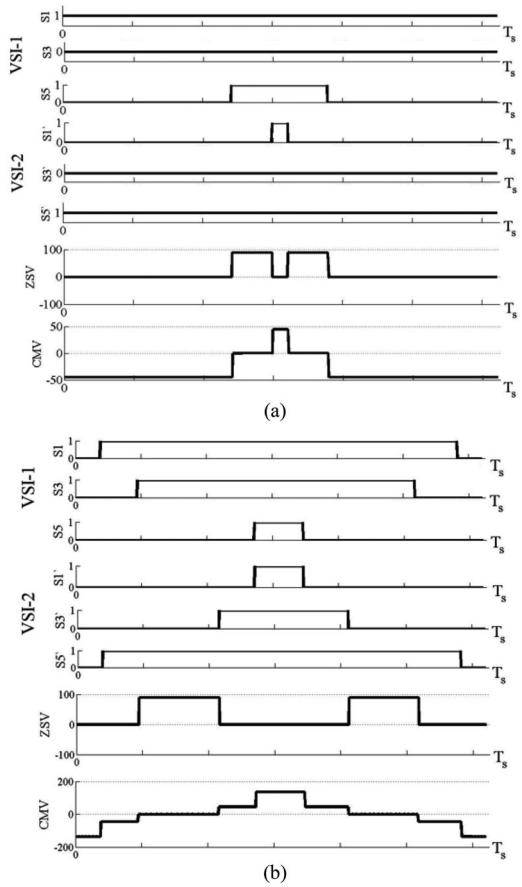

Fig. 19. Simulation results of ZSV/CMV in dual VSI controlled by: (a) proposed method at AMI = 1.6 (b) CSVM at $M_i = 0.8$, where $T_s = \frac{1}{f_s}$.

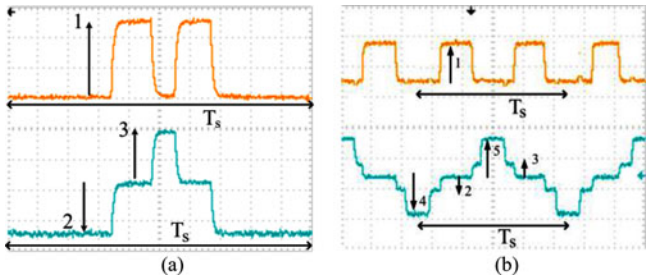

Fig. 20. Experimental results of ZSV/CMV of dual VSI operated by: (a) proposed method at AMI = 1.6 (b) CSVM at $M_i = 0.8$, where $T_s = \frac{1}{f_s}$.

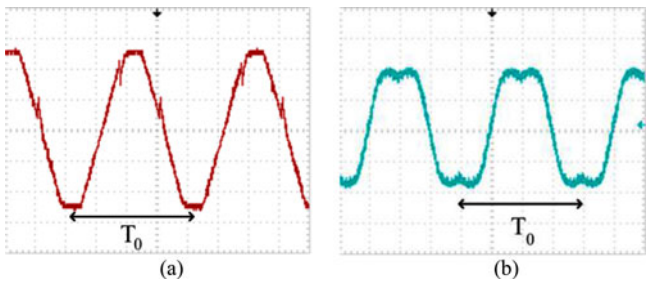

Fig. 21. Experimental result of low-order phase voltage in dual VSI controlled by: (a) proposed method at AMI = 1.654 (b) CSVM at $M_i = 0.827$, where $T_o = \frac{1}{f_o}$.

CSVM. The benefits of the proposed approach are theoretically and experimentally evaluated in this paper, by showing that the desired reference space vector has capability of being generated with adjusting appropriate phase-angle displacement between two references instead of forcing these to be in opposite direction.

AMI shows nonlinear sine-shaped profile versus angle displacement and contains full coverage feature. Modified CSVM is employed not only in order to highly suppress effective switching frequency but also to limit CMV levels and THD value.

Moreover, this paper introduces a promising solution to enhance efficiency, especially for electrical/hybrid vehicle applications by achieving at least 50% reduction in switching losses. This paper offers the pioneering approach to accurately extract voltage/current THD for the dual-VSI structure. The proposed method entirely reduces THD of the phase voltage and partially THD of the phase current.

Not only simulation and experimental results but also analytical approaches have proven that peak value of CMV meets reduction by 66% in a dual VSI modulated by the proposed method. Also, THD of the low-order phase voltage takes lower values. These features make the proposed method a strong candidate to be used in dual VSI without adding extra hardware, expenses, or complex calculation.

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