A Three-State Switching Boost Converter Mixed With Magnetic Coupling and Voltage Multiplier Techniques for High Gain Conversion

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***Abstract*— An asymmetrical three-state switching boost converter, combining the benefits of magnetic coupling and voltage multiplier techniques, is presented in this paper. The derivation procedure for the proposed topology is depicted. The new converter can achieve a very high-voltage gain and a very low-voltage stress on the power devices without high turn ratio and extreme duty cycles. Thus, the low-voltage-rated MOSFETs with low resistance r_{DS}(ON) can be selected to reduce the switching losses and cost. Moreover, the usage of voltage multiplier technique not only raises the voltage gain but also offers lossless passive clamp performance, so the voltage spikes across the main switches are alleviated and the leakage-inductor energy of the coupled inductors can be recycled. In addition, the interleaved structure is employed in the input side, which not only reduces the current stress through each power switch, but also constrains the input current ripple. In addition, the reverse-recovery problem of the diodes is alleviated, and the efficiency can be further improved. The operating principles and the steady-state analysis of the presented converter are discussed in detail. Finally, a prototype circuit with 400-W nominal rating is implemented in the laboratory to verify the performance of the proposed converter.**

***Index Terms*—Magnetic coupling, three-state switching, high-gain boost converter, voltage multiplier.**

I. Introduction

THE high step-up voltage gain dc–dc converters are widely used as an interface between the available low-voltage sources and the output loads, which are operated at much higher voltage [1]–[10]. Examples of such applications include high-intensity discharge lamp for automotives, dc back-up energy systems for uninterruptible power supplies, fuel-cell energy-conversion systems, photovoltaic generation systems, telecom back-up facilities, electric vehicles, and fuel cell vehicles. In above industrial applications, the high step-up dc–dc converters can be nonisolated but they should be operated at high efficiency, while taking high currents from low-voltage dc sources at their inputs. Generally, the classical boost is a popular choice for nonisolated applications because of a simple structure and a continuous input current. However, it will be operated at extreme duty cycle, and the rectifier diode must sustain a short pulse current with high amplitude when an extreme high-voltage gain is required. This leads to severe reverse recovery and the electromagnetic interference (EMI) problems. Moreover, the boost switch has to block a high-output voltage, and hence, the ON-state resistance r_{DS}(ON), which varies almost proportionally with the square of blocking voltage, will be very high so that low-voltage-rated MOSFETs may not be adopted. For those reasons, it is hard for a basic boost converter to achieve both high voltage conversion ratio and high efficiency at the same time.

Some single-switch high step-up boost converters were recently presented in many literatures [11], [12]. Use of cascade of converters is a feasible method for getting a desired voltage gain. In addition, previous single-switch converters with high gain also include quadratic boost type [13], voltage-lift type [14], switched-capacitor or switched-inductor type [15], and diode–capacitor voltage-multiplier type [16]. Although these converters can achieve higher voltage gain than the basic boost converter, the voltage gain of the converters is determined only by the duty cycle of the active switch. Thus, these converters must cascade more power stages to obtain higher voltage gain, which will result in the complex circuit and low efficiency. Many converters have been developed to achieve a high step-up voltage ratio without using an extreme duty cycle by using tapped inductor or coupled inductor [17]–[27]. However, the leakage-inductor energy of the coupled inductor may cause higher voltage stress on an active switch. For this reason, the converters with an active-clamp circuit have also been researched [22], [23], in which the cost and the circuit complexity are increased. The boost-flyback converters using the coupled inductor and output stacking techniques are proposed [24], which presents low-voltage stress across the switch, and the leakage-inductor energy of the coupled inductor is recycled to the output, but it must be noted that the single active switch will suffer high-current stress during the switch-on period for high step-up applications for the aforementioned converters, which is nontrivial to get higher power. Therefore, it is a major challenge to operate a single-switch boost converter at high efficiency for high step-up voltage gain.

As a prominent solution for high input current applications, some interleaved boost converters based on the three-state

Manuscript received May 5, 2014; revised May 17, 2015; accepted June 23, 2015. Date of publication July 8, 2015; date of current version November 30, 2015. This work was supported by the Anhui Provincial Natural Science Foundation (1408085ME80), the Natural Science Foundation of Anhui Education Committee (KJ2012A048), and the National Natural Science Foundation (51577002). Recommended for publication by Associate Editor T.-F. Wu.

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Digital Object Identifier 10.1109/TPEL.2015.2453634

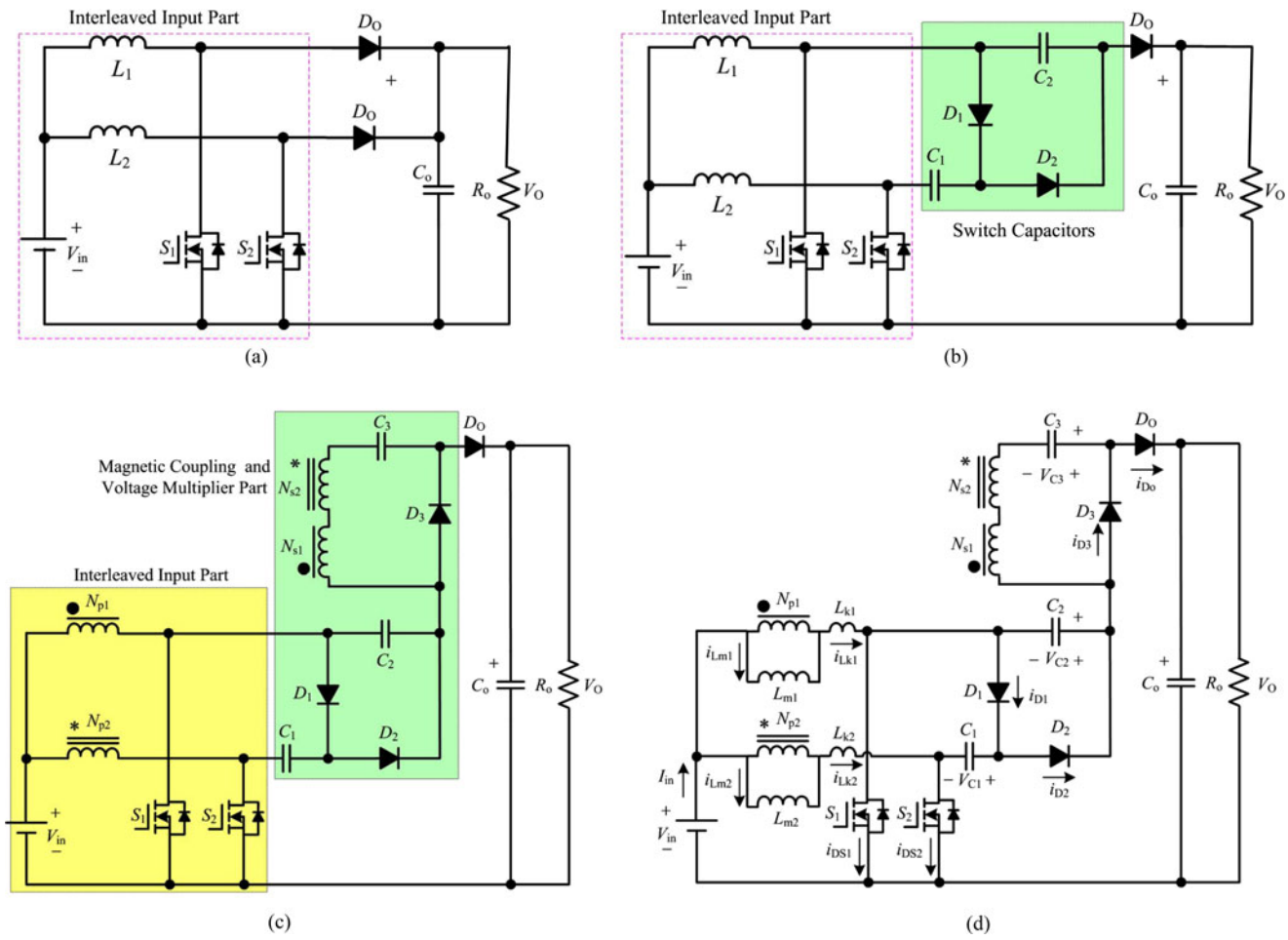

Fig. 1. Procedure to obtain the proposed converter mixed with magnetic coupling and voltage multiplier. (a) Conventional interleaved boost converter. (b) Interleaved boost converter integrating switched capacitors. (c) Circuit configuration of the proposed converter. (d) Equivalent circuit of the proposed converter.

switching cell (3SSC) have been proposed [28]–[41]. It has been demonstrated that the interleaved technique based on 3SSC can provide the advantages of partially input current ripple cancellation, doubling the switching frequency, and reducing the passive component size [29]. However, the voltage gain of a conventional interleaved boost is the same as the classical boost converter, and the voltage stress of the switches is still equivalent to the output voltage. To improve the voltage gain, several three-state switching high step-up boost converters have been presented by using voltage multiplier cells of diodes and capacitors [29], [30] whose advantages are: the input current is continuous with low ripple; the voltage stress across the switches is limited to half of the output voltage for the configuration with just one multiplier stage, and naturally clamped by one output filter capacitor. As possible drawbacks, more diodes and capacitors are needed for higher voltage gain, which leads to complex circuit and high cost. Another interleaved high step-up converters with transformers or coupled inductors are proposed [31]–[37], which can get a considerably high-voltage conversion ratio by increasing the number of turns ratio. A family of interleaved high step-up boost converters with winding-cross-coupled inductors is presented [38], where a modified-coupled inductor with three windings and its third winding inserted into another phase is proposed [39], [40], achieving good performance. Unfortunately, it is difficult to design the coupled inductor including three windings for the industrial manufacture. Also, once the current-flowing path of the leakage inductor is cut and the energy of leakage inductor cannot be released to output totally, some energy may dissipation on switch. Thus, the active-clamp circuit for coupled-inductor converter is used, which can recycle the energy of leakage, but the cost increases due to the extra power switch and high-side driver.

This paper presents a novel high step-up interleaved-input boost converter mixed with magnetic coupling and voltage multiplier techniques based on three-state switching. The derivation procedure for the proposed topology is shown in Fig. 1. To achieve low input current ripples, an interleaved boost can be used among many transformer-less converters in high power application as shown in Fig. 1(a). Fig. 1(b) is the derived topology, which integrates switched capacitors into the conventional interleaved boost converter. Then, the double independent inductors in derived topology are separately replaced by the primary windings of coupled inductors, which are employed as energy storage and filtering as shown in Fig. 1(c). The secondary windings of two coupled inductors are connected in series for a voltage multiplier rectifier module, which is embedded into above converter.

The proposed converter inherits the merits of interleaved technique, switch-capacitor and coupled-inductor techniques, which is suitable for high-voltage gain and high power applications. The features of this converter are as follows: this converter can achieve very high-voltage gain without extreme duty cycles and high turn ratio. In other words, the turns ratio of the coupled inductor for the presented converter may be designed to be less than its competitions under the same voltage gain and duty ratio; the primary sides of two coupled inductor are used to share the input current by interleaved operation at the input, which reduces the current ripples, the size of magnetic core, and the switches conduction loss, because the diode–capacitor circuit not only raises the step-up voltage gain but also offers lossless passive clamp performance, the voltage spikes across the main switches are alleviated and the leakage-inductor energy of the coupled-inductors can be recycled; the voltage stresses on power devices are substantially lower than the output voltage. Thus, the switches with low voltage rating and low ON-state resistance $R_{\rm DS}$ (ON) are selected. The current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated.

II. Topology and Operation Principle of the Presented Converter

The equivalent circuit of the proposed converter is shown in Fig. 1(d), in which each coupled inductor is modeled as a combination of a magnetizing inductor $L_{\rm m}$, an ideal transformer, and a leakage inductance $L_{\rm k}$ (it can be taken as in series to the primary winding), respectively. Moreover, the current through magnetizing inductor $L_{\rm m}$ is continuous. The coupling references of the inductors are denoted by the marks "$*$" and "$\bullet$". The duty cycles of the active switches during steady operation are interleaved with 180° phase shift and greater than 0.5. That is to say, the two switches can only be in one of the three states (S_1: ON, S_2: ON; S_1: ON, S_2: OFF; S_1: OFF, S_2: ON), whose main objective is to obtain high-voltage gain and such characteristic is achieved when the duty cycle is greater than 0.5, hence the steady-state analysis is made only for this case. It is important to point out that the proposed converter cannot obtain high-voltage gain for duty cycle lower than 0.5. The theoretical waveforms in one switching period contain eight stages, which are plotted in Fig. 2. The corresponding topological circuits for each operating stages will be described briefly as follows.

Stage I $[t_0, t_1]$*:* In this transition interval, the corresponding equivalent circuit is shown in Fig. 3. At $t = t_0$, the switches S_1 begins to turn ON and S_2 remains conducting. The diodes D_1, D_2, and D_3 are still turned OFF, and only $D_{\rm O}$ is still turned ON. The dc-source $V_{\rm in}$ delivers its energy to the leakage inductor $L_{\rm k1}$, so the current through leakage inductor $L_{\rm k1}$ increases rapidly. However, the magnetizing inductor $L_{\rm m1}$ keeps on transferring its energy to the output terminal through diode $D_{\rm O}$, the current through series second sides of coupled inductors decreases linearly. Thus, the current through leakage inductor $L_{\rm k2}$

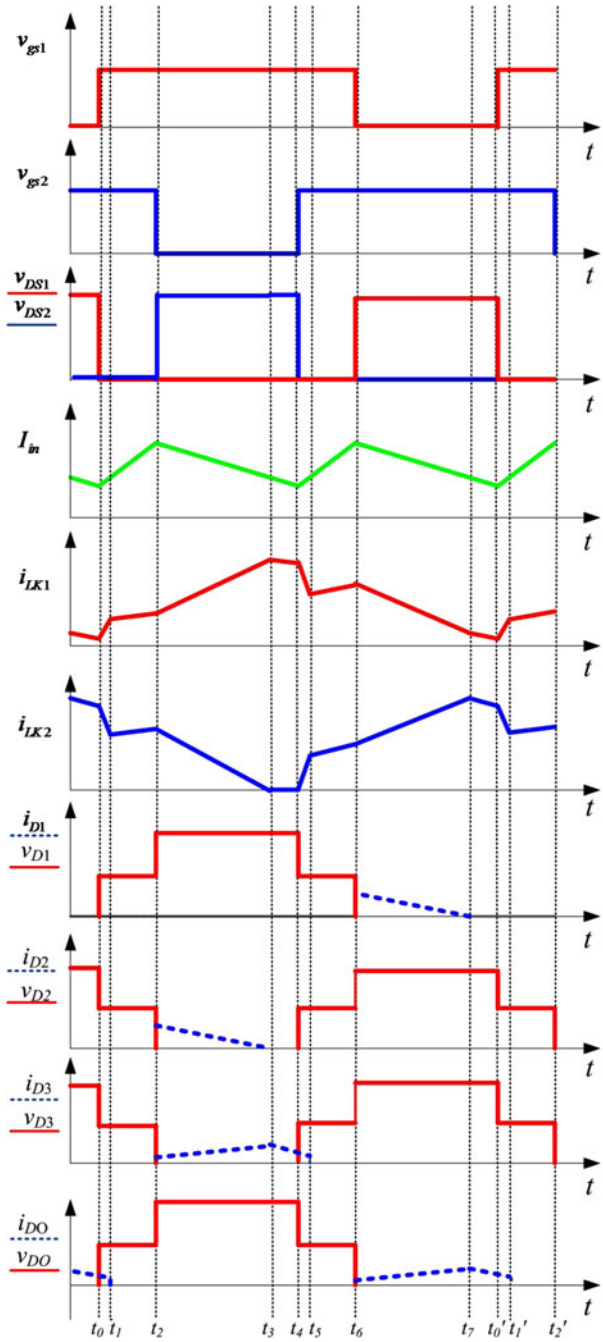

Fig. 2. Key theoretical waveforms.

decreases linearly

$$i_{\rm D_O}(t) \approx I_{\rm D_O}(t_0) - \frac{V_O - V_{C3} - V_{C2}}{N^2(L_{\rm k1} + L_{\rm k2})}(t - t_0). \qquad (1)$$

Stage II $[t_1, t_2]$*:* In this stage, the current-flow path is shown in Fig. 4. Both of the switches S_1 and S_2 remain conducting, and all of the diodes are turned OFF. Magnetizing inductors $L_{\rm m1}$ and $L_{\rm m2}$ and leakage inductors $L_{\rm k1}$ and $L_{\rm k2}$ are charged by the

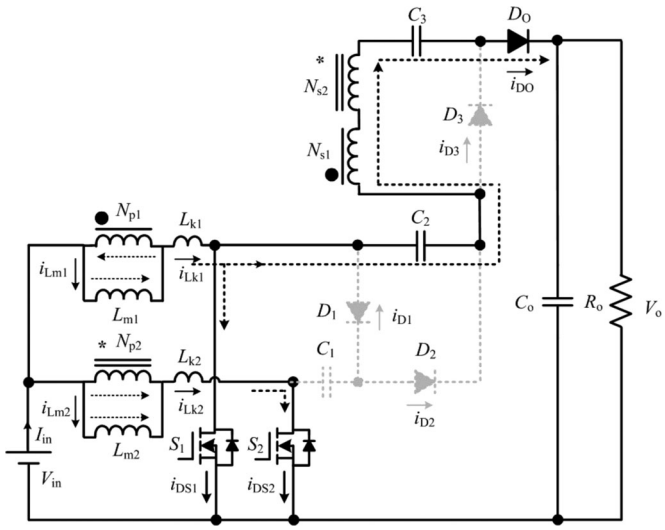

Fig. 3. Stage I.

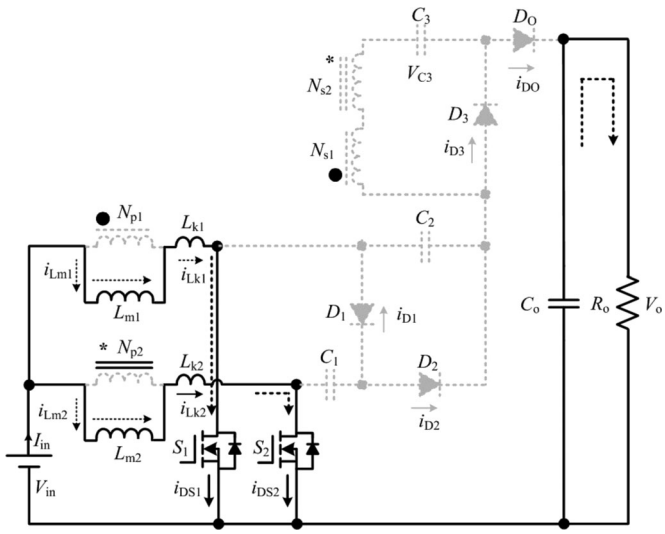

Fig. 4. Stage II.

input dc source, the currents through them increase linearly

$$i_{Lk1}(t) \approx I_{Lm1}(t_1) + \frac{V_{\text{in}}}{(L_{\text{m1}} + L_{\text{k1}})}(t - t_1) \quad (2)$$

$$i_{Lk2}(t) \approx I_{Lm2}(t_1) + \frac{V_{\text{in}}}{(L_{\text{m2}} + L_{\text{k2}})}(t - t_1). \quad (3)$$

Stage III $[t_2, t_3]$*:* During this time interval, the switch S_2 is turned OFF, and the switch S_1 is still conducting. The diodes D_1 and D_O are turned OFF, and D_2, D_3 are turned ON. The current-flow path is shown in Fig. 5. Magnetizing inductors L_{m1} and leakage inductors L_{k1} are charged by the input dc source, and the currents through them increase linearly. The magnetizing inductor L_{m2} still transferring its energy through the secondary side to charge the capacitor C_3, but the energy is decreasing. The energy that leakage inductor i_{Lk2} has stored is recycled to the capacitor C_2 through D_2 and S_1. At the same time, the capacitor

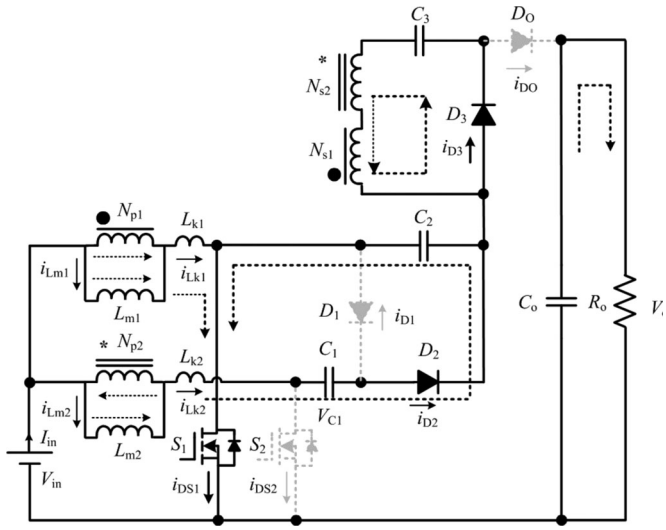

Fig. 5. Stage III.

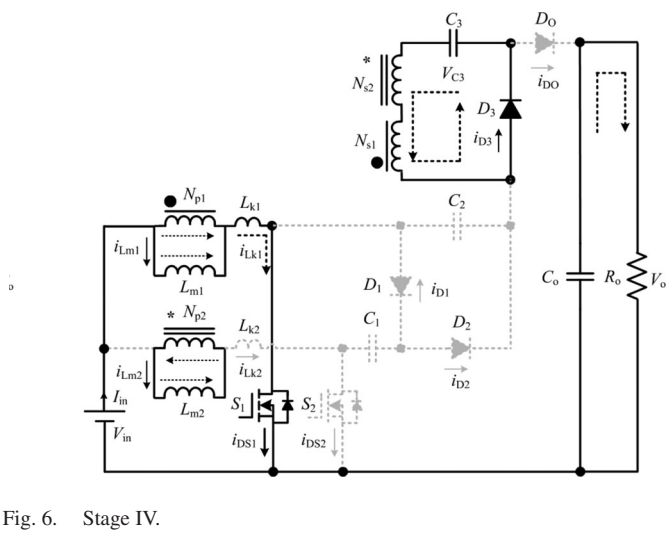

Fig. 6. Stage IV.

C_1 also releases energy to the capacitor C_2. Once the leakage-inductor current i_{Lk2} equals magnetizing inductor current i_{Lm2} at $t = t_3$, this stage ends

$$i_{Lk1}(t) \approx I_{Lm1}(t_2) + \frac{N(V_{C2} - V_{C1}) - V_{C3}}{N(L_{\text{k1}} + L_{\text{k2}})}(t - t_2) \quad (4)$$

$$i_{\text{Lk2}}(t) \approx I_{\text{Lm2}}(t_2) - \frac{N(V_{C2} - V_{C1}) - V_{C3}}{N(L_{\text{k1}} + L_{\text{k2}})}(t - t_2) \quad (5)$$

$$i_{\text{D}_3}(t) \approx \frac{(V_{C2} - V_{C1}) - V_{C3}/N}{N(L_{\text{k1}} + L_{\text{k2}})}(t - t_2). \quad (6)$$

Stage IV $[t_3, t_4]$: In this stage, the switch S_1 remains conducting, and the switch S_2 is still OFF. The current-flow path is shown in Fig. 6. Since the total energy of the leakage inductance L_{k2} has been completely released to the capacitor C_2, the diode D_2 is naturally turned OFF, and there is no reverse-recovery problem for the diode D_2. Magnetizing inductance L_{m2} still transfers energy to the secondary side charging the capacitor C_3

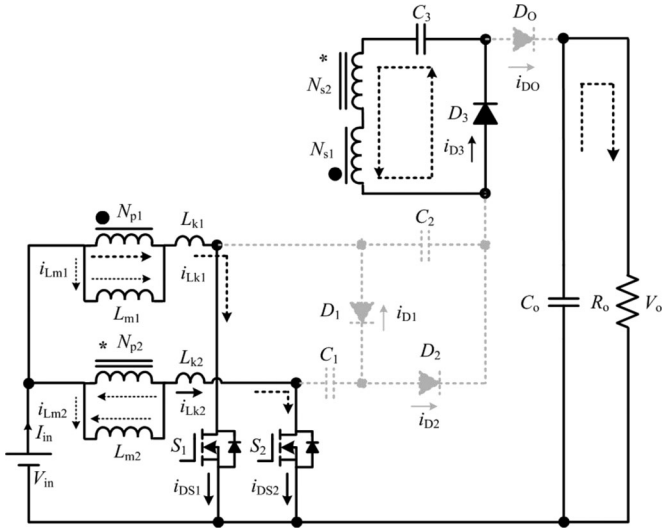

Fig. 7. Stage V.

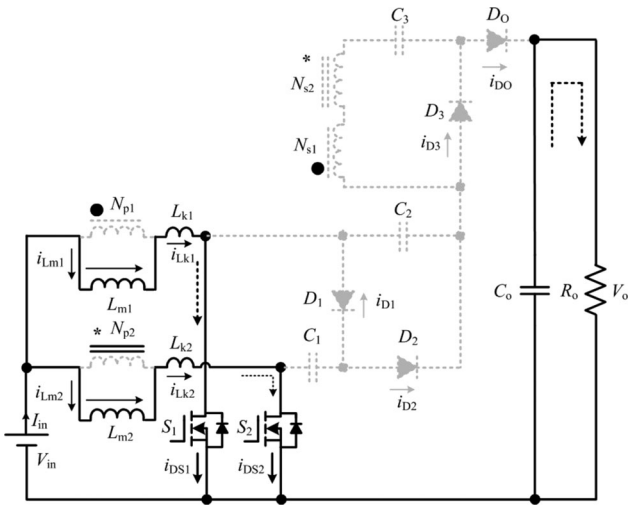

Fig. 8. Stage VI.

via diode D_3, but the current and i_{C3} and i_{D3} are decreasing. The leakage-inductor current i_{Lk1} is declining and i_{Lk2} is equal to zero. The current of the switch S_1 is equal to the summation of the currents of the magnetizing inductances L_{m1} and L_{m2}.

Stage V $[t_4, t_5]$*:* At $t = t_4$, the switch S_2 is turned ON again, and S_1 remains conducting. Only diode D_3 is turned ON. The current-flow path is shown in Fig. 7. The current through L_{k2} increases linearly, and the current through L_{k1} increases linearly. The energy stored in magnetizing inductor L_{m2} still transfers to secondary side of the coupled inductor charging the capacitor C_3. Once the i_{Lk2} is equal to i_{Lm2}, the stage ends

$$i_{D3} = i_{C3} \approx I_{D3}(t_4) - \frac{V_{C3}}{N^2(L_{m1} + L_{k2})}(t - t_4). \quad (7)$$

Stage VI $[t_5, t_6]$*:* During this stage, both of S_1 and S_2 remain conducting. All of the diodes are reversed biased as shown in Fig. 8. Magnetizing inductors L_{m1} and L_{m2} and leakage inductors L_{k1} and L_{k2} are charged by the input dc source, the currents through them increase linearly.

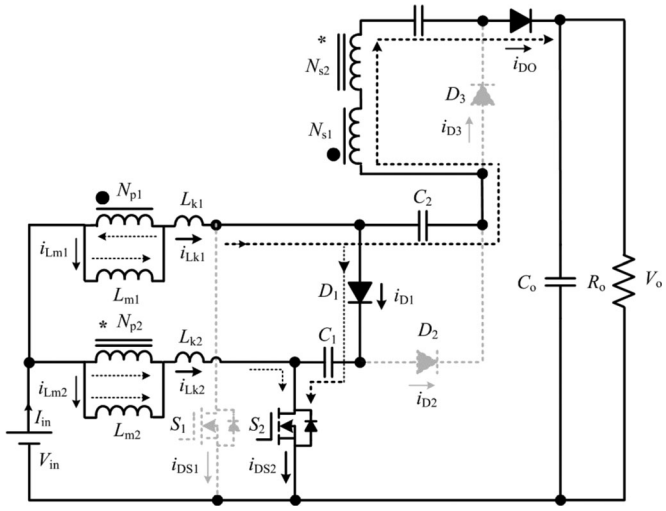

Fig. 9. Stage VII.

Stage VII $[t_6, t_7]$*:* At $t = t_6$, the switch S_1 is turned OFF, and S_2 is still conducting. The current-flow path is shown in Fig. 9. The energy stored in the leakage inductor L_{k1} is discharged to capacitor C_1 via D_1. The leakage-inductor current i_{Lk1} is declining, and the current i_{Lk2} increases linearly. Meanwhile, the dc-source V_{in} is in series connected with N_{p1}, C_2, N_{S1}, N_{S2}, and C_3 to transfer energy to the output terminal

$$i_{Lk1}(t) \approx I_{Lm1}(t_6) - \frac{(N+1)V_{C1} + V_{C2} + V_{C3} - V_O}{N(L_{k1} + L_{k2})}(t - t_6) \quad (8)$$

$$i_{Lk2}(t) \approx I_{Lm2}(t_6) + \frac{(N+1)V_{C1} + V_{C2} + V_{C3} - V_O}{N(L_{k1} + L_{k2})}(t - t_6) \quad (9)$$

$$i_{D_O}(t) \approx \frac{(N+1)V_{C1} + V_{C2} + V_{C3} - V_O}{N^2(L_{k1} + L_{k2})}(t - t_6). \quad (10)$$

Stage VIII $[t_7, t_0']$*:* During this stage, both the switches S_1 and S_2 remain previous states and the diode D_1 automatically switches OFF. The current-flow path is shown in Fig. 10. The current through leakage inductor L_{k2} increases linearly, and the leakage-inductor current i_{Lk1} decreases linearly.

III. Steady-State Performance Analysis of the Proposed Converter

To simplify the circuit performance analysis of the proposed converter in CCM, the following conditions are assumed.

1) All of the power devices are ideal. That is to say, the on-state resistance $R_{DS(ON)}$ and all parasitic capacitors of the main switches are neglected, and the forward voltage drop of the diodes is ignored.
2) The coupling-coefficient *k* of each coupled inductor is defined as $L_m/(L_m + L_k)$. The turn ratio *N* of each coupled inductor is equal to N_S /N_P.
3) The parameters of two coupled inductors are considered to be the same, namely $L_{m1} = L_{m2} = L_m, L_{k1} = L_{k2}$

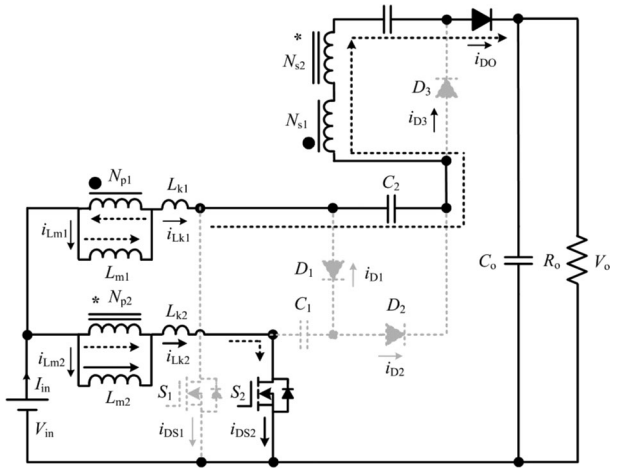

Fig. 10. Stage VIII.

$= L_k, N_{S1}/N_{P1} = N_{S2}/N_{P2} = N$, $k_1 = L_{m1}/(L_{m1} + L_{k1}) = k_2 = L_{m2}/(L_{m2} + L_{k2}) = k$.

4) Capacitors C_1, C_2, C_3, and C_O are large enough. Thus, the voltages across these capacitors are considered as constant in one switching period.

A. Voltage Gain Expression

If the transient characteristics of circuit are disregarded, each magnetizing inductance has two main states in one switching period. In one state, the magnetizing inductance is charged by the input source. In the other state, the magnetizing inductance is discharged. Since the time of modes I, IV, V, and VIII are significantly short, only modes II, III, VI, and VII are considered at CCM operation for the steady state. At stages II and VI, the following equations across magnetizing inductors can be written from Figs. 4 and 8

$$V_{Lm1}^{II} = V_{Lm2}^{II} = kV_{in} \tag{11}$$

$$V_{Lm1}^{VI} = V_{Lm2}^{VI} = kV_{in}. \tag{12}$$

During mode III, the following equations can be written:

$$V_{Lm1} = k \cdot V_{in} \tag{13}$$

$$V_{Lm2} = k \cdot (V_{in} - V_{C2} + V_{C1}) \tag{14}$$

$$V_{C3} = k \cdot N \cdot (V_{C2} - V_{C1}). \tag{15}$$

During the time duration of modes VII, the following voltage equations can be derived based on Fig. 9:

$$V_{Lm1} = k \cdot (V_{in} - V_{C1}) \tag{16}$$

$$V_{Lm2} = k \cdot V_{in} \tag{17}$$

$$V_O = V_{C1} + V_{C2} + V_{C3} + k \cdot N \cdot V_{C1}. \tag{18}$$

By applying the volt–second balance on the magnetizing inductor, the following equation is given:

$$\int_0^{\frac{(2D-1)T}{2}} (V_{Lm1}^{II} + V_{Lm1}^{VI})dt + \int_0^{(1-D)T} (V_{Lm1}^{III} + V_{Lm1}^{VII})dt = 0 \tag{19}$$

$$\int_0^{\frac{(2D-1)T}{2}} \left(V_{Lm2}^{II} + V_{Lm2}^{VI}\right) dt + \int_0^{(1-D)T} \left(V_{Lm2}^{III} + V_{Lm2}^{VII}\right) dt = 0. \tag{20}$$

From (19) and (20), the voltage across capacitors C_1 and C_2 can be derived:

$$V_{C1} = \frac{V_{in}}{1-D} \tag{21}$$

$$V_{C2} = \frac{2V_{in}}{1-D}. \tag{22}$$

Substituting (21) and (22) into (15) yields

$$V_{C3} = \frac{k \cdot N \cdot V_{in}}{1-D}. \tag{23}$$

Substituting (21)–(23) into (18), the voltage gain M is obtained as

$$M = \frac{V_O}{V_{in}} = \frac{3+2kN}{1-D}. \tag{24}$$

B. Voltage and Current Stress Analysis

According to the operating principle, the voltage and current stresses on power devices are discussed as follows. If the leakage inductance of coupled inductor and the voltage ripples on the capacitors are ignored, the voltage stresses on the main switches are expressed as

$$V_{DS1} = V_{DS2} = \frac{V_{in}}{1-D} = \frac{V_O}{3+2N}. \tag{25}$$

Also, the voltage stress of diodes D_1–D_O are given as

$$V_{D1} = V_{D2} = \frac{2V_{in}}{1-D} = \frac{2V_O}{3+2N} \tag{26}$$

$$V_{D3} = \frac{2N \cdot V_{in}}{1-D} = \frac{2N \cdot V_O}{3+2N} \tag{27}$$

$$V_{DO} = \frac{(1+2N)V_{in}}{1-D} = \frac{(1+2N)V_O}{3+2N}. \tag{28}$$

The relationship between the normalized voltage stresses on all the semiconductor components and the turns ratio N is also illustrated in Fig. 11. It can be seen that the active switch voltage stress is only equal to 1/5 of the output voltage, and the voltage stresses on D_1, D_2 are only equal to 2/5 of the output voltage when the turns ratio of the coupled inductors is 1. Moreover, their voltage stress will decrease rapidly with the increasing turns ratio. Although the voltage stresses on the diodes D_3 and D_O increase when the turns ratio N increases, the voltage stresses on the diodes D_3 and D_O are always lower than the output voltage.

The rms currents that flow through D_1, D_2, D_3, and D_O are calculated in

$$I_{D1\_rms} = I_{D2\_rms} = I_{D3\_rms} = I_{DO\_rms} \approx \frac{I_O}{\sqrt{1-D}}. \tag{29}$$

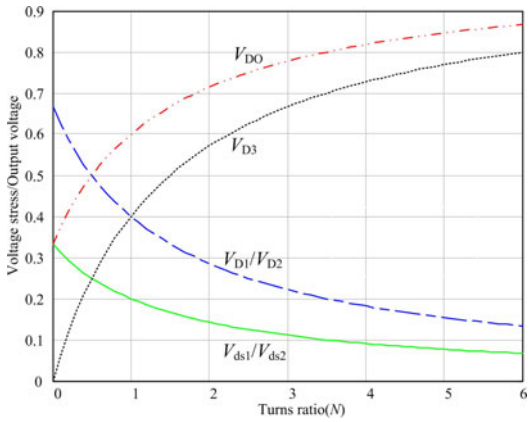

Fig. 11. Relationship between normalized voltage stresses and turns ratio.

According to the steady operating principle, the rms currents through the active switches can be approximated as

$$I_{\mathrm{S1\_rms}} \approx \frac{I_O}{\sqrt{D}(1-D)} \tag{30}$$

$$I_{\mathrm{S2\_rms}} \approx \frac{(3-D)I_O}{\sqrt{D}(1-D)}. \tag{31}$$

The rms value of the current through capacitors C_1, C_2, and C_3 can be estimated as

$$I_{C1} = I_{C2} = I_{C3} \approx \frac{I_O}{(1-D)^2}. \tag{32}$$

The input current ripple is found be

$$\Delta I_{\mathrm{in}} \approx \frac{D(1-D)V_O}{f_s(3+2N)(L_{\mathrm{m}}+L_{\mathrm{k}})}. \tag{33}$$

C. Limitation of Duty Cycle and Turns Ratio

In the proposed converter, the duty cycles of the power switches are interleaved with 180° phase shift, and the duty cycles are greater than 0.5. That is to say, the two switches can only be in one of three states (S_1: ON, S_2: ON; S_1: ON, S_2: OFF; S_1: OFF, S_2: ON), which ensures the normal transmission of energy from the coupled inductor's primary side to the secondary one. Therefore, the limitation of the turns ratio is given by

$$N \le \frac{1}{4}\frac{V_O}{V_{\mathrm{in}}} - \frac{3}{2}. \tag{34}$$

D. Key Performance Comparison

In order to demonstrate the performance of the proposed converter, Table I shows the number of key components, the voltage gain, and the normalized voltages stress of semiconductor devices of the proposed converter and other similar converters. These converters can be as a candidate for high step-up and high power conversion applications.

From Table I, one can see that the presented converter has the highest voltage gain and the lowest voltage stress on the active switches compared with the other converter. Moreover, the quantities of diodes and the secondary side windings used in the proposed converter are least as the converter introduced in [34], which will help to improve the reliability and reduce the cost.

TABLE I
PERFORMANCE COMPARISON OF SIMILAR PROTOTYPES

Similar prototypes with high voltage gain	Converter [40]	Converter [39]	The proposed converter
Quantities of switches	2	Two	2
Quantities of diodes	6	6	4
Quantities of cores	2	2	2
Quantities of secondary side windings	1	2	1
Quantities of capacitors	5	5	4
Voltage gain	$(2N+2)/(1-D)$	$(2N+2)/(1-D)$	$(2N+3)/(1-D)$
Voltage stress on active switches	$V_O/(2N+2)$	$V_O/(2N+2)$	$V_O/(2N+3)$
The maximum voltage stress on diodes	$NV_O/(N+1)$	$(2N+1)V_O/(2N+2)$	$(2N+1)V_O/(2N+3)$
duty-ratio (D) limited	$D \ge 0.5$	$D \ge 0.5$	$D \ge 0.5$

TABLE II
UTILIZED COMPONENTS AND PARAMETERS OF PROTOTYPE

Components	Parameters
Input voltage V_{in}	16–22 V
Output voltage V_o	200 V
Maximum output power P	400 W
Switching frequency f_s	50 kHz
Turns ratio N_s/N_p	1:1
Magnetizing inductor $L_{\mathrm{m}1}$, $L_{\mathrm{m}2}$	55 μH
Leakage inductor $L_{\mathrm{k}1}$, $L_{\mathrm{k}2}$	1.65 μH
Power switches S_1, S_2	FDP2532
Diodes D_1, D_2, and D_3	MUR2020
Diode D_O	MUR2040
Capacitors C_1 and C_2	10 μF/100 V
Capacitor C_3	22 μF/100 V
Capacitor C_O	470 μF/200 V

IV. DESIGN CONSIDERATIONS

A. Coupled-Inductor Design

Since the turns ratio determines the voltage gain and voltage stress on the semiconductor devices, it is one of the key parameters for the presented converter. To be clear, the proposed converter can work under different turns ratio for the double coupled inductors, but increase the complexity of circuit analysis and design. Moreover, large turns ratio difference may cause the raise of input current ripple. So the turns ratio of the coupled inductors will be designed as same as possible in this paper. Usually, the duty cycle should be less than 0.8 to reduce the conduction loss of the switches. If the voltage gain and switch duty cycle are selected, the turns ratio of the coupled inductor can be calculated by

$$N = \frac{1}{2}[M \cdot (1-D) - 3]. \tag{35}$$

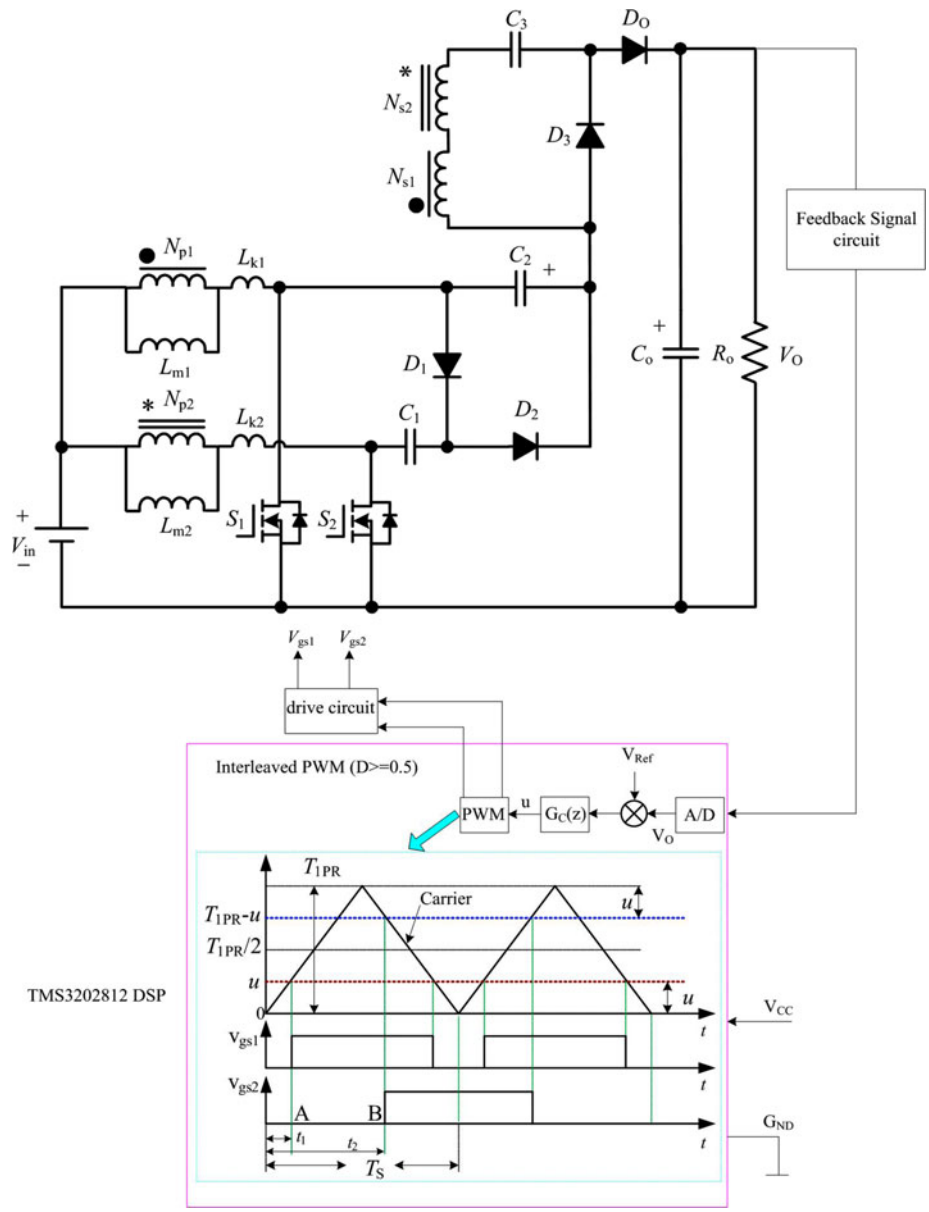

Fig. 12. Simple digital control strategy for the proposed converter based on DSP.

According to Fig. 11, the voltage gain will be less affected by the leakage inductance of the coupled inductors. Fortunately, the leakage inductance can be used to limit the diode current falling rate and alleviate the diode reverse-recovery problem. Therefore, a compromise should be made to optimize the performance of the converter. Moreover, considering the input current ripples, the leakage inductance of the coupled inductors should be designed as symmetrical as possible. The relationship of the leakage inductance, the diode current falling rate, and the turns ratio is expressed by

$$\frac{di_{\mathrm{D3}}}{dt} = \frac{di_{\mathrm{DO}}}{dt} \approx \frac{V_{C3}}{N^2(L_{\mathrm{k1}} + L_{\mathrm{k2}})}. \tag{36}$$

B. Active Switches and Diodes Selection

The voltage rating of the power components have been derived from (25)–(28). In practice, voltage spike may be produced during switch transition process because of the effect of parasitic parameters in the layout circuit. Therefore, regarding the margin of safety, the voltage rating of the selected power devices will usually be more than 150% of the calculated value.

C. Considerations of Capacitor Design

The capacitors C_1, C_2, and C_3 play the roles of buffering energy, clamping the voltage stress on the power devices, and improving voltage gain. Calculating the minimum capacitance of the switched capacitors depends on the maximum transferring power, the capacitor's voltage, and the switching frequency [42]. The voltage of C_1, C_2, and C_3 can be obtained by (21)–(23), respectively. The estimated capacitances are

$$C_1 \geq \frac{2P_{O\_\max}}{{V_{C1}}^2 f_s}, \quad C_2 \geq \frac{2P_{O\_\max}}{{V_{C2}}^2 f_s}, \quad C_3 \geq \frac{2P_{O\_\max}}{{V_{C3}}^2 f_s}. \tag{37}$$

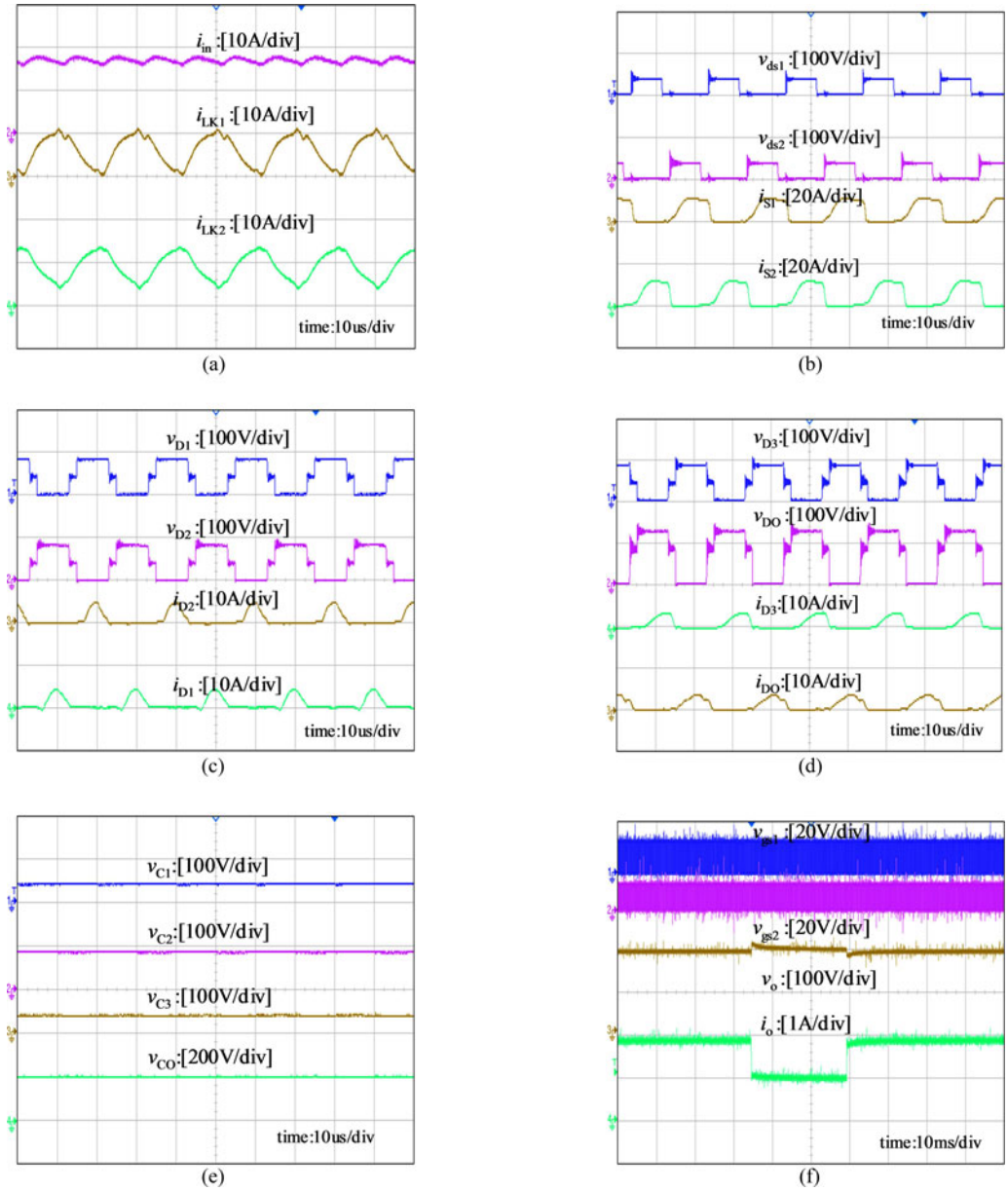

Fig. 13. Key experimental waveforms.

Generally, the equivalent series resistor (ESR) of an aluminum electrolytic capacitor will be smaller as the capacitance increases. So the aluminum electrolytic capacitor is usually selected to be larger than the calculated value for reducing the power losses caused by the ESR, but the large capacitor is bulky volume and high cost. In practice, it is a favorable solution that parallel several capacitors are adopted to make the equivalent ESR minimum. In addition, the film capacitors could be used to improve the efficiency and minimize the capacitances, but the cost of film capacitors is higher.

V. Experimental Verifications

In order to verify the operation and evaluate the performance of the proposed three-state switching boost converter, an experimental prototype for the structure mixed with diode–capacitors and coupled inductors has been designed according to the previous guidelines and implemented in laboratory. The components used in the prototype are listed in Table II.

In control strategy, the proposed converter is controlled by the microchip TMS3202812DSP as shown in Fig. 12. This technique consists in sampling the output voltage and comparing it to a reference, which generates an error voltage. This error serves as a parameter to the compensator, providing the control voltage, which, after the modulation, provides pulse width modulation pulses for driving switches, with adjusted duty cycle for stabling output voltage on the desired level.

Fig. 13(a) presents the behavior of the input current and the currents through the primary-side leakage-inductor currents i_{LK1} and i_{LK2} of the dual coupled inductors, where it can be

seen that the currents through L_{k1} and L_{k2} are operated in interleaving. Consequently, the stresses regarding the active switches are reduced and the input current ripples are very low.

Fig. 13(b) shows the gate signals of S_1 and S_2, current waveforms, and the voltage stresses passing through them. One can see that the active switches are turned ON from lower current, which reduces the switching losses and the EMI noise. In addition, the voltage stresses V_{ds1} and V_{ds2} on the main switches are equal, which is one-fifth of the output voltage during the steady-state period about 40 V. Thus, low voltage ratings and low on-state resistance levels active switches can be selected for high conversion efficiency.

Fig. 13(c) displays that the voltage and current stresses on the diodes D_1 and D_2. One can see that the voltage stresses of the diodes D_1 and D_2 are approximately 80 V, which are lower than the half of the output voltage in the steady-state period. Therefore, low-voltage-rated diodes with high performance can be adopted for the presented converter. Moreover, the diodes D_1 and D_2 are automatically turned OFF.

Fig. 13(d) illustrates that the voltage and current stresses on the diodes D_3 and D_O. The voltage stress of the diodes D_3 is about 80 V, and the voltage stress of the diode D_O is approximately 120 V, which are lower than the output voltage in the steady-state period. In addition, the currents through D_3 and D_O at the instant of the turning OFF are reduced what favors the turning OFF behavior, which agree with the operating principle and the steady-state analysis.

Fig. 13(e) shows the experimental results of voltage on all capacitor to illustrate the theoretical analysis. The V_{C1} equal to the output voltage of the conventional boost converter, and the V_{C3} is nearly equal to V_{C1} because the turns ratio N is set 1. The V_{C2} is about twice of V_{C1}, which is agreement with theoretical analysis. Fig. 13(f) shows the dynamic response due to the step load variation between 200 and 400 W, and the output voltage is maintained at 200 V.

VI. Conclusion

In this paper, a three-state switching boost converter with high-voltage gain has been successfully developed, which is mixed with magnetic coupling and voltage multiplier techniques, and suitable for low input-voltage and high step-up power conversion applications. Moreover, the generation methodology for the proposed topology is described. The key theoretical waveforms, steady-state operational principle, and the main circuit performance are clearly analyzed and verified, exploring the advantages of the proposed converter. The proposed converter can achieve a very high-voltage gain and avoid operating at extreme duty cycle and high turn ratio for the combining the benefits of magnetic coupling and switch capacitor. Also, the voltage stresses of the main switches are very low, which are one-fifth of the output voltage under $N = 1$. Thus, the low-voltage-rated MOSFETs with low resistance $r_{DS}(ON)$ can be selected to reduce the switching losses and cost. Moreover, the interleaved PWM operation reduces the current through each switch and restrains the input current ripples effectively. In addition, the current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated, and the leakage-inductor energy can be recycled to the output through capacitors C_1 and C_2; meanwhile, there will be no overshoot current of capacitors C_1 and C_2 for the existence of leakage inductor. Therefore, the proposed converter is promising for high step-up applications. Still, the disadvantage of this topology is that the duty cycle of each switch shall be not less than 0.5 under the interleaved control with 180° phase shift, in order to ensure the normal energy transmission.

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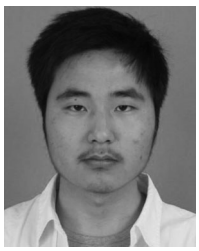

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