87% Overall High Efficiency and 11 μA Ultra-Low Standby Current Derived by Overall Power Management in Laptops With Flexible Voltage Scaling and Dynamic Voltage Scaling Techniques

Shang-Hsien Yang, Chao-Chang Chiu, Chih-Wei Chang, Chen-Min Chen, Che-Hao Meng, and Ke-Horng Chen

***Abstract*—The proposed overall power management in laptops can improve overall power conversion efficiency by the flexible voltage scaling (FVS) technique in cooperation with conventional dynamic voltage scaling (DVS) technique. The FVS technique separates the controller into two parts. One is a simple primary side controller and the other is emerged into the power management unit in the laptop for getting direct power control from the microprocessor. 12% light load efficiency and 7% peak efficiency are improved compared to conventional design with the DVS technique only but without the FVS technique. Furthermore, green mode is proposed to effectively reduce chip quiescent current to 11μA and to suppress power loss to 10 mW in ultra-light load, which is much smaller than 500 mW standby power defined by the restriction of Energy Star Standard and 40 mW of state-of-art commercial products.**

***Index Terms*—Dynamic voltage scaling (DVS) technique, flexible voltage scaling (FVS) technique, green mode (GM), overall power management (OPM).**

I. Introduction

In conventional power management applications for laptop computers, the adapter converts the ac input voltage to a regulated dc voltage, i.e., 10, 12 or 19 V, to supply the laptop computer [1]–[6]. The adapter operation is independent from the charger and DC–DC converter circuits of the laptop computer, as illustrated in Fig. 1. Due to the lack of a feedback path, the laptop side has no ability to control the operation of the AC–DC conversion, and the efficiency curves of the AC–DC and DC–DC conversion are independent of each other. Unfortunately, overall power conversion efficiency is not optimized be simply improving either the individual efficiency of AC–DC or DC–DC conversion. This leads to higher adapter temperature and limits the minimum size of the heat sink required to prevent the adapter from overheating.

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The authors are with the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu300, Taiwan (e-mail: shanghsienyang@hotmail.com; teddy.ece99g@nctu.edu.tw; kone.fivesix@msa.hinet.net; eejmchen@gmail.com; blue955381@yahoo.com.tw; khchen@cn.nctu.edu.tw).

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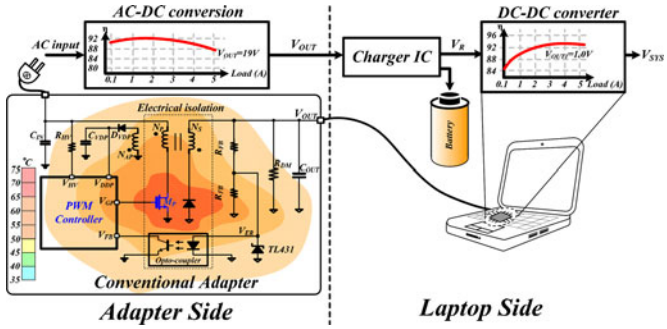


Fig. 1. Conventional power management has the disadvantage of low flexibility of controlling both sides at the same time.

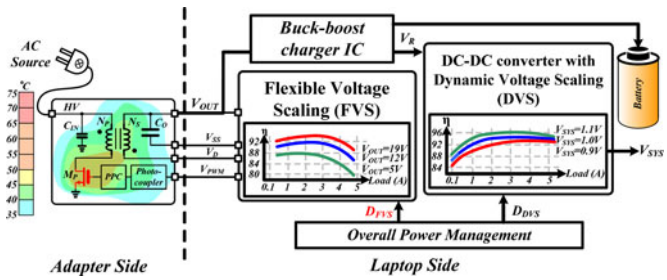


Fig. 2. OPM uses the FVS and the DVS techniques to derive high efficiency and reduce heat on both sides.

Fig. 2 shows the proposed overall power management (OPM) minimizes the adapter side controller to a simple power pulse controller (PPC). Meanwhile, the OPM moves the main controller to the laptop side to consider overall efficiency from the adapter to the laptop by the proposed flexible voltage scaling (FVS) technique. High efficiency can be achieved by the FVS technique in cooperation with conventional dynamic voltage scaling (DVS) technique [7]–[10] used in DC–DC converter. The advantage of using this control scheme includes the laptop side has the ability to control the AC–DC conversion voltage for achieving overall high efficiency, which allows the size of the adapter to be reduced. The proposed OPM allows the adjustment of the output voltage $V_{\rm SYS}$ of the DC–DC converter according to code $D_{\rm DVS}$ from the OPM. The FVS controller simultaneously obtains the voltage adjustment code $D_{\rm FVS}$ from the OPM to decide the value of $V_{\rm OUT}$ to improve efficiency from the adapter to the laptop. As depicted in Fig. 2, from the two different curves of DVS function in DC–DC converter,

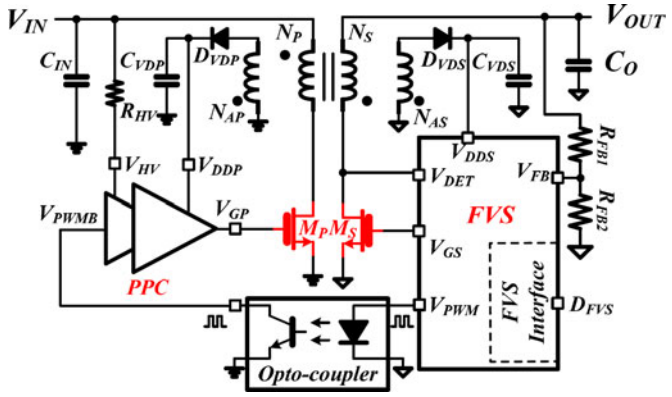


Fig. 3. Overview of the proposed FVS converter.

OPM can find an optimum FVS function in AC–DC conversion to achieve maximum efficiency. The overhead of the FVS function is the modification to the charger from buck topology to the buck-boost topology, because the output voltage of the FVS function ranges from 5 to 19 V instead of a fix voltage. Another apparent advantage of the proposed control scheme is the reduction in operating temperature, which maintains the heat of the adapter below 50 °C. A lower operating temperature improves overall user experience, because the uncomforting experience associated with dissipated heat is eliminated.

Owing to direct monitoring the laptop side voltage to control the AC–DC conversion, the proposed green mode (GM) uses the concept of conventional burst mode with variable switching frequency to further improve efficiency at light loads. Furthermore, most circuits of FVS controller can be completely shut down for low quiescent current in the standby mode. Thus, the standby current of the chip is reduced to 11 μA in the GM mode, and the system power consumption is reduced to 10 mW when considering all power consumption of all external components. By contrast, conventional power consumption in the standby mode is about 500 mW due to restriction of Energy Star Standard and state-of-the-art commercial product has the standby power 40 mW [11].

Fig. 3 shows the proposed FVS converter. The laptop side circuit is completely merged into the FVS converter so that the circuit complexity and the PCB area are reduced effectively. The overall system is controlled by the FVS at laptop side, and the adapter side control IC is simplified to a drive circuit which can receive the PWM signal from laptop side to drive the adapter side power switch M_P. Compared to the conventional works, the FVS can receive the back-end information, allowing the AC–DC converter to cooperate with the back-end device easily. Thanks to the FVS control, the output voltage adjustment can be easily achieved. The proposed FVS converter adopts the synchronous topology, and can control both the M_P and M_S at adapter side and laptop side simultaneously. The main goal of this topology is to enhance conversion efficiency [12]–[13], by replacing the power diode with a power switch, M_S.

When the back-end device is removed from AC–DC converter, the load current becomes ultra-light load. The power conversion efficiency of flyback converter [14]–[18] at ultra-light load condition is another serious problem which decreases the conversion efficiency significantly. [19] extends the off-time period to reduce the switching frequency and the switching loss. However, the conversion efficiency still suffers from the quiescent current of the controller. By directly monitoring the output voltage of the AC–DC converter, $V_{\rm OUT}$, at the laptop side, the GM mechanism is designed into the FVS which can disable most of circuit blocks of controller to reduce the quiescent current power consumption. That is, the ultra-light load efficiency can be improved effectively.

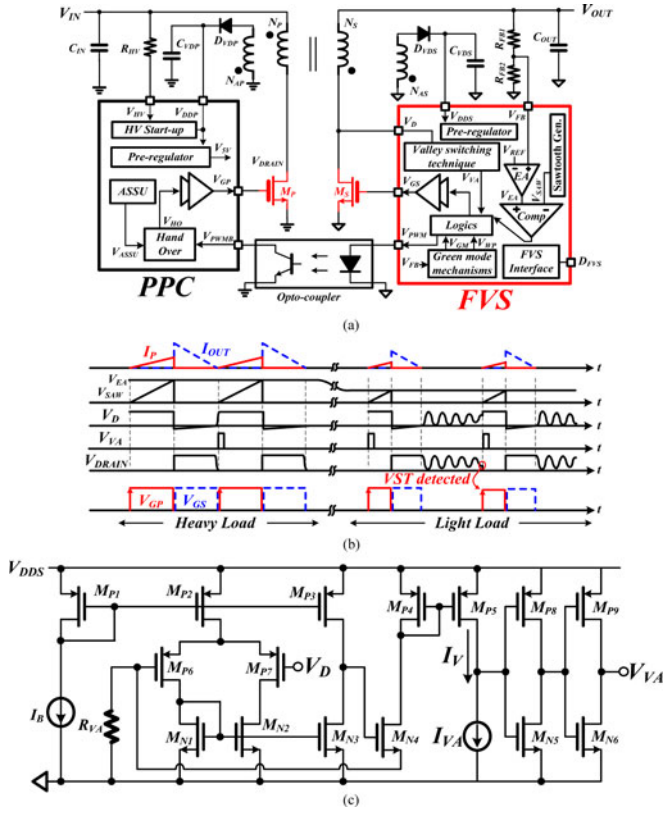


Fig. 4. Proposed FVS converter. (a) Implementation of the FVS converter. (b) Operation waveform of the FVS converter. (c) Implementation of the VST circuit.

The proposed FVS converter is described in Section II. The adapter side start-up technique is illustrated in Section III. The GM mechanism and the light load efficiency are analyzed in Section IV. Experimental results are shown in Section V. Finally, conclusions are made in Section VI.

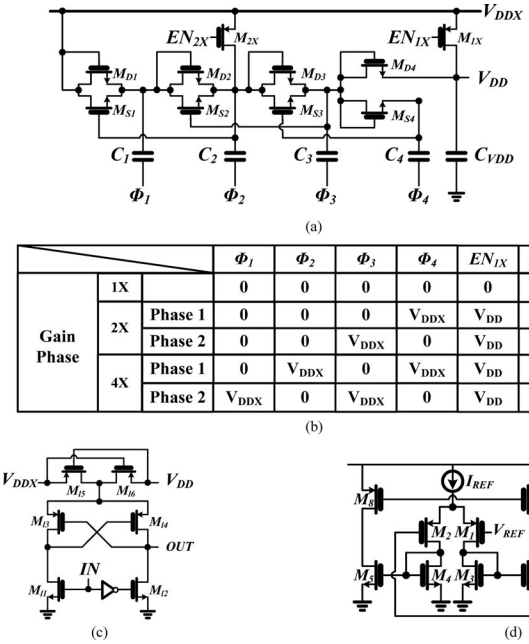
II. Proposed Laptop Side Regulation Converter

Fig. 4(a) shows the detail implementation of the proposed FVS converter. The power of the laptop side circuit is supplied by the axillary transformer and the supply voltage can be expressed as (1), where N_S and $N_{\rm AS}$ are the transformer turns ratio of the secondary and the auxiliary sides, respectively. The $V_{\rm OUT}$ is equal to zero in the start of power-on sequence. Therefore, there is no power available for the FVS during the start-up period and the system is not operational. To solve this problem, the adapter side start-up (ASSU) circuit is designed

and established in PPC which is a mechanism generating pulse signals to power on the FVS converter and charge the $C_{\rm VDS}$ for supplying FVS. Fig. 4(b) shows the control method of FVS converter. The on-time of M_P is determined by value of error amplifier $V_{\rm EA}$ which represents energy demands of the output load; and off-time is determined by the valley switching technique (VST) [20], which ensures the power transistor M_P is turned on when its drain voltage resonates to the lowest value for reducing switching power loss. When the back-end device is removed from the proposed FVS system, the GM mechanism can significantly extend the off-time period to increase the light load efficiency. In Fig. 4(c), the VST circuit transfers the V_D, which stands for the inverting value of the drain voltage $V_{\rm DRAIN}$ of the M_P, to the current signal I_V. The value of I_V is compared with the reference current $I_{\rm VA}$ to detect the peak value of V_D so that the valley voltage of $V_{\rm DRAIN}$ can be derived. This allows the laptop-side FVS controller to control laptop side power switch directly without adding any additional components. Instead of using a power diode, the synchronous rectification control of M_S improves the power efficiency in comparison with asynchronous control. Meanwhile, soft-switching is achieved to prevent short-through situation. The adaptive dead-time control is implemented with digital logic circuits based on the information sensed from the $V_{\rm GP}$ and $V_{\rm GS}$ signals. In different profiles, the FVS interface circuit will adjust the voltage division ratio of $V_{\rm OUT}$ to meet the energy requirement according to data code, $D_{\rm FVS}$. The back-end device communicates with adapter directly through the embedded FVS interface

$$V_{\rm DDS} = V_{\rm OUT} \times \frac{N_{\rm AS}}{N_S}. \tag{1}$$

Both the FVS controller and the PPC are supplied by auxiliary winding $N_{\rm AP}$ and $N_{\rm AS}$, respectively. Owing to the FVS function, the supply voltage varies under different output condition. To supply the FVS controller with a stable voltage source, the preregulator needs to have a stable supply voltage source. The preregulator is composed of a Dickson charge pump and a low-dropout regulator (LDO). In Fig. 5(a), the conventional Dickson charge pump is used to generate a higher voltage source ($V_{\rm DD}$) for the driver circuit with good driving capability. On the other hand, the LDO is implemented to suppress noise from the charge pump and to convert the $V_{\rm DD}$ to the 5 V voltage source ($V_{\rm 5V}$) for the controller. The standard supply voltage $V_{\rm DDX}$, which represents $V_{\rm DDP}$ and $V_{\rm DDS}$, is 19 V. If $V_{\rm DDX}$ is 5 or 12 V, it will be scaled up through the predetermined factor of 4 X or 2 X by the charge pump, respectively. For the preregulator, the conversion ratio is determined by the control signals $EN_{\rm 2X}$ and $EN_{\rm 1X}$ as shown in Fig. 5(b). An additional level shifter is used to generate $EN_{\rm 2X}$ and $EN_{\rm 1X}$ to guarantee the preregulator function. Fig. 5(c) shows the level shifter which converts the gate control voltage to the highest voltage between $V_{\rm DDX}$ and $V_{\rm DD}$. Fig. 5(d) shows the circuit implementation of the LDO where capacitorless topology is adopted for area efficient.



			Φ_1	Φ_2	Φ_3	Φ_4	EN_{1X}	EN_{2X}
Gain Phase	1X		0	0	0	0	0	V_{DDX}
	2X	Phase 1	0	0	0	V_{DDX}	V_{DD}	0
		Phase 2	0	0	V_{DDX}	0	V_{DD}	0
	4X	Phase 1	0	V_{DDX}	0	V_{DDX}	V_{DD}	V_{DD}
		Phase 2	V_{DDX}	0	V_{DDX}	0	V_{DD}	V_{DD}

Fig. 5. Preregulator for proposed FVS converter. (a) Circuit implementation of Dickson charge pump. (b) Operation diagram of Dickson charge pump. (c) Circuit implementation of level shift. (d) Circuit implementation of the LDO circuit.

III. Adapter Side Start-Up (ASSU) Technique

The proposed FVS converter can be directly powered on by the ac power source even when the controller is implemented on the laptop side. Fig. 6(a) shows the flowchart of the power-on sequence. The whole system operation can be correctly controlled by the FVS controller at the laptop side when the ac source is plugged-in to the FVS converter and $V_{\rm DDS}$ is greater than $V_{\rm ST}$, which is the minimum acceptable supply voltage. Owing to the adequate power source $V_{\rm DDS}$, the FVS controller directly controls the laptop side power transistor, M_S transmits the laptop side power transistor control signal $V_{\rm PWM}$ to PPC to control the M_P by an opto-coupler as shown in Fig. 6(b). One scenario should be carefully considered if the $V_{\rm DDS}$ is lower than the $V_{\rm ST}$ where the FVS controller will not be enabled as illustrated is Fig. 6(c). To avoid any abnormal turning off problems, the HV start-up in the PPC is directly powered on by the input high voltage *HV* for supplying the FVS system correctly [19]. The ASSU circuit generates the gate pulse signal $V_{\rm ASSU}$ with a constant frequency to drive the M_P and the whole system is working under an open loop operation. In the meanwhile, the power switch M_S at the laptop side is always turned off. The output current $I_{\rm OUT}$ flows through the body diode of M_S to charge the output capacitor $C_{\rm OUT}$. Besides, the auxiliary winding, $N_{\rm AS}$, provides the charging current, $I_{\rm VSD}$, to the bypass capacitor, $C_{\rm VDS}$. This open loop operation will not be terminated until the $V_{\rm DDS}$ is higher than $V_{\rm ST}$ to ensure that the FVS controller can be enabled correctly. Once the FVS controller starts to work and the first rising edge of the control signal, $V_{\rm PWMB}$, is detected, the hand over circuit in the PPC will disable the ASSU circuit. Then, the FVS controller starts to dominate the whole system behavior again.

The circuit implementation of the ASSU circuit is illustrated in Fig. 7. During the power-on interval, the enable signal *EN* would be set high to start the ASSU circuit and to generate a constant frequency signal, $V_{\rm ASSU}$, as long as $V_{\rm DDS}$ is lower

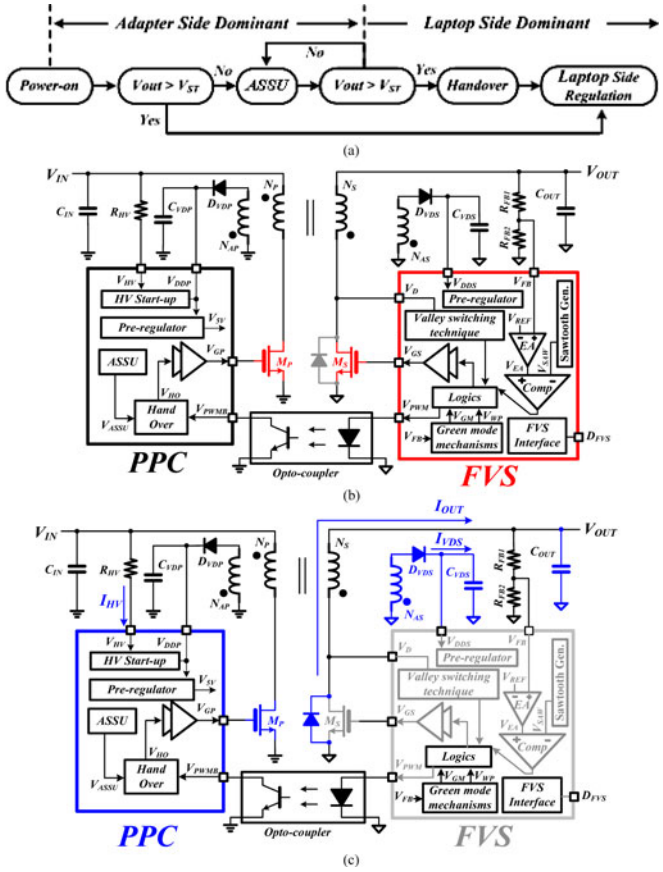


Fig. 6. Start-up procedure of the proposed FVS converter. (a) Flowchart of the power-on sequence. (b) Circuit operation when $V_{\rm DDS} < V_{\rm ST}$. (c) Circuit operation when $V_{\rm DDS} > V_{\rm ST}$.

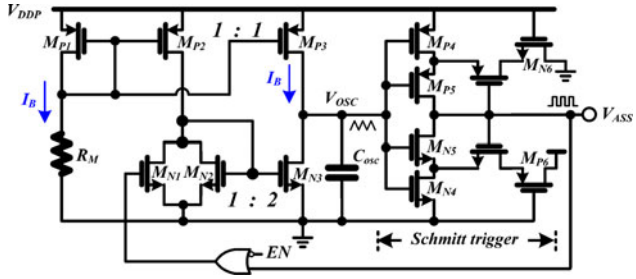


Fig. 7. ASSU circuit implementation.

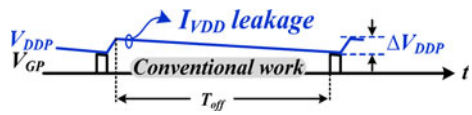


Fig. 8. Influence of $\Delta V_{\rm DDP}$ on $V_{\rm GP}$.

than $V_{\rm ST}$. The resistor R_M is connected to M_{P1} to generate the basic bias current I_B which is used to determinate the start-up frequency of the ASSU circuit. The current flowing through M_{N3} is twice that of M_{P3} by the operation of the current mirror. Charging and discharging currents induce the voltage variation at the capacitor $C_{\rm OSC}$. When the $V_{\rm OSC}$ across the $C_{\rm OSC}$ is greater than the upper-bound of the Schmitt trigger circuit, the output signal $V_{\rm ASSU}$ is set low. At the moment, the discharging current flows through M_{N3} and causes the decrease at $V_{\rm OSC}$. Once $V_{\rm OSC}$ approaches the lower-bound of the Schmitt trigger circuit, the output signal $V_{\rm OSC}$ is set high. That is, the oscillation frequency of $V_{\rm ASSU}$ can be expressed as (2) where $V_{\rm schmitt}$ is the threshold voltage of the Schmitt trigger circuit. The resulting waveform of $V_{\rm OSC}$ has a duty cycle of near 50% due to the fact that the charging and discharging transistors are biased by the same current. The oscillation frequency can be changed by adjusting the resistance value of R_M. Consequently, the ASSU circuit is so simple that it is appropriate for the PPC to simplify the circuit architecture

$$f_{\rm OSC} = \frac{I_{\rm OSC}}{2 \times \Delta V_{\rm schmitt} \times C_{\rm OSC}}. \tag{2}$$

IV. Green Mode (GM) Mechanism

To further improve the ultra-light load power conversion efficiency, the proposed GM mechanism reduces both the switching frequency and the quiescent power dissipation. In order to improve light load efficiency, conventional flyback converter reduces the switching frequency to reduce switching power loss. However, the low bound of switching frequency is limited by the quiescent current of controller because the undesired supply voltage drop, $\Delta V_{\rm DDP}$, of the controller occurs with the value proportional to the off-time of one switching cycle as shown in Fig. 8. The lower operation frequency brings the lower $V_{\rm DDX}$ due to the power consuming of adapter side quiescent current. Besides, the charge pump provides a constant voltage conversion ratio to generate $V_{\rm DD}$. That is, the voltage level of $V_{\rm DD}$ is determined by $V_{\rm DDX}$. The controller may fail to function correctly due to the decreasing supply voltage. Moreover, the decreasing deteriorates the on-resistance of the power switches and thus causes the increase of the conduction power loss due to the deteriorated driving capability of power switches. The$\Delta V_{\rm DDP}$ can be expressed as (3), where $I_{\rm VDP}$ is the quiescent current of controller, the $T_{\rm off}$ is the off-time in one switching cycle, and the $C_{\rm VDP}$ is the supply energy storage capacitor as shown in Fig. 3

$$\Delta V_{\rm DDP} = \frac{I_{\rm VDP} \times T_{\rm off}}{C_{\rm VDD}}. \tag{3}$$

During the on-time interval, the instantaneous conduction power loss, $P_{\rm CON\_LOSS}$, is given by (4) where the charging current, I_P, flows through the turn-on resistance, $R_{\rm ds,on}$, of N-type MOSFET M_P. The process parameters of the N-type MOSFET M_P include μ_n is the mobility, $C_{\rm OX}$ is gate capacitance per area, *W/L* is the aspect ratio, and $V_{\rm TH}$ is the threshold voltage

$$P_{\rm CON\_LOSS} = \int_0^T I_P(t)^2 R_{\rm ds,on}(t) dt$$

$$\text{where } R_{\rm ds,on} = \frac{1}{\mu_n C_{\rm OX} \frac{W}{L} (V_{\rm GS} - V_{\rm TH})}. \tag{4}$$

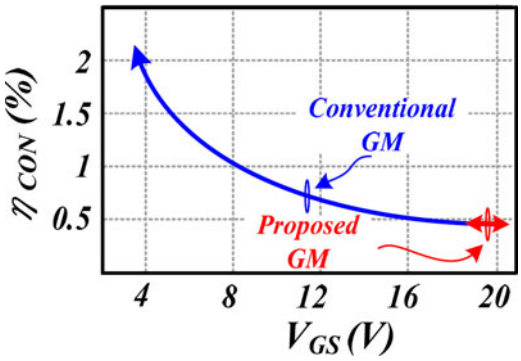


Fig. 9. Influence of conduction loss on light load conversion efficiency in different V_{GP}.

The charging current in (5) flowing through the power transistor is proportional to the input voltage V_{IN} where L_m is the magnetizing inductance of the transformer. Thus, the total conduction power loss $P_{\mathrm{CON\_LOSS}}$ in one switching period T can be derived in (6) by substituting (5) into (4)

$$I_P(t) = \frac{V_{\mathrm{IN}}}{L_m} t \tag{5}$$

$$P_{\mathrm{CON\_LOSS}} = \int_0^{t_{\mathrm{on}}} \left(\frac{V_{\mathrm{IN}}}{L_m} t\right)^2 \frac{1}{\mu_n C_{\mathrm{OX}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{TH}})} dt = \frac{1}{3} \frac{\left(\frac{V_{\mathrm{IN}}}{L_m}\right)^2 t_{\mathrm{on}}^3}{\mu_n C_{\mathrm{OX}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{TH}})}. \tag{6}$$

On the other hand, the input power P_{IN} can be expressed in (7), where the average input current $I_{\mathrm{IN,AVG}}$ is shown in (8). It indicates that P_{IN} is proportional to the product of the square of V_{IN} and the square of the on-time t_{on}

$$P_{\mathrm{IN}} = V_{\mathrm{IN}} I_{\mathrm{IN,AVG}} = V_{\mathrm{IN}} \cdot \frac{I_{P,\mathrm{MAX}} \cdot t_{\mathrm{on}}}{2T} = \frac{V_{\mathrm{IN}}^2 \cdot t_{\mathrm{on}}^2}{2 L_m T} \tag{7}$$

$$\text{where } I_{\mathrm{IN,AVG}} = \frac{1}{2} \cdot \frac{I_{P,\mathrm{MAX}} t_{\mathrm{on}}}{T}. \tag{8}$$

If the calculation of power conduction efficiency η_{CON} in (9) is simplified bt considering the conduction loss $P_{\mathrm{CON\_LOSS}}$, the relationship between η_{CON} and the driving voltage V_{GS} can be determined as shown in Fig. 9

$$\eta_{\mathrm{CON}} = \frac{P_{\mathrm{CON\_LOSS}}}{P_{\mathrm{IN}}} = \frac{2}{3} \cdot \frac{t_{\mathrm{on}} T}{L_m \mu_n C_{\mathrm{OX}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{TH}})}. \tag{9}$$

The driving voltage V_{GS} changes from 19 to 4 V, and correspondingly η_{CON} changes from 0.5% to 2%. Obviously, low driving voltage supplied by V_{DDP} results in the increase of on resistance of power transistor M_P in an exponential relationship. That is to say, the efficiency becomes poor drastically because the charging current I_P flows through the equivalent large on resistance. Much more conduction power loss occurs during the on-time period. In the proposed PPC circuit, the I_{VDP} is composed of the gate leakage current to avoid the V_{DDP} dropping rapidly. Small on resistance can be maintained to effectively reduce conduction power loss.

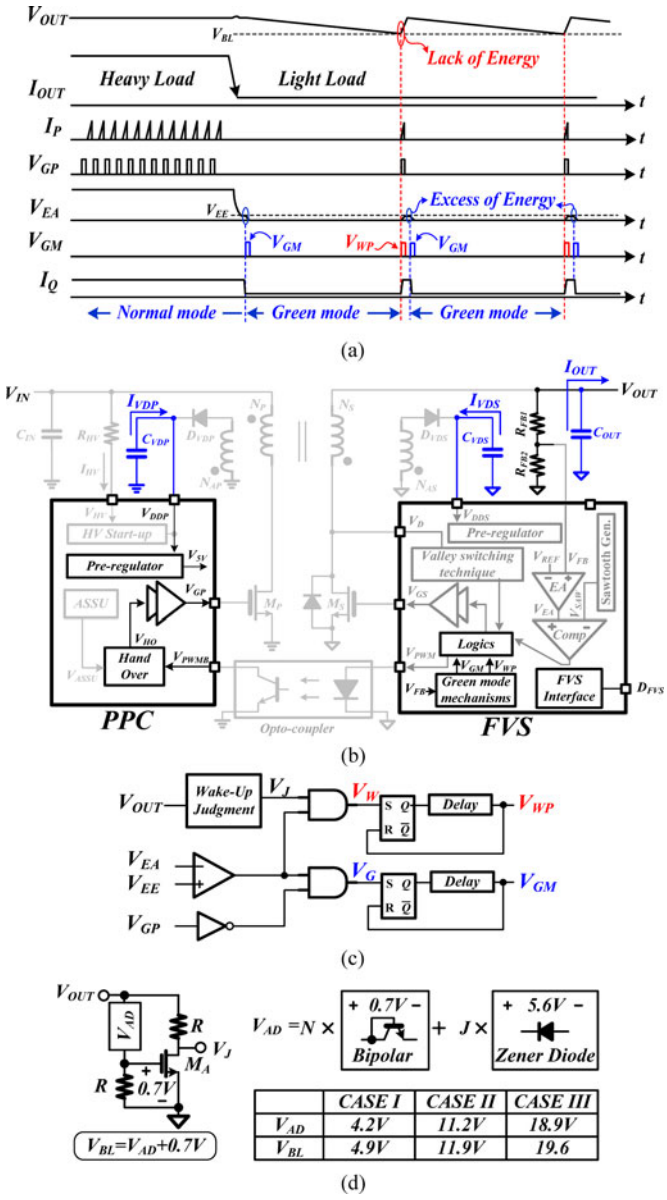


Fig. 10. GM mechanism of the proposed FVS converter. (a) Timing diagram. (b) Circuit implementation of GM mechanism. (c) Circuit implementation of the wake-up judgment circuit and (d) WDJ circuit.

Fig. 10(a) shows the operation of the proposed GM mechanism. At the laptop side, the load condition of the FVS converter can be detected by the output voltage of error amplifier, V_{EA}. Here, lower output loading brings lower V_{EA}. Once the V_{EA} is lower than the predefine reference voltage, V_{EE}, the GM signal, V_{GM}, will be generated immediately to enable the GM mechanism for power saving.

In the GM operation, most of the circuit blocks in the FVS controller excluding logic circuit and GM mechanism will be disabled to reduce power consumption, as depicted in Fig. 10(b). On the other hands, the only power loss is contributed by gate leakage current in the PPC circuit because it is a driver circuit

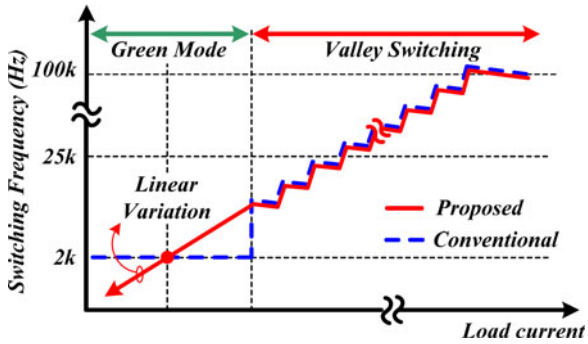


Fig. 11. Switching frequency versus the loading current.

is implemented completely with static digital circuits. The PPC circuit and the FVS controller are supplied by the energy stored in the $C_{\rm VDP}$ and the $C_{\rm VDS}$, respectively. Without unnecessary power consumption of analog circuits, light load efficiency can be improved significantly compared to conventional primary side controllers. Once the $V_{\rm OUT}$ drops to reach the boundary voltage, $V_{\rm BL}$, the pulse signal $V_{\rm WP}$ will be generated to disable the GM mechanism and to wake up the FVS controller. This is followed by the operation of constant on-time gate pulses, which are generated to obtain the minimum energy for the $V_{\rm OUT}$. If the $V_{\rm EA}$ is still lower than the $V_{\rm EE}$, the GM mechanism will be enabled again to impose restrictions on the FVS chip. Therefore, the lower power demand brings the lower switching frequency.

With GM mechanism, the abovementioned merits contribute to good power efficiency at light loads. Fig. 10(c) shows the GM mechanism circuit to determine the $V_{\rm GM}$ and the $V_{\rm WP}$. Once the condition that the $V_{\rm EA}$ is lower than the $V_{\rm EE}$ is detected in the normal mode, the V_G would be set to high. Then, $V_{\rm GM}$ generates a pulse signal to set $V_{\rm GP}$ low. The $V_{\rm GP}$ holds the low state until the $V_{\rm OUT}$ is lower than the boundary $V_{\rm BL}$, which is generated by the wake-up judgment (WDJ) circuit. As a result, V_W is set to high, and $V_{\rm WP}$ generates a pulse signal to set $V_{\rm GP}$ high. The GM circuit repeats the above steps as long as $V_{\rm EA}$ is lower than $V_{\rm EE}$. Once $V_{\rm EA}$ is higher than $V_{\rm EE}$, the GM circuit will be disabled and the FVS converter gets back to the normal operation. Fig. 10(d) shows the circuit implementation of the WDJ circuit. The WDJ circuit can compare the $V_{\rm OUT}$ with the boundary voltage $V_{\rm BL}$, which is the summation of an adjustable voltage $V_{\rm AD}$ and the threshold voltage of M_A. The $V_{\rm AD}$ is determined by different number of bipolar devices and Zener diodes in series. The cross voltages of the bipolar devices and Zener diodes are 0.7 and 5.6 V, respectively. The WDJ circuit changes the number of bipolar devices and Zener diodes in series according to different output voltage for laptop applications. The $V_{\rm BL}$ is designed at 4.9 V for 5 V output voltage, 11.9 V for 12 V output voltage level, and 18.2 V for 19 V output voltage level.

Fig. 11 shows the relationship between the switching frequency and the load current. During the valley switching interval, the off-time control can be derived by selecting one of the valleys at different loads. At ultra-light loads, the conventional converter enters the GM and decreases the switching frequency to be a constant frequency operation. Compared to conventional

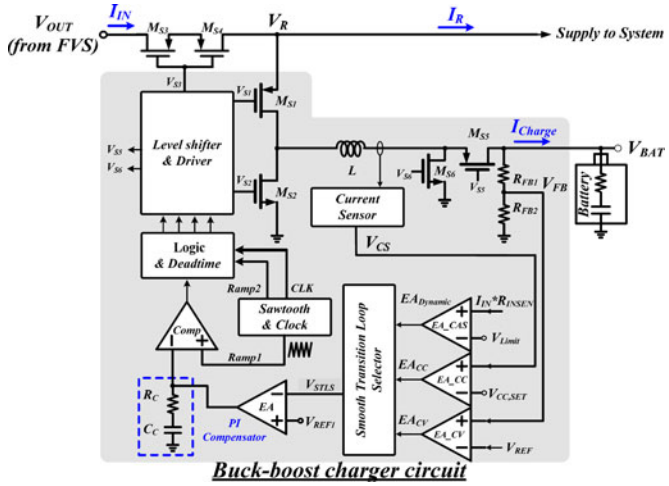


Fig. 12. Design of buck-boost charger circuit.

flyback converter, the FVS converter monitors the output voltage directly and causes the switching frequency decreases continuously. Consequently, the switching frequency becomes lower than 2 kHz. That is, the switching loss can be reduced efficiently without the limit of minimum output loading state.

Fig. 12 shows the modification of the charger circuit compared to conventional charger designs. Owing to the output voltage ranging from 5 to 19 V, the topology of the charger circuit should be modified to the buck-boost topology. Thus, the output voltage $V_{\rm OUT}$ from the FVS controller can be controlled by the main switches $M_{\rm S3}$ and $M_{\rm S4}$ to the system and the battery. The switches $M_{\rm S1}, M_{\rm S2}, M_{\rm S5}$, and $M_{\rm S6}$ constitute the buck-boost converter to control the energy from the $V_{\rm OUT}$ to the $V_{\rm BAT}$. Besides, three error amplifiers, $EA_{\rm dynamic}$, $EA_{\rm CC}$, and $EA_{\rm CV}$, are used to implement the function of dynamic power management, constant current control, and constant voltage control, respectively. The details of the buck-boost operation were shown in [21] and [22].

V. Experimental Results

The proposed FVS converter with the ASSU technique and the GM mechanism was implemented in a 0.5 μm 500 V UHV process. Fig. 13 shows the measurement results of the different output powers of laptop with the input ac rms voltage of 110 V. The variable output voltage including 5, 12, and 19 V is selected by the FVS interface according to output power varying from 10 to 100 W. The FVS controller generates the gate control signal $V_{\rm GS}$ to control the laptop side power stage and the gate control signal $V_{\rm GP}$ to control the adapter side power stage through the feedback path of the photo-coupler. Fig. 13(a) shows the output power is 10 W when $V_{\rm OUT}$ is regulated at 5 V. Fig. 13(b) and (c) shows the output power is 18 and 36 W, respectively, when $V_{\rm OUT}$ is regulated at 12 V. Fig. 13(d) and (e) shows the output power is 60 and 100 W, respectively, if $V_{\rm OUT}$ is regulated at 19 V. Here, 100 W is the maximum output power of the FVS converter. Fig. 14 shows measurement results

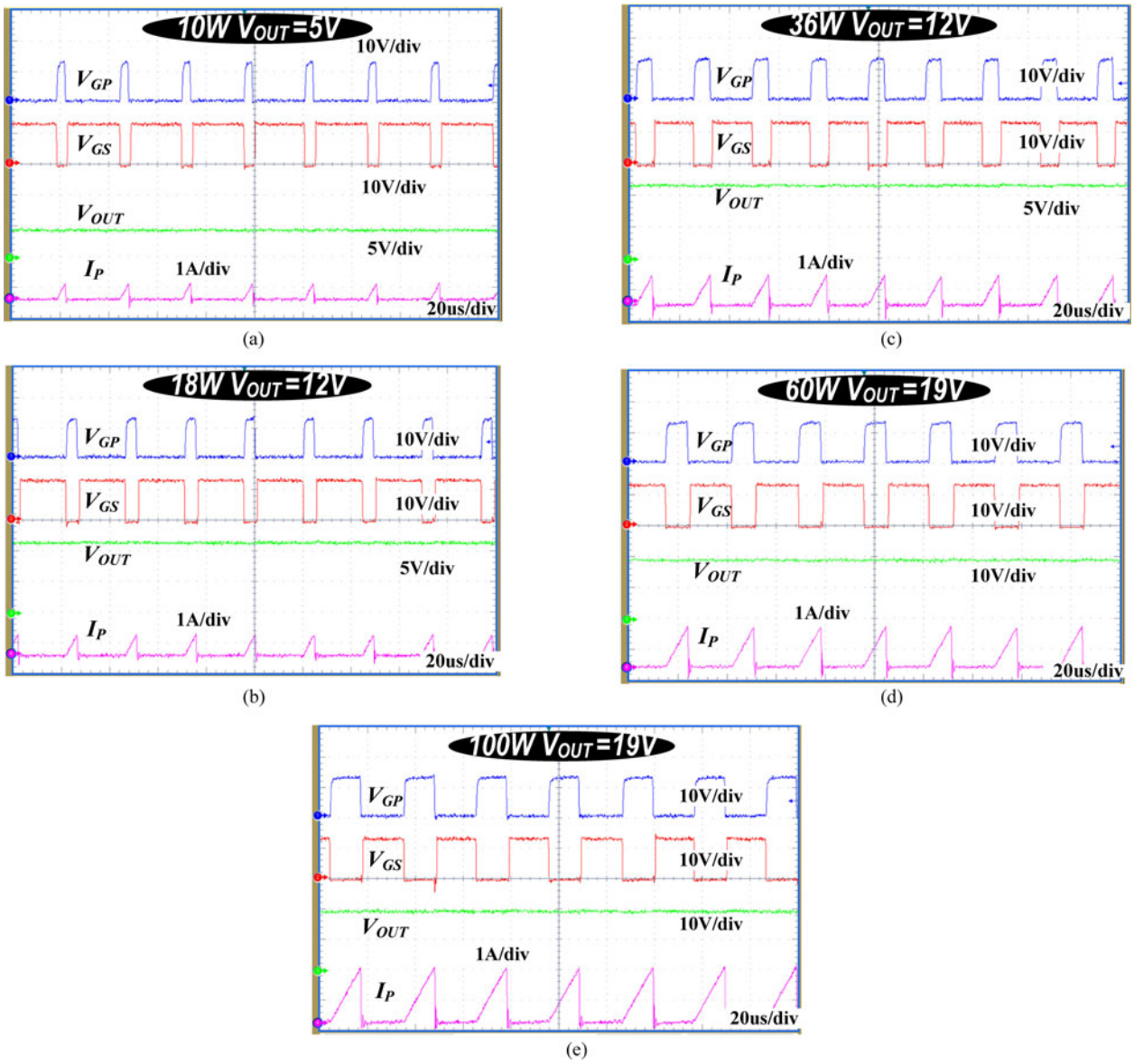


Fig. 13. Measurement results of five different output power. (a) 10 W output power. (b) 18 W output power. (c) 36 W output power. (d) 60 W output power. (e) 100 W output power.

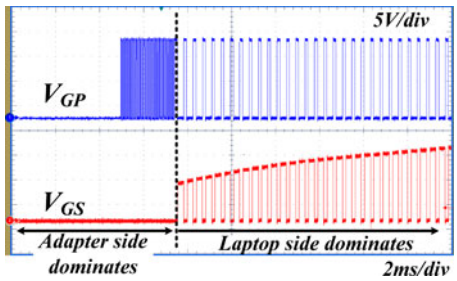


Fig. 14. Adapter side start-up procedure.

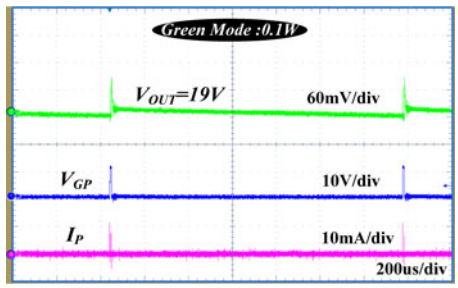


Fig. 15. GM mechanism.

of the start-up procedure at the adapter side. The PPC circuit is directly powered on by the high voltage. Meanwhile, the ASSU circuit generates constant frequency gate pulses to power on the FVS controller. Once the FVS controller starts to work, the PPC circuit is turned off and the FVS controller dominates the whole system behavior. Fig. 15 shows measurement results

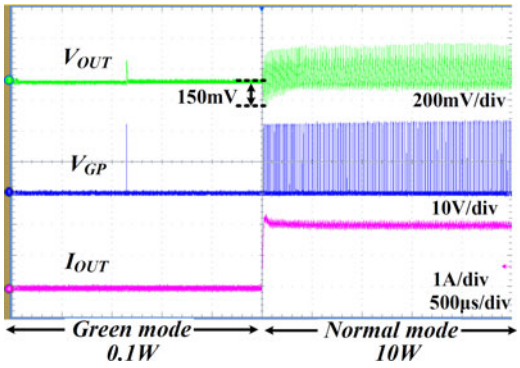


Fig. 16. Load transient response ($V_{\rm OUT} = 5$ V).

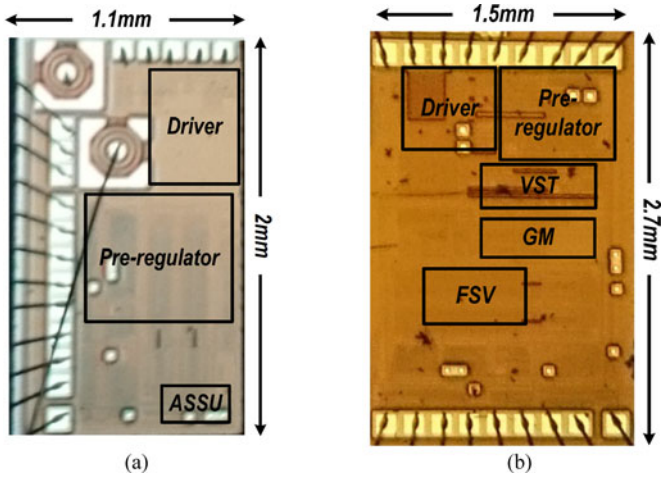


Fig. 17. Chip micrographs of (a) PPC circuit and (b) FVS controller.

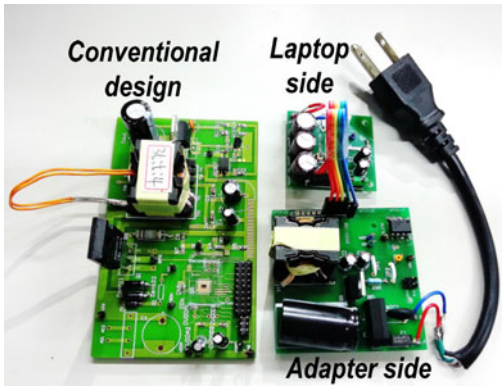


Fig. 18. Prototype of the FVS converter in comparison with a conventional design.

under the GM mechanism. When the requirement of output power decreases to 0.1 W, the GM mechanism reduces the switching frequency to 800 Hz correspondingly. At this time, the voltage ripple is about 100 mV.

Fig. 16 shows the load transient response of the proposed FVS converter during the GM operation. The output load changes

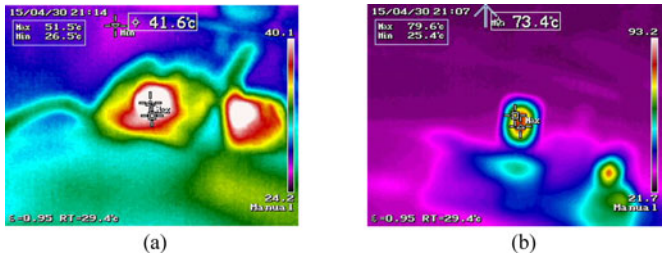


Fig. 19. Infrared thermal image of (a) proposed prototype and (b) conventional adapter.

TABLE I
DESIGN SPECIFICATIONS

Design Summary	
Technology	0.5 μm 500 V UHV
Input voltage (V)	AC 90–264
Output voltage (V)	5–19
Primary inductor (L_m)	400 μH
Primary winding turns (N_P)	25 T
Secondary winding turns (N_S)	5 T
Auxiliary winding turns ($N_{\rm AP}$)	5 T
Secondary auxiliary winding turns ($N_{\rm AS}$)	5 T
Output capacitor ($C_{\rm out}$)	200 μF
Maximum output power (W)	100
Switching frequency (Hz)	0.1 k–60 k
Overall efficiency	87%@2.4 A
Chip area (mm^2)	2.2 + 4.05

from 0.1 to 10 W. The FVS converter gets back to the normal operation when $V_{\rm OUT}$ is lower than the boundary $V_{\rm BL}$, 4.9 V. The voltage drop in case of the mode changing operation is about 150 mV. Chip micrographs including the PPC circuit and the FVS controller are shown in Fig. 17(a) and (b), respectively. Silicon area of the PPC chip and the FVS chip is 2.2 and 4.05 mm^2, respectively. The prototype of FVS converter is shown in Fig. 18 in comparison with a conventional design. The dimension of the proposed FVS converter has a size reduction of approximately 30% in comparison with a conventional design. The operation temperature of the prototype is also lowered from 75°C to 50°C in comparison with a conventional design, as shown in Fig. 19(a) and (b), respectively. The detailed design specifications are listed in Table I.

Fig. 20 shows the measurement results of conversion efficiency and the design summary. Considering overall power efficiency from the ac to the dc, light-load efficiency and peak efficiency are 65% and 80%, respectively, in conventional design with only the DVS technique but without the FVS technique. The FVS function is turned off to obtain the efficiency of DVS-only curve. The FVS function is turned on to obtain the efficiency of FVS + DVS curve. In contrast, 77% light-load efficiency and 87% peak efficiency are achieved by the FVS and the DVS techniques at the same time in this study. As a result, 12% light load efficiency and 7% peak efficiency are improved. Besides, the efficiencies of [12] and [13] are compared to the proposed FVS converter if cascading the same DC-DC converter

TABLE II
EFFICIENCY MEASUREMENTS IN DIFFERENT TECHNIQUES

	Load (A)	0.1	0.5	1	1.5	2	2.5	3	3.5	4	4.5	5
Laptop Efficiency	dc/dc converter (5 V)	0.9	0.92	0.925	0.94	0.955	0.961	0.962	0.961	0.96	0.958	0.95
	dc/dc converter (12 V)	0.86	0.88	0.9	0.905	0.92	0.92	0.92	0.91	0.91	0.9	0.89
	dc/dc converter (20 V)	0.81	0.83	0.85	0.87	0.88	0.885	0.89	0.89	0.89	0.888	0.885
Adapter Efficiency	DVS only (V_{OUT} = 20 V)	0.81	0.85	0.875	0.89	0.9	0.9	0.9	0.89	0.89	0.88	0.87
	Ref [12] (V_{OUT} = 20 V)		0.86	0.88	0.878	0.87	0.86	0.855	0.84	0.82		
	Ref [13] (V_{OUT} = 12 V)			0.92	0.925	0.935	0.932	0.93	0.925			
	FVS	0.83	0.84	0.89	0.89	0.92	0.93	0.925	0.89	0.89	0.88	0.87
Overall Efficiency	DVS only	0.65	0.7	0.74	0.77	0.79	0.79	0.8	0.79	0.79	0.78	0.77
	Ref [12]		0.71	0.74	0.76	0.76	0.76	0.76	0.74	0.72		
	Ref [13]			0.82	0.83	0.86	0.85	0.85	0.84			
	FVS	0.74	0.77	0.82	0.83	0.84	0.85	0.85	0.8	0.79	0.78	0.76

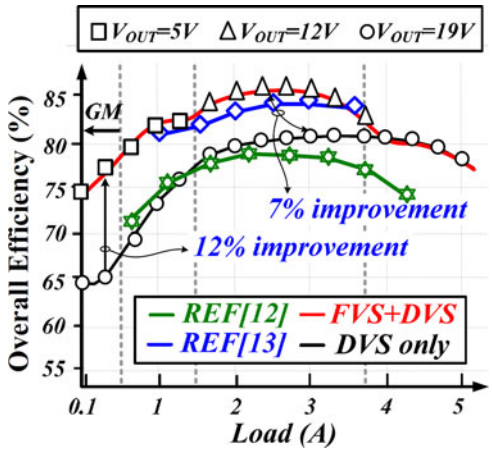


Fig. 20. Overall power conversion efficiency.

as shown in Fig. 20. The detail measured efficiency results are shown in Table II in comparison with the other designs.

VI. CONCLUSION

To achieve high efficiency ac/dc converter with minimized the number of external components, the proposed OPM in laptop can improve the overall conversion efficiency by the FVS technique in cooperation with conventional DVS technique. The proposed GM mechanism disables most of circuit blocks in the FVS controller and the switching frequency is scaled down to 0.1 kHz to effectively reduce chip quiescent current to 11 μA and to suppress ultra-light load power loss to 10 mW. This value is significantly lower than the 500 mW standby power defined by the restriction of Energy Star Standard and 40 mW of state-of-the-art commercial products. The OPM implemented in laptops improves 12% light load efficiency and 7% peak efficiency by the FVS and the DVS techniques at the same time compared to conventional design simply using DVS technique only.

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Shang-Hsien Yang received the B.S. and M.S. degrees in electrical engineering from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2009 and 2011, respectively. He is currently working toward the Ph.D. degree at the Institute of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan.

He is presently a Member of the Mixed Signal and Power Management IC Laboratory, National Chiao Tung University. His current research interest includes envelope tracking supply modulators for RF power amplifiers used in LTE applications, class-D audio amplifiers and ac/dc power converters.

Chao-Chang Chiu received the B.S. degree from Fu Jen Catholic University, Taipei, Taiwan, in 2008, the M.S. degree from National Central University, Taoyuan, Taiwan, in 2010, and the Ph.D. degree from National Chiao Tung University, Hsinchu, Taiwan, in 2014.

He joined MediaTek in 2014. His research interests include power management integrated circuit designs and analog integrated circuit designs.

Chih-Wei Chang was born in Taichung, Taiwan. He received the B.S. and M.S. degrees from the Department and Institute of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2012 and 2014, respectively.

He joined MediaTek in 2014. His research interests include the power management IC design, analog integrated circuits, mixed signal IC design, and high power ac/dc power converter designs.

Chen-Min Chen was born in Changhua City, Taiwan. He received the B.S. degree from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2003, and the M.S. degree from the Institute of Electrical and Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2014.

He is currently a Technical Marketing Manager at Advanced Power Electronics Corp., Zhubei, Taiwan. He is a Member of the Mixed-Signal and Power Management IC Laboratory, Department of Electrical and Control Engineering, National Chiao Tung University. His research interests include the ac/dc converter power system design and analog integrated circuit designs.

Che-Hao Meng was born in Taipei, Taiwan. He received the B.S. and M.S. degrees from the Department and Institute of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2012 and 2014, respectively.

He joined MediaTek in 2014. His research interests include power management IC designs, analog circuit designs, and high power ac/dc power converter designs.

Ke-Horng Chen (M'04–SM'09) received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1994, 1996, and 2003, respectively.

He is currently a Director and Professor at the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he organized the Mixed-Signal and Power Management IC Laboratory. He is the author or coauthor of more than 200 papers published in journals and conferences, and also holds more than 40 U.S. patents and 40 Taiwan patents. His current research interests include power management ICs, display algorithm and driver designs of liquid crystal display TV, wireless power transfer, and energy harvesting circuit designs.

Dr. Chen has served as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS. He serves as the CAS Taipei Section Chair from 2015. He is the Technical Program Committee Member, European Solid-State Circuits Conference (ESSCIRC) (2014–present). He is on the IEEE Circuits and Systems (CAS) VLSI Systems and Applications Technical Committee, and the IEEE CAS Power and Energy Circuits and Systems Technical Committee.