Simplified Three-Level Five-Phase SVPWM

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***Abstract*—A simplified space vector pulse width modulation (SVPWM) is proposed for a three-level five-phase inverter. The proposed method generates the duty cycle of the three-level inverter switches based on dwell times of the two-level inverter and carrier index. The proposed method automatically determines the eligible vectors, region, and switching sequence of optimized five vectors based on the modulation index. Out of 243 available vectors, 113 most eligible vectors are used for generation of desired voltage reference in main subspace, while zeroing the average voltage in the auxiliary subspace by using the proper switching sequence. This method also uses the redundant vectors in each subcycle thus balances the dc-link capacitor voltages and no additional algorithm or techniques are needed to balance the dc-link capacitor voltage. The identification of the reference location with the carrier index using the signum function simplifies the algorithm implementation. Thus, the proposed method eases the implementation of optimum five vectors to a greater extent. Based on only changing the carrier index, the proposed method can be easily extended for any multiphase multilevel (5, 7, . . . , n) inverter. The simulation and hardware results of the three-level five-phase inverter validate the proposed simplified method.**

***Index Terms*—Multiphase multilevel inverter, space vector pulse width modulation (SVPWM), three-level five-phase inverter.**

I. Introduction

MULTILEVEL inverters are proposed as an alternative for medium- and high-power applications in industries due to their advantages like low-output harmonics in the voltage and current, low switching loss, reduced *dv/dt*, and reduced common mode voltage [1]–[3]. On the other hand, multiphase drives gained attention for the applications like ship propulsion, electric traction, hybrid and electrical vehicles due to their advantages like higher fault tolerance, reduced amplitude, and increased frequency of torque pulsation, reduced dc-link current harmonics, reduced size due to higher power density, and reduced current per phase compared with traditional three-phase drives [4]–[6]. Hence, the multilevel multiphase drives possess both of the previously mentioned advantages. In multiphase drive systems, major research works have focused on developing space vector pulse width modulation (SVPWM) for two-level inverters initially and then for three-level, due to their inherent advantages.

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In [7], an SVPWM technique is proposed to produce the sinusoidal voltage which is free from lower-order harmonics by making the average voltage in the auxiliary subspace to zero by applying the large vector 1.618 times more than the medium vector time in each sampling interval. In [8], an SVPWM technique is proposed for the nine-phase two-level inverter based on the unified method by centering the active vectors by offset addition. In case of three-level five-phase applications, an algorithm based on three nearest vectors was proposed in [9], but it does not consider the auxiliary subspace. In [10], an SVPWM technique is proposed for three-level five-phase with the aim of reducing the torque ripple based on "walking pattern" to select the vectors but does not consider the auxiliary space. In [11], a novel multilevel multiphase SVPWM algorithm with switching redundancy is proposed for the five-phase three-level inverter and implemented with FPGA. In [12], a novel algorithm for the three-level five-phase SVPWM technique is developed by considering the auxiliary subspace also. The average voltage in the auxiliary space is made to zero by selecting proper vector and switching sequences. A novel region determination scheme is proposed to locate the reference vector and subregion. A number of voltage vectors are minimized by selecting the eligible vectors based on the phase voltage relationship. All the switching sequence will not yield the average zero voltage in the auxiliary subspace. To make the auxiliary subspace voltage to zero, the optimized five vector (OFV) strategy and the efficient switching sequence are proposed instead of the nearest three vector concept.

In [13] and [14], SVPWM is proposed for the three-phase three-level inverter by simplifying the three-level SVPWM into a two-level SVPWM diagram. In this, the three-level SVPWM diagram is modified into a two-level SVPWM diagram by constructing many small hexagon from the three-level SVPWM diagram, and dwelling times of three-level voltage vectors are calculated in same manner as two-level. But this method cannot be used for five-phase, since decagons formed in five phase are asymmetrical, whereas hexagon formed in three phase is symmetrical. Hence, small decagons cannot be formed and above method cannot be directly extended for multiphase applications.

In this paper, a novel simplified implementation of OFV is proposed based on two-level switching times and carrier index signals. The proposed method selects the OFVs and their switching sequence based on the modulation index value. The simulation and prototype results for different modulation index are presented, and this validates the effectiveness of the proposed implementation technique. The complexity of its implementation is sorted out by using the decoding logic through multiplexer. Hence, the proposed algorithm reduces the complexity in determining the OFVs. Also, the proposed method uses the five PWM modules and five I/O blocks of the DSP Controller TMS320 F28027. Thus, the need of DSP with more

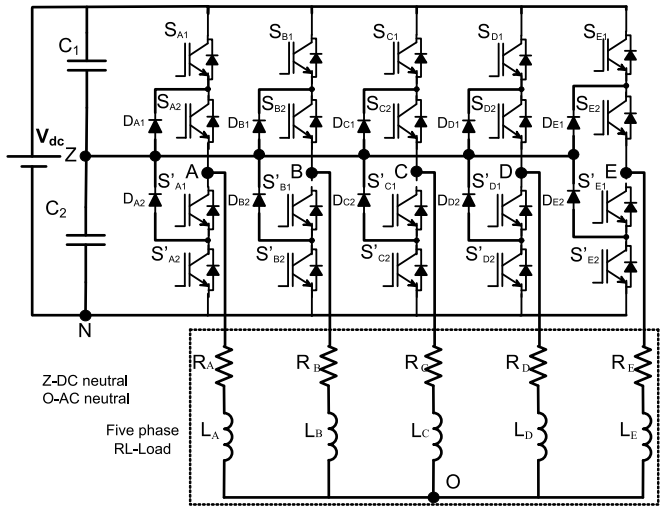

Fig. 1. Three-level five-phase inverter.

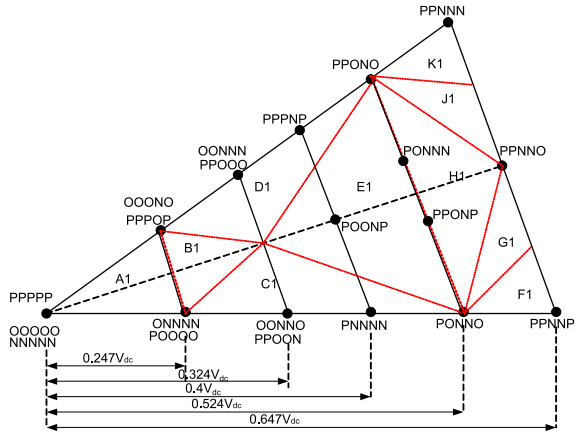

Fig. 2. Eligible vectors.

TABLE I
SWITCHING STATES AND LEG VOLTAGES ($x = A, B, C, D, E$)

Switching states	Device States				Leg Voltage (V_{xZ})
	S_{x1}	S_{x2}	S'_{x1}	S'_{x2}	
P (or) 1	ON	ON	OFF	OFF	$V_{dc}/2$
O (or) 0	OFF	ON	ON	OFF	0
N (or) -1	OFF	OFF	ON	ON	$-V_{dc}/2$

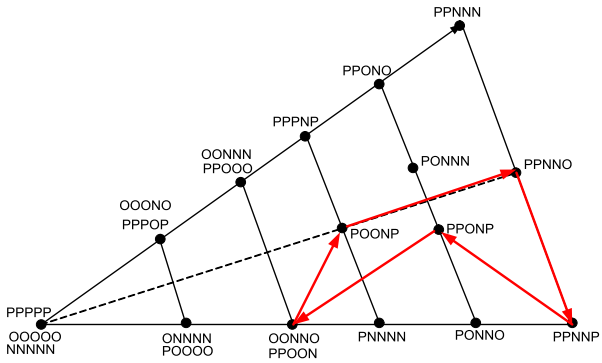

Fig. 3. Optimum switching sequence in Region F1.

number of PWM modules [12] or an FPGA [11] is eliminated by simple I/O pins of standard low-cost DSP for multiphase multilevel applications.

II. Three-Level Five-Phase Diode Clamped Inverter

The hardware topology of a three-level five-phase inverter is shown in Fig. 1. It consists of five legs and each leg has four switches that must be controlled in two complementary combination pair only. The switches S_{x1} and S'_{x1} ($x = A, B, C, D, E$) are one complementary pair, and S_{x2} and S'_{x2} the other. Each leg voltages can attain three voltage levels by controlling the four switches as listed in Table I.

Thus, total number of possible switching states are $3\text{^}5 = 243$. Out of these, 240 are nonzero vectors, and 3 are zero vectors. By joining the tips of nonzero vectors, a number of decagons are formed, which consists of ten distinct sectors spanning 360°.

The detailed explanation of projection of voltage vectors in the main and auxiliary subspace is given in [12]. All the 243 vectors are not eligible since some of the voltage vectors do not obey the phase voltage relationship in each sector as elaborated in [12], and by application of some vectors cause magnetic flux to counteract each other as covered in [9]. The total eligible vectors available are reduced to 113 vectors only. Throughout this paper, Sector-I is taken as an example case to prove the validity of algorithm and for other sectors it can be proved in a similar manner. Total 21 vectors are eligible in Sector-I including zero vectors. Each sector is divided into subregions as explained in Fig. 2 by dotted red lines. The optimum five vectors switching sequence in Region F1 based on [12] is shown in Fig. 3.

III. Mapping of Two-Level Dwell Time to Three-Level

The switching states available for each leg of the two-level inverter are 1 and 0. The switching states for the three-level inverter are "*P*," "*O*," and "*N*" as shown in Table I. The idea behind the mapping of the switching state of two level to three level is based on the following conditions.

1) if the reference phase voltage is positive, then the corresponding leg voltage should also be positive and vice versa;
2) the average positive leg voltage in a sampling interval will be obtained by applying combination "*P*"' and "*O*" switching state in three level;
3) to obtain the average negative leg voltage combination of "*N*" or "*O*" switching state is applied in three level;
4) when the leg voltage is positive, the order and duty of "*P*" or "*O*" switching state of three level is determined by the two-level switching state;

5) on the other hand, if the leg voltage is negative the order and duty of "*N*" or "*O*" switching state of three level is determined by the two-level switching state.

Thus, based on the two-level dwell time and reference phase voltage carrier index, the dwell time of the three-level inverter can be obtained. The two-level dwell time can be found out by a simple method as specified in [15]. The generation of the carrier index from the reference voltage is explained in following section.

A. Two-Level Dwell Time Calculation

The imaginary time equivalent of the phase voltage can be obtained from (1) by extending the concept described in [13] and [15]. This provides the two-level switching time

$$T_a = \frac{2^* V_{\mathrm{AO}}}{V_{\mathrm{dc}}} T_s; T_b = \frac{2^* V_{\mathrm{BO}}}{V_{\mathrm{dc}}} T_s; T_c = \frac{2^* V_{\mathrm{CO}}}{V_{\mathrm{dc}}} T_s;$$
$$T_d = \frac{2^* V_{\mathrm{DO}}}{V_{\mathrm{dc}}} T_s; T_e = \frac{2^* V_{\mathrm{EO}}}{V_{\mathrm{dc}}} T_s \quad (1)$$

$$T_{\mathrm{eff}} = T_{\max} - T_{\min} \quad (2)$$

$$T_{\max} = \mathrm{Max}(T_a, T_b, T_c, T_d, T_e) \quad (3)$$

$$T_{\min} = \mathrm{Min}(T_a, T_b, T_c, T_d, T_e) \quad (4)$$

$$T_{\mathrm{offset}} = \frac{1}{2}\left(2^* T_s - (T_{\max} - T_{\min})\right). \quad (5)$$

V_{AO}, V_{BO}, V_{CO}, V_{DO}, and V_{EO} are sampled amplitudes of the reference voltage of phases A, B, C, D, and E, respectively, T_s is the sampling time period, and T_{eff} is the effective time. The switching time obtained by (1) could be negative if reference voltage is negative. In order to eliminate the negative time of switches, an offset has to be added based on the effective time and it is given by (5). The actual duty cycle is obtained by following equations:

$$T_{ga} = \frac{2^* V_{AO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}} \quad (6)$$

$$T_{gb} = \frac{2^* V_{BO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}} \quad (7)$$

$$T_{gc} = \frac{2^* V_{CO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}} \quad (8)$$

$$T_{gd} = \frac{2^* V_{DO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}} \quad (9)$$

$$T_{ga} = \frac{2^* V_{AO}}{V_{\mathrm{dc}}} T_s + T_{\mathrm{offset}}. \quad (10)$$

B. Generation of the Carrier Index

The carrier index is used to find the location of the reference voltage [16]. Basically, it is used to determine whether the reference voltage is greater than zero or less than zero in case of a three-level inverter. The carrier index for three level can be obtained from the signum function

As shown in Fig. 4, if the reference voltage is greater than zero, it gives output as 1; and if it is less than zero, it gives output as 0. The carrier index for each of the five-phase is found by the signum function.

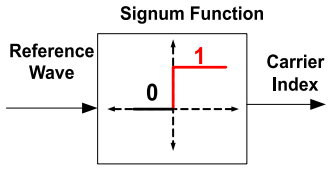

Fig. 4. Carrier index generation.

TABLE II
MAPPING OF TWO-LEVEL SWITCHING STATE TO THREE-LEVEL SWITCHING STATE

Carrier Index	Two-Level Switching State	Three-Level Switching State
0	0	*N*
0	1	*O*
1	0	*O*
1	1	*P*

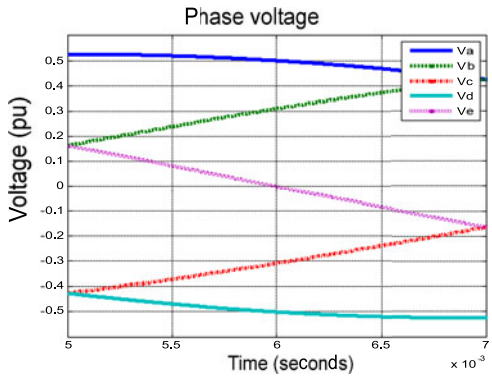

Fig. 5. Phase voltage relationship in Sector-I.

C. Mapping

Based on the two-level switching time and carrier index, the logic for mapping two-level switching state to three-level switching state as explained in Section III can be summarized as truth table format in Table II.

Based on the above truth table, mapping of two-level switching state to three level is explained for all the five-phase graphically for two cases in Sector-I. The phase voltage relationship in Sector-I is shown in Fig. 5. The Case-I is $(V_{\mathrm{AO}}, V_{\mathrm{BO}}, V_{\mathrm{EO}}) \geq 0$ and $(V_{\mathrm{CO}}, V_{\mathrm{DO}}) < 0$ and Case-II is $(V_{\mathrm{AO}}, V_{\mathrm{BO}}) \geq 0$ and $(V_{\mathrm{CO}}, V_{\mathrm{DO}}, V_{\mathrm{EO}}) < 0$. The switching states of three level for Case-I and Case-II in Sector-I are shown in Figs. 6 and 7, respectively.

From mapping only, the switching state of three level is obtained but not duty cycle of each switch. The duty cycle of each switch can be obtained with the help of Table I. The duty cycle for phases "A" and "E" for Case-II obtained using Table I are shown in Figs. 8 and 9, respectively.

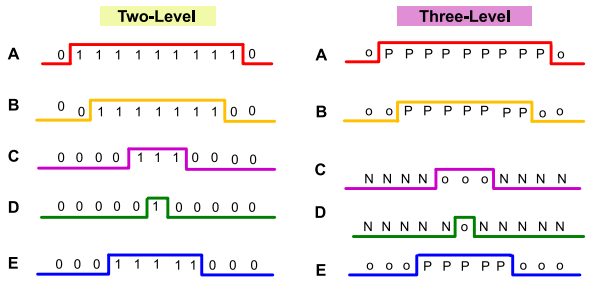

Fig. 6. Case-I.

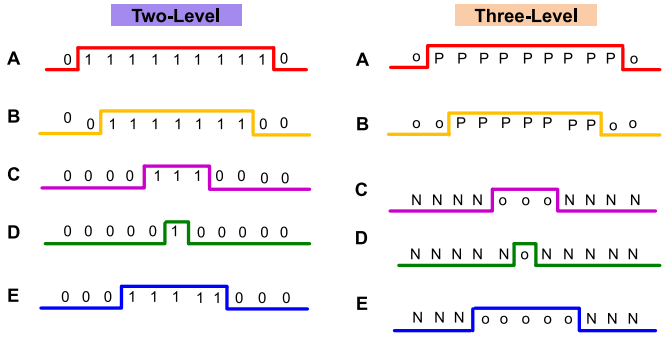

Fig. 7. Case-II.

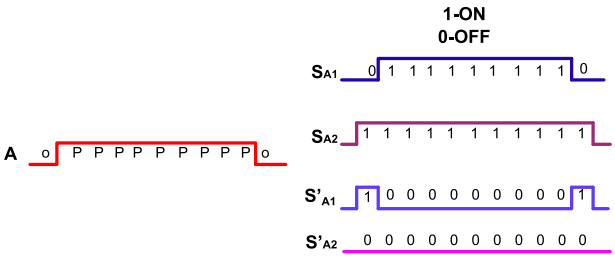

Fig. 8. Duty cycle of phase A.

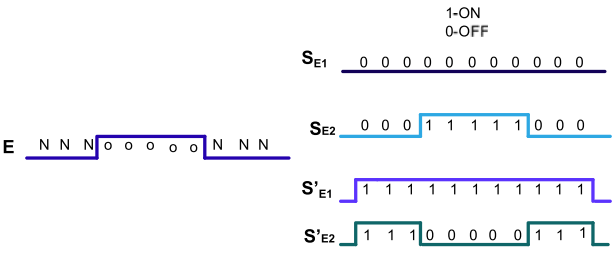

Fig. 9. Duty cycle of phase E.

D. Validation of the Algorithm for the Optimal Five-Vector Switching Strategy

The mapping of the switching state for the three-level inverter based on the two-level switching state automatically selects the OFV based on the modulation index is 1, the reference vector is in Sector-I and in the Region F1.

As per [12], the optimum five-vector switching strategy is shown in the Fig. 3 by red lines with arrow heads. The switching sequence obtained from the proposed method is OONNO-PONNO-PPNNO-PPNNP-PPONP-PPOOP based on Fig. 6 which is same as that of the optimum vector in [12]. Also this method does not require any additional algorithm for balancing the dc-link capacitor voltages since in each cycle redundant voltage vectors are used and applied for same duration.

For example, in the Region F1, OONNO and PPOOP are redundant vectors which are of same magnitude and their application only vary the current direction through the capacitors and not the output voltage magnitude. Thus, in each switching cycle, the capacitor is charged and discharged for equal time and hence maintains the dc-link midpoint voltage of capacitors to be zero always in each subcycle. The OFVs in Sector-I for different subregions are shown in Table III.

TABLE III
OPTIMUM FIVE-VECTOR SWITCHING SEQUENCE IN SECTOR-I

Subregion	Inverter states used during switching sequence
1 (A1)	OONNO-OOONO-OOOOO-POOOO-PPOOO-PPOOP
2 (B1)	OONNO-OOONO-POONO-POOOO-PPOOO-PPOOP
3(C1)	OONNO-PONNO-POONO-POOOO-PPOOO-PPOOP
4 (D1)	OONNO-PONNO-POONO-PPONO-PPOOO-PPOOP
5 (E1)	OONNO-OOONO-POONO-PPONO-PPOOO-PPOOP
6 (F1)	OONNO-PONNO-PPNNO-PPNNP-PPONP-PPOOP
7(G1)	OONNO-PONNO-PPNNO-PPONO-PPONP-PPOOP
8(H1)	OONNO-PONNO-PPNNO-PPONO-PPOOO-PPOOP
9(I1)	OONNN-PONNN-PONNO-PPNNO-PPONO-PPOOO
10(J1)	OONNN-PONNN-PPNNN-PPNNO-PPONO-PPOOO

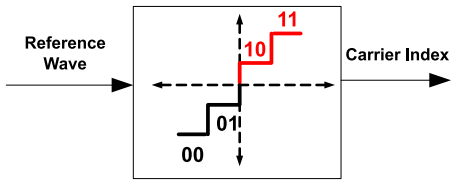

Fig. 10. Carrier index generator for five level.

E. Extension to Multilevel SVPWM

The proposed method is also applicable for the multilevel having odd numbers greater than three. Since for even number of phases, T_{offset} will be zero. For example, to implement SVPWM for the five-level five-phase inverter from two-level switching sequences, only the carrier index has to be changed. Basically, the carrier index represents the carrier region in which the reference wave is located in the present sampling interval. For five level, the carrier index will be 00, 01, 10, and 11 indicating the location of the reference wave as shown in Fig. 10.

IV. SIMULATION RESULTS

Initially, to verify the proposed algorithm, the simulations are made with the help of MATLAB SIMULINK blocks and S-functions to generate the gate pulse for the five-phase three-level inverter. The parameters used for the simulation are: $V_{\text{dc}} = 250$ V, the value of dc-link capacitors are C_1, $C_2 = 2200$ uF/450 V with ESR of 0.06 Ω and *RL* load is used with $R = 350$ Ω,

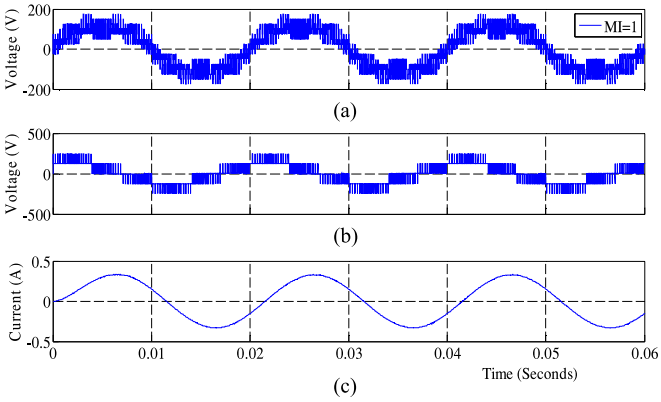

Fig. 11. Simulated phase voltage, line voltage, and line current for $\mathrm{MI} = 1$.

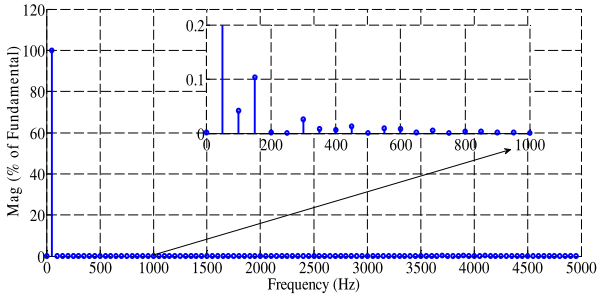

Fig. 12. FFT analysis of the line current for $\mathrm{MI} = 1$.

$L = 600$ mH per phase. The output frequency (f) of the inverter is 50 Hz, the switching frequency is $f_s = 4$ kHz, and the sampling interval T_s is 0.25 ms. For simulation, the dead time between the complementary switches is not considered.

The adjacent line voltage is used as the line voltage throughout this paper. Fig. 11 shows the phase and line voltage obtained from simulation for the modulation index $(\mathrm{MI}) = 1$ using the simplified SVPWM method for the three-level five-phase inverter. Fig. 12 shows the simulated harmonic spectrum of the line current waveform for $\mathrm{MI} = 1$. The low-order harmonics in the line current is around 0.2% of the fundamental. The dc-link capacitors voltage variation for $\mathrm{MI} = 1$ in C1 and C2 is around 0.02 V only as shown in Fig. 13. Figs. 14 and 15 show the phase, line voltage, line current, and their harmonic spectrum, respectively, for $\mathrm{MI} = 0.4$. The dc-link capacitor variation for $\mathrm{MI} = 0.4$ is shown in Fig. 16.

V. Experimental Results

The proposed algorithm is validated by conducting the experiments on prototype of the five-phase three-level inverter build in the laboratory for different modulation index values. The power semiconductor switch used for making inverter is IGBT (IRG4PH50UD). The dc-link voltage of VSI is generated from the single-phase diode bridge rectifier. The hardware specifications are same as the one used in simulation. The switching frequency is kept at 4 kHz, and TMS320F28027 launch pad

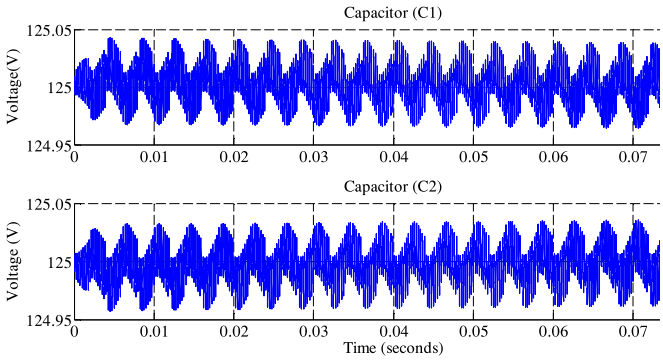

Fig. 13. Simulated dc-link capacitor voltage for $\mathrm{MI} = 1$.

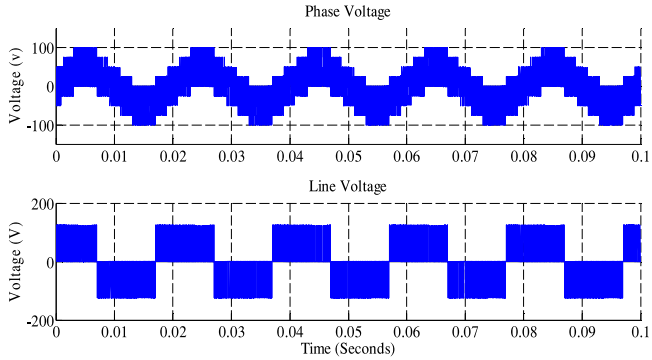

Fig. 14. Simulated phase and line voltage for $\mathrm{MI} = 0.4$.

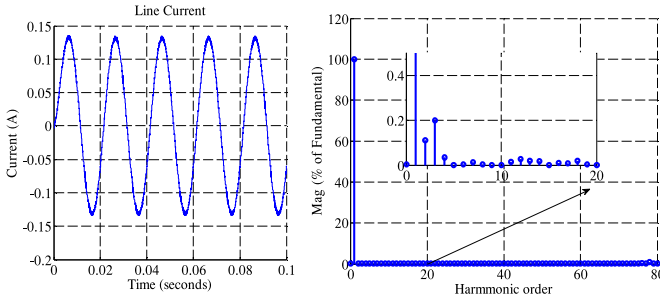

Fig. 15. Line current and its FFT analysis for $\mathrm{MI} = 0.4$.

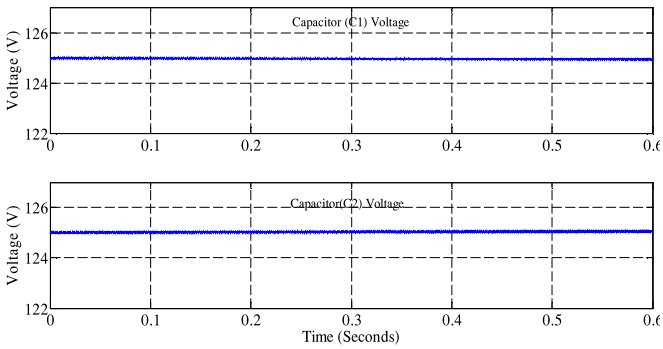

Fig. 16. DC-link capacitor voltage for $\mathrm{MI} = 0.4$.

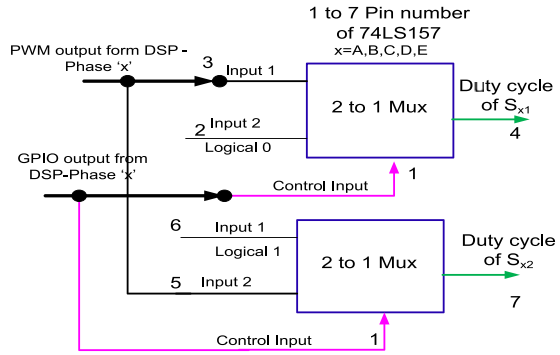

Fig. 17. Decoding logic using multiplexer.

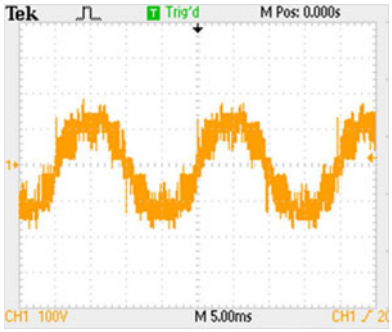

Fig. 18. Experimental result of the phase voltage for $\mathrm{MI} = 1$ (CH1:5 ms/div, 100 V/div).

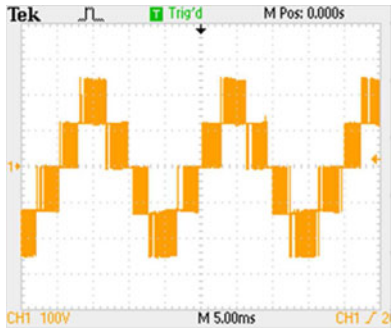

Fig. 19. Experimental result of the line voltage for $\mathrm{MI} = 1$ (CH1:5 ms/div, 100 V/div).

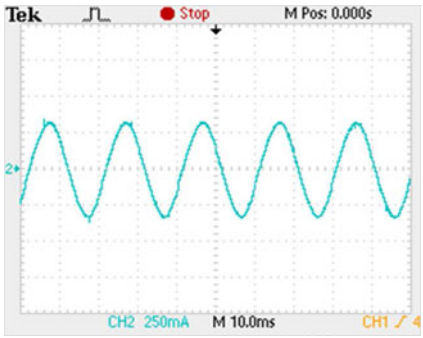

Fig. 20. Line current of prototype result for $\mathrm{MI} = 1$ (CH1:10 ms/div, 250 mA/div).

is used for generation of pulses needed for the inverter. The DSP TMS320F28027 launch pad used in the experiment is a 60 MHz, 32-bit fixed point processor having four enhanced PWM modules for pulse generation. Each PWM module can generate two independent PWM outputs and thus total eight independent PWM outputs are possible from it. In addition to this, there are general purpose I/O pins and other peripheral functions like analog-to-digital converter, enhanced quadrature encoder pulse, enhanced capture modules, and communication modules like CAN, I2C, SPI are available which makes its best suitable for electric drive applications.

The two-level switching times are obtained using enhanced PWM blocks of TMS320F28027 for all the five phase, and the carrier index information is obtained from five independent general purpose I/O ports of DSP. The generation of three-level switching time is obtained as per the truth table shown in Tables I and II. The decoding of the logic is implemented by using simple 2 to 1 multiplexer 74LS157 and it is explained in Fig. 17. The complementary output and dead band are obtained with the help of driver IC IR2111.

The waveforms are shown for two different modulation indices to show effectiveness of the algorithm. Fig. 18–Fig. 22 show the experimental results obtained from the hardware prototype build for $\mathrm{MI} = 1$. The number of voltage levels in phase voltage and line voltage is found to be 15 and 5, respectively, for five-phase balanced star-connected load when $\mathrm{MI} = 1$. In the hardware prototype also, the phase voltage has 15 voltage levels

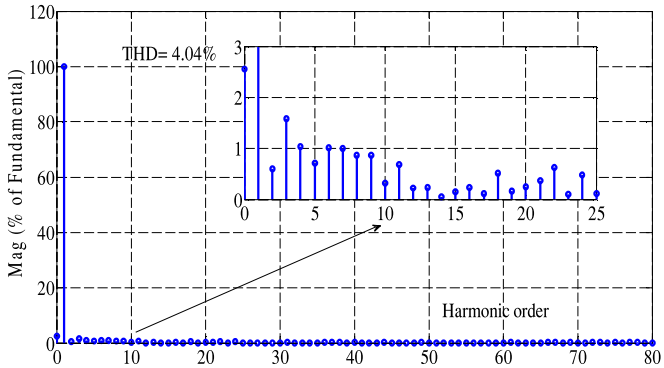

Fig. 21. Line current harmonic spectrum for $\mathrm{MI} = 1$.

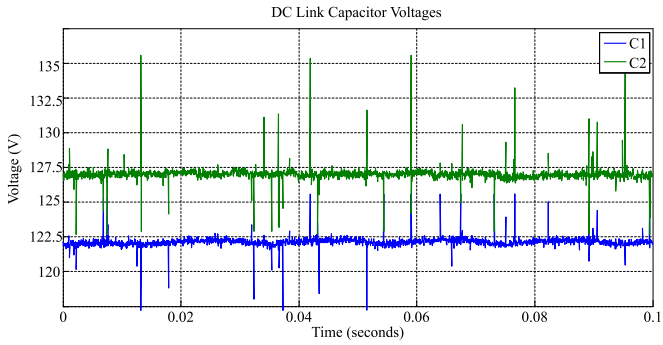

Fig. 22. DC-link voltage for $\mathrm{MI} = 1$.

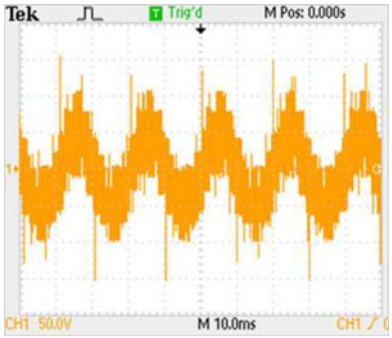

Fig. 23. Phase voltage of prototype result for MI = 0.4 (CH1:5 ms/div, 50v/div).

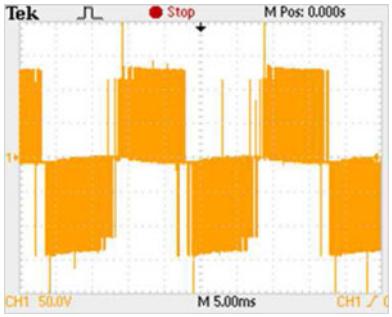

Fig. 24. Line voltage of prototype result for $\mathrm{MI} = 0.4$ CH1:5 ms/div, 50 V/div.

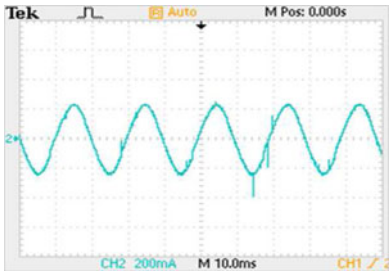

Fig. 25. Line current of prototype result for $\mathrm{MI} = 0.4$ (CH1:5 ms/div, 250 mA/div).

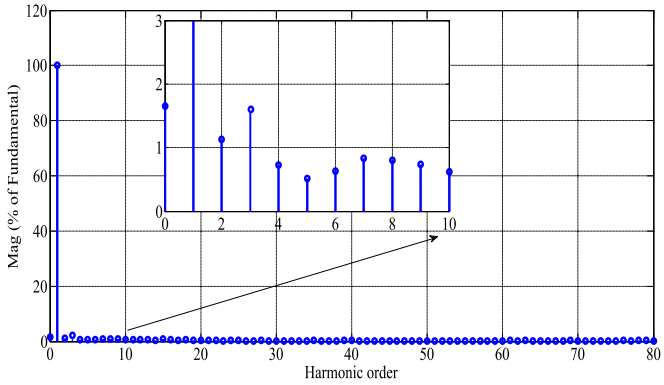

Fig. 26. Harmonics spectrum of the line current for $\mathrm{MI} = 0.4$.

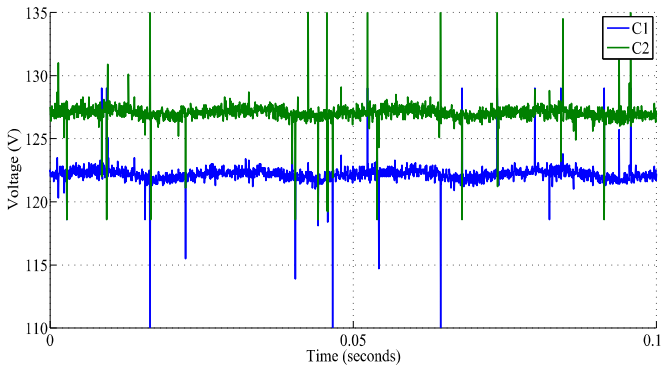

Fig. 27. DC-link voltage for $\mathrm{MI} = 0.4$.

TABLE IV
DC-LINK CAPACITOR VOLTAGE VARIATION FOR DIFFERENT MODULATION INDEX

DC MI	DC bus (V)	C_1 (V)	C_2 (V)	Difference
1	249.6	122.4	127.2	4.8
0.8	250.2	122.8	127.7	4.9
0.6	249.3	122.1	127.2	5.1
0.4	250.1	122.5	127.6	5.1

and the line voltage has 5 voltage levels when $\mathrm{MI} = 1$, which signifies that the validation of number of levels in phase and line voltages are in line with theoretical analysis. The harmonic spectrum validates that the current is free from low-order harmonics, and dc-link capacitor variation shows the effective balancing neural point voltage. Also, the hardware results obtained from prototype are near to the simulation. Fig. 23–Fig. 27 show the performance at lower modulation index of 0.4. At lower modulation index, the number of voltage levels in phase voltage and line voltage is reduced since the larger magnitude vectors are not available in the lower modulation range. The FFT analysis of the current waveform reveals that at lower modulation index also the current waveform is free from low-order harmonics.

The variation in dc-link capacitors voltage is around 5 V for a dc-bus voltage $(V_{\mathrm{dc}}) = 250$ V throughout the linear modulation range. The variation in the capacitor voltage is given in Table IV for different modulation index which shows that there is no significant variation in the neutral point voltage. Thus, the proposed algorithm does not require any additional techniques to balance the dc-link capacitor voltages. The reason for increased current THD in hardware performance are due to the nonlinearities like dead band that is around 650 ns, which is not considered in simulation but practically dead band has to be provided to avoid shoot through condition of dc link.

VI. CONCLUSION

In this paper, a simplified SVPWM is proposed for the three-level five-phase inverter. The proposed method does not require the fuzzy process like sector identification, region identification in particular sector based on the modulation index, and an optimum switching sequence to obtain the dwell time. Rather, it

uses the two-level switching time and carrier index to obtain the dwell time of optimum five vector switching strategy. As a result, the complexity in selecting optimum vectors for three-level five-phase is greatly reduced. The proposed method applies the optimum switching sequence based on two-level switching state and carrier index.

Also, the proposed simplified method utilizes the redundant voltage vectors to balance the dc-link capacitor voltage by applying the redundant vectors time for equal time. The variation in dc midpoint voltages of the capacitor is found to be around 2% experimentally. The carrier index has only to be changed for extension of this algorithm to a multilevel inverter having odd number of phases more than three. The simulation and experimental results validate the performance of the proposed simplified method.

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