Phase-Shift-Controlled Isolated Buck-Boost Converter With Active-Clamped Three-Level Rectifier (AC-TLR) Featuring Soft-Switching Within Wide Operation Range

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***Abstract*—An active-clamped three-level rectifier (AC-TLR) is derived from the diode-clamped three-level inverter, by replacing the active switches and the diodes in the three-level inverter with the diodes and active switches, respectively. Novel isolated buck-boost converters, featuring single-stage conversion and soft-switching within wide operation range, are developed based on the proposed AC-TLR. By utilizing the AC-TLR, the voltage stress on the power devices and passive components, including the rectifying diodes, the active-clamping switches, the flying capacitor, and output filter capacitors, is reduced to the half of the output voltage. Low-voltage rating switching devices with better switching and conduction performances and a transformer with reduced turns ratio and parasitic parameters are used to enhance the efficiency. The full-bridge isolated buck-boost converter with the proposed AC-TLR is analyzed in detail as an example. An optimized phase-shift control strategy is employed to realize isolated buck and boost conversion. Soft switching of all of the switching devices in both the primary- and secondary-side circuits is achieved within the whole operation range by using the proposed AC-TLR and the phase-shift control strategy. Experimental results on a prototype with 380-V output verify the effectiveness of the proposed AC-TLR and its derived isolated buck-boost converters.**

***Index Terms*—DC–DC converter, isolated buck-boost (IBB) converter, phase-shift control, soft-switching, three-level rectifier.**

I. Introduction

ISOLATED dc–dc converters have been widely used for the applications in which the input voltage is much lower or much higher than the output voltage, or in which galvanic isolation is required, for example, the battery-sourced front-end converters for uninterruptible power supplies and stand-alone renewable power systems [1], battery chargers for electric vehicles [2], [3], and the maximum power point tracking converter for renewable power generation systems [4]. The isolated converters can be classified into three categories: buck converters [3], boost converters [4], and buck-boost converters [5], [6]. Generally, the conversion efficiency of buck converters decreases as the voltage conversion ratio decreases, and the efficiency of boost converters is found to decrease as the voltage conversion ratio increases. It is very important to achieve high-efficiency power conversion within a wide voltage range, especially for the power systems fed by renewable energy and batteries [7], [8]. An isolated buck-boost (IBB) converter can operate either as a buck converter or as a boost converter; it is more flexible in terms of conversion efficiency and voltage range.

For the isolated step-down and step-up applications, many isolated buck and boost topologies have been proposed. However, few works on IBB dc–dc converter topologies have been reported in the literature. Most of the IBB converters root in the nonisolated converters. For example, the flyback converter is the isolated version of nonisolated buck/boost converter [9]. Likewise, isolated Cuk [10], Sepic [11], and Zeta [12] converters can be derived by inserting a transformer into the original nonisolated Cuk, Sepic, and Zeta converters, respectively. However, the efficiencies of these single-switch IBB converters are still low because of the high voltage/current stress on the components and the hard-switching of active switches and rectifying diodes. In addition to the low conversion efficiency and high stress, these single-switch IBB converters can only be used for low-power applications. A family of IBB converters is proposed in [5] based on the nonisolated two-switch buck-boost converter [13], [14]. These IBB converters are built with cascading connection of isolated buck converters and nonisolated boost converters. They have the advantages of isolated buck and boost conversion, wide voltage gain range, and flexible control. However, the power has to be processed through the cascaded two-stage architecture, which lowers the conversion efficiency. On the other hand, the voltage stress of the devices on the secondary side is much higher than the output voltage. The efficiency is further reduced due to the hard-switching operation of the rectifying diodes and active switches. The semi-dual-active-bridge (SDAB) converters presented in [15]–[18], which are the simplified versions of dual-active-bridge (DAB) converters [19]–[21], can be good options for IBB power conversion. In comparison with the DAB converter, topology and control of the SDAB converters are simpler and soft-switching operation range is extended. However, some drawbacks for these

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SDAB converters are presented in [15]–[18]: 1) Soft-switching performance will be lost for the active switches and diodes in the semi-active-bridge if the normalized voltage gain is less than 1.0 and the converters work in the continuous conduction mode (CCM) II; 2) the voltage stress on the MOSFETs in the semi-active-bridge is up to the output voltage, which makes them unsuitable for high output voltage applications; and (3) the current flows through the body diodes of the MOSFETs in the semi-active-bridge, which leads to severe reverse-recovery problem when the MOSFETs are hard-switching due to the poor characteristics of body diodes. This problem becomes worse as the output voltage increases. It should be noticed that the output voltages of all SDAB converters in [15]–[18] are lower than 300 V.

For high output voltage applications, the reduction of the voltage stress on rectifying devices, especially on the active switching devices such as MOSFETs, is very important for efficiency improvement, because both the conduction losses and switching losses increase significantly as the voltage-rating increases. Low-voltage stress on the rectifying devices can be achieved by employing a capacitive output filter, because the voltage of the rectifying devices can be clamped directly by the filter capacitor. There are many kinds of rectification circuits with capacitive filters, such as the center-tapped rectifier, the full-bridge rectifier, and the voltage-doubler rectifier [22], [23]. The voltage-doubler rectifier is suitable for high-voltage applications, because its output voltage is twice that of the transformer secondary winding, and hence, the turns ratio of the transformer can be reduced. However, the voltage stress of the rectifying diodes in the voltage-doubler rectifier is still as high as the output voltage. There is a straightforward relation between an inverter circuit and a rectification circuit, which means a rectification circuit can be derived directly by replacing the active switches in the corresponding inverter circuit with diodes, and vice versa. It would be possible to derive novel rectification circuits for high output voltage applications by referring to the inverter circuits which are suitable for high-input-voltage applications, such as the multilevel inverter circuits [24], [25].

The major contribution of this paper is to propose a novel active-clamped three-level rectifier (AC-TLR) based on the diode-clamped three-level inverter topology. Novel IBB converters are harvested based on the proposed AC-TLR as well. Single-stage power conversion, low-voltage stress, and soft-switching operation over the whole operation range can be achieved in the proposed converters by adopting the optimized phase-shift control strategy. This paper is organized as follows. In Section II, the AC-TLR and its derived IBB converters are presented. In Section III, the operational principles of a full-bridge IBB (FB-IBB) converter are analyzed in detail. The performance of this converter is analyzed in Section IV, and experimental results are presented in Section V. Finally, Section VI concludes the paper.

II. Derivation of the AC-TLR and IBB Converters

A. Derivation of the AC-TLR

There is a straightforward relationship between an inverter circuit and a rectification circuit. A rectification circuit can be derived by replacing the active switches in an inverter circuit with diodes, and vice versa. Two examples are shown in Fig. 1. It can be seen that the rectification circuit corresponding to the full-bridge inverter is the full-bridge rectifier, as shown in Fig. 1(a), and the corresponding rectification circuit of the half-bridge inverter is the voltage-doubler rectifier as given in Fig. 1(b).

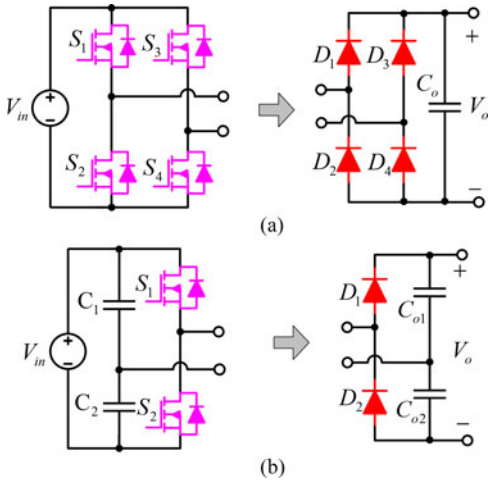

Fig. 1. (a) Full-bridge inverter and full-bridge rectifier. (b) Half-bridge inverter and voltage-doubler rectifier.

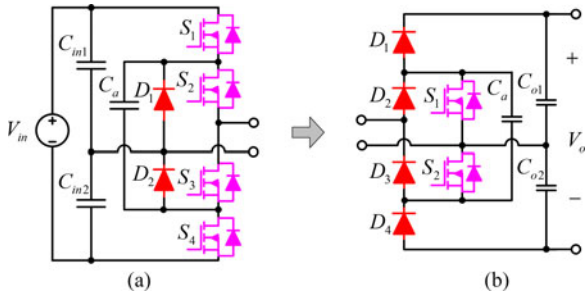

Fig. 2. Derivation of the AC-TLR from the diode-clamped three-level inverter. (a) Three-level inverter. (b) Three-level rectifier.

The above suggests that the other types of rectification circuits for high output voltage applications could be derived from the corresponding inverter circuit suitable for high-input-voltage applications. For example, the diode-clamped three-level inverter circuit shown in Fig. 2(a) is one of the major multilevel topologies known to be suitable for the high-voltage and high-power applications [24]. Another attractive feature of this circuit is that the voltages of the dividing capacitor $C_{\rm in1}$ and $C_{\rm in2}$ can be balanced automatically by using a small flying capacitor C_a in parallel with the clamping diodes [24]. Based on the rectification circuit derivation principle mentioned above, a novel AC-TLR can be derived by replacing the active switches and diodes in the diode-clamped three-level inverter circuit with diodes and active switches, respectively, as illustrated in Fig. 2(b). The voltage stress of all rectification diodes and clamping switches in the AC-TLR is only half of the output voltage, which is beneficial for high output voltage applications. Meanwhile, the voltage

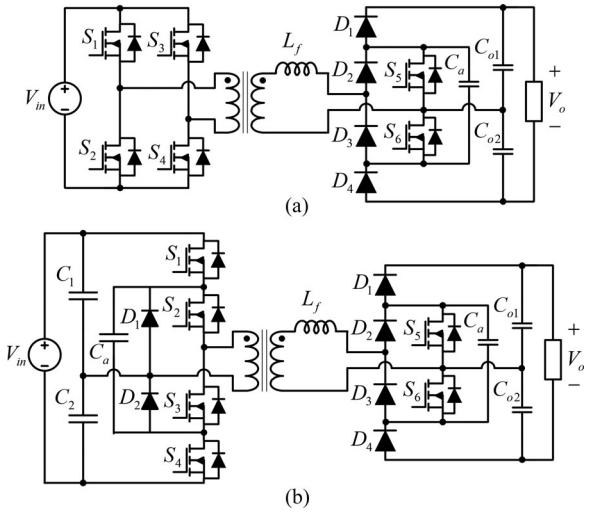

Fig. 3. AC-TLR-based isolated converters with (a) full-bridge input stage and (b) three-level input stage.

balance of the output dividing capacitors, C_{o1} and C_{o2}, can be realized due to the built-in flying capacitor C_a in the AC-TLR.

B. AC-TLR-Based IBB Converters

Novel isolated converters can be constructed based on the proposed AC-TLR. For the primary side of the derived AC-TLR-based isolated converters, the voltage-fed push–pull, half-bridge, full-bridge, three-level input stages, and other advanced input stages can be used. Since the AC-TLR has a capacitive output filter, a high-frequency current source should be used as the input of the AC-TLR. In practice, the high-frequency current source can be realized by a high-frequency voltage source in series with an inductor. In order to construct an isolated converter, the AC-TLR and the input stage should be linked by a high-frequency inductor and a high-frequency transformer. Two examples of the constructed topologies are shown in Fig. 3. The converter of Fig. 3(b) can be a preferred topology for high-input-voltage applications due to its three-level input stage.

From another point of view, the output stage of the derived converters in Fig. 3 is composed of an inductor and the AC-TLR, which looks like a three-level boost converter. The primary-side circuit of the converter is a voltage-fed buck-type input stage, which shows that the proposed converters are inherently IBB converters. These IBB converters have several attractive features such as low-voltage stress and single-stage power conversion. More importantly, the high-frequency inductor L_f in the IBB converters can be partly or fully implemented by using the leakage inductance of the transformer, which results in effective utilization of parasitic parameters and high power density. From topological point of view, the proposed converter can be seen as a SDAB converter because the AC-TLR is composed of an active bridge and a diode bridge. However, the analysis given in the following sections indicates that the disadvantages of the SDAB converters in [15]–[18] are overcome and soft switching over the whole operation range can be achieved by adopting an optimized phase-shift control strategy.

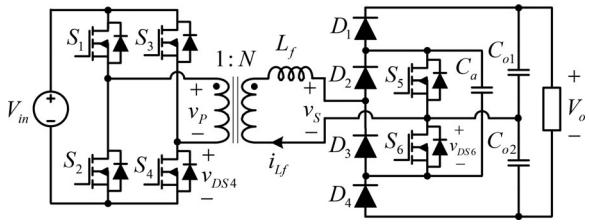

Fig. 4. Topology of the proposed FB-IBB converter.

III. Operational Principles of the Proposed FB-IBB Converter

The main focus of this paper is the AC-TLR. The input stage can be selected according to different applications. The AC-TLR-based FB-IBB converter shown in Fig. 3(a) is taken as an example for analysis. The topology of the FB-IBB converter is illustrated in Fig. 4, and *N* is the secondary-to-primary turns ratio of the transformer. The square-wave voltage produced by the primary-side full-bridge inverter is indicated as v_P in Fig. 4, while the square voltage waveform produced by the AC-TLR is indicated as v_S.

For simplicity, the normalized voltage gain *G* is defined as follows:

$$G = \frac{V_o}{2NV_{\rm in}}. \tag{1}$$

The converter operates in the boost mode when $G \geq 1$ and operates in the buck mode when $G < 1$. All of the six active switches, $S_1 - S_6$, on the primary and secondary sides have a constant duty cycle of 0.5. The switch pairs S_1 and S_2, S_3 and S_4, and S_5 and S_6 are driven complementary, respectively. The primary-side phase-shift angle φ_P is defined to be the phase difference between the gating signals of S_1 and S_3, and the secondary-side phase-shift angle φ_S is defined to be the phase difference between the gating signals of S_4 and S_6. Because the primary- and secondary-side phase-shift angles serve the same function as the duty cycles of the buck and boost converters, respectively, the equivalent primary- and secondary-side duty cycles are defined to simplify the analysis

$$\begin{cases} D_P = \dfrac{\varphi_P}{\pi} \\ D_S = \dfrac{\varphi_S}{\pi}. \end{cases} \tag{2}$$

To achieve soft switching and improve the conversion efficiency, an optimized phase-shift control strategy is developed for the FB-IBB converter. To simplify the analysis, the parasitic capacitance of MOSFET is ignored and the transformer is assumed to be ideal.

A. Boost Mode Operating

In the boost mode, the primary-side duty cycle D_P should be maximized with $D_P = 1$, and the secondary-side duty cycle D_S is used to regulate the output voltage and power, which is similar to the nonisolated two-switch buck-boost converter [13], [14]. According to the waveforms of the inductor current i_{Lf},

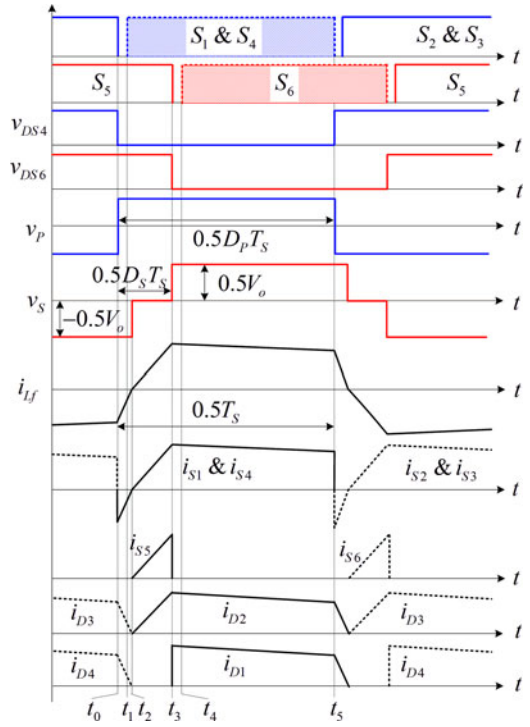

Fig. 5. Switching waveforms of the FB-IBB converter in the Boost-CCM mode.

there are two possible operating modes: CCM and discontinuous conduction mode (DCM).

1) Boost-CCM Mode: Fig. 5 shows the waveforms of the FB-IBB converter in the boost-CCM mode, where T_s is the switching period. From the waveform of v_S in Fig. 5, it is obviously that three voltage levels, positive level, zero level, and negative level, have been produced by the AC-TLR. There are ten switching stages in one switching period. Due to the symmetry of the circuit, only five stages are analyzed here and corresponding equivalent circuits for each stage are shown in Fig. 6.

Stage 1 [t_0, t_1] [see Fig. 6(a)]: Before t_0, the switches S_2, S_3, and S_5, and diodes D_3 and D_4 are ON. The inductor current i_{Lf} is negative $i_{Lf} < 0$. The input source V_{in} and the energy stored in the inductor L_f are delivered to the output capacitor C_{o2}. Capacitor C_{o2} is charged, whereas C_{o1} is discharged. At t_0, S_2 and S_3 are turned OFF. The body diodes of the switches S_1 and S_4 begin to conduct due to the energy stored in L_f. In this stage, the inductor current i_{Lf} can be calculated as follows:

$$i_{Lf}(t) = \frac{NV_{\text{in}} + \frac{V_o}{2}}{L_f}(t - t_0) + i_{Lf}(t_0). \tag{3}$$

Stage 2 [t_1, t_2] [see Fig. 6(b)]: At t_1, the switches S_1 and S_4 are turned ON with zero-voltage switching (ZVS). This stage ends when i_{Lf} returns to zero. Because the current slope is limited by the inductor L_f, the diodes D_3 and D_4 are OFF naturally with zero current and without reverse-recovery loss.

Stage 3 [t_2, t_3] [see Fig. 6(c)]: At t_2, i_{Lf} returns to zero. Because both the S_1 and S_4 are ON, the primary-side circuit produces a positive voltage v_P and applies on the transformer

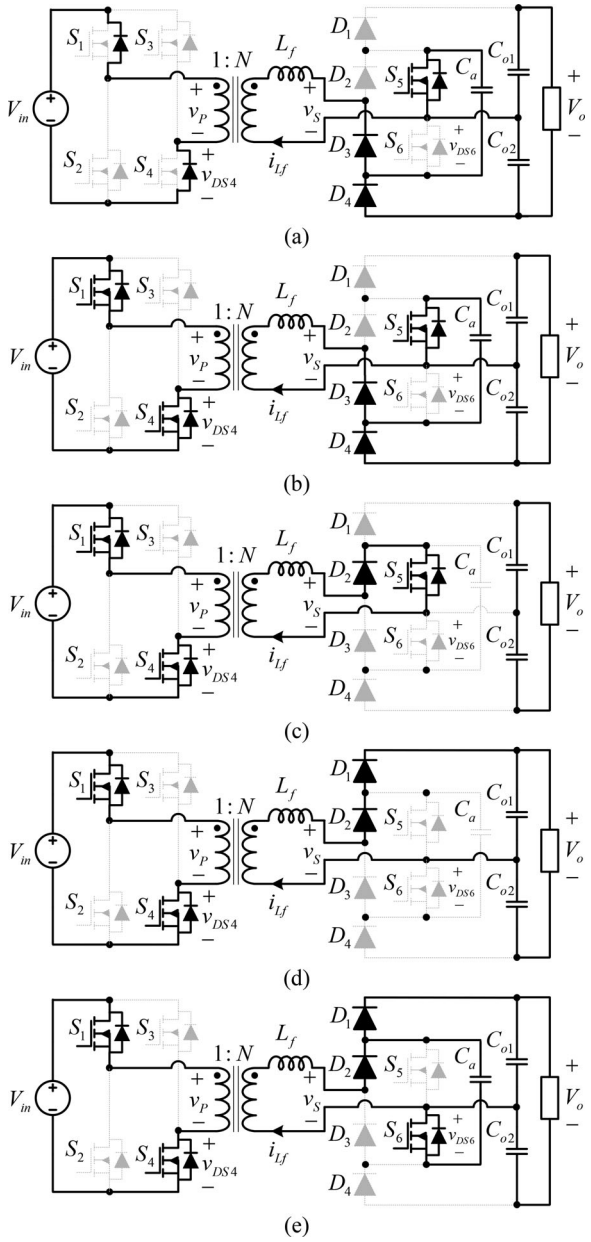

Fig. 6. Equivalent circuits for each switching stage in the Boost-CCM mode: (a) Stage 1 [t_0, t_1]. (b) Stage 2 [t_1, t_2]. (c) Stage 3 [t_2, t_3]. (d) Stage 4 [t_3, t_4]. (e) Stage 5 [t_4, t_5].

winding. The diode D_2 begins to conduct due to the on-state of the switch S_5, which results in a zero-voltage level v_S. So the inductor L_f is charged by the input voltage, which is similar to the operation of a conventional boost converter. During this stage, the inductor current i_{Lf} is given as follows:

$$i_{Lf}(t) = \frac{NV_{\text{in}}}{L_f}(t - t_2). \tag{4}$$

Stage 4 [t_3, t_4] [see Fig. 6(d)]: At t_3, the switch S_5 turns OFF. Since the current i_{Lf} is positive, the diode D_1 begins to conduct. Hence, the input source and the energy stored in the inductor L_f are delivered to the load. In this stage, the capacitor C_{o1} is charged, while C_{o2} is discharged. The inductor current

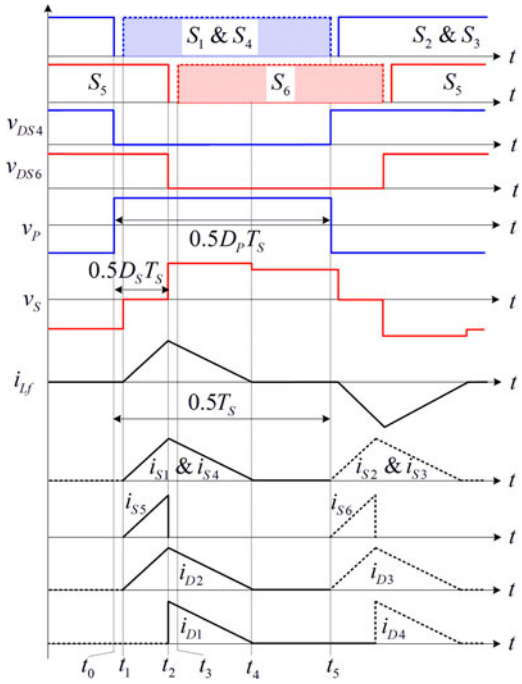

Fig. 7. Switching waveforms of the FB-IBB converter in the Boost-DCM mode.

i_{Lf} is calculated as follows:

$$i_{Lf}(t) = \frac{NV_{\text{in}} - \frac{V_o}{2}}{L_f}(t - t_3) + i_{Lf}(t_3). \tag{5}$$

It should be noted that, once D_1 and D_2 are ON, the drain–source voltage of the switch S_6 is clamped to zero, because the voltage of the flying capacitor is equal to the voltage of output dividing capacitor C_{o1}.

Stage 5 [t_4, t_5] [see Fig. 6(e)]: At t_4, the switch S_6 turns ON with zero voltage and zero current.

Similar operation is conducted in the remaining stages of the switching period. It can be seen that ZVS can be achieved for all the active switches, while zero-current switching (ZCS) can be achieved for all the rectifying diodes in the boost-CCM mode.

2) Boost-DCM Mode: If the inductor current i_{Lf} has decreased to zero before the primary-side switches commutate, the converter enters the boost-DCM mode. Fig. 7 shows the waveforms of the FB-IBB converter in the boost-DCM mode. There are five switching stages in half of the switching cycles as well.

Stage 1 [t_0, t_1] [see Fig. 8(a)]: Before t_0, i_{Lf} decreases to zero. So, even though the switches S_2, S_3, and S_5 are ON, there is no power transferred between the primary and secondary sides. At t_0, S_2 and S_3 are turned OFF.

Stage 2 [t_1, t_2], Stage 3 [t_2, t_3], and Stage 4 [t_3, t_4]: At t_2, S_1 and S_2 are turned ON with ZCS. The operating principle of this state is the same as that of State 3 in the boost-CCM mode, whereas the operating principles of Stages 3 and 4 of the boost-DCM mode are the same as that of the States 4 and 5, respectively, in the boost-CCM mode.

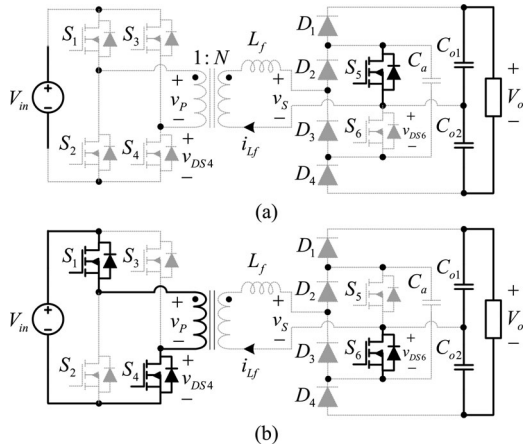

Fig. 8. Equivalent circuits of the Boost-DCM mode: (a) Stage 1 [t_0, t_1]. (b) Stage 5 [t_4, t_5].

Stage 5 [t_4, t_5] [see Fig. 8(b)]: At t_4, i_{Lf} reaches zero and is kept at zero in this stage. Thus, there is no energy transferred between the input and output.

Similar operation is conducted in the rest stages of the switching period. It can be seen that ZCS can be achieved for the primary-side switches and the rectifying diodes, while ZVS can be achieved for the switches in the AC-TLR.

B. Buck Mode Operation

Once the normalized voltage gain is less than one, $G \leq 1$, the converter works in the buck mode. According to the waveform of the inductor current i_{Lf}, the converter can work in either the CCM mode or the DCM mode.

1) Buck-CCM Mode: In the buck-CCM mode, to overcome the disadvantage of hard switching of previous SDAB converters with only secondary-side phase-shift control, an optimized duty cycle equal to the normalized voltage gain G is applied on the primary-side switches to achieve soft switching for all of the switching devices and diodes

$$D_P = \frac{V_o}{2NV_{\text{in}}} = G. \tag{6}$$

The power flow is controlled by regulating the secondary-side duty cycle D_S. Fig. 9 shows the waveforms of the FB-IBB converter in the buck-CCM mode. There are seven switching stages in half of a switching cycle, and corresponding equivalent circuits for each stage are shown in Fig. 10.

Stage 1 [t_0, t_1] [see Fig. 10(a)]: Before t_0, the switches S_2, S_3, S_5 and diodes D_3, D_4 are ON, and the inductor current $i_{Lf} < 0$. The input source and the energy stored in the inductor L_f are delivered to the load. The output capacitor C_{o2} is charged, whereas C_{o1} is discharged. At t_0, the switch S_2 is turned OFF, and hence, the body diode of S_1 begins to conduct due to the energy stored in the L_f. In this stage, the inductor current i_{Lf} can be calculated by

$$i_{Lf}(t) = \frac{V_o}{2L_f}(t - t_0) + i_{Lf}(t_0). \tag{7}$$

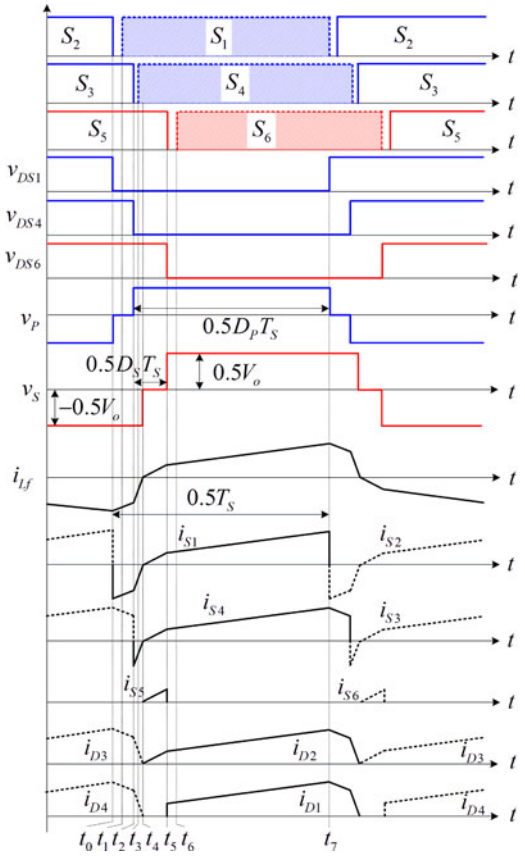

Fig. 9. Switching waveforms of the FB-IBB converter in the Buck-CCM mode.

Stage 2 [t_1, t_2] [see Fig. 10(b)]: At t_1, S_1 is turned ON with ZVS. This stage ends when the switch S_3 is turned OFF at t_2.

Stage 3 [t_2, t_3] [see Fig. 10(c)]: At t_2, S_3 is turned OFF, and then, the body diode of S_4 begins to conduct due to the energy stored in the L_f. In this stage, the inductor current i_{Lf} can be calculated by

$$i_{Lf}(t) = \frac{NV_{\text{in}} + \frac{V_o}{2}}{L_f}(t - t_2) + i_{Lf}(t_2). \tag{8}$$

Stage 4 [t_3, t_4] [see Fig. 10(d)]: At t_3, the switch S_4 is turned ON with ZVS. This stage ends when i_{Lf} returns to zero, and the diodes D_3 and D_4 are OFF naturally with zero current and without reverse-recovery loss.

Stage 5 [t_4, t_5] [see Fig. 10(e)]: At t_4, i_{Lf} returns to zero. The diode D_2 is ON, which results in a zero-voltage level of v_S. Therefore, the inductor L_f is charged by the input source, and the current i_{Lf} can be calculated as

$$i_{Lf}(t) = \frac{NV_{\text{in}}}{L_f}(t - t_4). \tag{9}$$

Stage 6 [t_5, t_6] [see Fig. 10(f)]: At t_5, the switch S_5 turns OFF. Since the current i_{Lf} is positive, the diode D_1 begins to conduct. Hence, the input source and the energy stored in the inductor L_f are delivered to the load. In this stage, the capacitor C_{o1} is charged, while C_{o2} is discharged. The inductor current

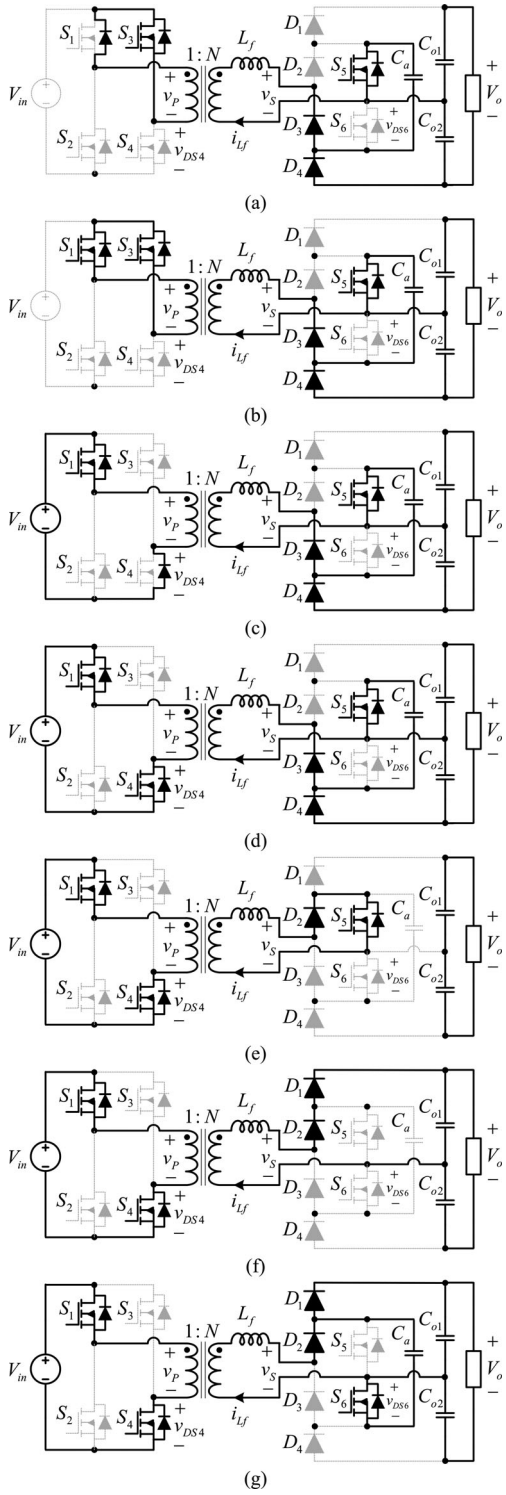

Fig. 10. Equivalent circuits of each stage in the Buck-CCM mode: (a) Stage 1 [t_0, t_1]. (b) Stage 2 [t_1, t_2]. (c) Stage 3 [t_2, t_3]. (d) Stage 4 [t_3, t_4]. (e) Stage 5 [t_4, t_5]. (f) Stage 6 [t_5, t_6]. (g) Stage 7 [t_6, t_7].

i_{Lf} is calculated as

$$i_{Lf}(t) = \frac{NV_{\text{in}} - \frac{V_o}{2}}{L_f}(t - t_5) + i_{Lf}(t_5). \tag{10}$$

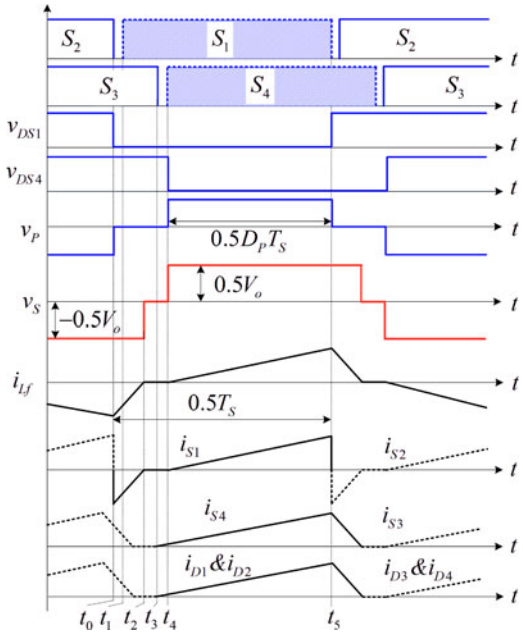

Fig. 11. Switching waveforms of the FB-IBB converter in the Buck-DCM mode.

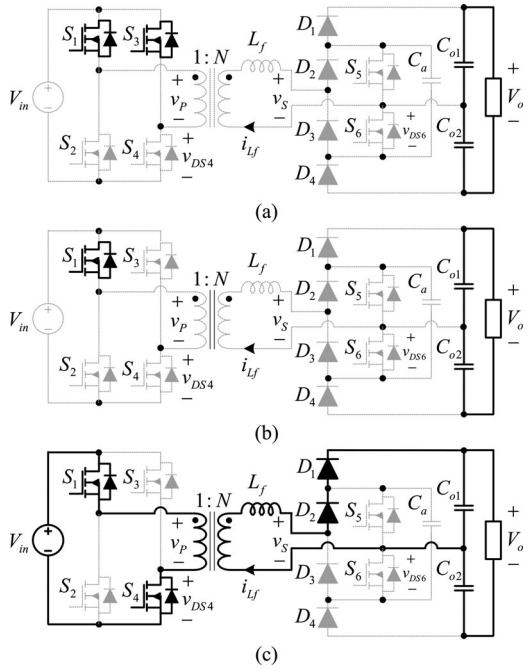

Fig. 12. Equivalent circuits of each stage in the Buck-DCM mode: (a) Stage 3 $[t_2, t_3]$. (b) Stage 4 $[t_3, t_4]$. (c) Stage 5 $[t_4, t_5]$.

Since the voltage of the flying capacitor C_a is equal to the voltage of the C_{o1}, the drain–source voltage of the switch S_6 is clamped to zero.

Stage 7 $[t_6, t_7]$ [see Fig. 10(g)*]*: At t_6, the switch S_6 turns ON with zero voltage and zero current. The power is transferred to the load from the source continuously in this stage. Similar operation is conducted in the rest stages of the switching period.

2) Buck-DCM Mode: If the equivalent secondary duty cycle, D_S, decreases to zero, the converter operates at the boundary between buck-CCM mode and buck-DCM mode. In this scenario, if the output power or the normalized voltage gain decreases further, the converter will enter the buck-DCM mode. In the buck-DCM mode, the switches S_5 and S_6 in the AC-TLR can be kept in the off-state because the secondary duty cycle D_S is zero. On the other hand, the switches S_5 and S_6 can also be turned ON/OFF synchronously with the switches S_3 and S_4, respectively, to keep the secondary duty cycle D_S at zero. During the buck-DCM operation, the output power/voltage is regulated by the primary-side duty cycle D_P.

Fig. 11 shows the waveforms of the FB-IBB converter in the buck-DCM mode. Suppose that the switches S_5 and S_6 are always in the off-state. There are five switching stages in half of the switching cycle, and the corresponding equivalent circuits are shown in Fig. 12.

Stage 1 $[t_0, t_1]$ and Stage 2 $[t_1, t_2]$: The operating principles of the Stages 1 and 2 in the buck-DCM mode are similar as that of Stages 1 and 2, respectively, in the buck-CCM mode. In these two stages, the switch S_1 is turned ON with ZVS at t_1, the energy stored in the inductor L_f is transferred to the load, and finally, the inductor current i_{Lf} decreases to zero at t_2.

Stage 3 $[t_2, t_3]$ [see Fig. 12(a)]: At t_2, i_{Lf} decreases to zero, and the diodes D_3 and D_4 are OFF with ZCS. Since $i_{Lf} = 0$, all the rectifying diodes are kept in the off-state in this stage. There is no power transferred between the input and output.

Stage 4 $[t_3, t_4]$ [see Fig. 12(b)]: At t_3, the switch S_3 is turned OFF with zero current.

Stage 5 $[t_4, t_5]$ [see Fig. 12(c)]: At t_4, the switch S_4 is turned ON with zero current. The diodes D_1 and D_2 begin to conduct due to the positive voltage of v_P. Hence, the input source transfers power to the load, and the inductor current i_{Lf} increases linearly

$$i_{Lf}(t) = \frac{NV_{\text{in}} - \frac{V_o}{2}}{L_f}(t - t_4). \tag{11}$$

This stage ends when the switch S_1 is turned OFF at t_5, and the second half of the switching cycle begins.

IV. Performance Analysis and Discussion

A. Output Power and Voltage Gain Analysis

1) Boost Mode: According to the operational principle of the boost-CCM mode and waveforms shown in Fig. 5, we have $i_{Lf}(t_0) = i_{Lf}(t_5)$, and $i_{Lf}(t_2) = 0$. Then, based on (1)–(5), the values of $i_{Lf}(t_0), i_{Lf}(t_3)$, and ΔT_2 can be derived as

$$\begin{cases} i_{Lf}(t_0) = \dfrac{V_o}{4f_S L_f} \dfrac{(1+G)(G - D_S G - 1)}{G(G+2)} \\ i_{Lf}(t_3) = \dfrac{V_o}{4f_S L_f} \dfrac{2D_S + G - 1}{G(G+2)} \\ \Delta T_2 = t_2 - t_0 = \dfrac{1}{2f_S} \dfrac{1 - G(1 - D_S)}{G+2} \end{cases} \tag{12}$$

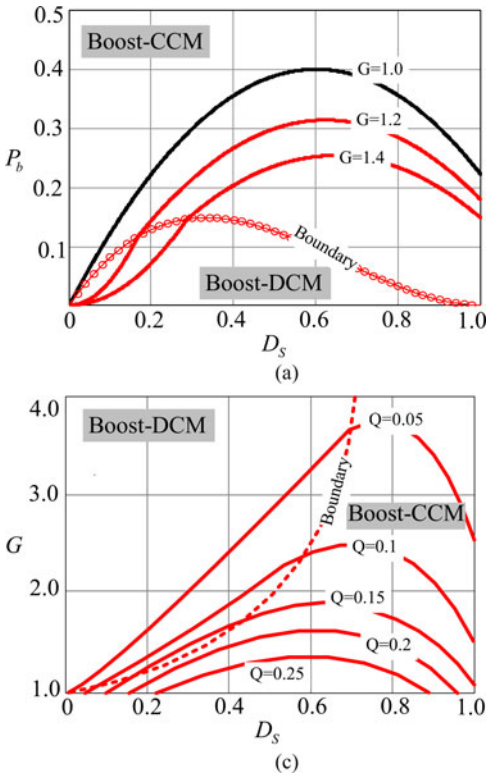

Fig. 13. Output characteristics of the Boost mode. (a) Output power versus D_S. (b) Voltage gain versus D_S.

where f_S is the switching frequency. Then, the average output power P_o can be calculated as

$$P_{o\_\mathrm{Boost-CCM}} = \frac{V_o^2}{16 f_S L_f} \frac{(G+1)(1+4D_S-4D_S^2)-G^2(2-4D_S+2D_S^2)}{G(G+2)^2}. \quad (13)$$

On the other hand, based on (12) and $i_{Lf}(t_0)=0$, the boundary condition of boost-CCM mode can be derived as

$$D_{\mathrm{SB}} = 1 - \frac{1}{G}. \quad (14)$$

which means that the converter operates in the boost-CCM mode if $D_S \geq D_{\mathrm{SB}}$, and in the boost-DCM mode if $D_S < D_{\mathrm{SB}}$.

The same analysis can be performed for the boost-DCM mode. When the converter operates in the boost-DCM mode, the current value i_{Lf} at t_2 can be given as follows:

$$i_{Lf}(t_2) = \frac{V_o}{4 f_S L_f}\frac{D}{G} \quad (15)$$

and the output power is

$$P_{o\_\mathrm{Boost-DCM}} = \frac{V_o^2}{16 f_S L_f}\frac{D_S^2}{G(G-1)}. \quad (16)$$

According to (13) and (16), the curves of the output power, which is normalized by power base $P_b = (V_o^2)/(16 f_S L_f)$, versus the secondary-side equivalent duty cycle D_S are plotted in Fig. 13(a).

On the other hand, the output power can also be expressed as follows:

$$P_o = \frac{V_o^2}{R_o} \quad (17)$$

where R_o is the load resistance of the converter. Substituting (17) into (13) and (16), the normalized voltage gain G versus the equivalent secondary-side duty cycle D_S can be obtained. The curves of the voltage gain G are shown in Fig. 13(b), where Q is the characteristic factor and defined as follows:

$$Q = \frac{16 L_f f_S}{R_o}. \quad (18)$$

2) Buck Mode: According to the operational principles of the converter in the buck-CCM, the waveforms shown in Fig. 9, and (6)–(10), the current values $i_{Lf}(t_0), i_{Lf}(t_2), i_{Lf}(t_5)$, and the time interval ΔT_4 can be derived as follows:

$$\begin{cases} i_{Lf}(t_0) = \dfrac{V_o}{4 f_S L_f}\dfrac{-D_S(G+1)+G^2+G-2}{G+2} \\ i_{Lf}(t_2) = \dfrac{V_o}{4 f_S L_f}\dfrac{-D_S(G+1)}{G+2} \\ i_{Lf}(t_5) = \dfrac{V_o}{4 f_S L_f}\dfrac{2D_S}{G(G+2)} \\ \Delta T_4 = t_4 - t_0 = \dfrac{1}{2 f_S}\dfrac{GD_S+2-G-G^2}{G+2}. \end{cases} \quad (19)$$

Then, the output power can be calculated and given as (20), shown at the bottom of the next page.

On the other hand, according to the waveforms shown in Fig. 9, the condition that allows the converter work in the buck-CCM mode is $i_{Lf}(t_2) < 0$, which yields $D_S > 0$. It means, if the primary-side duty cycle $D_P = G$, the converter will work in the buck-CCM mode if and only if $D_S > 0$.

As illustrated in Fig. 11, the operation of the buck-DCM mode is very simple, and the output power can be given as follows:

$$P_{o\_\mathrm{Buck-DCM}} = \frac{V_o^2}{16 f_S L_f}\frac{D_P^2(1-G)}{G^2}, \quad 0 \leq D_P \leq G. \quad (21)$$

Substituting (17) and (18) into (20) and (21), the normalized voltage gain versus the equivalent duty cycle can be derived. Meanwhile, for a given Q, the voltage gain G_B at the boundary of buck-DCM and buck-CCM modes can be derived as follows:

$$G_B = 1 - Q. \quad (22)$$

The curves of the output power with different voltage gains and the curves of the voltage gain with different characteristic factors are shown in Fig. 14(a) and (b), respectively.

3) Discussion: From the curves of Figs. 13 and 14, it can be seen that the converter works as a buck converter with the voltage gain $0 \leq G \leq 1$, or as a boost converter with the voltage gain $G \geq 1$ by employing the phase-shift control strategy, which proves that the proposed converter is an IBB converter. No matter the converter works in boost mode or buck mode, the CCM operation range increases with a larger characteristics factor Q, which means the CCM operation range is proportional to the value of high-frequency-link inductor L_f and output power.

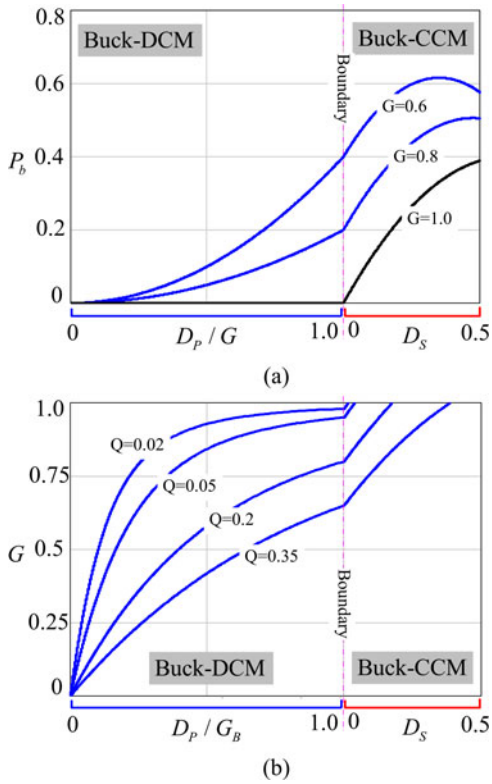

Fig. 14. Output characteristics of the Buck mode. (a) Output power versus D_S. (b) Voltage gain versus D_S.

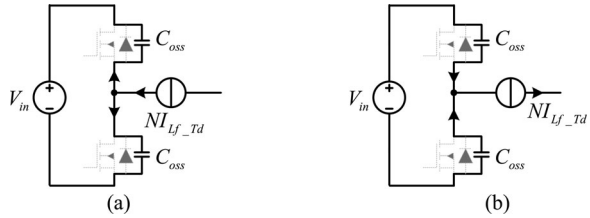

Fig. 15. Equivalent circuit during the dead time: (a) S_1 or S_3 is discharged. (b) S_2 or S_4 is discharged.

TABLE I
ZVS CONDITIONS OF PRIMARY-SIDE SWITCHES

	S_1 & S_2	S_3 & S_4
Boost-CCM	$i_{Lf}(t_0) \le -I_{Lf\_Td\_min}$	
Boost-DCM	N/A	
Buck-CCM	$i_{Lf}(t_0) \le -I_{Lf\_Td\_min}$	$i_{Lf}(t_2) \le -I_{Lf\_Td\_min}$
Buck-DCM	$i_{Lf}(t_5) \ge I_{Lf\_Td\_min}$	N/A

For a given duty cycle and output voltage, the output power decreases as the voltage gain increases. Therefore, the maximum voltage gain and the maximum output power must be taken into account for the parameter design, i.e., the value of the inductor L_f and the switching frequency, of the converter. From the point of view of output ripples, the characteristic of the proposed AC-TLR is very similar to a conventional boost converter. For a given output current, DCM operation will lead to higher current ripples and voltage ripples on the output side due to high peak value of i_{Lf}. Therefore, CCM operation is better for heavy-load output, while DCM operation only occurs in light-load conditions.

B. Soft-Switching Performance

According to the operating principles of different modes, it has been shown that ZCS soft switching of all the rectifying diodes in the AC-TLR is achieved within the whole operation range. For the active switches, S_5 and S_6, in the AC-TLR, the operating principles and waveforms (in Figs. 5, 7, 9, and 11) show that the drain–source voltage of S_6 will decrease to zero if and only if the current i_{Lf} flows through D_1 and D_2, while the drain–source voltage of S_5 will decrease to zero if and only if i_{Lf} flows through D_3 and D_4. It means that ZVS soft switching of S_5 and S_6 can be achieved if and only if the converter supplies power to the load. Therefore, ZVS of the active switches S_5 and S_6 in the AC-TLR is independent of the operating conditions of the converter and the output capacitance of S_5 and S_6, and it can be achieved within the whole operation range.

If the output capacitances of the primary-side MOSFETs are taken into account, the ZVS of the primary-side switches will be affected by the values of output capacitance, dead time, and high-frequency-link inductors when switches are turned ON/OFF. For simplicity, the output capacitances of the primary-side switches are assumed to be linear and equal to $C_{\rm oss}$. If $C_{\rm oss}$ can be discharged to be zero during the dead time, T_d, by the high-frequency-link inductor current i_{Lf}, the ZVS of corresponding MOSFET can be realized. Because the value of high-frequency-link inductor L_f is much higher (more than one thousand times) than $C_{\rm oss}$, i_{Lf} can be seen as constant and L_f can be seen as a current source during the dead time. Assuming the value of i_{Lf} during the dead time is I_{Lf_Td}, the equivalent circuits of the primary-side upper switch, S_1 or S_3, and lower switch, S_2 or S_4, are discharged by L_f during the dead time as shown in Fig. 15.

As shown in Fig. 15, the following condition must be satisfied to discharge $C_{\rm oss}$ to zero during the dead time

$$I_{Lf\_Td} \ge \frac{2V_{\rm in}C_{\rm oss}}{NT_d} = I_{Lf\_Td\_\min}. \tag{23}$$

Basing on Fig. 15 and (23), the ZVS conditions for the primary-side switches in different operation modes are listed in Table I.

$$P_{o\_\rm Buck-CCM} = \frac{V_o^2}{16 f_S L_f} \frac{G^2[D_S(2+2G) - 2D_S^2 - (G^2+1)] - (G+1)[4D_S^2 - 4GD_S + (3G^2 - 4G)]}{G(G+2)^2} \tag{20}$$

TABLE II
ZVS CONDITIONS OF BUCK MODE

	S_1 & S_2	S_3 & S_4
Buck-CCM	$D_S \geq \frac{-2+G+G^2}{G+1} + \frac{(G+2)}{(G+1)} \frac{4 f_S L_f C_{\rm oss}}{N^2 T_d}$	$D_S \geq \frac{(G+2)}{(G+1)} \frac{4 f_S L_f C_{\rm oss}}{N^2 T_d}$
Buck-DCM	$D_P \geq \frac{1}{(1-G)} \frac{4 f_S L_f C_{\rm oss}}{N^2 T_d}$	N/A

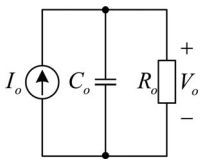

Fig. 16. Low-frequency small-signal model of the proposed converter.

Substituting (12) and (23) into the equations in Table I, the ZVS condition for the boost-CCM mode can be obtained as

$$D_S \geq 1 - \frac{1}{G} + \frac{(G+2)}{(G+1)} \frac{4 f_S L_f C_{\rm oss}}{N^2 T_d}. \tag{24}$$

By following the same analysis procedures, the ZVS conditions of buck-CCM and buck-DCM can be obtained as well and listed in Table II.

From (14), (24), and equations in Table II, it can be seen that ZVS of all of the primary-side switches can always be achieved in the boost-CCM and buck-CCM modes if $C_{\rm oss}$ is zero, and ZVS of S_1 and S_2 can be always achieved as well in the buck-DCM mode if $C_{\rm oss}$ is zero. But the ZVS range will be reduced if $C_{\rm oss}$ is not zero. It should be noted that discussion on ZCS is of no sense for MOSFETs if ZVS is not achieved, because there must be switching loss due to the discharging of $C_{\rm oss}$ when the switch is getting ON.

C. Small-Signal Model

Because the topology and operation principles of the proposed converter are similar to the DAB and SDAB converters, a current-source-based model (as shown in Fig. 16) is developed for the proposed converter for small-signal analysis by modifying the current-source model of the DAB converter, which is presented in [26] and [27]. The detailed modeling process has been presented in [18] and [27]. Since the modeling method is not the focus of this paper and limited by the page number, only the boost-CCM is analyzed here to show the effective of the current-source-based model.

The output current I_o in steady state can be obtained from (1)–(5) for an arbitrary secondary-side duty cycle D_s as

$$I_{o\_\rm Boost-CCM}\left(D_S\right) = \frac{2NV_{\rm in}}{16 f_s L_f} \frac{(G+1)\left(1+4D_S-4D_S^2\right) - G^2\left(2-4D_S+2D_S^2\right)}{(G+2)^2}. \tag{25}$$

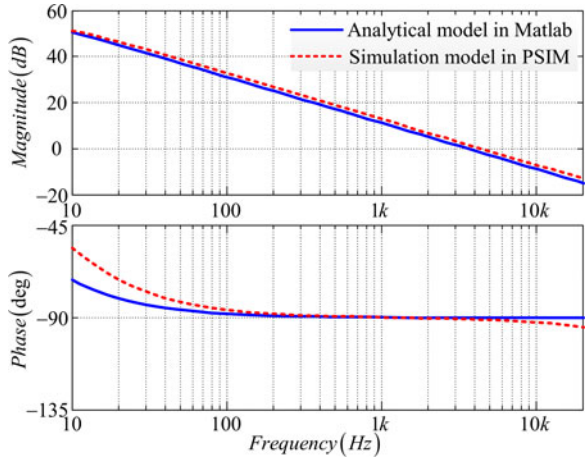

Fig. 17. Bode plots of control-to-output voltage transfer function.

The control-to-output transfer function can be derived by keeping the input voltage $V_{\rm in}$ and applying a small disturbance ΔD_S to the D_S, which causes a small disturbance ΔI_o and produces a disturbance ΔV_o around V_o. Then, the small-signal model for a resistive load shown in Fig. 16 can be obtained as

$$G_{vd\_\rm Boost-CCM}\left(s\right) = \frac{\Delta V_o\left(s\right)}{\Delta D_S\left(s\right)} = \frac{\rm NV_{in}}{2 f_s L_f} \frac{(G+1)\left(1-2D_S\right) + G^2\left(1-D_S\right)}{(G+2)^2} \frac{R_o}{1+sR_oC_o} \tag{26}$$

where Fig. 17 shows the comparison of the analytical result of (26) with the simulation result by using PSIM. The comparison is carried out under the following conditions: $V_{\rm in} = 48$ V, $V_o = 380$ V, $P_o = 500$ W, $f_s = 100$ kHz, $L_f = 41.8$ μH, $C_{o1} = C_{o2} = 330$ μF, $N = 23/6$, and $D_S = 0.228$. It can be seen that the analytical result agrees with the simulation result very well, which verifies the effective of the current-source-based model. Based on this model, the controller has been designed.

D. Design Considerations

The soft-switching performance is achieved by using the phase-shift modulation. To achieve high conversion efficiency, the focus should be on the conduction losses. As analyzed above, the performance of the AC-TLR-based FB-IBB converter is mainly affected by the characteristic factor Q. A 500-W prototype operating at 100 kHz with 40–56 V input voltage and 380-V output voltage for battery discharging is implemented to test the main design considerations of Q.

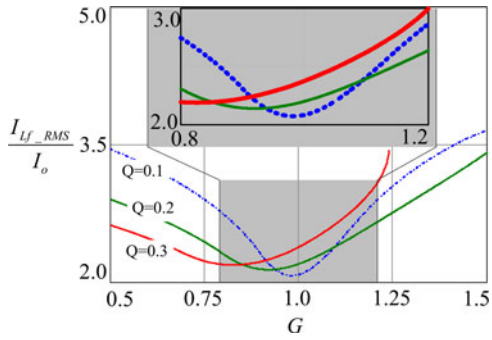

Fig. 18. Normalized inductor RMS currents versus normalized voltage gain under different characteristic factors.

TABLE III
SPECIFICATIONS OF THE PROTOTYPE

Components	Parameters
Input voltage ($V_{\rm in}$)	40–56 V
Output voltage (V_o)	380 V
Rated output power (P_o)	500 W
Switching frequency	100 kHz
Turns ratio of transformer (N)	$N = N_S : N_P = 23 : 6$
Inductor L_f	42 μH
Primary-side MOSFETs ($S_1 \sim S_4$)	IPP037N08N
Secondary-side MOSFETs (S_5, S_6)	IRF4229
Secondary-side diodes ($D_1 - D_4$)	DPG20C300PB
Flying Capacitor (C_a)	6.8 μF
Output Capacitors (C_{o1}, C_{o2})	330 μF

The root-mean-square (RMS) currents of the high-frequency inductor L_f normalized with load current are calculated by using MathCAD to indicate the conduction losses, which are shown in Fig. 18. It can be seen that when G is close to 1.0, a smaller Q value means less conduction losses and is beneficial for efficiency enhancement. However, smaller Q will lead to high conduction loss if G is far away from 1.0. If $G < 1$, a larger Q value results in a higher efficiency. However, if $G > 1, Q = 0.3$ will make the conduction loss get worse in the range of $G > 0.9$. Taking these factors into consideration and to achieve high conversion efficiency within a wide operation range, $Q = 0.2$ is a recommended choice. For the design example with $f_s = 100$ kHz, $P_o = 500$ W, and $V_o = 380$ V, $Q = 0.2$ means the value of L_f is about 40 μH.

Once Q is determined, the turns ratio of transformer can be selected according to the range of G and the maximum efficiency point. In this design, the maximum efficiency point is located at the 52-V input voltage where the minimum conduction loss is achieved with normalized voltage gain $G = 0.95$ and $Q = 0.2$, as shown in Fig. 18. Substituting $G = 0.95$, $V_{\rm in} = 52$, and $V_o = 380$ into (1), the turns ratio N is 3.84.

V. EXPERIMENTAL VERIFICATION AND ANALYSIS

A 500-W prototype of the proposed FB-IBB converter shown in Fig. 4 is built to verify the feasibility and effectiveness of the proposed AC-TLR and its derived IBB converters. The specifications of this prototype are listed in Table III.

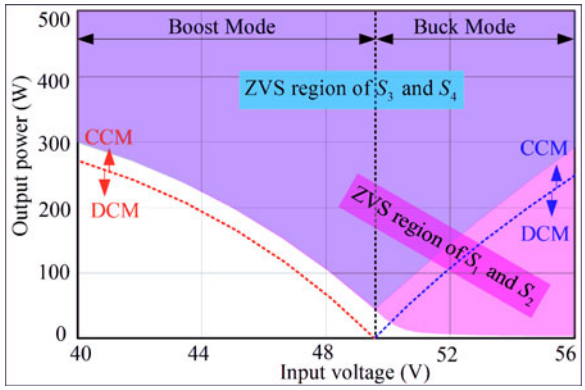

Fig. 19. Operation range and soft-switching range of the prototype.

The operation range and soft-switching range of the primary-side switches are calculated and shown in Fig. 19 based on the parameters listed in Table III. The dead time is set at 100 ns. It can be seen that the operation ranges of boost-DCM and buck-DCM modes increase when the normalized voltage gain far away from 1.0. The ZVS of the S_1 and S_2 is easier to realize than S_3 and S_4. Therefore, the ZVS region of S_1 and S_2 is wider than S_3 and S_4. Meanwhile, it can be seen that CCM operation is better than DCM operation for the soft switching of primary-side switches.

Fig. 20 shows the experimental waveforms of the converter in the boost-CCM mode, which are tested under 40-V input voltage with normalized voltage gain $G > 1$. Three voltage levels can be seen from the voltage waveform of v_S in Fig. 20(a). The current waveform of i_{Lf} in Fig. 20(a) coincides with the theoretical waveform in Fig. 5 pretty well, which verifies the effectiveness of the analysis. Meanwhile, ZVS of the primary-side switches S_1 and S_2 has been achieved as shown in Fig. 20(b). Since all the primary-side switches work in the same pattern symmetrically, ZVS is accomplished for all of them. Moreover, ZVS is also achieved for the secondary-side switches S_5 and S_6 as shown in Fig. 20(c).

The experimental waveforms in the boost-DCM mode with 90-W output power are shown in Fig. 21. Three voltage levels, including the zero-voltage level, can be seen from the waveform of v_S in Fig. 21(a). From Fig. 21(b) and (c), it can be seen that ZVS/ZCS turn OFF is achieved for the primary-side switches, but ZVS turn ON is lost due to the lack of energy to discharge output capacitances of MOSFETs. Meanwhile, ZVS can also be achieved for the secondary-side switches S_5 and S_6, as shown in Fig. 21(d). It should be noted that, when the converter works in the boost-DCM mode and the inductor current i_{Lf} reaches zero, the oscillation of the v_S is caused by the resonance between the inductor L_f and the parasitic capacitances of these switches.

Fig. 22 shows the experimental waveforms in the buck-CCM mode. The primary-side and secondary-side voltages v_P, v_S and the driving voltages of the switches S_1, S_4, and S_5 are shown in Fig. 22(a) and (b). It can be seen that both the primary-side full-bridge inverter and the secondary-side AC-TLR generate three voltage levels due to the dual phase-shift control in the buck-CCM mode. The waveforms coincide with the analysis of Fig. 9 pretty well. Meanwhile, ZVS have been achieved for all

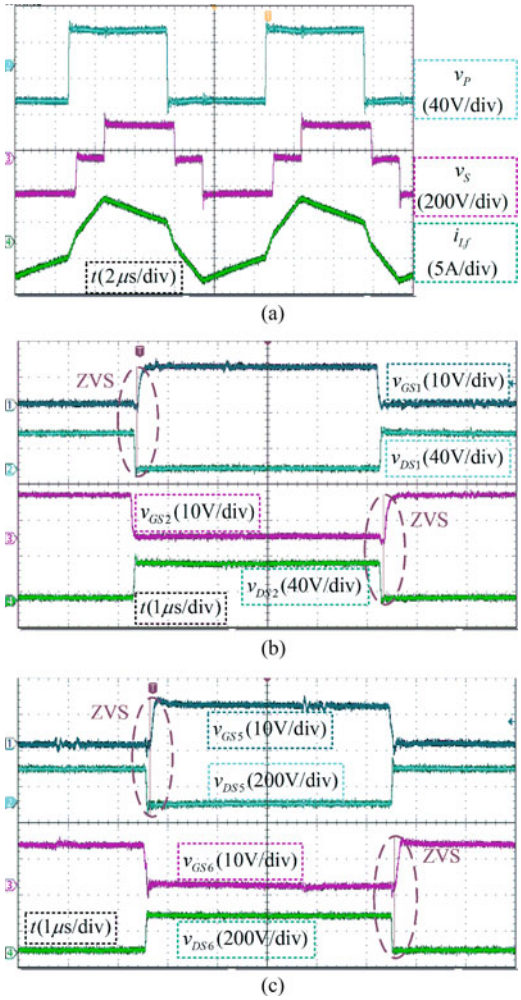

Fig. 20. Experimental waveforms in Boost-CCM mode with $G > 1$. (a) Voltage produced by the primary-side full-bridge inverter (v_P), voltage produced by the AC-TLR (v_S), and current through the inductor (i_{Lf}). (b) Driving voltages (v_{GS1}, v_{GS2}) and drain–source voltages (v_{DS1}, v_{DS2}) of S_1 and S_2. (c) Driving voltages (v_{GS5}, v_{GS6}) and drain–source voltages (v_{DS5}, v_{DS6}) of S_5 and S_6.

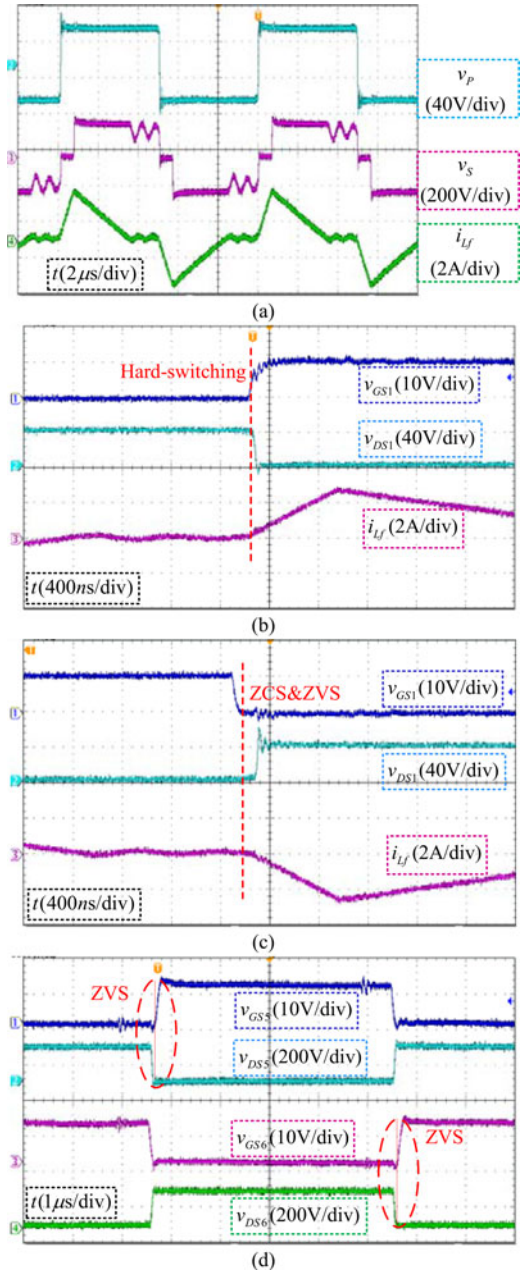

Fig. 21. Experimental waveforms in Boost-DCM mode with $G > 1$. (a) Voltage produced by the primary-side full-bridge inverter (v_P), voltage produced by the AC-TLR (v_S), and current through the inductor (i_{Lf}). (b) and (c) Driving voltage (v_{GS1}), drain–source voltage (v_{DS1}) of S_1 and i_{Lf}. (d) Driving voltages (v_{GS5}, v_{GS6}) and drain–source voltages (v_{DS5}, v_{DS6}) of S_5 and S_6.

the primary-side switches and the secondary-side switches, as shown in Fig. 22(c) and (d).

The experimental waveforms in the buck-DCM mode with 90-W output power are shown in Fig. 23. In this case, the switches in the AC-TLR are kept in the off-state. Hence, only the primary-side full-bridge inverter generates a three-level voltage waveform v_P as shown in Fig. 23(a). When the inductor current i_{Lf} decreases to zero, the inductor L_f resonates with the parasitic capacitance and results in the oscillation of v_S. As shown in Fig. 23(b) and (c), ZVS is achieved for the switch S_1, and ZVS/ZCS turn OFF is achieved for the switch S_4, but ZVS cannot be achieved for S_4.

The efficiency curves versus output power under different input voltages are shown in Fig. 24. When the input voltage is 40 V, the maximum efficiency is 96.6% and the efficiency at full load is 95.6%; when the input voltage is 50 V, the maximum efficiency is 97.3% and the efficiency at full load is 96.7%; when the input voltage is 56 V, the maximum efficiency is 96.8% and efficiency at full load is 96.6%. To evaluate the performance of the proposed topology, the isolated-boost topology presented in [23] is selected as the reference for some quantitative comparisons. In the topology in [23], a full-bridge circuit and four rectifying diodes are used, and the voltage stress of rectifying diodes is half of the output voltage as well. The input and output voltages of experimental prototype in [23] are the same as the proposed converter. The experimental results in [23] indicate

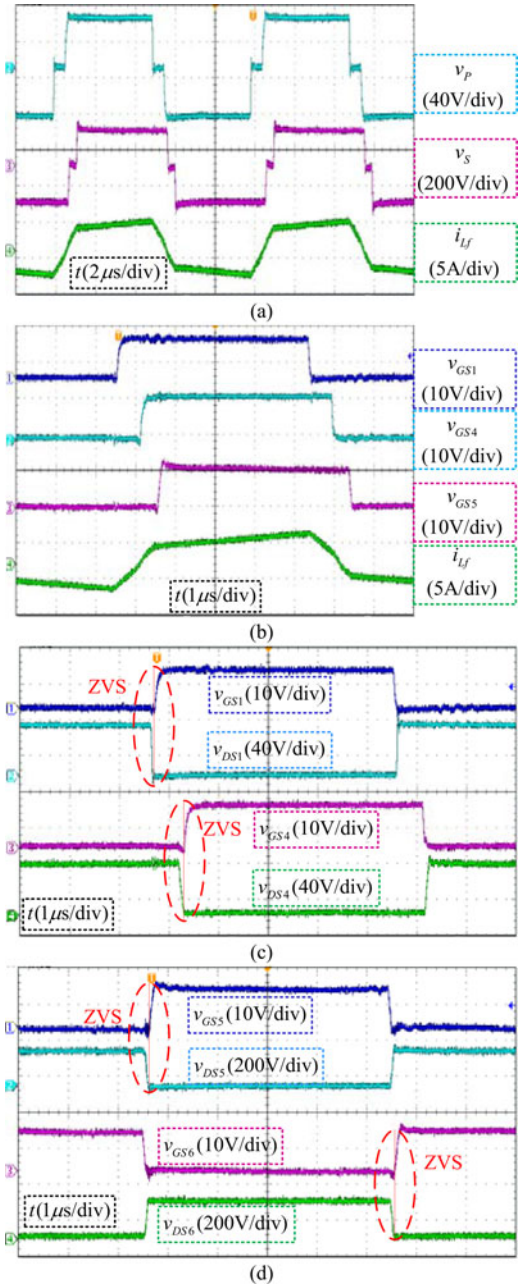

Fig. 22. Experimental waveforms in Buck-CCM mode with $G < 1$. (a) Voltage produced by the primary-side full-bridge inverter (v_P), voltage produced by the AC-TLR (v_S), and current through the inductor (i_{Lf}). (b) Driving voltages of S_1 (v_{GS1}), S_4 (v_{GS4}) and S_5 (v_{GS5}), and i_{Lf}. (c) Driving voltages (v_{GS1}, v_{GS4}) and drain–source voltages (v_{DS1}, v_{DS4}) of S_1 and S_4. (d) Driving voltages (v_{GS5}, v_{GS6}) and drain–source voltages (v_{DS5}, v_{DS6}) of S_5 and S_6.

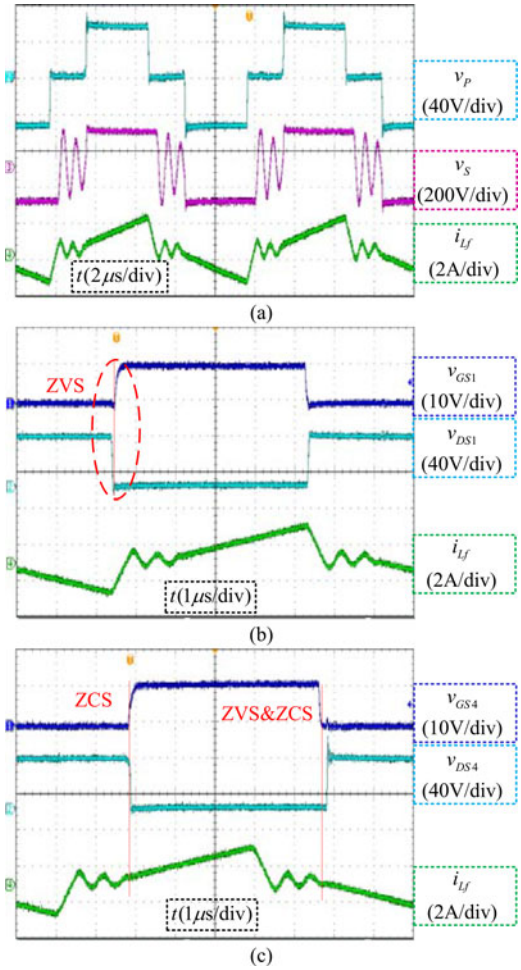

Fig. 23. Experimental waveforms in Buck-DCM mode with $G < 1$. (a) Voltage produced by the primary-side full-bridge inverter (v_P), voltage produced by the AC-TLR (v_S), and current through the inductor (i_{Lf}). (b) Driving voltage (v_{GS1}), drain–source voltage (v_{DS1}) of S_1 and i_{Lf}. (c) Driving voltage (v_{GS4}), drain–source voltage (v_{DS4}) of S_4 and i_{Lf}.

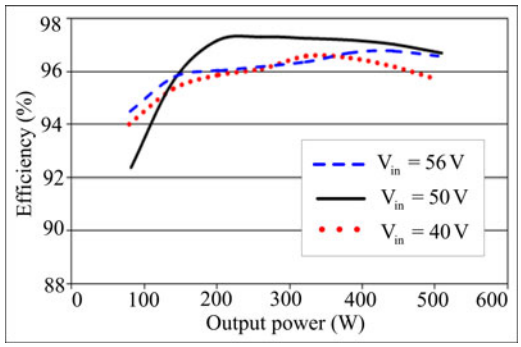

Fig. 24. Efficiency curves of the FB-IBB converter with different input voltages and output load.

that the conversion efficiency of the isolated boost converter decreases as the input voltage decreases. As a result, tradeoffs among the efficiencies under maximum, normal, and minimum input voltages are very difficult to make. The highest efficiency of the isolated boost converter occurs when the input voltage is 56 V. When the input voltage is 56 V, the maximum efficiency of the isolated-boost converter is only 96.3% and the efficiency at full-load is only 95.6%, which are lower than the proposed topology. It is because the voltage stress on the primary-side switches in the isolated-boost converter is much higher than the input voltage. 200-V rated MOSFETs have to be used for a 40–56-V input voltage application. In comparison, 80-V rated MOSFETs can be employed in the proposed converter.

VI. Conclusion

An AC-TLR, which roots in the diode-clamped three-level inverter, is proposed to fulfill the requirements of high output voltage and IBB conversion. The voltage stress on the components in the AC-TLR is reduced to half of the output voltage, which enhances the voltage transfer ratio. Meanwhile, low-voltage rated devices with lower conduction and switching losses are used to improve efficiency. IBB converters based on the proposed AC-TLR are developed. An FB-IBB converter is taken as an example for the detailed analysis of the proposed AC-TLR. An optimized phase-shift control strategy is proposed for the FB-IBB converter. The operating principles, output characteristics, and soft switching performances are discussed. The theoretical analysis and experimental results indicate that soft-switching within wide operation range has been achieved in the proposed converter. Hence, high efficiency has been achieved within a wide operation range. As a novel solution for IBB converters, the proposed AC-TLR and its derived IBB converter are good candidates for high-efficiency IBB conversion systems with high output voltage.

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