Fundamental Study of Influence of Ripple Noise From DC–DC Converter on Spurious Noise of Wireless Portable Equipment

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***Abstract*—Power supply noise is a serious concern in noise-sensitive radio frequency or analog circuits. This paper presents an analysis of the influence of the synchronous rectification buck-type dc–dc converters for power amplifiers. An output ripple noise equation of the converter and a spurious noise equation of the carrier output voltage of the class-A amplifier powered by the converter are derived to analyze fundamental characteristics of these noise components theoretically. The amplifier's output spurious noise is calculated by these equations and measured by the evaluation circuit board. The spurious noise variation caused by the parameter variations of the amplifier or the converter is discussed based on these experimental and theoretical results. The spurious noise can be suppressed by decreasing the channel length modulation coefficient of the n-channel MOSFET constituting the amplifier and the natural frequency of the converter output *LC* filter. The spurious noise is reduced to low level below − 60 dB compared to the carrier signal by setting the channel length modulation coefficient below 0.1 V^{-1} and the natural frequency below 120 kHz. Furthermore, when the natural frequency is below 40 kHz, the spurious noise is − 80 dB below the carrier signal.**

***Index Terms*—Amplitude modulation, channel length modulation coefficient, dc–dc converter, natural frequency, power amplifier (PA), ripple noise, spurious noise.**

I. Introduction

SINCE more and more integration of multiple functions in the wireless portable equipment, such as cellular phones, tablet computers, and laptop computers, is advanced, the feature of the longer battery life but small/light weight has become strong interested trend in recent application. The key technology for matching the target is to enhance the efficiency of the power supplies [1], [2].

Linear regulators, which have just input and output capacitors as external parts, are advantageous to achieve small size; hence, they have been employed extensively as main power supplies of portable equipment. Although, because the supply voltage of the electronic components keeps decreasing year by year, the efficiency of linear regulators decreases for low output voltage range caused by the dropout loss in the variable resistor [3], [25]. Therefore, to replace linear regulators with high-efficiency switching dc–dc converters has been advancing.

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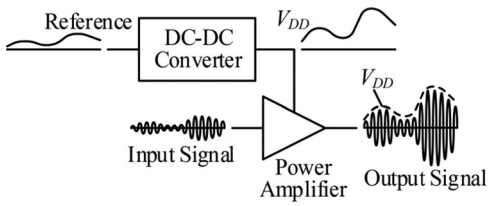

Fig. 1. Block diagram of ET PA supplied from dc–dc converter.

Conventional dc–dc converters have a problem with their large size due to magnetic devices, which occupy the main volume of converters. Nevertheless, in recent years, research of the miniaturization of magnetic devices has been advanced extensively [4]–[11]. Furthermore, small-size dc–dc converter modules for portable equipment have been developed with integrating planar inductors in [12] and [13].

Radio frequency (RF) power amplifiers (PAs) are the most power-consuming components in typical wireless portable equipment [23]–[25]. In modern cellular phones after the third generation, since the amplitude of the carrier signal is modulated in order to achieve higher data rates, high linearity is required in RF PAs [14]. However, the PAs are generally operated in class-A or class-AB mode where their efficiencies are poor. Additionally, as the PAs are always transmitting, their power consumptions are rapidly increasing. Since the PAs have poorer efficiencies in the low output power region, the efficiency improvement by reducing the PA supply voltage is studied. As a result, high efficiency is maintained even at low power region [14]–[28]. The envelope tracking (ET) technique that modulates the supply voltage according to the RF PA output voltage envelope has been reported in [14]. Moreover, the method for generating this variable supply voltage with an efficient switching dc–dc converter has been proposed [15]. Similar investigations have also conducted in [16]–[28]. Fig. 1 shows the block diagram of the ET PA supplied from the switching dc–dc converter [21].

However, switching dc–dc converters are plagued by their noisy output with broadband frequency range caused by their switching operation [29]. Therefore in general, series regulators have been used to provide power for high precision RF or analog components that are sensitive to noise. The conducted output voltage noise of the switching dc–dc converter consists of the ripple noise and the ringing noise. The ripple noise consists of switching frequency fundamental and harmonics; the ringing noise is caused by the resonance of the parasitic inductors

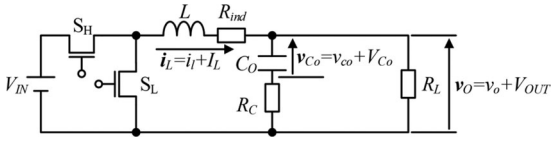

Fig. 2. Equivalent circuit of synchronous rectification buck-type dc–dc converter.

and capacitors of electronic components, lead wires, and circuit board [30]. The periodic noise of the converters generates spurious noise by the high and low sidebands of the carrier signal [15], [16]. Since the noise of the dc–dc converters is usually low frequency compared to RF signals, the sizes of filter passive components are enlarged; this is not desirable for portable equipment. In this case, it is important to know how much supply voltage noise is tolerable to secure the RF signal quality. Stauth and Sanders have analyzed the influence of a sine wave which is injected on the supply voltage by an arbitrary waveform generator to the RF PA [19].

This paper presents the fundamental analysis of the influence of the output ripple noise of the dc–dc converters to the high precision analog circuits such as class-A amplifiers that constitute RF PAs or weak signal processing circuits. The spurious noise of the carrier output voltage of the typical class-A amplifier consisting of an n-channel MOSFET using the synchronous rectification buck-type dc–dc converter as its power supply is analyzed experimentally and theoretically. The ratio of spurious noise to carrier output signal is independent of the amplitude of the carrier output signal; however, it increases with the converter input voltage, the channel length modulation coefficient of the n-channel MOSFET, and the natural frequency of the converter output *LC* filter.

In Section II, the output voltage ripple equation of the dc–dc converter is derived. In Section III, the spurious noise equation of the carrier output voltage of the class-A amplifier powered by the dc–dc converter is derived. In Section IV, the details of the fabricated test circuit system are described. Section V presents measurement and calculated results of the spurious noise caused by the output voltage ripple of the dc–dc converter. Conclusions are presented in Section VI.

II. Output Voltage Equation of DC–DC Converter

In this section, the output voltage spectrum equation to analyze an influence of the ripple noise from the synchronous rectification buck-type dc–dc converter is described in the equivalent circuit shown in Fig. 2.

A. State Equations [12]

In Fig. 2, $V_{\rm IN}$ and $V_{\rm OUT}$ are the input voltage and the output voltage, respectively. $R_{\rm SH}$ and $R_{\rm SL}$ are the on-resistances of the high-side switch S_H and the low-side switch S_L, respectively. L and $R_{\rm ind}$ are the inductance and the series resistance of the inductor in the output *LC* filter, respectively. C_O and R_C are the capacitance and the equivalent series resistance of the capacitor in the output *LC* filter, respectively. R_L is the resistance of the load resistor. Switches S_H and S_L are turned ON and OFF complementarily and output the pulse voltage. The dc and low-frequency components of the pulse voltage are then outputted through the output *LC* filter.

As shown in (1), the inductor current i_L is expressed as the sum of the ac current i_l and the dc current I_L, the capacitor voltage ν_{Co} is expressed as the sum of the ac voltage ν_{co} and the dc voltage V_{Co}, and the output voltage ν_O is expressed as the sum of the ac voltage ν_o and dc voltage $V_{\rm OUT}$

$$\boldsymbol{i}_L = i_l + I_L,\ \ \boldsymbol{v}_{Co} = v_{co} + V_{Co},\ \ \boldsymbol{v}_O = v_o + V_{\rm OUT}. \quad (1)$$

In state 1 where the high-side switch is in on-state and the low-side switch is in off-state, the state equations are expressed as

$$\begin{aligned}\frac{d\boldsymbol{i}_L}{dt} &= \frac{1}{L}\left\{V_{\rm IN} - \left(R_{\rm SH} + R_{\rm ind} + \frac{R_L \cdot R_C}{R_L + R_C}\right)\boldsymbol{i}_L \right. \\ &\qquad \left. - \frac{R_L}{R_L + R_C} v_{Co}\right\} \\ \frac{d\boldsymbol{v}_{Co}}{dt} &= \frac{1}{C_O\,(R_L + R_C)}\left(R_L \cdot \boldsymbol{i}_L - \boldsymbol{v}_{Co}\right) \\ \boldsymbol{v}_O &= \frac{R_L}{R_L + R_C}\left(R_C \cdot \boldsymbol{i}_L + \boldsymbol{v}_{Co}\right). \end{aligned} \quad (2)$$

In state 2 where the high-side switch is in off-state and the low-side switch is in on-state, the state equations are expressed as

$$\begin{aligned}\frac{d\boldsymbol{i}_L}{dt} &= -\frac{1}{L}\left\{\left(R_{\rm SL} + R_{\rm ind} + \frac{R_L \cdot R_C}{R_L + R_c}\right)\boldsymbol{i}_L \right. \\ &\qquad \left. + \frac{R_L}{R_L + R_C}\boldsymbol{v}_{Co}\right\} \\ \frac{d\boldsymbol{v}_{Co}}{dt} &= \frac{1}{C_o\,(R_L + R_C)}\left(R_L \cdot \boldsymbol{i}_L - \boldsymbol{v}_{Co}\right) \\ \boldsymbol{v}_O &= \frac{R_L}{R_L + R_C}\left(R_C \cdot \boldsymbol{i}_L + \boldsymbol{v}_{Co}\right). \end{aligned} \quad (3)$$

B. Waveform of Output Voltage

In steady state, a cycle average becomes constant. Therefore, (2) and (3) result in

$$\boldsymbol{v}_O = \begin{cases} V_{\rm OUT} + E\left\{\frac{f_S}{D}t^2 + \left(\frac{2f_S \cdot C_O \cdot R_C}{D} - 1\right)t \quad \left(0 \le t \le \frac{D}{f_S}\right)\right. \\ \qquad \left. -C_O \cdot R_C - \frac{1-2D}{6f_S}\right\} \\ V_{\rm OUT} - E\left\{\frac{f_S}{1-D}\left(t - \frac{D}{f_S}\right)^2\right. \\ \qquad \left. + \left(\frac{2f_S \cdot C_O \cdot R_C}{1-D} - 1\right)\left(t - \frac{D}{f_S}\right) \quad \left(\frac{D}{f_S} \le t \le \frac{1}{f_S}\right)\right. \\ \qquad \left. -C_O \cdot R_C - \frac{1-2D}{6f_S}\right\} \end{cases} \quad (4)$$

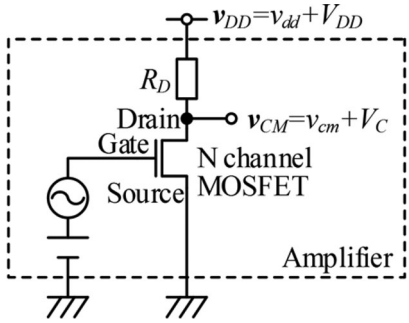

Fig. 3. Circuit configuration of amplifier for analyzing influence of power supply noise.

where

$$E = \frac{(1-D)\,V_{\mathrm{OUT}}}{2f_s \cdot C_o \cdot L}\left(1+\frac{R_{\mathrm{SL}}+R_{\mathrm{ind}}}{R_L}\right)$$
$$D = \frac{(R_{\mathrm{SL}}+R_{\mathrm{ind}}+R_L)\,M}{R_L\,(R_{\mathrm{SL}}-R_{\mathrm{SH}})\,M}, \quad M = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}}. \tag{5}$$

Here, f_S is the switching frequency and D is the duty ratio in state 1.

The waveform of the output voltage can be expressed by a Fourier series as

$$\boldsymbol{v}_O = V_{\mathrm{OUT}} + \sum_{n=1}^{\infty} A_n \sin(npt+\theta_n) \tag{6}$$

where

$$p = 2\pi f_S$$
$$A_n = \frac{V_{\mathrm{OUT}}\,|\sin(\pi nD)|}{(\pi n)^2 f_S \cdot D \cdot L}\left(1+\frac{R_{\mathrm{SL}}+R_{\mathrm{ind}}}{R_L}\right) \cdot \sqrt{R_c^2+\left(\frac{1}{2\pi n \cdot f_S \cdot C_O}\right)^2}$$
$$\theta_n = \tan^{-1}\left[\frac{2\pi n \cdot f_S \cdot C_O \cdot R_C \sin(2\pi nD)+\cos(2\pi nD)-1}{2\pi n \cdot f_S \cdot C_O \cdot R_C\,\{\cos(2\pi nD)-1\}+\sin(2\pi nD)}\right]. \tag{7}$$

The output voltage ripple $\Delta\nu_o$ that is amplitude of the ac output voltage ν_o is expressed as

$$\Delta\nu_o = \frac{(1-D)\,V_{\mathrm{OUT}}}{8f_s^2 L \cdot Co}\left(1+\frac{R_{\mathrm{SL}}+R_{\mathrm{ind}}}{R_L}\right) \cdot \left(1+\frac{4C_o^2 R_c^2 f_s^2}{D\,(1-D)}\right). \tag{8}$$

III. Theory of Spurious Noise Generation of Class-A Amplifier

Fig. 3 describes the circuit configuration of the amplifier for analyzing an influence of the power supply noise. This circuit is a basic class-A amplifier constituted by an n-channel MOSFET and a resistance.

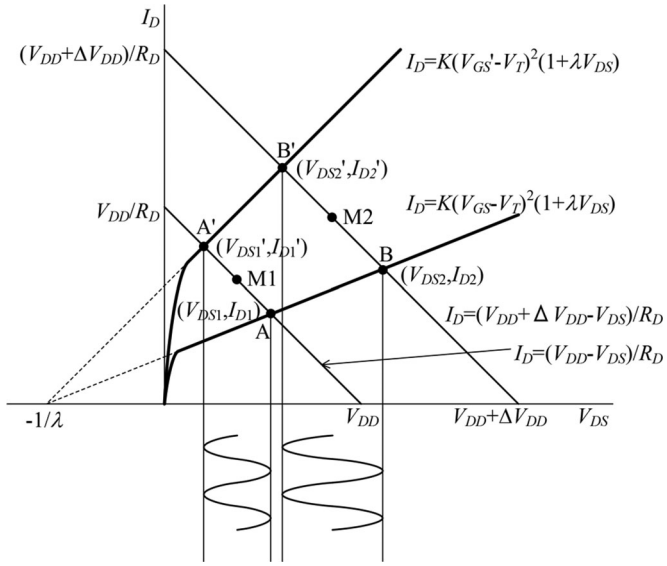

Fig. 4. Load lines of class-A amplifier.

In Fig. 3, R_D is the resistances of the load resistor of the amplifier.

As shown in (9), the supply voltage ν_{DD} is expressed as the sum of the ac voltage ν_{dd} and the dc voltage V_{DD}, and the carrier signal voltage ν_{CM} that is the output voltage of the amplifier is expressed as the sum of the ac voltage ν_{cm} and dc voltage V_C

$$\boldsymbol{v}_{\mathrm{DD}} = v_{\mathrm{dd}} + V_{\mathrm{DD}}, \boldsymbol{v}_{\mathrm{CM}} = v_{\mathrm{cm}} + V_C. \tag{9}$$

A. Spurious Noise Generation by Periodic Variation of Supply Voltage

Fig. 4 explains load lines of the amplifier. V_{DS1}, $V_{\mathrm{DS1}}{}'$, V_{DS2}, and $V_{\mathrm{DS2}}{}'$ are the drain-to-source voltage of the n-channel MOSFET in the point A, A′, B, and B′, respectively. $I_{D1}, I_{D1}{}', I_{D2}$, and $I_{D2}{}'$ are the drain current of the n-channel MOSFET in the point A, A′, B, and B′, respectively. V_{GS} and $V_{\mathrm{GS}}{}'$ are the gate-to-source voltage of the n-channel MOSFET. V_T and λ are the threshold voltage and the channel length modulation coefficient of the n-channel MOSFET, respectively.

It is assumed that the sinusoidal voltage of the amplitude $V_{\mathrm{GS}}{}' - V_{\mathrm{GS}}$ is applied between the gate and the source, and the supply voltage varies infinitesimally by the width of ΔV_{DD}.

In the situation where the supply voltage of the amplifier is V_{DD}, it is assumed that the n-channel MOSFET in Fig. 4 operates at the operating point M1, and the drain-to-source voltage and the drain current are sine wave which vary between the point A and A′. In the point A, the drain current I_{D1} is expressed as

$$I_{D1} = (V_{\mathrm{DD}} - V_{\mathrm{DS1}})/R_D \tag{10}$$
$$I_{D1} = K\,(V_{\mathrm{GS}} - V_T)^2\,(1+\lambda V_{\mathrm{DS1}}) \tag{11}$$

where K is a proportionality coefficient. Equations (10) and (11) result in

$$V_{\mathrm{DS1}} = \frac{V_{\mathrm{DD}} - K \cdot R_D \left(V_{\mathrm{GS}} - V_T\right)^2}{1 + \lambda \cdot K \cdot R_D \left(V_{\mathrm{GS}} - V_T\right)^2}. \tag{12}$$

In the same way as (12), the drain-to-source voltage $V_{\mathrm{DS1}}{}'$ at the point A$'$ is expressed as

$$V_{\mathrm{DS1}}{}' = \frac{V_{\mathrm{DD}} - K \cdot R_D \left(V_{\mathrm{GS}}{}' - V_T\right)^2}{1 + \lambda \cdot K \cdot R_D \left(V_{\mathrm{GS}}{}' - V_T\right)^2}. \tag{13}$$

The variation width of the drain-to-source voltage ΔV_{DS1} between the point A and A$'$ is given by

$$\Delta V_{\mathrm{DS1}} = V_{\mathrm{DS1}} - V_{\mathrm{DS1}}{}'. \tag{14}$$

In the situation where the supply voltage of the amplifier is $V_{\mathrm{DD}} + \Delta V_{\mathrm{DD}}$, it is assumed that the n-channel MOSFET in Fig. 4 operates at the operating point M2, and the drain-to-source voltage and the drain current are sine wave which vary between the point B and B$'$. The variation width of the drain-to-source voltage ΔV_{DS2} between the point B and B$'$ is expressed as

$$\Delta V_{\mathrm{DS2}} = V_{\mathrm{DS2}} - V_{\mathrm{DS2}}{}' \tag{15}$$

where

$$V_{\mathrm{DS2}} = \frac{V_{\mathrm{DD}} + \Delta V_{\mathrm{DD}} - K \cdot R_D \left(V_{\mathrm{GS}} - V_T\right)^2}{1 + \lambda \cdot K \cdot R_D \left(V_{\mathrm{GS}} - V_T\right)^2}$$

$$V_{\mathrm{DS2}}{}' = \frac{V_{\mathrm{DD}} + \Delta V_{\mathrm{DD}} - K \cdot R_D \left(V_{\mathrm{GS}}{}' - V_T\right)^2}{1 + \lambda \cdot K \cdot R_D \left(V_{\mathrm{GS}}{}' - V_T\right)^2}. \tag{16}$$

Equations (14) and (15) result in

$$\Delta V_{\mathrm{DS2}} = \Delta V_{\mathrm{DS1}} \left(1 + \frac{\lambda \Delta V_{\mathrm{DD}}}{1 + \lambda V_{\mathrm{DD}}}\right). \tag{17}$$

The ac carrier signal voltage ν_{cm} in Fig. 3 is expressed as

$$v_{\mathrm{cm}} = V_c \left(1 + F_A \sin pt\right) \sin \omega_c t \tag{18}$$

where

$$v_{\mathrm{dd}} = V_{\mathrm{dd}} \sin pt, F_{_A} = \lambda \cdot V_{\mathrm{dd}} / (1 + \lambda \cdot V_{\mathrm{DD}}). \tag{19}$$

Here, V_c and ω_c are the amplitude and the angular frequency of ν_{cm} at the ac supply voltage $\nu_{\mathrm{dd}} = 0$ V, respectively. V_{dd} and p are the amplitude and the angular frequency of ν_{dd}, respectively. Equation (19) indicates that ν_{cm} is modulated by the amplitude modulation factor F_A consisting of the supply voltage variation V_{dd} and the channel length modulation coefficient λ of the n-channel MOSFET. Equation (19) results in

$$v_{\mathrm{cm}} = V_c \sin \omega_c t + \frac{F_A \cdot V_c}{2} \cos\left(\omega_c - p\right) t - \frac{F_A \cdot V_c}{2} \cos\left(\omega_c + p\right) t. \tag{20}$$

It is means that when the supply voltage is varied, the noise components are generated by the high and low sidebands of the carrier signal. The spurious noise ratio S_A that is the ratio between the voltage amplitude of the sideband noise components and that of the fundamental carrier signal is given by

$$S_A = F_{_A} / 2. \tag{21}$$

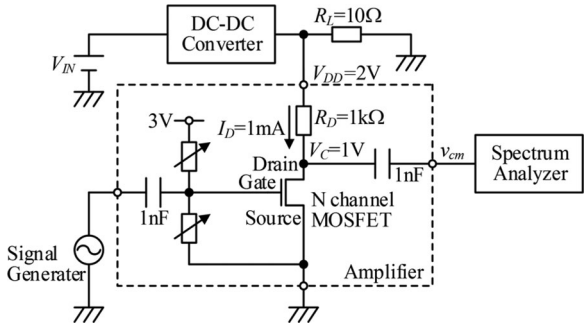

Fig. 5. Circuit configuration of evaluation system.

B. Spurious Noise Generation by Ripple Noise From DC–DC Converter

When the dc–dc converter in Fig. 2 is used as the supply for the amplifier in Fig. 3, the carrier signal ν_{cm} can be expressed by substituting (6) into (20) as

$$v_{\mathrm{cm}} = V_c \sin 2\pi f_c t + \sum_{n=1}^{\infty} \frac{F_{\mathrm{An}} \cdot V_c}{2} \cos\left\{2\pi \left(f_c - n \cdot f_S\right) t - \theta_n\right\} - \sum_{n=1}^{\infty} \frac{F_{\mathrm{An}} \cdot V_c}{2} \cos\left\{2\pi \left(f_c + n \cdot f_S\right) t + \theta_n\right\} \tag{22}$$

where

$$F_{\mathrm{An}} = \frac{\lambda}{1 + \lambda \cdot V_{\mathrm{DD}}} \frac{2 f_N^2 V_{\mathrm{DD}} \left|\sin\left(\pi n \cdot D\right)\right|}{\pi n^3 f_S^2 \cdot D} \cdot \left(1 + \frac{R_{\mathrm{SL}} + R_{\mathrm{ind}}}{R_L}\right) \cdot \sqrt{1 + \left(2\pi n \cdot f_S \cdot C_O \cdot R_C\right)^2}$$

$$f_N = 1/2\pi \sqrt{L \cdot C_O}, \quad V_{\mathrm{DD}} = V_{\mathrm{OUT}}. \tag{23}$$

Here, f_N is the natural frequency of the output LC filter of the converter. The spurious noise ratio S_{An} caused by the nth harmonic of the output voltage ripple of the converter is given by

$$S_{\mathrm{An}} = F_{_{\mathrm{An}}} / 2. \tag{24}$$

S_{An} is expressed using the channel length modulation coefficient λ of the n-channel MOSFET and parameters of the converter.

IV. Test Circuit Configuration

Fig. 5 shows the circuit configuration of the evaluation system. The dc–dc converter drives the class-A amplifier. The output voltage of the amplifier is monitored by a spectrum analyzer.

A. DC–DC Converter

Figs. 6 and 7 show the circuit configuration and the external view of the dc–dc converter. Specifications of the converter are shown in Table I. The converter is a synchronous rectification

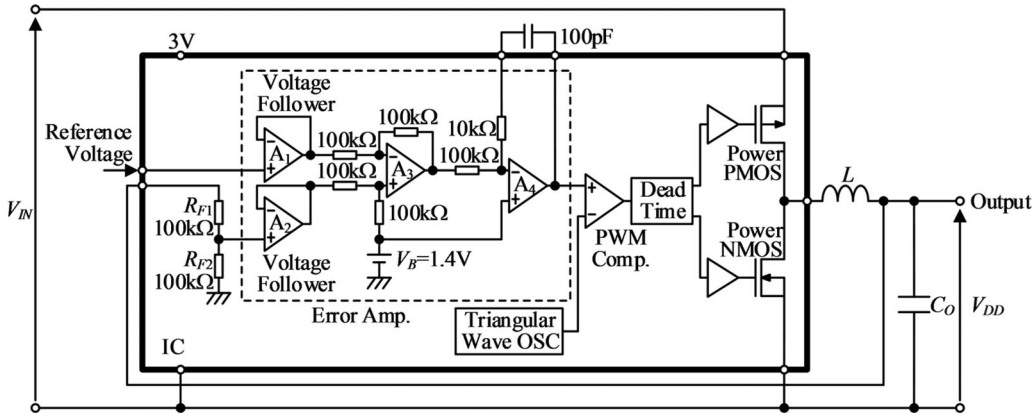

Fig. 6. Circuit configuration of dc–dc converter.

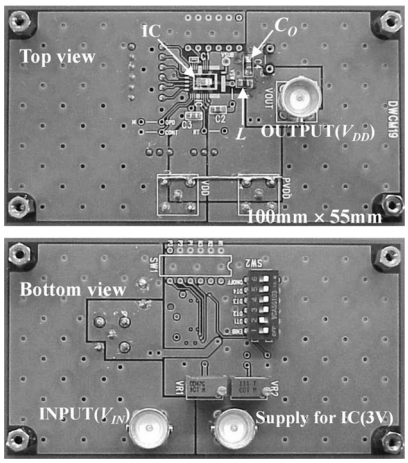

Fig. 7. External view of dc–dc converter board.

TABLE I
SPECIFICATIONS OF DC–DC CONVERTER

Switching frequency f_S [MHz]	2.0
Input voltage $V_{\rm IN}$ [V]	3.0, 4.0, 5.0
Output voltage $V_{\rm DD}$ [V]	2.0
Load resistance R_L [Ω]	10
p-channel MOS on resistance $R_{\rm SH}$ [Ω]	0.5
n-channel MOS on resistance $R_{\rm SL}$ [Ω]	0.5
Dead time t_D [ns]	15

buck-type converter controlled by the pulse width modulation (PWM) scheme. p-channel MOSFET is used for the high-side switch and n-channel MOSFET is used for the low-side switch.

In the circuit of Fig. 6, the reference voltage level according to the carrier signal amplitude of the class-A amplifier is supplied from the outside of the IC in order to change the output voltage according to change of the carrier signal amplitude. The error amplifier in Fig. 6 consists of cascade connection of input buffer amplifiers A1, A2, the differential amplifier A3, and the proportional integral (PI) controller A4. In this composition, the operating points of the differential amplifier A3 and PI controller A4 are fixed by bias voltage V_B. As a result, the operating points of A3 and A4 are not changed when the reference voltage changes. Therefore, excessive overshoot or undershoot of voltage does not occur in the error amplifier output. Hence, the output voltage of the converter can obtain the stable transient response characteristic decided by the gain of the PI controller.

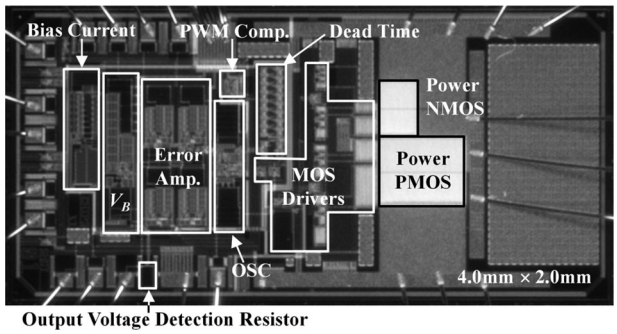

Fig. 8. Top view of control IC.

In Fig. 6, the feedback signal from the output voltage is applied to the error amplifier through the output voltage detection resistors R_{F1} and R_{F2}. The output voltage of the error amplifier depends on the difference between the reference voltage and the feedback signal. The PWM comparator comperes the output voltage error signal of the error amplifier and the triangular wave signal and then generates the PWM pulse signal with its duty ratio varied with the error signal. The PWM pulse signal is then passed through the dead time circuit to the MOSFETs drivers to drive the output power MOSFETs. The switching frequency is 2.0 MHz.

Fig. 8 depicts a top view of the prepared control IC. The power MOSFETs are monolithically integrated within the IC in a standard 1-μm CMOS process. The chip size is 2.0×4.0 mm^2.

Tables II and III summarize specifications of the inductor and the capacitor constituting the output *LC* filter of the converter, respectively.

B. Class-A Amplifier

The prepared evaluation board of the class-A amplifier is shown in Fig. 9. Table IV shows experimental values of the channel length modulation coefficient λ of n-channel

TABLE II
SPECIFICATIONS OF INDUCTOR OF OUTPUT *LC* FILTER

Sample name	L1	L2	L3
Inductance L [μH]	1.04	2.13	4.62
Resistance R_{ind} [Ω]	0.12	0.25	0.21

TABLE III
SPECIFICATIONS OF CAPACITOR OF OUTPUT *LC* FILTER

Sample name	C1	C2
Capacitance C_O [μF]	0.87	5.07
Resistance R_C [mΩ]	9.95	5.41

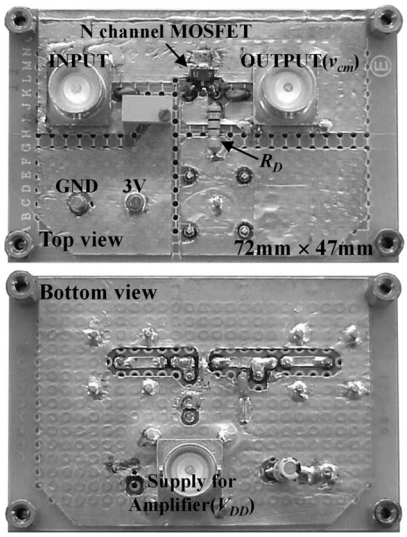

Fig. 9. External view of class-A amplifier board.

TABLE IV
EXPERIMENTAL VALUES OF CHANNEL LENGTH MODULATION COEFFICIENT OF N-CHANNEL MOSFETS USED IN CLASS-A AMPLIFIER

Sample name	M1	M2	M3
Channel length modulation coefficient λ [V^{-1}]	0.10	0.42	0.63

TABLE V
OPERATION CONDITION OF CLASS-A AMPLIFIER

Drain-to-source dc bias voltage V_C [V]	1.0
Drain dc bias current I_D [mA]	1.0
Carrier frequency f_c [MHz]	600

MOSFETs used in the amplifier under an operation condition of 1.0-V drain-to-source voltage and 1.0-mA drain current. The n-channel MOSFET are for analog signal amplifiers and on the market. Table V shows the operation condition of the amplifier.

Fig. 10 presents the external view of the evaluation system consisting of the converter board and the amplifier board. Table VI describes specifications and operating conditions of instruments used to measure the amplifier's output noise.

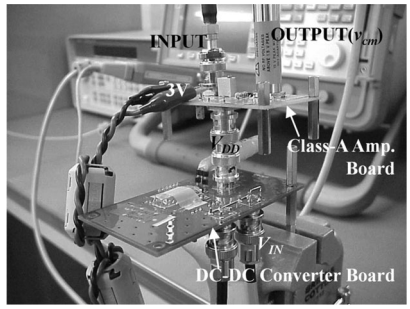

Fig. 10. External view of evaluation system.

TABLE VI
SPECIFICATIONS AND OPERATING CONDITIONS OF MEASURING INSTRUMENTS

Spectrum analyzer	Model	E4411B (Hewlett Packard)
	Frequency range	9 kHz–1.5 GHz
	Input impedance	50 Ω
	Detector mode	Peak detection
	Resolution bandwidth	1 kHz
	Video bandwidth	1 kHz
Probe	Model	85024A (Hewlett Packard)
	Frequency range	300 kHz–3.0 GHz
	Input impedance	0.7 pF, 50 Ω
Signal generator	Model	8648B (Agilent)
	Frequency range	9 kHz–2 GHz
	Output impedance	50 Ω
	Waveform	Sine
	Output frequency	600 MHz

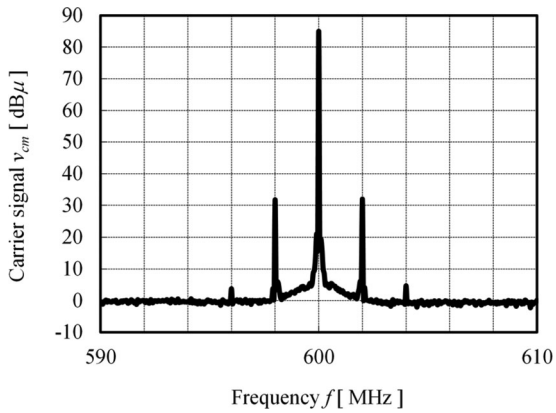

Fig. 11. Output spectrum of class-A amplifier.

V. MEASUREMENT RESULTS

Fig. 11 demonstrates the measured output spectrum of the class-A amplifier with the sinusoidal input under an operation condition: $V_c = 88$ dBμ, $V_{\rm IN} = 4.0$ V, $L = 1.04$ μH, $C_O = 0.87$ μF, and $\lambda = 0.42$ V^{-1}. Sideband's spurious noise caused by ripple on the dc–dc converter output voltage $V_{\rm DD}$ is observed from the fundamental carrier output by ± 2 and ± 4 MHz in this figure. These ± 2 and ± 4 MHz components are amplitude-modulated signal by the fundamental and second harmonic of $V_{\rm DD}$ ripple, respectively, as explained in (22). It is found that

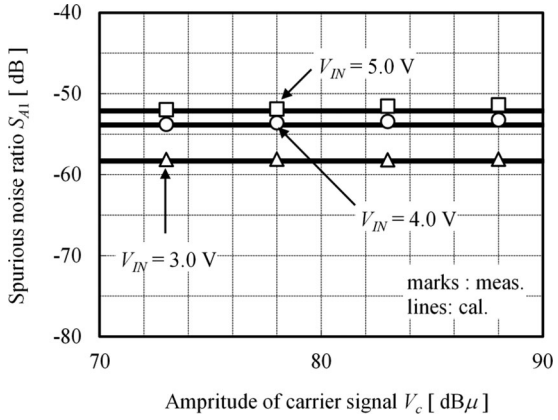

Fig. 12. Measured and calculated spurious noise ratio versus fundamental voltage amplitude of carrier output signal of class-A amplifier.

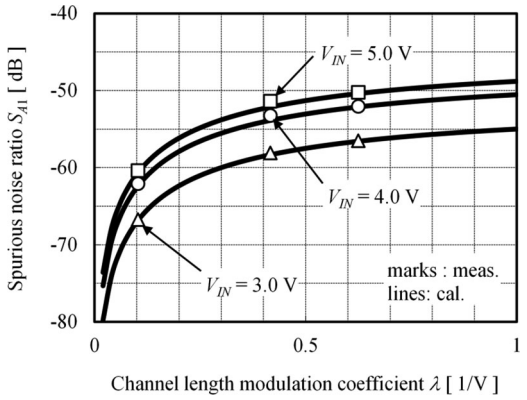

Fig. 13. Measured and calculated spurious noise ratio versus channel length modulation coefficient of n-channel MOSFETs used in class-A amplifier.

the noise caused by the fundamental of $V_{\rm DD}$ ripple is the largest noise component in the sideband's spurious noise. The spurious noise ratio S_{A1} which is the ratio of the noise voltage caused by the fundamental of $V_{\rm DD}$ ripple to the fundamental voltage amplitude V_c of the carrier output signal of the amplifier is approximately $-$ 53 dB in Fig. 11. Next, S_{A1} is discussed.

Fig. 12 shows the measured and calculated spurious noise ratio versus the fundamental voltage amplitude of the carrier output signal of the class-A amplifier under an operation condition: $L = 1.04$ μH, $C_O = 0.87$ μF, and $\lambda = 0.42$ V^{-1}. The calculated values are given by (23) and (24). As shown in Fig. 12, the calculated values agree with the measured values. S_{A1} is kept almost constant because it is independent of V_c as shown in (23) and (24). S_{A1} increases with increasing $V_{\rm IN}$. Assuming the loss resistances $R_{\rm SH}$, $R_{\rm SL}$, and $R_{\rm ind}$ are much smaller than the load resistance R_L, (25) is derived from (5), (23), and (24)

$$S_{A1} \propto \frac{V_{\rm IN}}{V_{\rm DD}} \sin\left(\pi \frac{V_{\rm DD}}{V_{\rm IN}}\right). \tag{25}$$

Equation (25) indicates that S_{A1} is an increasing function of $V_{\rm IN}$.

Fig. 13 shows the measured and calculated spurious noise ratio versus the channel length modulation coefficient of the n-channel MOSFETs used in the class-A amplifier under an operation condition: $V_c = 88$ dBμ, $L = 1.04$ μH, and $C_O = 0.87$ μF. As shown in this figure, the calculated values agree with the measured values. S_{A1} increases with increasing λ because S_{A1} is an increasing function of λ as shown in (23) and (24). When λ is below approximately 0.1 V^{-1}, low S_{A1} below $-$ 60 dB is achieved.

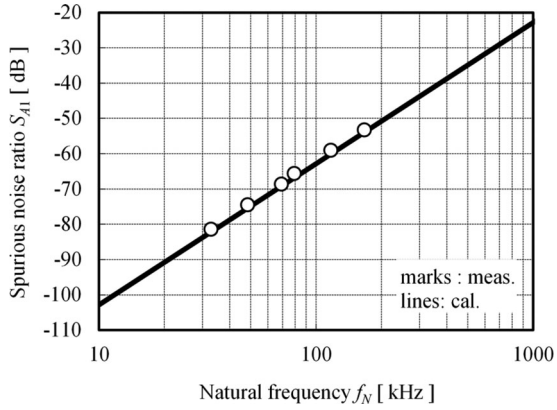

Fig. 14. Measured and calculated spurious noise ratio versus natural frequency of output *LC* filter of dc–dc converter.

In portable electronic communication devices, the input voltage of a dc–dc converter is not constant because this voltage is from a battery, for example, Li-ion battery. Therefore, it is difficult to avoid the dependence of the spurious noise on the converter input voltage. For the spurious noise reduction, in addition to designing the channel length modulation coefficient of the amplifier as small as possible, reducing the output ripple noise of the converter is required over the entire input voltage range of the converter.

Fig. 14 shows the measured and calculated spurious noise ratio versus the natural frequency of the converter output *LC* filter to reduce the output ripple noise at $V_c = 88$ dBμ, $V_{\rm IN} = 4.0$ V, and $\lambda = 0.42$ V^{-1}. The natural frequency f_N can be given by substituting the *LC* combinations in Tables II and III into (23) and solving f_N. As shown in this figure, the calculated values agree with the measured values. S_{A1} increases with increasing f_N because S_{A1} is proportional to the square of f_N as shown in (23) and (24). Therefore, the spurious noise improves by reducing f_N. When f_N is set below approximately 120 kHz, low S_{A1} below $-$ 60 dB is achieved. For the further improvement of noise reduction like $S_{A1} < -80$ dB, lower f_N below approximately 40 kHz is needed.

Assuming the equivalent series resistance R_C of the capacitor in the output *LC* filter is enough small to ignore, (24) results in

$$S_{\rm An} \propto \frac{f_N^2}{f_S^2}. \tag{26}$$

From this equation, it is found that if the output *LC* filter has to be miniaturized in order to reduce the size of the system although f_N increases by reduction of the inductance and capacitance of the filter, the increase in $S_{\rm An}$ can be suppressed by increasing f_S in proportion to f_N.

VI. Conclusion

We have analyzed experimentally and theoretically the influence of the output ripple noise of a buck-type dc–dc converter

on the spurious noise generation in the carrier signal of a class-A amplifier. The results obtained are as follows.

1) The spurious noise equation of the carrier output voltage of the class-A amplifier when using the dc–dc converter as its power supply was derived in consideration of the characteristics of the component parts.
2) Both the experimental and theoretical analysis results of the spurious noise caused by the converter output ripple are explained.
3) The spurious noise ratio is independent of the fundamental voltage amplitude of the carrier output signal, but it increases with increasing the converter input voltage, the channel length modulation coefficient of the amplifier, and the natural frequency of the converter output *LC* filter.
4) Even in the case of relatively small inductance and capacitance of the converter output *LC* filter, such as about 1 μH and 1 μF, when the channel length modulation coefficient of the amplifier was below 0.1 V^{-1}, the spurious noise ratio was suppressed below $-$ 60 dB.
5) The spurious noise ratio below $-$ 60 dB was obtained at the natural frequency below 120 kHz. When the natural frequency was below 40 kHz, the lower spurious noise ratio below $-$ 80 dB was achieved.
6) The spurious noise ratio is suppressed by increasing the switching frequency of the converter.

The output noise of a class-A amplifier can be analyzed qualitatively and quantitatively by the derived spurious noise equation. For other various amplifying systems such as class-AB and class-B amplifiers, the spurious noise equation can be generalized by replacing the resistive load in Fig. 3 with the complex impedance load and by estimating the coefficient similar to the channel length modulation coefficient of the MOSFET in Fig. 3. These studies will lead to optimization and high performance of wireless portable equipment and their power supply.

REFERENCES

[1] S. Zhou and G. A. Rincon-Mora, "A high efficiency, soft switching dc–dc converter with adaptive current-ripple control for portable applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 4, pp. 319–323, Apr. 2006.

[2] W. Lee, Y. Wang, D. Shin, N. Chang, and M. Pedram, "Optimizing the power delivery network in a smartphone platform," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 33, no. 1, pp. 36–49, Jan. 2014.

[3] Y. Ahn, H. Nam, and J. Roh, "A 50-MHz fully integrated low-swing buck converter using packaging inductors," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4347–4356, Oct. 2012.

[4] S. Sugahara, M. Edo, T. Sato, and K. Yamasawa, "The optimum chip size of a thin film reactor for a high-efficiency operation of a micro dc-dc converter," in *Proc. IEEE Power Electron. Spec. Conf.*, May 1998, pp. 1499–1503.

[5] H. Nakazawa, M. Edo, Y. Katayama, M. Gekinozu, S. Sugahara, Z. Hayashi, K. Kuroki, E. Yonezazwa, and K. Matsuzaki, "Micro-dc/dc converter that integrates planar inductor on power IC," *IEEE Trans. Magn.*, vol. 36, no. 5, pp. 3518–3520, Sep. 2000.

[6] M. Wens and M. S. J. Steyaert, "A fully integrated CMOS 800-mW four-phase semiconstant on/off-time step-down converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 326–333, Feb. 2011.

[7] M. Wang, J. Li, K. D. T. Ngo, and H. Xie, "A surface-mountable microfabricated power inductor in silicon for ultracompact power supplies," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1310–1315, May 2011.

[8] M. Araghchini, J. Chen, V. Doan-Nguyen, D. V. Harburg, D. Jin, J. Kim, M. S. Kim, S. Lim, B. Lu, D. Piedra, J. Qiu, J. Ranson, M. Sun, X. Yu, H. Yun, M. G. Allen, J. A. del Alamo, G. DesGroseilliers, F. Herrault, J. H. Lang, C. G. Levey, C. Murray, D. Otten, T. Palacios, D. J. Perreault, and C. R. Sullivan, "A technology overview of the powerchip development program," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4182–4201, Sep. 2013.

[9] D. Yao, C. G. Levey, R. Tian, and C. R. Sullivan, "Microfabricated v-groove power inductors using multilayer Co-Zr-O thin films for very-high-frequency dc-dc converters," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4384–4394, Sep. 2013.

[10] T. M. Andersen, C. M. Zingerli, F. Krismer, J. W. Kolar, N. Wang, and C. O. Mathuna, "Modeling and Pareto optimization of microfabricated inductors for power supply on chip," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4422–4430, Sep. 2013.

[11] C. Feeney, N. Wang, S. C. O Mathuna, and M. Duffy, "A 20-MHz 1.8-W dc-dc converter with parallel microinductors and improved light-load efficiency," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 771–779, Feb. 2015.

[12] S. Sugahara, K. Yamada, M. Edo, T. Sato, and K. Yamasawa, "90% high efficiency and 100-W/cm^3 high power density integrated dc–dc converter for cellular phones," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1994–2004, Apr. 2013.

[13] C. D. Meyer, S. S. Bedair, B. C. Morgan, and D. P. Arnold, "A micromachined wiring board with integrated microinductor for chip-scale power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6052–6063, Nov. 2014.

[14] A. Brackle, L. Rathgeber, F. Siegert, S. Heck, and M. Berroth, "Power supply modulation for RF applications," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, Sep. 2012, pp. LS8d.3-1–LS8d.3-5.

[15] G. Hanington, P.-F. Chen, P. M. Asbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.

[16] N. Schlumpf, M. Declercq, and C. Dehollain, "A fast modulator for dynamic supply linear RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1015–1025, Jul. 2004.

[17] V. Yousefzadeh, N. Wang, Z. Popovic, and D. Maksimovic, "A digitally controlled dc/dc converter for an RF power amplifier," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 164–172, Jan. 2006.

[18] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 549–552, Mar. 2006.

[19] J. T. Stauth and S. R. Sanders, "Power supply rejection for RF amplifiers: Theory and measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 10, pp. 2043–2052, Oct. 2007.

[20] M. C. W. Hoyerby and M. A. E. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2387–2398, Sep. 2008.

[21] M. Rodriguez, P. Fernandez-Miaja, A. Rodriguez, and J. Sebastian, "A multiple-input digitally controlled buck converter for envelope tracking applications in radiofrequency power amplifiers," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 369–381, Feb. 2010.

[22] M. Vasie, O. Garcia, J. A. Oliver, P. Alou, D. Diaz, and J. A. Cobos, "Multilevel power supply for high-efficiency RF amplifiers," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 1078–1089, Apr. 2010.

[23] J. Choi, D. Kim, D. Kang, and B. Kim, "A new power management IC architecture for envelope tracking power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 7, pp. 1796–1802, Jul. 2011.

[24] M. Bathily, B. Allard, and F. Hasbani, "A 200 MHz integrated buck converter with resonant gate drivers for an RF power amplifier," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 610–613, Feb. 2012.

[25] V. Pala, H. Peng, P. Wright, M. M. Hella, and T. P. Chow, "Integrated high-frequency power converters based on GaAs pHEMT: Technology characterization and design examples," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2644–2656, May 2012.

[26] P. F. Miaja, M. Rodriguez, A. Rodriguez, and J. Sebastian, "A linear assisted dc/dc converter for envelope tracking and envelope elimination and restoration applications," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3302–3309, Jul. 2012.

[27] J. Kim, D. Kim, Y. Cho, D. Kang, B. Park, and B. Kim, "Envelope-tracking two-stage power amplifier with dual-mode supply modulator for LTE applications," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 1, pp. 543–552, Jan. 2013.

[28] P. F. Miaja, J. Sebastian, R. Marante, and J. A. Garcia, "A linear assisted switching envelope amplifier for an UHF polar transmitter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1850–1861, Apr. 2014.

[29] K. Koo, J. Kim, M. Kim, and J. Kim, "Impact of PCB design on switching noise and EMI of synchronous dc-dc buck converter," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Jul. 2010, pp. 67–71.
[30] K. Kam, D. Pommerenke, F. Centola, C.-W. Lam, and R. Steinfeld, "EMC guideline for synchronous buck converter design," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Aug. 2009, pp. 47–52.

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