Letters

Failure Analysis of 1200-V/150-A SiC MOSFET Under Repetitive Pulsed Overcurrent Conditions

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***Abstract*—SiC MOSFETs are a leading option for increasing the power density of power electronics; however, for these devices to supersede the Si insulated-gate bipolar transistor, their characteristics have to be further understood. Two SiC vertically oriented planar gate D-MOSFETs rated for 1200 V/150 A were repetitively subjected to pulsed overcurrent conditions to evaluate their failure mode due to this common source of electrical stress. This research supplements recent work that demonstrated the long term reliability of these same devices [1]. Using an *RLC* pulse-ring-down test bed, these devices hard-switched 600 A peak current pulses, corresponding to a current density of 1500 A/cm^2. Throughout testing, static characteristics of the devices such as B_{VDSS}, $R_{\mathrm{DS(on)}}$, and $V_{\mathrm{GS(th)}}$ were measured with a high power device analyzer. The experimental results indicated that a conductive path was formed through the gate oxide; TCAD simulations revealed localized heating at the SiC/SiO$_2$ interface as a result of the extreme high current density present in the device's JFET region. However, the high peak currents and repetition rates required to produce the conductive path through the gate oxide demonstrate the robustness of SiC MOSFETs under the pulsed overcurrent conditions common in power electronic applications.**

***Index Terms*—Failure modes, gate oxide failure, MOSFET, pulsed overcurrent, SiC.**

I. Introduction

SIC power semiconductor devices have been identified as a prime option for increasing the power density and high temperature capability of power electronics [1]–[5]. High power and high voltage power electronic designs currently utilize silicon insulated-gate bipolar transistors (IGBTs) for the active components. However, silicon IGBTs are currently limiting achievable power density due to their inherently slow switching speed, high conduction losses, and relatively low maximum operating temperature [6]–[9]. SiC has several notable material properties that make it superior to silicon for high voltage and high power applications including a three times wider energy bandgap, ten times higher critical electric field strength, and three times higher thermal conductivity [10], [11]. These properties enable the utilization of SiC MOSFETs at the voltages and power levels currently implemented with silicon IGBTs [6]–[11]. This substitution enables increased switching frequency and reduced switching losses [2], [12] due to the lack of minority carrier recombination, maintains low conduction losses [3], and allows operation at higher temperatures [13]–[17]. The increased switching frequency capability of SiC MOSFETs allows for the utilization of smaller magnetic and capacitive components in applications such as dc–dc converters. In applications where industry standards limit d*V*/d*t* and d*I*/d*t* for the purposes of preventing insulation degradation [18] and reducing electromagnetic interference [19], such as motor drives, the benefit of superior switching speed of SiC MOSFETs may be negated; however, the SiC devices still yield reduced losses resulting from their lower on-state voltage as compared to the saturation voltage of Si IGBTs under comparable conduction current and voltage ratings [20]. In addition, the overall module or device form factor is smaller for SiC MOSFETs than Si IGBTs for comparable power levels, while improved thermal properties and reduced losses decrease thermal management overhead. As a result of these improvements, overall system size is decreased yielding increased power densities with SiC MOSFETs compared to existing commercial systems utilizing Si IGBTs [9]. However, for SiC technology to displace the well-known and accepted Si devices, its performance and failure modes must be understood across all conditions expected in commercial applications [21]–[27]. Work has previously been performed to understand the effect of pulsed overcurrents on the long-term reliability of SiC MOSFETs [1], [24]; however, these results did not examine the failure mode, which must be analyzed through further testing and modeling.

In this letter, a failure mode of SiC MOSFETs during pulsed overcurrents is presented. This letter supplements a recent *IEEE Transactions on Power Electronics* letter that demonstrated the long-term reliability of a SiC MOSFET during pulsed overcurrent conditions [1], and builds on the present body of knowledge by determining their failure mechanism through both experimental results and TCAD simulation. In this letter, two SiC MOSFETs rated for 1200 V/150 A were hard-switched with pulsed overcurrents of approximately four times their given rating, resulting in peak currents of 600 A (corresponding to an extremely high peak current density of 1500 A/cm^2). The devices are the vertically oriented planar gate D-MOSFET

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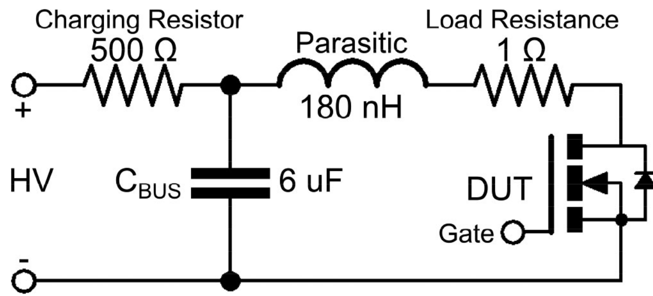

Fig. 1. Schematic of *RLC* pulse-ring-down circuit used to generate pulsed overcurrents [1].

TABLE I
OVERVIEW OF TESTS PERFORMED

Device ID	Pulses	Freq. (Hz)	Voltage (V)	Current (A)
X2Y5	5000	1	600	600
	5000	2	600	600
	5000	5	600	600
	14 000	10	600	600
Total: 29 000 Pulses				
X2Y6	4000	1	600	600
	4000	2	600	600
	4000	5	600	600
	4000	10	600	600
	$764\,000 < x < 774\,000$	2	600	600
Total: $780\,000 < x < 790\,000$ Pulses				

previously described in [1]; a generic description of the DMOSFET structure and operation can be found in [29]. The transient currents were generated with an *RLC* pulse-ring-down circuit overviewed in [1]. The devices were subjected to the pulsed overcurrents at frequencies of 1, 2, 5, and 10 Hz corresponding to duty cycles of 0.002, 0.004, 0.1, and 0.02%, respectively, to characterize their performance as a function of frequency. This experimental data indicated that the devices' failure mode was a gate oxide-conductive path formed by localized heating of the JFET region; TCAD simulations were performed to validate these results. Due to the high rep-rates and high current densities required to induce a gate oxide failure, these devices displayed robust performance in pulsed overcurrent conditions.

II. Test Setup and Procedure

An *RLC* pulse-ring-down circuit generated the 1500 A/cm^2 pulsed overcurrents used to test the SiC MOSFETs at a blocking voltage of 600 V. This circuit was described in detail in [1], and the circuit schematic can be seen in Fig. 1. The characteristic current waveform of this circuit is a fast rising edge limited by the parasitic inductance of the circuit followed by an *RC* decay of the energy stored in the bus capacitance through the load resistor and device under test (DUT). This waveform simulates the pulsed overcurrents common in power electronic circuits such as dc-bus shoot-through, capacitive loads, short-circuit conditions, and circuits specifically designed to produce repetitive high peak currents such as capacitor chargers and plasma igniters.

The SiC power MOSFETs' failure mode during pulsed overcurrent conditions was determined through a process of measuring the devices' electrical characteristics, exposing the devices to pulsed overcurrents in the *RLC* test bed, and then remeasuring the devices' electrical characteristics. This process allowed for the devices' degradation to be clearly documented as a function of the number of current pulses. The testing setup used to determine the failure mode was identical to the setup presented in [1] and is briefly described here. The devices' electrical characteristics including B_{VDSS}, $R_{\mathrm{DS(on)}}$, $V_{\mathrm{GS(th)}}$, and transconductance were measured with an Agilent B1505A high power device analyzer. The waveforms generated by the DUT in the *RLC* pulse-ring-down circuit were captured with a Tektronix MSO4054 oscilloscope. The drain–source voltage, gate–source voltage, drain current, and gate current were all captured with the probes described in [1]. These waveforms were then processed using OriginPro to calculate the devices' peak power, energy dissipation, and gate charge. The number of switching cycles was increased semilogarithmically during testing to allow initial degradation and device "burn in" to be clearly captured. The gates of the DUTs were driven from -5 to $+25$ V with a Fairchild FOD3182 optically isolated push–pull gate driver as described in [1]. The tests performed on both of the SiC MOSFETs are summarized in Table I and detailed in Section IV. Note that the variable, x, at the bottom of Table I indicates the range of pulses in which the device labeled X2Y6 failed.

III. TCAD Simulation Overview

In order to have a better understanding of the device failure mechanism under high current density pulsed condition, physics-based simulations were performed using Silvaco ATLAS TCAD software. Physics-based simulation provides a comprehensive visualization of the various physical phenomena occurring within the device such as electric field distribution, electron–hole plasma formation, and lattice temperature variation. In this research, Silvaco simulation was performed to replicate the conditions of the experimental work and verify the cause of device failure. Due to meshing requirements and computational limitations, it is impractical to design a complete MOSFET in Silvaco, so a 2-D 4H-SiC DMOSFET cell with a blocking voltage of 1200 V and a cell pitch of 10 μm was designed as shown in Fig. 2. The detailed design of the DMOSFET structure is discussed in [28] and [29].

Simulation models were included to account for mobility, recombination, avalanche breakdown, and lattice heating [30]. The device structure was simulated using the RLC pulse-ring-down circuit with parameters matched to the hardware setup. The ring-down circuit generated a current pulse with a peak current magnitude which corresponded to a current density of 1500 A/cm^2 with respect to the 2-D DMOSFET cell.

IV. Results and Discussion

The described experimental setup and TCAD simulation were used in conjunction to determine the failure mode of SiC MOSFETs under repetitive pulsed overcurrent conditions. Exemplar

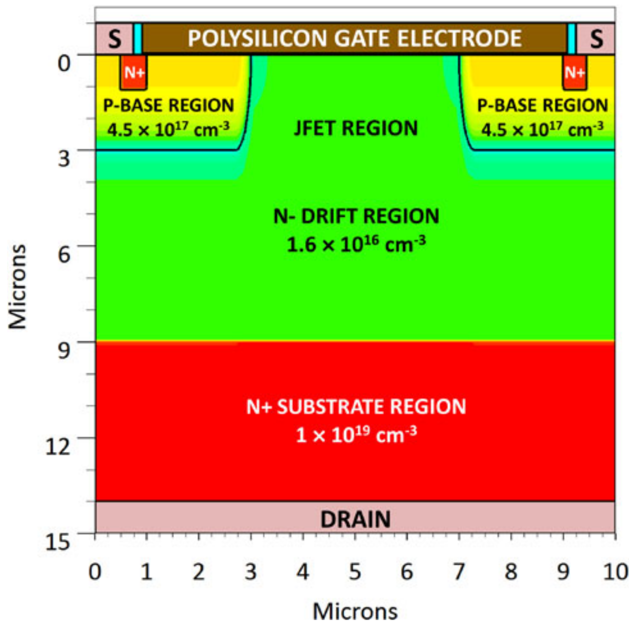

Fig. 2. 1200 V 4H-SiC DMOSFET complete cell structure designed in Silvaco ATLAS. The image shows the contour plot of doping profile.

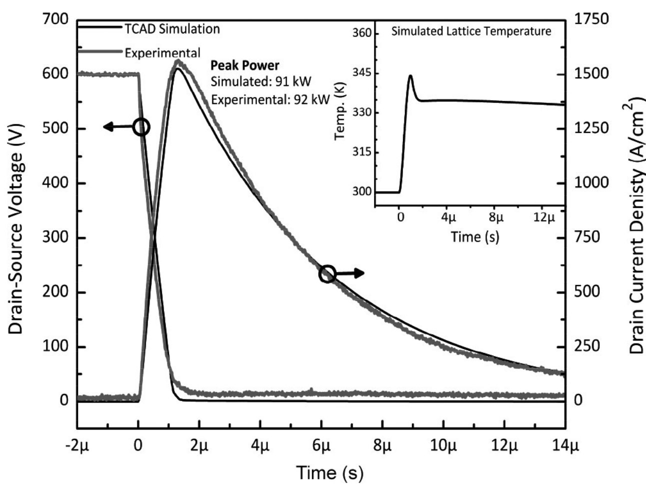

Fig. 3. Comparison of an exemplar experimental device waveform and TCAD simulation; the similarity of the two demonstrates the accuracy of the model, while the experimental waveform demonstrates the capability of the SiC MOSFET to maintain a low forward voltage drop when subjected to extreme pulsed overcurrents.

waveforms are shown in Fig. 3, specifically a comparison of the 20 000th switching cycle performed at 10 Hz and 25 °C of the device labeled X2Y5 compared with the TCAD simulation of the device's structure. The experimental data are plotted in gray and the TCAD result is plotted in black. Fig. 3 displays the similarity between the experimental and simulation results, demonstrates the accuracy of the model, and shows the simulated temperature rise for a single pulse. In addition, the low on-state voltage drop at the peak current confirms that the tested SiC MOSFET does not saturate under severe transient overcurrent conditions. The juxtaposition of the experimental

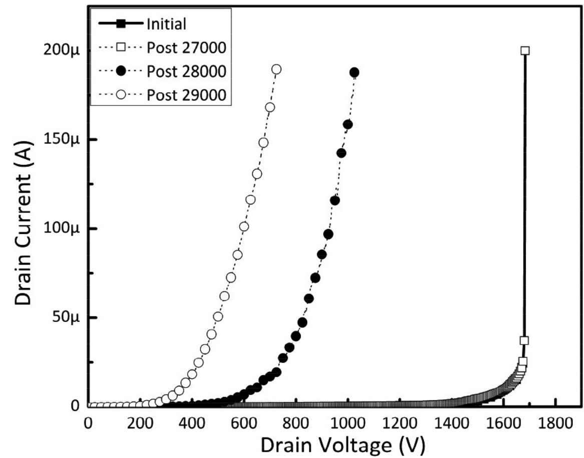

Fig. 4. Blocking voltage curve traces of the SiC MOSFET labeled X2Y5 as measured at four instances during the 29 000 shot test run detailed in Table I. The curve traces demonstrate breakdown voltage degradation during the final 2,000 pulses.

waveform with the TCAD waveform shows a strong similarity between the two, thereby verifying the electrical accuracy of the TCAD model, and supporting the validity of the conclusions drawn from the simulation results about the operation of the physical devices.

As seen in Table I, the device labeled X2Y5 was pulsed 29 000 times with the failure occurring during the 10 Hz operation, and the device labeled X2Y6 was pulsed between 780 000 to 790 000 times with the failure occurring during this 2 Hz interval. Prior to failure, neither device showed signs of degradation to their forward I–V characteristics, $V_{\mathrm{GS(th)}}$, or transconductance. The testing of the device labeled X2Y5 will be described first, the failure mode will be explained and supported with TCAD simulation results, and then the failure of X2Y6 will be discussed.

The SiC MOSFET labeled X2Y5 was pulsed 27 000 times with 5000 pulses performed at each frequency of 1, 2, and 5 Hz, and with 12 000 pulses performed at 10 Hz. These 27 000 pulsed overcurrents were performed without inducing measureable degradation to the device's dc or transient characteristics. However, over the next 2000 cycles performed at 10 Hz, the device's ability to block drain–source voltage rapidly degraded. This breakdown voltage degradation is evident in Fig. 4. It can be seen that the blocking voltage curve trace measured after pulse number 27 000 exactly overlaps the initial blocking voltage curve trace. However, after pulse number 28 000, the breakdown voltage is reduced to 1 kV, followed by a further reduction to 700 V by pulse 29 000. The cause of this degradation is revealed in Figs. 5 and 6 through analysis of the gate current measured during breakdown. Fig. 5 shows the breakdown voltage of X2Y5 measured prior to the degradation, after pulse number 27 000, with the drain and gate current plotted on a semilog scale. It can be seen that the device enters avalanche breakdown, and that the gate current is unaffected by the avalanche phenomena due to the insulating properties of the gate oxide. However, Fig. 6 shows the breakdown voltage of X2Y5 measured after the

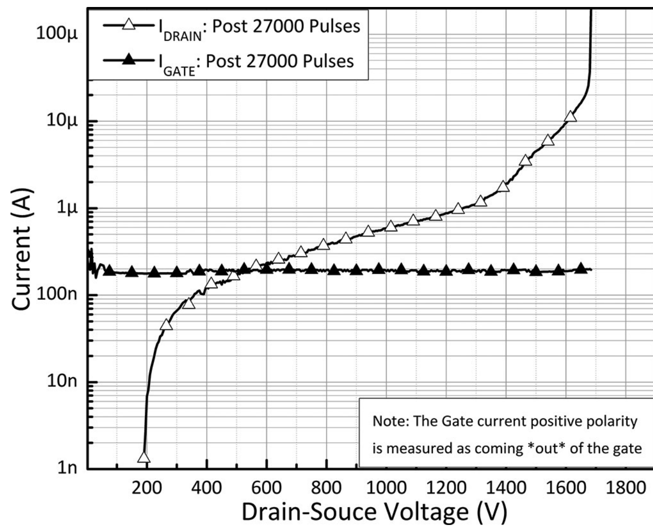

Fig. 5. Blocking voltage curve trace of the SiC MOSFET labeled X2Y5 measured following shot number 27 000 with the drain and gate current plotted on a semilog scale showing no correlation between the gate and drain leakage currents.

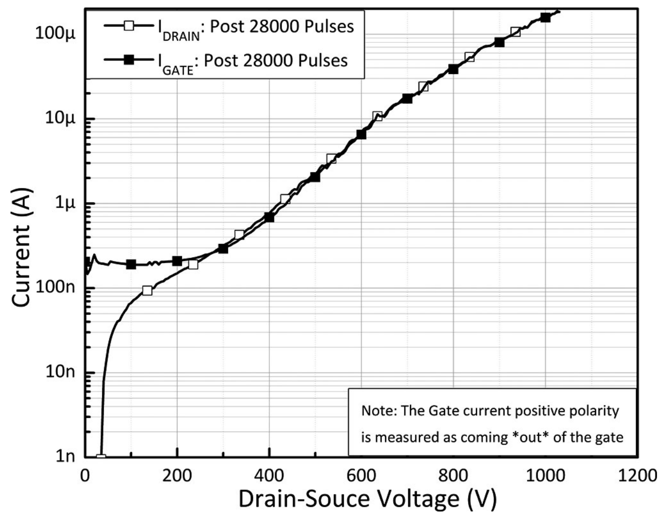

Fig. 6. Blocking voltage curve trace of the SiC MOSFET labeled X2Y5 measured following shot number 28 000 with the drain and gate current plotted on a semilog scale. The coupling of the drain leakage current and gate current indicates the formation of a conductive path through the gate oxide.

initial degradation had occurred, after the 28 000th pulse, with the drain and gate current again plotted on a semilog scale. In this plot, it can be seen that the drain–source junction now fails to block voltage and that the drain current is conducted completely through the gate rather than the source. This drain–gate leakage current indicates that the failure mode for high pulsed overcurrents is the formation of a conductive path through the gate oxide.

The cause of the gate oxide failure is evident through analysis of the device structure and the TCAD simulation results. Specifically, the cause of failure can be seen through the formation of a thermal hot spot and analysis of heat propagation through the device's structure. Fig. 7 shows the formation of the thermal

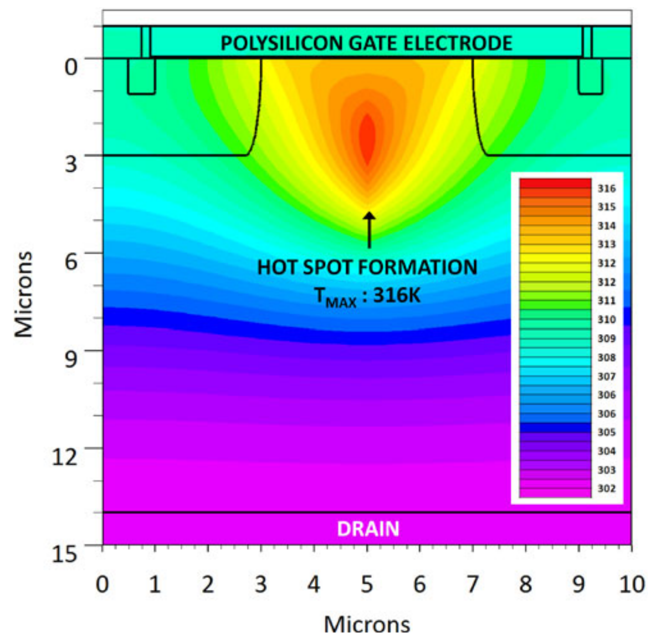

Fig. 7. MOSFET unit cell structure showing thermal hot spot formation at 520 ns into the pulsed overcurrent.

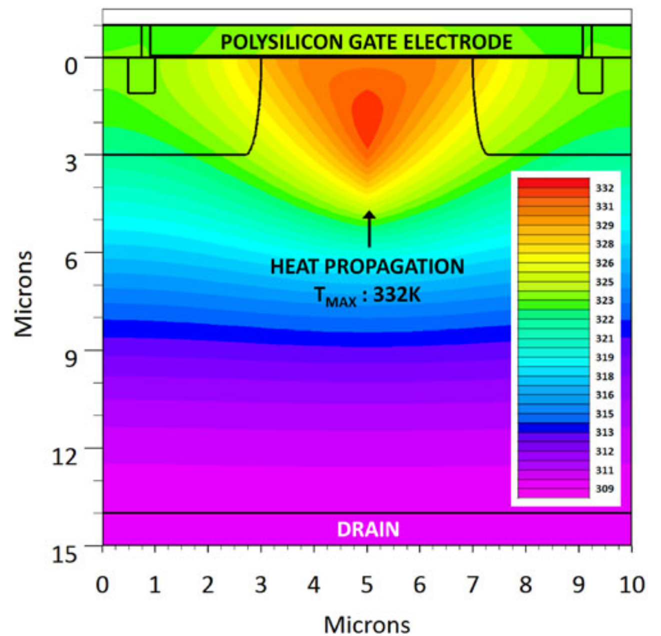

Fig. 8. MOSFET unit cell structure showing heat propagation through the device's structure at 760 ns into the pulsed overcurrent.

hotspot due to the inrush of the high dI/dt current pulse. Prior to device turn-ON, the device is in the blocking phase resulting in the formation of a depletion region at the drain–source junction. During the turn-ON transient, the confinement of high current in the JFET region formed by the depletion layer expansion at the interface of the p-base and drift regions causes extreme high current density resulting in localized high power dissipation and lattice heating. Fig. 8 shows the propagation of the heat through

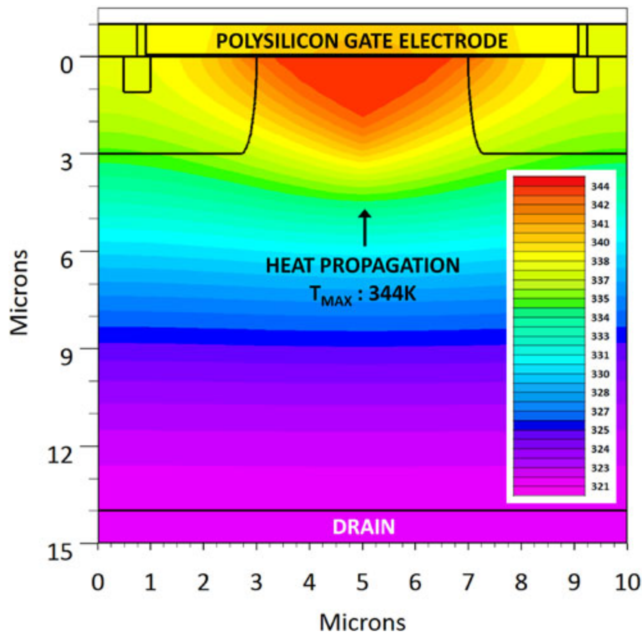

Fig. 9. MOSFET unit cell structure showing heat buildup at the SiC/SiO_2 interface at 1.07 μs into the pulsed overcurrent.

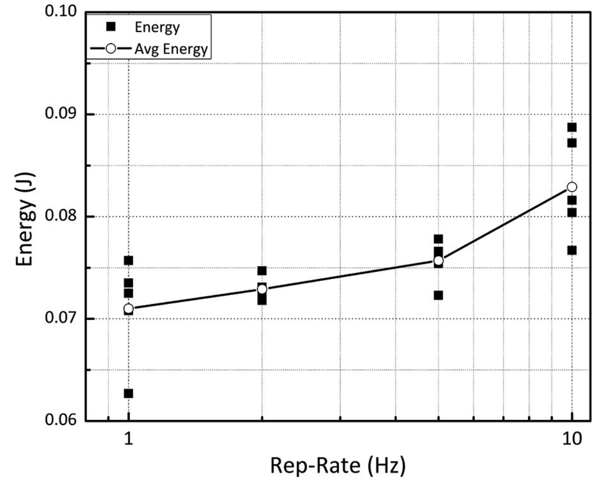

Fig. 10. Energy dissipation per pulse versus rep-rate of the SiC MOSFET labeled X2Y5. The energy dissipation per pulse increases as a function of temperature.

the JFET region and toward the gate oxide. Fig. 9 shows that the heat propagation terminates at the gate oxide, resulting in the concentration of heat at the SiC/SiO_2 interface. Under the repetitive pulsed overcurrent scenario, there is a gradual buildup of heat at the gate oxide, as evident from Figs. 3 and 9. This buildup of heat can result in the formation of a conductive path through the gate oxide, as seen in Fig. 6. The device's long-term ability to withstand the pulsed overcurrents without the formation of a gate oxide conductive path depends upon the repetition rate, pulse width, and peak current, as these factors determine the maximum rise of the gate oxide temperature.

It can be inferred from the data shown in Table I in combination with the experimental and TCAD results that the SiC MOSFETs maintain robust long term reliability under high pulsed overcurrent condition provided there is adequate time between successive pulses to prevent excessive heat buildup at the SiC/SiO_2 interface. This can be concluded because the device labeled X2Y5 failed after 29 000 pulses with 14 000 of those performed at 10 Hz, whereas the device labeled X2Y6 survived greater than three quarters of a million pulses at 2 Hz after only 4000 pulses performed at 10 Hz. The effect of repetition rates on energy deposited per pulse can be observed in Fig. 10. Higher repetition rates result in increased cumulative energy dissipation thereby yielding excessive heat buildup and increasing the likelihood of device failure.

V. Conclusion

Two 1200 V/150 A SiC MOSFETs were electrically stressed with pulsed overcurrent conditions in an *RLC* pulse-ring-down test bed to analyze their failure mode. This letter supplemented previous research that demonstrated their long-term reliability [1]. It was determined that the SiC MOSFET failed rather rapidly after a few thousand overcurrent pulses during 10 Hz operation while surviving over 750 000 overcurrent pulses at 2 Hz operation. Device curve traces indicate that the gate oxide interface was the failure point of the device; the observed failure was the formation of a conductive path through the oxide yielding an inability to block drain–source voltage. It can be concluded from the experimental and simulation results that the failure mode is purely thermal due to the localized heating at the interface between the gate oxide and JFET region. It was observed that there was an increase in the energy dissipation per pulse at higher rep-rates. Therefore, the device would be less prone to failure at low pulse repetition frequency. While it is important to identify and promote awareness of this failure mechanism so that designers may have a better awareness of the safe operating area of these devices, the extreme high current density and high pulse repetition rate required to create this failure mode demonstrate that SiC MOSFETs should offer a robust and power dense alternative to the Si IGBT when subjected to the pulsed overcurrent conditions common in power electronic applications.

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