Design and Analysis of an Adaptively Biased Low-Dropout Regulator Using Enhanced Current Mirror Buffer

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***Abstract*—This paper presents an adaptively biased low-dropout regulator using an enhanced current mirror (ECM) buffer for effectively driving the gate of the PMOS power transistor. The proposed ECM buffer offers very low output impedance, which pushes out the pole at the gate of the PMOS power transistor to improve the stability. At the same time, it offers a symmetric pull-up/down slew rate to enhance the speed of the buffer, whenever the regulator is under large signal operation during the load transient. Moreover, the ECM buffer is modified to develop the regulator topology without introducing an error amplifier as a separate independent stage. It helps to minimize the overall quiescent current consumption at low-load condition and makes frequency compensation easier. Finally, the speed of the adaptive bias loop is increased by avoiding the highly capacitive gate node of the PMOS power transistor. A comprehensive small-signal analysis of the proposed regulator is also carried out for a clear understanding of the stability of each loop considering the interaction of the other loop. The regulator is implemented in a 0.18-μm CMOS technology with a quiescent current of 900 nA. A maximum transient output voltage variation of 2.1% is observed with $C_o = 470$ nF.**

***Index Terms*—Adaptive bias loop (ABL), current mirror, low-dropout regulator (LDR), main feedback loop (MFL), voltage buffer.**

I. Introduction

MULTIPLE voltage sources are required in portable applications to power up different functional blocks [1], [2]. A low-dropout regulator (LDR) provides cleaner output and does not require any bulky inductor compared to a switching converter. The critical performance requirements for any regulator are a fast transient response [3]–[14], maintaining a tight voltage tolerance band that includes overshoot, undershoot upon load switching, and a stable operation over the entire load range [15], [16]. The transient response of the regulator mainly depends on the loop gain bandwidth and the slew rate at the gate of the power transistor [17], [18]. For an externally compensated regulator, both of these requirements demand a higher quiescent current. Therefore, it is a major challenge to achieve the transient specifications with a low quiescent current [19]. Different biasing philosophies like constant biasing [20], [21], dynamic biasing [22], [23], and adaptive biasing [24]–[27] are adopted in various regulator topologies. In constant biasing, the bias current of the regulator is fixed and independent of the load current. In dynamic biasing, the same remains fixed at the steady state, but it increases momentarily to a high value only at the load transient edges. In adaptive biasing, the bias current proportionally varies with the load current. In this case, the increased bias current at high load current expands the loop bandwidth sacrificing a very little amount in the current efficiency. There are many advantages of using adaptive biasing over a dynamic one. First, this scheme provides a better transient response due to the combined effects of bandwidth expansion and slew-rate enhancement. A fast recovery in the settling time is generally observed in the transient response. Second, the internal poles along with the output pole vary with the load current. So, the stability margin is relatively constant throughout the load range. Finally, as it speeds up the transient response, there is a flexibility to minimize the quiescent current at low-load condition. Needless to say, a low quiescent current considerably extends the battery lifetime in portable applications [28].

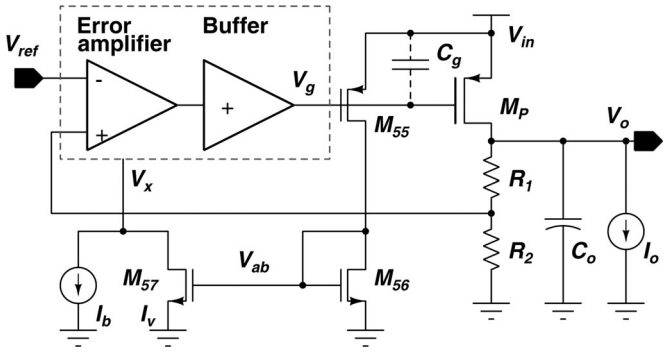

Fig. 1. Conventional AB-LDR architecture.

Fig. 1 shows a typical block diagram of a conventional adaptively biased LDR (AB-LDR) architecture. It consists of an error amplifier, a buffer, and a PMOS power transistor M_P. The adaptive biasing changes the bias current of the error amplifier and the buffer stage when the load current I_o changes and it is done through the path $M_{55} - M_{56} - M_{57}$. In an externally compensated regulator, the dominant pole is generated by the output capacitor C_o. As the PMOS power transistor M_P needs to have a large size to supply the load current demand, it offers a large gate capacitance C_g and creates the first nondominant pole. For stable behavior, it must be placed well above the unity gain frequency (ω_{UGF}) of the regulator loop. The buffer stage, having a low output impedance, is inserted to drive the highly capacitive gate node of M_P. For efficient driving, either an emitter (source) follower or a current mirror buffer is widely used in the

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literature. An emitter follower circuit as proposed in [17] using a costly Bi-CMOS process, has a very low output impedance and it pushes the first nondominant pole of the regulator beyond ω_{UGF}. It is also adaptively biased to reduce the quiescent current consumption at light-load condition. Al-Shyoukh *et al.* [29] proposed an adaptively biased source follower with shunt feedback to reduce the output impedance for expanding the loop bandwidth. An NPN bipolar transistor having a well-controlled current gain, is used as a shunt feedback device and the output impedance is decreased approximately by a factor equal to its current gain. As the shunt feedback is realized in the pull-down path, the gate of M_P discharges quickly during a large load step. However, the pull-up operation is realized by a fixed current source. For low power operation, a small value of current makes the pull-up function weaker. In other words, it requires more bias current to improve the pull-up operation. Also, for stable operation, it requires a compensation capacitor of 10 pF, which needs extra silicon space. Furthermore, the bias current of the error amplifier is fixed in both [17] and [29]. So, the output impedance of the error amplifier does not vary with the load current. Hence, the speed and overall current consumption of the regulator are difficult to optimize. Lam and Ki [25] proposed a fully AB-LDR using a super current mirror (SCM) as a buffer stage in a standard CMOS process. The SCM buffer is developed from an ordinary current mirror (OCM) buffer by introducing a transient enhancing circuit, which allows low-voltage operation. The same is formed by a localized shunt feedback similar to [29]. Here, an NMOS transistor is used as a shunt feedback device. As a result, the impedance of the node V_g is reduced and the bandwidth is enhanced approximately by the loop gain of the shunt feedback compared to the same of the OCM buffer. Hence, the speed of response of the SCM buffer is increased over the OCM buffer. However, due to bandwidth enhancement, the dominant pole of the SCM buffer comes relatively closer to the first nondominant pole and they form a complex pole pair. This creates a gain-peaking and a sharp phase degradation depending on the Q-factor. So, a higher value of output capacitor is required to stabilize the regulator. Moreover, in [17], [25], and [29], the bandwidth of the adaptive bias loop (ABL) is limited by the high gate capacitance of M_P. So, more quiescent current is required to get a faster transient response. Or and Leung[18] used a current mirror buffer to reduce the resistance of the node V_g for an effective improvement of the loop bandwidth. The current mirror buffer is driven by an asymmetric push–pull stage. The pull-down path is controlled by an amplifier stage and provides a high slew rate at V_g during large signal operation. Once again, the pull-up operation is controlled by a constant current source, which is not power efficient. Due to a weak pull-up operation, a high and prolonged overshoot is also observed in the experimental result during high-to-zero load step.

Apart from the architectural limitations, the extensive stability analysis of the AB-LDR topology is not readily available in the literature. The authors in [26] and [30] analyzed the regulation or the main feedback loop (MFL) without considering the effect of the ABL. Therefore, the interaction of the ABL with an MFL at low as well as high frequencies is not thoroughly studied. So, the presently available analytical framework does not give any insight of the effect of the ABL on dc load regulation. Additionally, it also fails to predict the stability of the AB-LDR accurately.

In this paper, we first review the OCM buffer for regulator applications. The OCM buffer has relatively high output resistance and asymmetric slew rate particularly at low bias current. To overcome the aforementioned limitations, an enhanced current mirror (ECM) buffer has been derived from the OCM buffer. The ECM buffer has wider bandwidth at low-load condition and offers a symmetric push–pull operation. Next, using the ECM buffer, an AB-LDR topology has been developed without adding a standalone error amplifier. This helps to minimize the quiescent current consumption in the regulator. Then, the transient response of the proposed regulator is improved by eliminating the highly capacitive gate node of the power transistor from the ABL. Finally, an accurate small-signal analysis of each loop is provided to demonstrate the interaction with the other loop which gives a complete understanding of the stability of both the loops in the AB-LDR. It also helps to understand the fact, how ABL helps to improve the dc load regulation.

This paper is organized as follows. Section II presents the development of the ECM buffer from an OCM buffer. The proposed regulator topology using the ECM buffer is discussed in Section III. The detailed stability analysis of the proposed regulator is given in Section IV. Finally, Sections V and VI provide the experimental results and the conclusions, respectively.

II. Development of ECM Buffer

An OCM buffer reported in [31] is shown in Fig. 2(a). A diode-connected transistor M_{50} drives M_P and their width ratio is $1:M$, where M is a large integer. So, M_{50} and M_P form a current mirror. The input transistor, M_{51} converts the input voltage V_{buf} to the current I_{50} which flows through M_{50}. To satisfy the dc current balancing, a relation $I_o = M \cdot I_{50}$ has to be maintained.

Whenever I_o varies (which is quite likely for a regulator application), the dc potential of V_{buf} should vary. Due to the diode connection, the small-signal output impedance of M_{50} is approximately equal to $(1/g_{m,50})$ as $r_{o,51} << 1/g_{m,50}$ and it effectively drives the highly capacitive node V_g. The small-signal voltage and current gains of the OCM buffer are given as follows:

$$A_{v,\mathrm{OCM}}(s) = \frac{\Delta V_g}{\Delta V_{\mathrm{buf}}} = -\frac{g_{m,51}}{\left(r_{o,51} \parallel \frac{1}{g_{m,50}}\right)^{-1} + sC_g} \approx -\frac{g_{m,51}}{g_{m,50}\left(1 + s\frac{C_g}{g_{m,50}}\right)} \quad (1)$$

$$A_{i,\mathrm{OCM}}(s) = \frac{\Delta I_o}{\Delta I_{50}} = \frac{g_{m,p}}{\left(r_{o,51} \parallel \frac{1}{g_{m,50}}\right)^{-1} + sC_g} \approx \frac{g_{m,p}}{g_{m,50}\left(1 + s\frac{C_g}{g_{m,50}}\right)}. \quad (2)$$

Both the voltage and current gain equations have a pole at a frequency of $\omega_{\mathrm{3dB,OCM}} = -g_{m,50}/C_g$. Depending on the magnitude of I_o, $g_{m,50}$ changes its magnitude. For moderate-to-high magnitude of I_o, M_{50} operates in the above-threshold ($V_{gs,50} \geq V_{\mathrm{th}}$) region, whereas for a smaller value of I_o, it enters

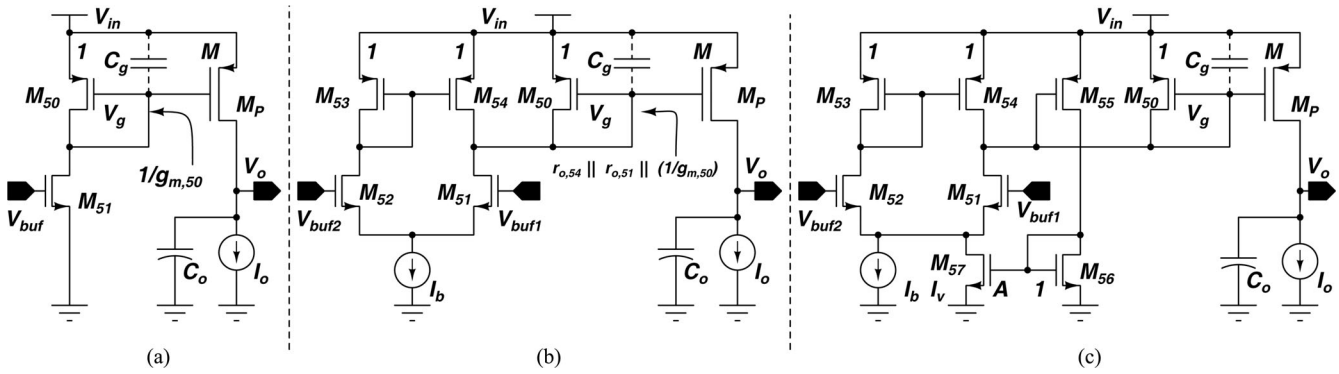

Fig. 2. (a) OCM buffer. (b) Basic structure of the proposed ECM buffer. (c) Adaptively biased ECM buffer.

in the subthreshold ($V_{gs,50} < V_{th}$) region. The corresponding trans-conductances in these two regions vary as follows: $g_{m,50}|_{(V_{gs,50} \geq V_{th})} \propto \sqrt{I_{50}}$ and $g_{m,50}|_{(V_{gs,50} < V_{th})} \propto I_{50}$.

In the above-threshold region, as the magnitude of I_{50} is relatively high, $1/g_{m,50}$ is quite low and this pushes $\omega_{3\text{dB,OCM}}$ to a higher frequency. Additionally, the slew rate at the gate of M_P is also high and it depends on the magnitude of I_{50}, which is directly correlated with I_o. However, for a lower value of I_o, $M_{50,51}$ carries a very small current and the impedance at the node V_g ($\approx 1/g_{m,50}$) increases exponentially. This not only pushes $\omega_{3\text{dB,OCM}}$ to a lower frequency, it also limits the slew rate at light-load condition. What is more, in the pull-up slewing mode when the node voltage V_g should rise, there is no active pull-up path. As M_{50} is in the verge of "OFF" condition, the node voltage V_g takes much longer time to settle. The higher the node voltage V_g, so also is the time constant $C_g/g_{m,50}$. Therefore, an exponential settling behavior results in a large overshoot at V_o for a large current step.

To avoid the aforementioned limitations, an ECM buffer has been proposed in Fig. 2(b). A pull-up path consisting of $M_{52} - M_{53} - M_{54}$ has been added in the modified circuit. Here, V_{buf1} and V_{buf2} are two out of phase signals. Since, the difference current of M_{51} and M_{52} flows through the transistor M_{50}, the dc bias current requirement of M_{51} and M_{52} should be much higher than that of M_{50}. Unlike the OCM buffer, the current through M_{51} (also M_{52}) is not equal to the current through M_{50} here, and hence, it is not a direct function of I_o. Rather, $M_{51,52}$ are biased with a current I_b, where $I_b > I_{50}$. The small-signal voltage created at the output of the buffer is given by

$$\Delta V_g = -\frac{g_{m,51}\Delta V_{\text{buf1}} + g_{m,52}\Delta V_{\text{buf2}}}{\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)^{-1} + sC_g}. \tag{3}$$

As M_{51} and M_{52} form a matched pair, it implies $g_{m,51} = g_{m,52}$. If $\Delta V_{\text{buf1}} = \Delta V_{\text{buf2}} = \Delta V_{\text{buf}}/2$, then the small-signal voltage gain of the circuit simplifies as

$$\begin{aligned} A_{v,\text{ECM}}(s) &= \frac{\Delta V_g}{\Delta V_{\text{buf}}} \\ &= -\frac{g_{m,51}}{\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)^{-1} + sC_g}. \end{aligned} \tag{4}$$

The output resistance of the node V_g in this case is $(r_{o,51} \parallel r_{o,54} \parallel 1/g_{m,50})$. Considering, $1/g_{m,50} \propto 1/I_o$, it increases exponentially with the decrease of load current. Now, as $I_b > I_{50}$ and the value of I_b is such that at low-load condition $(r_{o,51} \parallel r_{o,54}) << 1/g_{m,50}$, then the overall impedance of the node V_g no longer depends on $1/g_{m,50}$. Rather, it is more dominated by $(r_{o,51} \parallel r_{o,54})$. This expands the bandwidth of the ECM relative to the OCM at low-load condition. The small-signal current gain of the ECM buffer is given as follows:

$$\begin{aligned} A_{i,\text{ECM}}(s) &= \frac{\Delta I_o}{\Delta(I_{51} - I_{52})} \\ &= \frac{g_{m,p}}{\left(r_{o,51} \parallel r_{o.54} \parallel \frac{1}{g_{m,50}}\right)^{-1} + sC_g}. \end{aligned} \tag{5}$$

The working principle of the ECM buffer is based on the current generated by an artificial offset between the V_{buf1} and V_{buf2} to meet the load demand I_o. Once the value of I_o increases, the transistor M_{50} also needs to carry more current as the value of M is fixed. So, more artificial offset is required to generate extra current through M_{50}. In the worst case, as the value of I_b is fixed for lower load condition keeping the requirement of low quiescent current, its value may be insufficient at high-load condition. Therefore, the bias current needs to be increased according to the value of load current I_o. This is achieved by an adaptive biasing technique, which senses I_o and changes the bias current accordingly. As a result, the adaptive biasing minimizes the amount of the artificial offset even for a wider load current range. Fig. 2(c) shows the schematic of the adaptively biased ECM buffer. The path consisting of $M_{55} - M_{56} - M_{57}$ changes the bias current $I_v = f(I_o) = A \cdot I_o/M$, where $A = W_{57}/W_{56}$. For higher load condition, as more current flows through M_{50}, it makes $(r_{o,51} \parallel r_{o,54}) \gg 1/g_{m,50}$. As a result, the node impedance of V_g is dominated by $1/g_{m,50}$, which is similar to the OCM buffer. So, both OCM and ECM buffers have similar small-signal response at high-load condition.

Fig. 3 shows the comparison of the small-signal current gains of the OCM and ECM buffers at $I_o = 100\ \mu$A. As the ratio, M is chosen as 1800, the value of dc current gain is approximately 65 dB. The phase starts from 180° due to the non-inverting characteristics of the current gain. At light load, the ECM buffer has a unity gain bandwidth of 175 MHz, whereas for the OCM buffer, its value is 49 MHz as shown in 3. In summary, the bandwidth of the ECM buffer is enhanced at the low-load condition compared to the OCM buffer. Importantly, there is no gain peaking

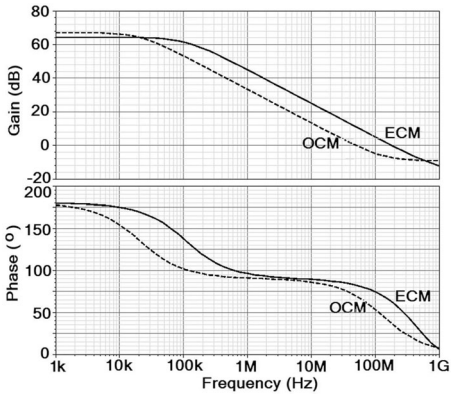

Fig. 3. Comparison of the current gains of the OCM and ECM buffers at $I_o = 100\ \mu$A.

TABLE I
COMPARISON OF THE SLEW RATE BETWEEN OCM AND ECM BUFFERS

Load Condition	SR	OCM	ECM
Low	SR_+	–	I_b/C_g
Low	SR_-	I_o/MC_g	I_b/C_g
High	SR_+	–	I_v/C_g
High	SR_-	I_o/MC_g	I_v/C_g

in the frequency response as it appears in the SCM buffer used in [25] due to the complex pole pair. This helps to stabilize the regulation loop even with a smaller value of output capacitor. The impact on slew rate of the buffer is discussed next.

For the adaptively biased ECM buffer, the total bias current at a particular load condition is, therefore, $(I_b + I_v)$. The slewing mode occurs under large-signal transients and the node V_g charges/discharges at a rate that is decided by the values of C_g and $(I_b + I_v)$. When V_g charges in the slewing mode, M_{51} is completely "OFF." In this condition, the total bias current pulls V_g up through the $M_{52} - M_{53} - M_{54}$ path. Similarly, when the V_g node discharges, M_{51} is "ON" and the path $M_{52} - M_{53} - M_{54}$ is "OFF." As $I_{50} \ll (I_b + I_v)$, both the slew rates are given by

$$\mathrm{SR}_{+/-} = \frac{I_b + I_v}{C_g}. \tag{6}$$

Table I summarizes the comparison of the slew rate between OCM and ECM buffers at two extreme load conditions. The major advantage of the ECM buffer over OCM one is that it provides both the pull-up/down ($SR_{+/-}$) slewing, whereas the OCM buffer only gives pull-down (SR_-) slewing. Further, the value of SR_- at low-load condition is higher for the ECM buffer compared to OCM as $I_b > (I_o/M)$. It should be noted that, if I_{50} is chosen to be more than I_o/M to match with I_b, it provides more dc offset at V_o as M is fixed. Similarly, the requirement of higher value of I_v in the ECM makes the SR_- at high-load condition faster compared to the same in OCM. In summary, the bandwidth as well as the slew rate of ECM buffer are much higher than those of an OCM.

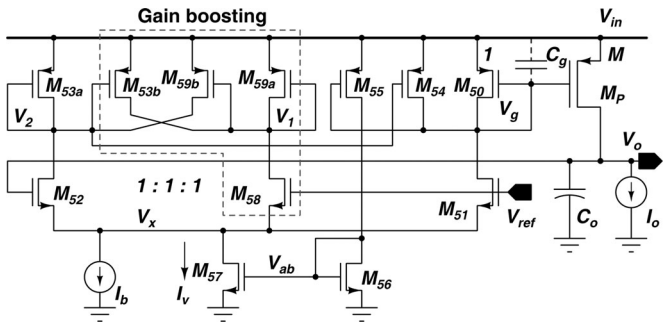

Fig. 4. Schematic of the regulator topology derived from the ECM buffer.

III. PROPOSED REGULATOR TOPOLOGY

In this section, the regulator topology is first developed using the ECM buffer. Like any regulator design, the main objectives here are to minimize the quiescent current consumption and speed up the transient response.

A. Development of the Regulator Topology

As shown in Fig. 1, the error amplifier is preceded by the buffer in the externally compensated regulator architecture. The error amplifier has a high dc gain to obtain a good load regulation. It is a separate stage altogether. However, adding more number of stages consumes higher quiescent current and introduces more nondominant poles, which may lead to instability if the regulator is not properly compensated. As the structure of the ECM buffer is a differential amplifier followed by the current mirror, the former one may be considered as an error amplifier of the regulator. Here, we consider a unity mode configuration of regulator with a feedback factor of 1. This does not create much difference while developing and designing the regulator topology. So, the gates of M_{52} and M_{51} should be connected to the nodes V_o and V_{ref}, respectively. If the error voltage is $\Delta V_e (= \Delta V_{\mathrm{ref}} - \Delta V_o)$, then the voltage gain of the MFL is given by

$$A_{v1}(s) = \frac{\Delta V_o}{\Delta V_e} = -\frac{g_{m,51} g_{m,p} r_o}{\left[\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)^{-1} + sC_g\right](1 + sC_o r_o)}. \tag{7}$$

Due to the diode connection of M_{53} and M_{50} as in Fig. 2(c), the dc gain is very low. Only the power stage provides a gain of $g_{m,p} r_o$, as its size is quite large. Therefore, the overall dc gain of the ECM buffer alone is insufficient for achieving a good dc load regulation.

To increase the dc gain of the loop, the transistors $M_{58} - M_{59a} - M_{59b}$ have been added as a gain boosting stage [32], [33] in the ECM buffer and the transistor M_{53} has been split into M_{53a} and M_{53b}. The detailed circuit topology is shown in Fig. 4. The sizing ratio of $M_{53a} : M_{53b}$, $M_{59a} : M_{59b}$ are $1 : \beta$, where $\beta < 1$ for amplifier operation [34]. The first stage provides differential output voltages V_1, V_2 and its gain is boosted by applying negative impedance at V_1 and V_2. The transistors

M_{53b} and M_{59b} provide the negative impedance at the nodes V_1 and V_2, respectively. The second stage is the ECM buffer consisting of $M_{50} - M_{51} - M_{54}$, which does not provide much gain. The power transistor acts as a third stage, which provides a reasonable gain due to its bigger size.

It should be noted that, the addition of the input transistor M_{58} in the common-mode node V_x requires 1.5 times the bias current (both in the values of I_b and I_v) than that of the ECM buffer. However, if the error amplifier needs to be realized separately, it would require a bias current approximately twice that of the ECM buffer, assuming that they consume almost the same bias current.

The tail current of the regulator has two components; one is the fixed current I_b and the other one is variable source I_v whose value changes adaptively according to I_o. The load current is sensed by the transistor M_{55}. The current through M_{55} is scaled down by a factor $1/M$ to reduce the quiescent current consumption of the regulator. The ratio between the transistors M_{56} and M_{57} is $1 : A$. Therefore, the adaptive biasing ratio is defined by $I_v : I_o$, which is $N_{AB} = (A/M)$. There are two different loops, i.e., MFL and ABL, respectively. The MFL is connected in unity feedback mode and it consists of the loop $V_o - V_2 - V_g - V_o$. On the other hand, the ABL consists of the loop $V_{ab} - V_x - V_1(V_2) - V_g - V_{ab}$. The stability analysis of each of the loops is investigated in the next section considering the effect of the other loop. Here, to understand the effect of the gain boosting circuit alone, the small-signal transfer function of the MFL ignoring the small-signal perturbation from the ABL under the condition $\beta < 1$ which is given in (8) at the bottom of the page. Due to the gain boosting circuit, the overall dc gain is increased by a factor of $(1 + \beta)/(1 - \beta)$. A higher value of β ($\beta < 1$) increases the dc gain of the regulator and expands the bandwidth of the loop. So, the dc regulation and the speed of the transient response improve. Importantly, as β is the width ratio of two transistors, these improvements are process, voltage, and temperature insensitive.

B. Slew-Rate Enhancement

In the AB-LDR, the dc operating point of the circuit changes with the load current. The speed of the transient response from the regulator not only depends on ω_{UGF} of the MFL, but also on the frequency response of the ABL. The ABL first senses the error voltage ΔV_e from the error amplifier and converts it to the tail current. The dc transconductance of the ABL decides the accuracy of the tail current across the range of load current. The ac (or high frequency) transconductance decides the speed of the change in the dc operating point. So, it is important to derive the transconductance of the ABL, which is given in (9) at the bottom of the page. The gain boosting circuit also improves the transconductance of the ABL. Equation (9) shows that the dominant pole is created from the node V_g and it is located at $1/C_g(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}})$. As the value of C_g is high for a power transistor, it slows down the speed of the ABL.

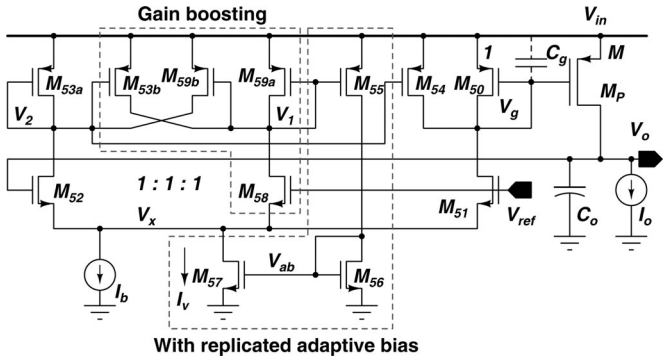

Fig. 5. Proposed regulator topology with replicated adaptive biasing.

To avoid the aforementioned limitation, a replica bias concept is applied in the ABL. The modified topology is shown in Fig. 5. Here, we introduce two notations; WOR-ABL and WR-ABL are for without replicated ABL and with replicated ABL as shown in Figs. 4 and 5, respectively. The dc gain from V_1 to V_g is equal to $g_{m,54}/g_{m,50}$ and it is made unity by choosing the sizes of M_{54} and M_{50} to be equal. In such a condition, the node voltage V_1 is an exact replica of V_g. If the gate of M_{55} is changed to V_1 instead of V_g, it bypasses the pole $1/C_g(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}})$. Essentially, this alters the ac transconductance of the loop and increases the speed of the same. Therefore, the overall load transient response of the regulator is improved. The modified transconductance of the case WR-ABL which is given in (10) at the bottom of the page.

IV. Stability Analysis of the Proposed Regulator

A. Development of a Unified Small-Signal Model and Its Block Level Equivalent

A unified small-signal model of the proposed regulator for the cases WOR-ABL and WR-ABL has been developed here

$$A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}} = -\frac{(1+\beta)g_{m,54}g_{m,52}g_{m,p}r_o\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)}{(1-\beta)g_{m,53}(1+sr_oC_o)\left\{1+sC_g\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)\right\}\left\{1+s\frac{(1+\beta)C_2}{(1-\beta)g_{m,53}}\right\}} \tag{8}$$

$$G_{m,\text{WOR-ABL}}(s) = \frac{\Delta I_v}{\Delta V_e} = -\frac{A(1+\beta)g_{m,51}g_{m,55}\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)}{(1-\beta)g_{m,53}\left\{1+sC_g\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)\right\}\left\{1+s\frac{(1+\beta)C_2}{(1-\beta)g_{m,53}}\right\}} \tag{9}$$

$$G_{m,\text{WR-ABL}}(s) = \frac{\Delta I_v}{\Delta V_e} = -\frac{A(1+\beta)g_{m,51}g_{m,55}\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)}{(1-\beta)g_{m,53}\left\{1+s\frac{(1+\beta)C_2}{(1-\beta)g_{m,53}}\right\}} \tag{10}$$

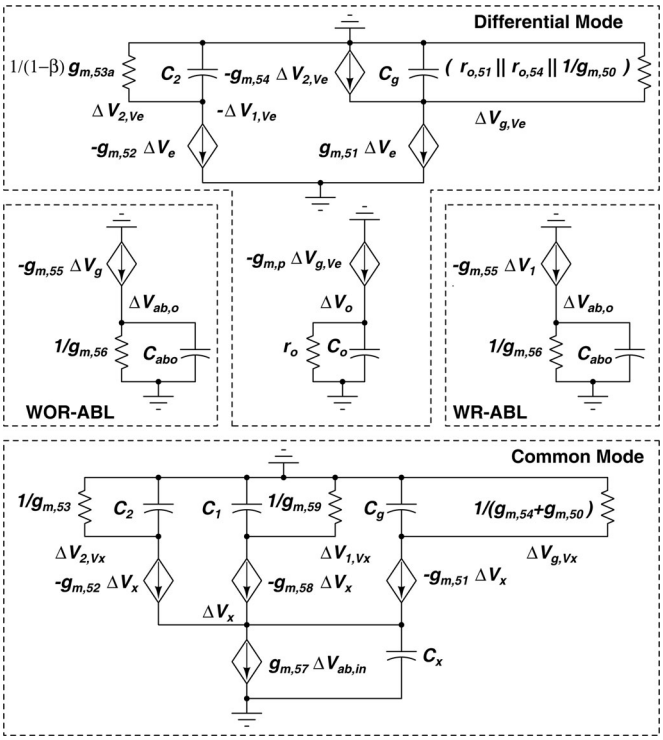

Fig. 6. Small-signal model of the proposed regulator for the cases WOR-ABL and WR-ABL.

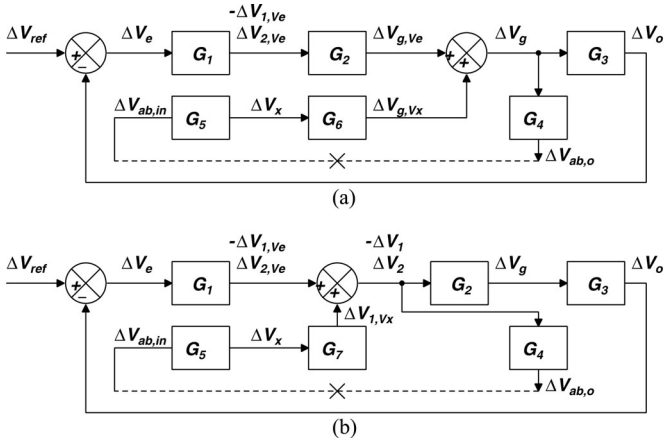

Fig. 7. Block diagram of the system for the cases (a) WOR-ABL and (b) WR-ABL.

to analyze the stability of the MFL and ABL. The small-signal model is shown in Fig. 6. Here, the two loops have been broken at two points. The MFL and ABL are broken at the gate of the transistor M_{52} and M_{57}, respectively. The small-signal perturbations are applied in the MFL and ABL, which are denoted as $\Delta V_e (= \Delta V_{\rm ref} - \Delta V_o)$ and $\Delta V_{ab,{\rm in}}$, respectively. The MFL operates in the differential mode, whereas the common-mode perturbation propagates through the ABL. The output resistance of the nodes V_1, V_2, and V_g are different in these two modes. In the differential mode of operation, the resistances seen at V_1 and V_2 are equal as $1/(1-\beta)g_{m,53a} = 1/(1-\beta)g_{m,59a}$, and at V_g, the same is $(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}})$. On the other hand, the resistances seen from the common-mode perturbation ΔV_x in the common-mode operation are $1/(g_{m,53a} + g_{m,53b}) = 1/g_{m,53}$ and $1/(g_{m,59a} + g_{m,59b}) = 1/g_{m,59}$ at V_1 and V_2, respectively. Due to perfect symmetry, $g_{m,53} = g_{m,59}$. The resistance seen at V_g is equal to $1/(g_{m,50} + g_{m,54})$.

As the resistances differ in differential and common mode of operation, the small-signal models in those two modes are different as shown in Fig. 6. The small-signal perturbation at V_1, V_2, and V_g due to ΔV_e are denoted as $\Delta V_{1,Ve}$, $\Delta V_{2,Ve}$, and $\Delta V_{g,Ve}$. Similarly, for ΔV_x, the same are $\Delta V_{1,Vx}$, $\Delta V_{2,Vx}$, and $\Delta V_{g,Vx}$, respectively. A voltage superposition is applied to analyze one loop while considering the effect of the other loop. This implies $\Delta V_1 = (\Delta V_{1,Ve} + \Delta V_{1,Vx})$, $\Delta V_2 = (\Delta V_{2,Ve} + \Delta V_{2,Vx})$, and $\Delta V_g = (\Delta V_{g,Ve} + \Delta V_{g,Vx})$. Therefore, the equivalent block diagrams of the system for the cases WOR-ABL and WR-ABL are shown in Fig. 7. Assuming $g_{m,51} = g_{m,52} = g_{m,58}$, $C_1 = C_2$, and $g_{m,53} = g_{m,59}$, the transfer functions of various blocks are given as follows:

$$G_1 = -\frac{(1+\beta)g_{m,52}}{(1-\beta)g_{m,53}\left\{1 + s\frac{(1+\beta)C_2}{(1-\beta)g_{m,53}}\right\}} \tag{11}$$

$$G_2 = -\frac{g_{m,54}\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)}{g_{m,50}\left\{1 + sC_g\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)\right\}} \tag{12}$$

$$G_3 = -\frac{g_{m,p}r_o}{(1 + sr_oC_o)} \tag{13}$$

$$G_4 = -\frac{g_{m,55}}{g_{m,56}\left\{1 + s\frac{C_{ab,o}}{g_{m,56}}\right\}} \tag{14}$$

$$G_5 = -\frac{g_{m,57}}{3g_{m,52}\left\{1 + s\frac{C_x}{3g_{m,52}}\right\}} \tag{15}$$

$$G_6 = \frac{g_{m,52}}{(g_{m,50} + g_{m,54})\left\{1 + s\frac{C_g}{(g_{m,50}+g_{m,54})}\right\}} \tag{16}$$

$$G_7 = \frac{g_{m,52}}{g_{m,53}\left\{1 + s\frac{C_2}{g_{m,53}}\right\}}. \tag{17}$$

To analyze an MFL without considering the interaction of the ABL, one should simply assume $\Delta V_{ab,{\rm in}} = 0$. Similarly, the transfer function of the ABL may be derived assuming $\Delta V_e = 0$, once the effect of an MFL is ignored. On the other hand, to understand the effect of the interaction of the other loop, one has to close the other loop. For example, the transfer function of the MFL with the interaction of the ABL should be derived by assuming $\Delta V_{ab,{\rm in}} = \Delta V_{ab,o} = \Delta V_{ab}$. Similarly, the interaction of the MFL on ABL is considered by assuming $\Delta V_e = \Delta V_o$ for $\Delta V_{\rm ref}$ =0.

As given before in (8), $A_{v,{\rm MFL}}(s)|_{\rm ABL,O}$ $(=G_1G_2G_3)$ represents the small-signal transfer function of the MFL without considering the effect of the ABL. Similarly, the transfer functions of the ABL without considering the effect of an MFL for the cases WOR-ABL and WR-ABL are denoted as $A_{v,{\rm WOR\text{-}ABL}}(s)|_{\rm MFL,O}$ and $A_{v,{\rm WR\text{-}ABL}}(s)|_{\rm MFL,O}$, which are

given as follows:

$$A_{v,\text{WOR-ABL}}(s)|_{\text{MFL,O}} = G_4G_5G_6 \quad (18)$$

$$A_{v,\text{WR-ABL}}(s)|_{\text{MFL,O}} = G_4G_5G_7. \quad (19)$$

The noninverting polarity of the factors $G_4G_5G_6$ and $G_4G_5G_7$ suggest that, the feedback is positive. If $g_{m,53} = (g_{m,54} + g_{m,50})$, the dc gains in both (18) and (19) are the same. However, their high frequency characteristics are different. As $C_g \gg C_2$, the dominant pole of the case WOR-ABL is placed at a much lower frequency than the same of WR-ABL. The other poles are present relatively at very high frequency. Thus, the speed of WR-ABL is much faster than the same in WOR-ABL. Now, the implication of the ABL on the stability of the MFL is discussed next.

Once the effect of the ABL is considered on the MFL, $A_{v,\text{MFL}}(s)|_{\text{WOR-ABL,C}}$ and $A_{v,\text{MFL}}(s)|_{\text{WR-ABL,C}}$ represent the transfer functions of the MFL for the cases WOR-ABL and WR-ABL, respectively, as given in (20) and (21) after combining with (8), (18), and (19)

$$A_{v,\text{MFL}}(s)|_{\text{WOR-ABL,C}} = \frac{G_1G_2G_3}{1 - G_4G_5G_6} = \frac{A_{v,\text{MFL}}(s)|_{\text{ABL,O}}}{1 - A_{v,\text{WOR-ABL}}(s)|_{\text{MFL,O}}} \quad (20)$$

$$A_{v,\text{MFL}}(s)|_{\text{WR-ABL,C}} = \frac{G_1G_2G_3}{1 - G_4G_5G_7} = \frac{A_{v,\text{MFL}}(s)|_{\text{ABL,O}}}{1 - A_{v,\text{WR-ABL}}(s)|_{\text{MFL,O}}}. \quad (21)$$

At a very low frequency, as $A_{v,\text{WOR-ABL}}(0)|_{\text{MFL,O}}$ and $A_{v,\text{WR-ABL}}(0)|_{\text{MFL,O}}$ are equal, the dc gains in (20) and (21) get affected equally in the cases WOR-ABL and WR-ABL. Moreover, to keep the overall feedback of the MFL negative, the dc gains $A_{v,\text{WOR-ABL}}(0)|_{\text{MFL,O}}$ and $A_{v,\text{WR-ABL}}(0)|_{\text{MFL,O}}$ should be less than unity, which gives as follows in (18) and (19)

$$A_{v,\text{WOR-ABL}}(0)|_{\text{MFL,O}} = \frac{g_{m,57}g_{m,55}}{3g_{m,56}(g_{m,54} + g_{m,50})} < 1 \quad (22)$$

$$A_{v,\text{WR-ABL}}(0)|_{\text{MFL,O}} = \frac{g_{m,57}g_{m,55}}{3g_{m,56}g_{m,53}} < 1. \quad (23)$$

In the present design, the different values are chosen as $g_{m,57}/g_{m,56}$ =2.5, $g_{m,55} = (g_{m,50} + g_{m,54})$ and $g_{m,55} = g_{m,54}$. The dc gain in (22) and (23) are chosen as 0.83, which is lower than unity.

B. *Stability of* MFL *at Low-Load Condition*

If $A_{v,\text{WOR-ABL}}(0)|_{\text{MFL,O}}$ and $A_{v,\text{WR-ABL}}(0)|_{\text{MFL,O}}$ have a very low dc gain (high dc attenuation $\ll 1$), then they have a very minimal affect on the MFL. This condition arises at very low-load condition where the ABL is not necessarily be so effective. In that condition, the dc gain of the MFL remains unaltered and this leads to $A_{v,\text{MFL}}(0)|_{\text{WOR-ABL,C}} = A_{v,\text{MFL}}(0)|_{\text{WR-ABL,C}} = A_{v,\text{MFL}}(0)|_{\text{ABL,O}}$. The high frequency characteristic also remains least affected by the ABL. For an externally compensated regulator, the dominant and first nondominant poles are created at $1/r_oC_o$ and $1/C_g\left(r_{o,51} \parallel r_{o,54} \parallel \frac{1}{g_{m,50}}\right)$. As the gain boosting technique at the first stage increases the impedance of the node V_2, the second nondominant pole located at $(1-\beta)g_{m,53}/(1+\beta)C_2$ approaches toward the unity gain frequency ω_{UGF} from a very high frequency. At ω_{UGF}, the phase should not be affected by the second nondominant pole. This creates a practical limitation of choosing the values of β.

C. *Stability of* MFL *at High-Load Condition*

As the load current increases, the ABL becomes more and more effective to meet the demand of the high load current. So, the amount of dc attenuation $A_{v,\text{WOR-ABL}}(0)|_{\text{MFL,O}}$ and $A_{v,\text{WR-ABL}}(0)|_{\text{MFL,O}}$ decreases with load current. If their values are becoming comparable to unity, the ABL starts interacting with an MFL. When $A_{v,\text{WOR-ABL}}(0)|_{\text{MFL,O}}$ and $A_{v,\text{WR-ABL}}(0)|_{\text{MFL,O}}$ are closer to unity, the dc gains of $A_{v,\text{MFL}}(s)|_{\text{WOR-ABL,C}}$ and $A_{v,\text{MFL}}(s)|_{\text{WR-ABL,C}}$ are increased according to (20) and (21). As $A_{v,\text{WOR-ABL}}(0)|_{\text{MFL,O}} = A_{v,\text{WR-ABL}}(0)|_{\text{MFL,O}}$, the respective dc gain improvements of $A_{v,\text{MFL}}(0)|_{\text{WOR-ABL,C}}$ and $A_{v,\text{MFL}}(0)|_{\text{WR-ABL,C}}$ are same. Due to the interaction of the ABL, the magnitudes of ω_{UGF} of the transfer functions in (20) and (21) are also likely to increase compared to the same of $A_{v,\text{MFL}}(s)|_{\text{ABL,O}}$. So, the stability at the high-load condition needs to be guaranteed for the transfer functions of the MFL considering the effect of an ABL. It may be noted that, their high frequency characteristics differ due to the presence of a low frequency dominant pole in $A_{v,\text{WOR-ABL}}(s)|_{\text{MFL,O}}$ as in (18). Moreover, it is located near the first nondominant pole of $A_{v,\text{MFL}}(s)|_{\text{ABL,O}}$. Thus, the denominator term $\{1 - A_{v,\text{WOR-ABL}}(s)|_{\text{MFL,O}}\}$ in (20) introduces a pole and zero pair, which are approximately located at $(1 - A_{v,\text{WOR-ABL}}(0)|_{\text{MFL,O}})(g_{m,54} + g_{m,50})/C_g$ and $(g_{m,54} + g_{m,50})/C_g$, respectively. As that pole is likely to be located before ω_{UGF} of $A_{v,\text{MFL}}(s)|_{\text{WOR-ABL,C}}$, it reduces the magnitude of ω_{UGF} as well as the phase margin. So, the stability of $A_{v,\text{MFL}}(s)|_{\text{WOR-ABL,C}}$ may worsen. On the other hand, in WR-ABL, the dominant pole of $A_{v,\text{WR-ABL}}(s)|_{\text{MFL,O}}$ is placed much higher than ω_{UGF}. As a result, the denominator term $(1 - A_{v,\text{WR-ABL}}(s)|_{\text{MFL,O}})$ does not significantly interact with an MFL near ω_{UGF}.

Fig. 8 shows the gain and phase plots of various transfer functions for both the cases at $I_o = 50$ mA with $C_o = 470$ nF. A low ESR ceramic capacitor is chosen to achieve a tight output voltage tolerance during the load transient. In simulation, we choose the value of the ESR equal to zero. Hence, the stability of the regulator is ensured without relying on the ESR zero compensation. At low frequency, the dc gain of MFL boosts from 37 to 52.4 dB due to the dc attenuation of 1.66 dB from the ABL. In Fig. 8(a), the $f_{\text{UGF}} = \omega_{\text{UGF}}/2\pi$ is not expanded in proportionate amount for the case WOR-ABL due to the interaction of ABL near that frequency. An additional pole-zero pair is created before f_{UGF}, which also creates an additional phase lag as the left half plane (LHP) pole comes first before the LHP zero. In this case, $A_{v,\text{MFL}}(s)|_{\text{WOR-ABL,C}}$ has an $f_{\text{UGF}} = 2.8$ MHz with a phase margin of 33°. In the case WR-ABL, $A_{v,\text{WR-ABL}}(s)|_{\text{MFL,O}}$ has dominant pole at very high frequency. So, the interaction with $A_{v,\text{MFL}}(s)|_{\text{ABL,O}}$ near f_{UGF} is much less. Therefore, f_{UGF} is

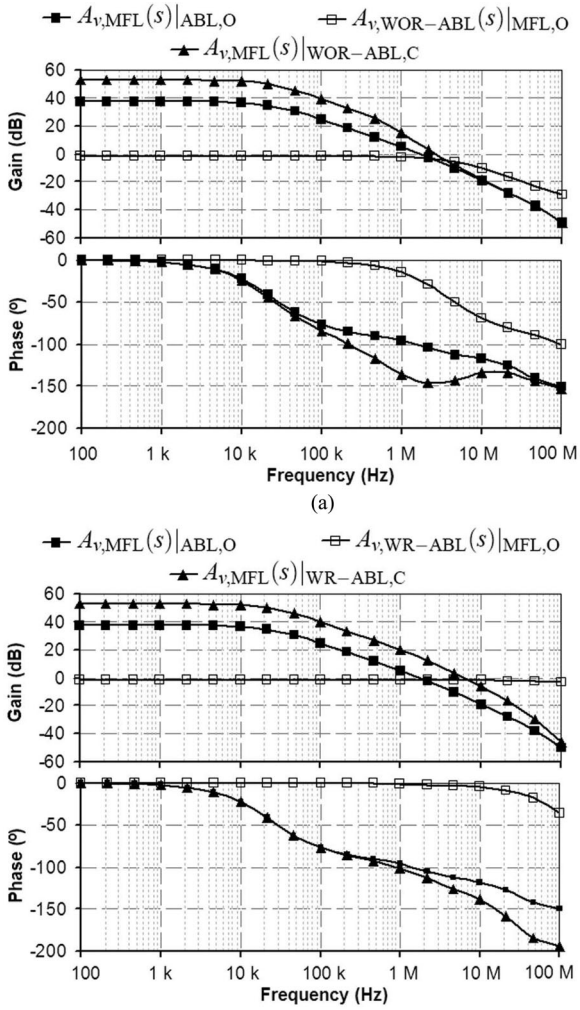

Fig. 8. Gain and phase plots of various transfer functions at $I_o = 50$ mA with $C_o = 470$ nF for the cases (a) WOR-ABL (b) WR-ABL.

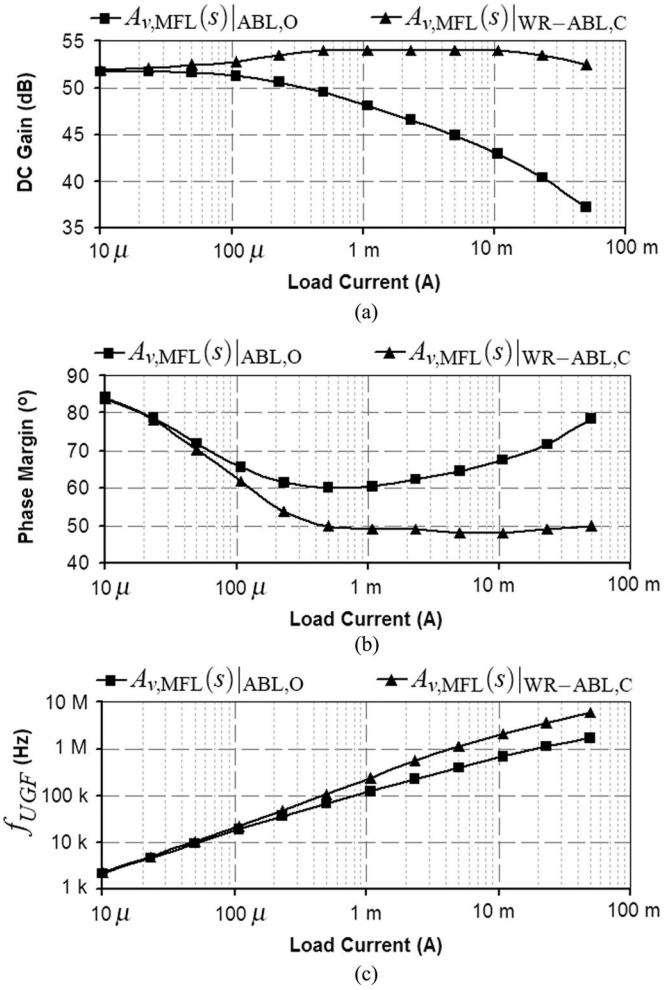

Fig. 9. Variation of different small-signal parameters of $A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}$ and $A_{v,\mathrm{MFL}}(s)|_{\mathrm{WR\text{-}ABL,C}}$ across load current with $C_o = 470$ nF. (a) DC gain. (b) Phase margin. (c) f_{UGF}.

expanded to 6.1 MHz, which is commensurate with the dc gain enhancement. In this case, the phase margin is 50°. This proves that the interaction of the ABL in the case WOR-ABL degrades the phase margin and f_{UGF} by 17° and 3.3 MHz, respectively, compared to the case WR-ABL.

Fig. 9 shows the variation of different small-signal parameters of $A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}$ and $A_{v,\mathrm{MFL}}(s)|_{\mathrm{WR\text{-}ABL,C}}$ against load current with $C_o = 470$ nF for the case WR-ABL. At $I_o = 10\,\mu$A, the ABL is not so effective, and hence, both of them have a dc gain of 52 dB. The corresponding phase margin and ω_{UGF} are equal to 84° and 2.1 kHz. At maximum load condition, i.e., I_o =50 mA, the dc gain of $A_{v,\mathrm{MFL,WR}}(s)|_{\mathrm{ABL,C}}$ is enhanced to 52 dB due to the ABL with a phase margin of 50°. The corresponding dc gain of $A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}$ is 37 dB at $I_o =$ 50 mA. The increased dc gain due to the ABL also helps to extend the ω_{UGF} from 1.7 to 6.1 MHz at $I_o = 50$ mA. Due to a smaller ω_{UGF} in $A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}$ compared with the same of $A_{v,\mathrm{MFL,WR}}(s)|_{\mathrm{ABL,C}}$, the phase margin is higher (78° versus 50°) in the former one. Therefore, the stability of the MFL at high-load condition should be guaranteed by design considering the interaction of the ABL.

D. *Stability of* ABL

Now, the effect of the MFL on the ABL is discussed. The transfer function of the ABL considering the effect of the MFL is given in (24), and (25). As $A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}$ comes in the denominator, the high differential gain of the same increases the dc attenuation of $A_{v,\mathrm{WOR\text{-}ABL}}(0)|_{\mathrm{MFL,O}}$ and $A_{v,\mathrm{WR\text{-}ABL}}(0)|_{\mathrm{MFL,O}}$

$$A_{v,\mathrm{WOR\text{-}ABL}}(s)|_{\mathrm{MFL,C}} = \frac{G_4G_5G_6}{1 - G_1G_2G_3} = \frac{A_{v,\mathrm{WOR\text{-}ABL}}(s)|_{\mathrm{MFL,O}}}{1 - A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}} \quad (24)$$

$$A_{v,\mathrm{WR\text{-}ABL}}(s)|_{\mathrm{MFL,C}} = \frac{G_4G_5G_7}{1 - G_1G_2G_3} = \frac{A_{v,\mathrm{WR\text{-}ABL}}(s)|_{\mathrm{MFL,O}}}{1 - A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}}. \quad (25)$$

Fig. 10(a) and (b) show the impact of $A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}$ on the small-signal response of the ABL for the cases WOR-ABL and WR-ABL, respectively. It is observed that

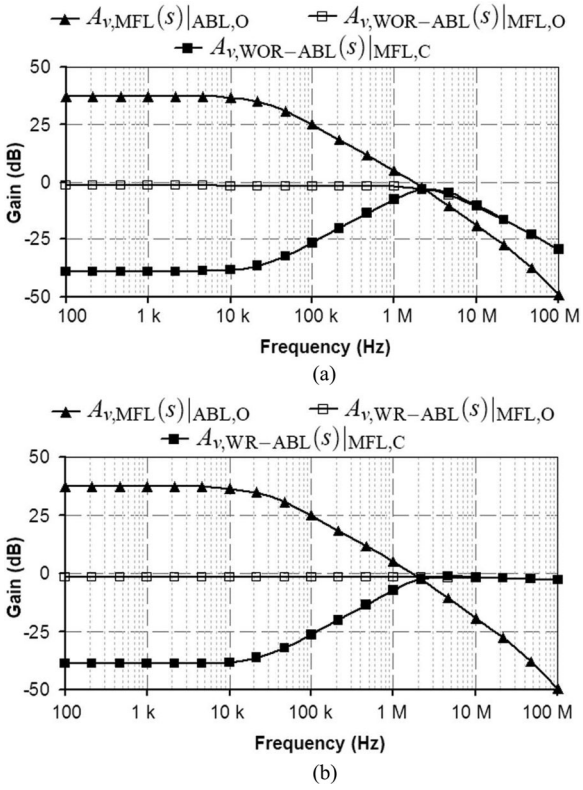

Fig. 10. Impact of $A_{v,\mathrm{MFL}}(s)|_{\mathrm{ABL,O}}$ on the small-signal response of (a) $A_{v,\mathrm{WOR\text{-}ABL}}(s)|_{\mathrm{MFL,C}}$ (b) $A_{v,\mathrm{WR\text{-}ABL}}(s)|_{\mathrm{MFL,C}}$.

$A_{v,\mathrm{ABL,WOR}}(0)|_{\mathrm{MFL,O}} = A_{v,\mathrm{ABL,WR}}(0)|_{\mathrm{MFL,O}} = -1.66$ dB. While the MFL is closed, $A_{v,\mathrm{MFL}}(0)|_{\mathrm{ABL,O}} = 37.2$ dB increase the dc attenuation of $A_{v,\mathrm{ABL,WOR}}(0)|_{\mathrm{MFL,C}}$ and $A_{v,\mathrm{ABL,WR}}(0)|_{\mathrm{MFL,C}}$ to -39 dB.

Fig. 11(a) shows the load transient response from no-load to full-load condition with a 10-ns rise time. The response time is improved to 260 ns from 1.7 μs for the case WR-ABL. As a result, the amount of undershoot is also improved from 167 mV as in WOR-ABL to 19 mV for WR-ABL. Due to a smaller phase margin, the case WOR-ABL shows more ringing in the settling behavior compared to the same in WR-ABL. Fig. 11(b) shows the comparison of the load transient response from full-load to no-load condition. Here, no overshoot is observed due to the presence of the pull-up path in the ECM buffer. The settling behavior is almost the same for both the cases due to a very minimal interaction of the ABL at the no-load condition.

In summary, the proposed small-signal analysis gives an in-depth understanding of the loop stability. It reveals that the interaction between the MFL and ABL is more likely in the case WOR-ABL. In the existing literature [17], [25], and [29], where the load current is sensed from the gate of M_P for the adaptive biasing similar to the case WOR-ABL, there is a possibility of an interaction between the MFL and ABL. This degrades the loop bandwidth with a reduced phase margin. A higher value of C_o is thus required to improve the phase margin and it reduces the loop bandwidth further. The conventional small-signal analysis in [26] and [30] fails to predict these phenomena.

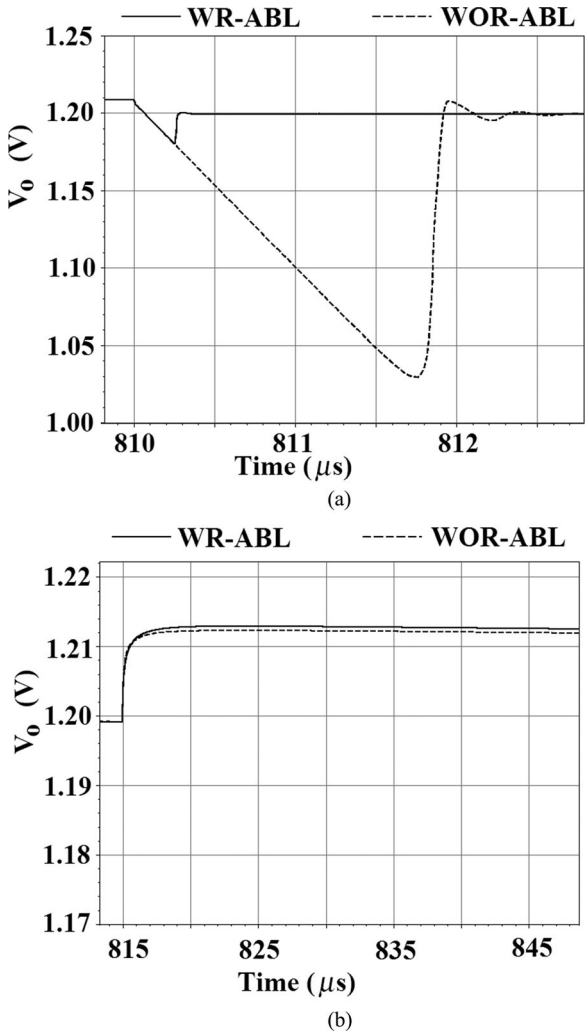

Fig. 11. Comparison of the load transient response for the cases WOR-ABL and WR-ABL. (a) 0–50 mA. (b) 50–0 mA.

In terms of performance, the use of WR-ABL in the proposed regulator topology has many advantages over WOR-ABL. First, the case WR-ABL has a higher phase margin and shows more stable settling behavior in the transient response. Second, the small signal ω_{UGF} of the MFL is also high in the case WR-ABL. Finally, WR-ABL improves the slew rate at the gate of the PMOS power transistor and improves the transient response significantly.

There are a few layout considerations, which are worth mentioning here. In the present design, the values of different parameters are chosen as follows: $\beta = 0.9$, $M = 1800$, $A = 2.5$, and $I_v/I_o = A/M = 1/720$. The transistors M_{53a}, M_{53b}, M_{59a}, and M_{59b} need to be placed in common centroid fashion for getting a good control of β. The input transistors M_{52}, M_{58}, and M_{51} are also to be matched in common centroid fashion to lower the offset. The perfect matching between the transistors M_{50}, M_{55}, and M_P is extremely difficult; only a good layout technique helps to reduce the mismatch between them. For example, M_{50} and M_{55} are placed at the center of the layout of M_P to minimize the on-die variation. Also, special care needs

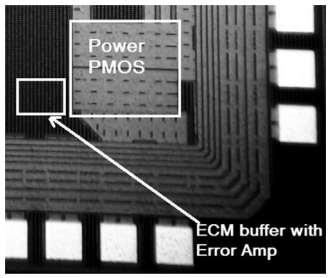

Fig. 12. Microphotograph of the proposed regulator.

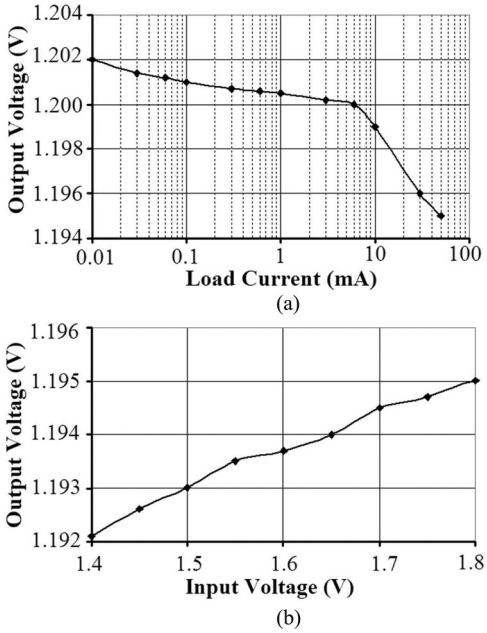

Fig. 13. Measured (a) load regulation (b) line regulation.

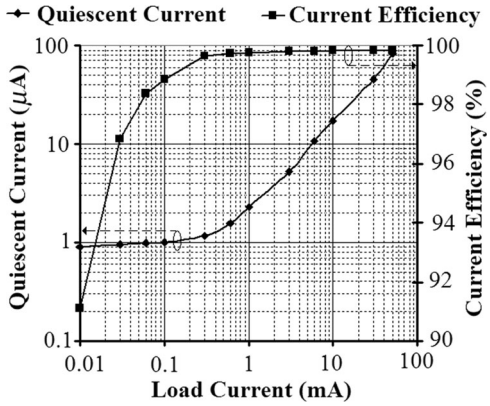

Fig. 14. Measured I_Q and current efficiency across load current.

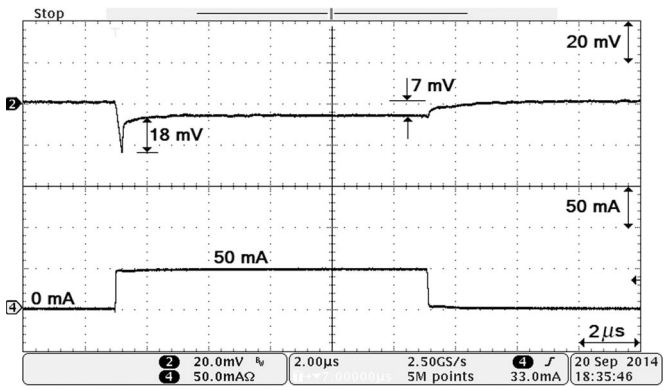

Fig. 15. Measured load transient response from 0–50 mA with a rise/fall time of 10 ns.

to be taken for matching M_{56} and M_{57}. As $A = 2.5$, a common centroid layout is only possible by appropriate fingering. For example, M_{57} and M_{56} are split into 4 and 10 fingers and M_{57} is laid at center, while placing the fingers of M_{56} around it.

V. Experimental Results

The proposed regulator structure (in Fig. 5) has been implemented in a 0.18-μm CMOS technology. Fig. 12 shows the microphotograph of the proposed regulator. The effective die area of the regulator is 0.039 mm^2. The input operating voltage is 1.4–1.8 V. The nominal output voltage is 1.2 V with a dropout voltage of 200 mV at a maximum load current of 50 mA.

Fig. 13(a) and (b) shows the measured load and line regulations graphs, respectively. The output voltage changes nearly by 7 mV across the load range as shown in Fig. 13(a). In the load range of 6–50 mA, the voltage falls sharply due to the IR voltage drop from the bond wire, metal, and printed circuit board parasitic. The measured load regulation is 0.14 mV/mA. When the input voltage changes from 1.4 to 1.8 V at $I_o = 50$ mA, the output voltage varies less than 3 mV as shown in Fig. 13(b) and it gives a line regulation of 7.25 mV/V.

Fig. 14 shows the measured quiescent current I_Q and current efficiency at different load conditions. The I_Q varies from 900 nA to 83 μA for a load range of 10 μA–50 mA. Due to adaptive biasing, the quiescent current increases at high-load condition. As the adaptive bias ratio A/M is chosen as 1:720, theoretically, the regulator should consume a quiescent current of 69 μA at $I_o = 50$ mA. However, due to the presence of mismatch in the large current mirror ratio M, the measured I_Q is recorded high by 20% than the theoretical value in the worst case. Due to the limited availability, the die-to-die variations is observed across ten samples. The maximum current efficiency is recorded as 99.8% at maximum load condition.

Fig. 15 shows the load transient response of the proposed regulator for a load step of 0–50 mA with rise and fall time of 10 ns. With $C_o = 470$ nF, an undershoot of 18 mV has been observed even with a very low quiescent current at no-load condition. No overshoot is observed for the load transient edge of 50–0 mA. This is due to the addition of pull-up path in the ECM buffer. The transient response shows a stable behavior, which does not rely on the ESR of the capacitance. With the use of 470 nF of ceramic capacitor, the maximum variation in the output voltage is close to 25 mV when $V_o = 1.2$ V and it includes the undershoot, overshoot, and the

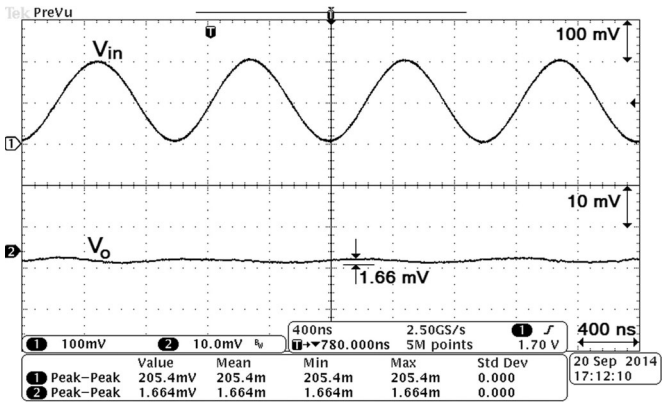

Fig. 16. Measured line transient response for $C_o = 470$ nF at $I_o = 50$ mA with a sinusoidal input frequency of 1 MHz.

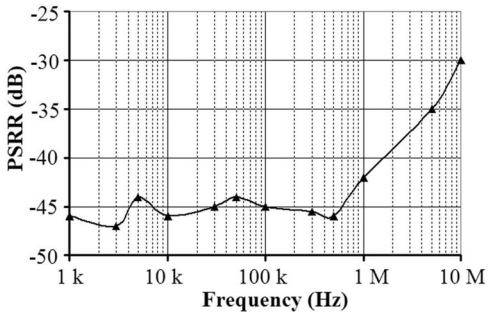

Fig. 17. Measured PSRR of the proposed topology at $I_o = 50$ mA.

dc load regulation. This 25-mV variation corresponds to about 2.1% of V_o. The settling time is nearly 400 ns. The proposed ECM and the slew-rate enhancement circuit helps the regulator to achieve fast transient response with a very small output variation.

The measured line transient response is shown in Fig. 16. A 200-mV peak-to-peak sinusoidal signal with a particular frequency is superimposed using a bias tee [35] with a dc voltage of 1.6 V to generate the input voltage V_{in}. For a sinusoidal frequency of 1 MHz, the peak-to-peak variations of the output voltage is 1.66 mV as shown in Fig. 16 with $C_o = 470$ nF at $I_o = 50$ mA. The power supply rejection ratio (PSRR) of the proposed regulator topology at $I_o = 50$ mA is shown in Fig. 17 and its value is less than -42 dB for the frequency range of 0–1 MHz.

Table II shows a performance comparison of some previously reported, externally compensated regulators with the proposed one. The proposed regulator consumes a very low quiescent current of 900 nA at no-load condition, and hence, increases the battery lifetime for portable applications. The regulator consumes a quiescent current of only 83 μA at the maximum load condition and offers a maximum current efficiency 99.8%. Although, the amount of maximum transient output-voltage variation $\Delta V_{o,\text{pp}}$ is more here compared to [21] and [25], it should be noted that this design uses a relatively smaller value of C_o and consumes a lower $I_{Q,\text{min}}$ (minimum value of I_Q). To quantify the tradeoffs between $I_{Q,\text{min}}$, C_o, and the maximum load current step ΔI_o, a figure of merit FOM $= T_r(I_{Q,\text{min}}/\Delta I_o)$ is adopted from [36] to compare the performance of different regulators. T_r is the response time of the regulator, which is given by $T_r = (C_o \Delta V_{o,\text{pp}})/\Delta I_o$. The smaller FOM implies a better performing regulator. From Table II, the proposed regulator achieves a very low FOM of 4 ps compared to the others. The study in [25] is the next best candidate and it has an FOM that is 2.6 times larger compared to this study. The reasons for achieving such a low FOM in this studt compared to others are as follows. First, the ECM buffer does not have a complex pole pair as it appears in the SCM buffer used in [25]. So, a smaller capacitor of 470 nF is sufficient to ensure the stability. As a result, the loop bandwidth, which controls the speed of the transient response, is also increased compared to [25]. Second, the use of WR-ABL also offers a better phase margin and loop bandwidth due to less interaction compared to the WOR-ABL, which was commonly used in the conventional AB-LDR topologies including the study in [25]. Third, the WR-ABL used in this study improves the slewing operation and helps to minimize the undershoot substantially even with a low quiescent current at no-load condition. Fourth, the push–pull slewing operation also becomes stronger as it is combined with the adaptive biasing. At high-load condition, the increased quiescent current attains a value of 83 μA. During high-to-low load step, a high pull-up current initially charges the gate of the power transistor quickly to reduce the current through it. So, even with a smaller output capacitor, no overshoot is observed. Finally, the use of minimum number of independent stages helps to significantly reduce the overall quiescent current.

VI. Conclusion

In this paper, we propose an ECM buffer developed from the OCM topology. The proposed ECM buffer is much superior to the OCM counterpart in terms of their small-signal bandwidth and slew rate performance. The ECM buffer is a useful cell to build up the proposed AB-LDR topology without adding more independent stages. The minimum number of stages helps to reduce quiescent current consumption significantly over the entire load range. It also makes it easy to achieve the stability of the regulator with an off-chip output capacitor of 470 nF. Finally, to speed up the transient response of the regulator, the slew rate at the gate of the PMOS power transistor is increased momentarily by using a WR-ABL. The proposed regulator is able to achieve an ultralow quiescent current of 900 nA at no-load condition, while maintaining a high current efficiency of 99.8% at maximum load condition. A very low FOM of 4 ps from the proposed regulator topology supports the superiority over the previously reported works.

This paper also presents a generalized way of carrying out the small-signal analysis of an AB-LDR. The key feature of the proposed analysis is the inclusion of the effect of the ABL in the MFL. As a result, it gives better understanding of improved dc load regulation due to the ABL and also predicts the stability of the MFL more accurately. With respect to our design, the extensive stability analysis suggests that an MFL in the WR-ABL has a better stability margin compared to the same in WOR-ABL.

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED, EXTERNALLY COMPENSATED REGULATORS

	[29]	[25]	[37]	[38]	[21]	[22]	[39]	[40]	**This work**
Year	2007	2008	2008	2010	2010	2010	2011	2012	**2015**
Technology (μm)	0.35	0.35	0.35	0.35	0.09	0.35	0.18	0.35	**0.18**
Active Area (mm^2)	0.264	0.053	0.409	0.146	0.00274	0.2254	0.10375	0.44	**0.039**
Minimum V_{in} (V)	2	1.05	2	2	1	2	2.1	3.3	**1.4**
Nominal V_o (V)	1.8	0.9	1.8	1.8	0.9	1.8	1.8	3	**1.2**
Dropout Voltage (mV)	200	150	200	200	100	200	300	300	**200**
Maximum Load (mA)	200	50	150	200	50	100	150	200	**50**
Quiescent current (μA)	20–340	4.04–164	27	30–75	9.3	4	23–150	147–314	**0.9-83**
Max. Current Eff. (%)	99.8	99.67	99.9	99.9	99.9	99.9	99.9	99.8	**99.8**
Load Reg. (mV/mA)	0.17	0.0614	0.11	0.09	0.082	10	–	0.45	**0.14**
Line Reg. (mV/V)	2	1.061	1.38	6	14	17	–	34	**7.25**
Compensation Cap. (pF)	10	No	0.4	No	No	Yes	No	10.5	**No**
Output Cap. (μF)	1	1	1	1	1	1	1	0.3	**0.47**
PSRR (dB) @ Freq. (Hz)	−45 @ 20k	−50 @ 1M	−40 @ 20k	–	−45 @ 1M	−32 @ 1M	–	−26 @ 1M	**−42 @ 1M**
ΔI_o (mA)	200	50	100	160	50	100	100	110	**50**
$\Delta V_{o,\text{pp}}$ (mV)	54	6.6	130	95	18.1	55	38	210	**25**
Settling time (μs)	∼16	∼0.3	∼5	∼2	∼1	–	–	∼3	**0.4**
FOM (ps)	27	10.6	351	111	67.3	22	87.4	765	**4**

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