Control and Experiment of an H-Bridge-Based Three-Phase Three-Stage Modular Power Electronic Transformer

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***Abstract*—Compared with conventional power transformer, the power electronic transformer (PET) or solid-state transformer has many attractive additional features. This paper focuses on an H-bridge-based three-phase three-stage modular PET, which consists of an input stage with series-connected H-bridge converters, an isolation stage with several independent dual-active-bridge converters, and an output stage with parallel-connected H-bridge converters. This PET suffers dc-link capacitor voltage unbalancing issue, and the parallel-connected module current unbalancing sharing issue. In this paper, a system control structure is proposed for the PET to deal with these issues. Different input-stage individual module dc-link voltage balancing control methods are analyzed and compared. It is found that the one implemented by directly trimming module output voltage amplitude is most suitable for PET. Moreover, a downscaled laboratory prototype is designed, built, and tested to verify the control strategy.**

***Index Terms*—DC-link capacitor voltage balancing, power electronic transformer (PET), three-stage structure, zero-sequence circulating current.**

I. Introduction

With the advancement of power semiconductor device and other power electronics technologies, the emerging technology power electronic transformer (PET), other technical aliases of which include solid-state transformer [1], intelligent universal transformer [2] etc., has got rapid development and caught increasing attention from both academia and industry in the past two decades [1]–[17]. Compared with conventional purely magnetic line-frequency power transformer, a PET could be regarded as a power converter employing power semiconductor devices, medium- or high-frequency transformers, and advanced control system. In addition to realizing voltage step-up/down and galvanic isolation, the utilization of power semiconductor devices and advanced control system also endows PET with many additional advantageous features [3], [10]–[12] such as the reduction of size and weight, power quality improvement, output voltage regulation, renewable energy interfacing, and many other potential functionalities.

Various PET topologies are reported and discussed in [2]–[5], [10]–[15], most of which focus on single-phase applications. These topologies can be classified into three main categories: the single-stage ac–ac ones, the two-stage ac–dc–ac ones, and the three-stage ac–dc–dc–ac ones. In general, the single-stage topologies have the best performance on efficiency and the reduction of size and weight, while the three-stage ones have the maximum potential functionalities and control flexibility [3], [10]–[12]. From topological point of view, the merit of the maximum potential functionality makes the three-stage PET topologies to be the most popular ones. These configurations consist of a grid-side rectifier stage or input stage, an isolated dc–dc stage, and a load-side inverter stage or output stage. Moreover, modular multilevel converters are commonly employed at the PET's grid-side rectifier stage due to that most PET applications are oriented to medium- or high-voltage level. On the other hand, Wang *et al.* [16] and Grider *et al.* [17] investigated the application of silicon carbide (SiC)-based power semiconductor devices for high-voltage PET. However, SiC power devices so far are still not commercially available with a reasonable price, and need further development. Therefore, it is practical to employ multilevel converters at the PET rectifier stage.

With the continuing efforts devoted by researchers and engineers, significant progress has been made on the PET applications in railway traction, renewable energy generation, and smart grid [1], [5]–[10], [14], [15]. Dujic *et al.* [14] proposed a single-phase PET topology and its control strategy for railway traction application. This configuration consists of an H-bridge-based cascaded multilevel input stage and an isolation stage with half-bridge-based isolated dc–dc resonant converters, which are input-series-output-parallel connected. Furthermore, they proposed control schemes for the efficiency improvement under light-load conditions in [15]. In [8], the PET-based wind power generation system is regarded as a possible trend in future. In [5] and [18], three-stage and single-stage PET topologies as the interface between the wind turbine and power grid are investigated, respectively. Falcones *et al.* [19] proposed dual-active-bridge (DAB) based and quad-active-bridge-based PETs integrated with photovoltaic (PV) power generation and storage. In [20]–[22], different control strategies are proposed for the same distribution-level-oriented single-phase PET topology, which is the key component of the future renewable electric energy delivery and management system [1]. Compared with

Manuscript received September 27, 2014; revised April 27, 2015; accepted May 12, 2015. Date of publication May 18, 2015; date of current version November 16, 2015. This work was supported by the State Key Laboratory of Electrical Insulation and Power Equipment under Grant EIPE14112. Recommended for publication by Associate Editor J. HR Enslin.

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Digital Object Identifier 10.1109/TPEL.2015.2434420

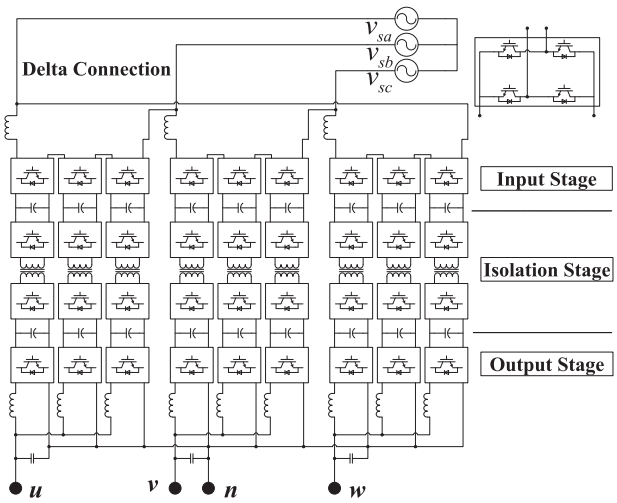

Fig. 1. Three-phase three-stage PET topology.

the topology shown in [14], this approach employs DAB not dc–dc resonant converter to serve as the isolation stage. This approach's load-side 400-V common dc bus serves as the dc distribution bus interfacing loads, residential-class renewable energy resources, and distributed energy storage devices [1]. Du *et al.* [23] reviewed and compared different magnetic core materials for PET high-voltage high-frequency transformer, and a 3-kHz 6.7-kVA transformer prototype was built and tested. Fan *et al.* [24] proposed dual-half-bridge dc–dc converter modules with high efficiency over wide load range for PET. Zhao *et al.* [25] proposed an input–output power synchronization control to minimize the single-phase H-bridge dc-link second-order fluctuation amplitude. Zheng *et al.* [26] proposed a control strategy for a single-phase PET with only one multiwinding high-frequency transformer. Most of the previous literatures are focusing on H-bridge-based three-stage single-phase PET topologies, which have one common low-voltage-side dc-link [1], [14] or a multiwinding transformer [19], [26].

In this paper, the authors focus on the H-bridge-based three-phase three-stage modular PET topology shown in Fig. 1. As is depicted, the input stage is a modular multilevel cascade ac–dc rectifier; the dc–dc isolation stage consists of several DAB converters with high-frequency transformers; the output stage is a three-phase full-bridge dc–ac inverter. Obviously, this PET topology has a good redundancy and the ability of bidirectional power flow. Furthermore, it provides three-phase four-wire output ability to deal with unbalanced load. On the other hand, the input stage suffers the dc-link voltage and power unbalance issue, which is caused by many factors [27] such as the tolerances of passive components, different power losses of semiconductor devices, signal imbalance, etc. Some existing work [28]–[31] focusing on dc-link voltage balancing control for H-bridge cascade multilevel converter provides reference value for this topology. Similarly, current-sharing control for the parallel modules is needed for the output stage. In this paper, a system control structure for this topology is proposed, which contains three parts related to the three stages. The input-stage control strategy is responsible for power quality and input-stage-side dc-link capacitor voltage balancing control; the isolation-stage control strategy is responsible for the output-stage-side dc-link voltage maintaining; and the output-stage control strategy is responsible for output voltage regulation and parallel-module current-sharing control. Moreover, different individual dc-link voltage balancing control methods for the input stage are analyzed and compared. It is found that the method implemented by trimming modulating voltage amplitude is the most suitable one for PET. A low-voltage downscaled prototype is designed, built, and tested in the lab. Experimental results verify the control strategy.

II. Circuit Configuration

Different research groups focus on various PET applications and related issues. In this paper, the authors mainly focus on high-voltage high-power three-phase PET applications, such as serving as the interfacing system between wind turbine and medium- or high-voltage power grid. In the authors' previous released paper [13], a series of new three-phase three-stage modular PET topologies are presented, analyzed, and compared. From a comprehensive point of view, it is found that the topologies shown in Fig. 1 have the best performance on redundancy, efficiency, semiconductor cost, and could provide three-phase four-wire output to deal with unbalanced load.

Fig. 1 illustrates the PET circuit configuration, which is comprised of three cascaded stages: the input stage with series-connected H-bridge converters, the isolation stage with several independent DAB converters, and the output stage with parallel-connected H-bridge converters. The topology has a delta connection configuration with utility grid at the input stage. Herein, the term input stage just means that this stage is connected to utility grid, while the term output stage means it is connected to load.

Obviously, the topology suffers the input-stage dc-link voltage and power unbalance issue, and the output parallel module current sharing issue. In this paper, a system control structure is designed for the topology. According to the three stages, the overall control strategy also can be divided into the input-stage one, the isolation-stage one, and the output-stage one. The input-stage control aims to implement power quality control and input-stage-side dc-link capacitor voltage balancing control. Each DAB is responsible for maintaining the output-stage-side dc-link capacitor voltage. The output-stage control aims to regulate the output voltage and implement parallel-module current-sharing control.

III. Input-Stage Control Strategy

Fig. 2 illustrates the input-stage equivalent circuit. For the input stage, many factors addressed in [27] would lead the voltage and power imbalance issue among multiple floating dc capacitors. For the sake of simplicity, these factors are regarded as power loss difference in this paper. The power loss difference among different modules and phases can be simply represented by the equivalent resistors paralleled with module

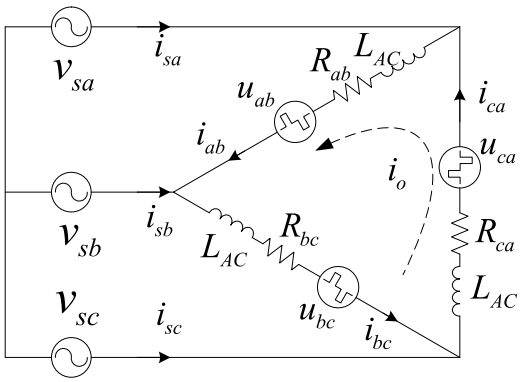

Fig. 2. Input-stage equivalent circuit.

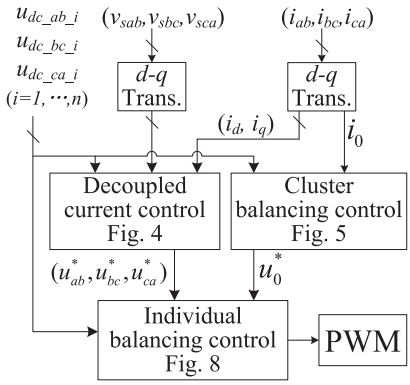

Fig. 3. Block diagram of input-stage total control.

dc-link capacitors and the equivalent resistors which are series-connected with converters, as shown in Fig. 2. Normally, these resistors are very small. Different control strategies focusing on dc-link voltage balancing are proposed for H-bridge cascade multilevel converter-based static synchronous compensator (STATCOM) in [28]–[31]. These control strategies consist of three parts: current and overall dc-link voltage control, cluster dc-link voltage balancing control, and individual module voltage control. In [28], Liu *et al.* proposed an individual dc capacitor voltage balancing control method based on a small-signal model, and compared it with the other three methods for STATCOM application but not for active rectifier application. In [29] and [30], fundamental-frequency zero-sequence voltage and circulating current are injected to balance cluster dc-link voltage for STATCOM with star and delta configurations, respectively. Maharjan *et al.* [31] mainly focused on the three-layer controller parameter design. Herein, a cluster means a set of input-stage series-connected converter cells in a phase.

As mentioned in the aforementioned section, the input-stage control objectives are the realization of unity power factor and input-stage-side dc-link voltage balancing control. The input-stage control strategy also consists of three parts: the decoupled current control of independent active and reactive power, the cluster balancing control, and the individual balancing control. Fig. 3 shows the input-stage total control block diagram.

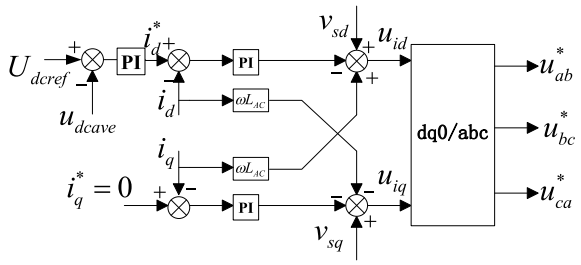

Fig. 4. Block diagram of input-stage-decoupled current control.

A. Decoupled Current Control

Referred to Fig. 2, the input-stage voltage–current equation is expressed as follows:

$$\begin{bmatrix} v_{sab} \\ v_{sbc} \\ v_{sca} \end{bmatrix} - \begin{bmatrix} u_{ab} \\ u_{bc} \\ u_{ca} \end{bmatrix} = L_{\mathrm{AC}} \frac{d}{dt} \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} + \begin{bmatrix} R_{ab} \\ R_{bc} \\ R_{ca} \end{bmatrix}^T \cdot \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} \tag{1}$$

where R_{ab}, R_{bc}, and R_{ca} represent the equivalent resistances of inductor equivalent series resistance, conducting and switching losses of power switching devices. Normally, they are almost the same and can be neglected. Applying the *dq* transformation of (1) along with neglecting the resistors, the equation in *dq* coordinate is derived as follows:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} - \begin{bmatrix} u_{id} \\ u_{iq} \end{bmatrix} = \begin{bmatrix} L_{\mathrm{AC}} \frac{d}{dt} & -\omega L_{\mathrm{AC}} \\ \omega L_{\mathrm{AC}} & L_{\mathrm{AC}} \frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2}$$

where v_{sd} and v_{sq} are the *d*- and *q*-axis components of grid line voltage, respectively; u_{id} and u_{iq} are the *d*- and *q*-axis components of converter ac-side voltage, respectively; and i_d and i_q are the *d*- and *q*-axis components of inductor current, respectively.

Fig. 4 depicts the input-stage-decoupled current control. The reactive current reference i_q^* is assigned zero to obtain unity power factor, meanwhile, it also could be assigned a certain value to generate or absorb reactive power to utility grid. Therefore, if the PET has adequate power capacity, it could not only take the place of the wind-turbine-side converter and step-down transformer but also the STATCOM in wind power generation application. This idea also could be extended to PV generation and other applications having similar requirements. As shown in Fig. 4, the active current reference i_{d}^* is adjusted by the voltage loop proportional–integral (PI) controller according to the voltage error between the input-stage dc-link capacitor voltage reference U_{dcref} and the average value u_{dcave} of all input-stage dc-link capacitor voltages. The process of PI controller design and decoupled current control analysis can be found in [29]. With the decoupled current control, the positive-sequence commands $u_{ab}{}^*$, $u_{bc}{}^*$, and $u_{ca}{}^*$ can be obtained. The unity power factor and the average value of all dc-link capacitor voltages tracking the dc-link voltage reference are implemented.

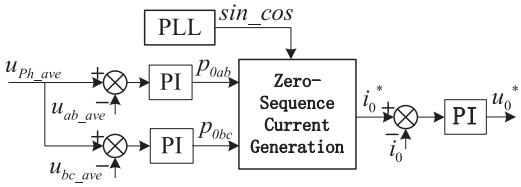

Fig. 5. Block diagram of input-stage cluster balancing control.

B. Cluster Balancing Control

The power loss difference among three clusters would lead the three-cluster dc-link voltage unbalancing issue. Moreover, the cluster unbalancing issue would be much more severe for SPC under unbalanced load. The cluster balancing control is needed to keep the dc-link capacitor dc mean voltage of each cluster equal to the capacitor dc mean voltage of the three clusters. The aforementioned decoupled current control only generates positive-sequence currents among three clusters, and distributes the same amount of average power to three clusters. Therefore, the cluster balancing control shall generate certain command currents to distribute or redistribute three clusters with different amounts of average power according to the power loss difference or unbalanced-load condition. With the input-stage delta configuration, zero-sequence circulating current is utilized. The zero-sequence circulating current would not flow into grid. Therefore, it would not affect the grid power quality.

As referred to Fig. 2, the command zero-sequence circulating current is injected and written as follows:

$$i_o = \sqrt{2} I_o \sin(\omega t + \theta) \tag{3}$$

where I_o and θ are the zero-sequence circulating current rms value and original phase angle, respectively. The average power redistributed by zero-sequence circulating current is expressed as follows:

$$\begin{cases} p_{0ab} = 1/T_s \displaystyle\int_t^{t+T_s} v_{sab} \cdot i_o dt = V_S I_o \cos(\theta) \\ p_{0bc} = 1/T_s \displaystyle\int_t^{t+T_s} v_{sbc} \cdot i_o dt = V_S I_o \cos(\theta + \frac{2\pi}{3}) \\ p_{0ca} = 1/T_s \displaystyle\int_t^{t+T_s} v_{sca} \cdot i_o dt = V_S I_o \cos(\theta - \frac{2\pi}{3}). \end{cases} \tag{4}$$

As shown in (4), the three power equations are different, and the summation of three equations equals zero. It indicates that the zero-sequence circulating current only leads to the active-power redistribution but has no impact on the active power amount absorbed from utility grid. Therefore, the cluster balancing control, as shown in Fig. 5, is implemented by injecting command zero-sequence circulating current [30]. The redistributed average power p_{0ab}, p_{0bc}, and p_{0ca} in three clusters can be divided into the power consumed by the cluster converter cells p_{0ab_C}, p_{0bc_C}, and p_{0ca_C}, and the power consumed by the equivalent resistors p_{0ab_R}, p_{0bc_R}, and p_{0ca_R}. Normally, the latter could be neglected. Therefore, the redistributed average power is almost approximately equal to the power consumed by the cluster converter cells. The power relationship is expressed as follows:

$$\begin{cases} p_{0ab} = p_{0ab\_C} + p_{0ab\_R} \approx p_{0ab\_C} \\ p_{0bc} = p_{0bc\_C} + p_{0bc\_R} \approx p_{0bc\_C} \\ p_{0ca} = p_{0ca\_C} + p_{0ca\_R} \approx p_{0ca\_C} \end{cases} \tag{5}$$

where

$$\begin{cases} p_{0ab\_C} = 1/T \displaystyle\int_t^{t+T_s} u_{ab} \cdot i_o dt \\ p_{0bc\_C} = 1/T \displaystyle\int_t^{t+T_s} u_{bc} \cdot i_o dt \\ p_{0ca\_C} = 1/T \displaystyle\int_t^{t+T_s} u_{ca} \cdot i_o dt \end{cases} \tag{6}$$

$$\begin{cases} p_{0ab\_R} = 1/T_s \displaystyle\int_t^{t+T_s} R_{ab} \cdot i_o^2 dt = R_{ab} I_o^2 \\ p_{0bc\_R} = 1/T_s \displaystyle\int_t^{t+T_s} R_{bc} \cdot i_o^2 dt = R_{bc} I_o^2 \\ p_{0ca\_R} = 1/T_s \displaystyle\int_t^{t+T_s} R_{ca} \cdot i_o^2 dt = R_{ca} I_o^2. \end{cases} \tag{7}$$

The proper redistributed power can be utilized to balance the dc-link capacitor voltages among three clusters, which is caused by power loss difference. As shown in Fig. 5, the amount of active power redistributed by zero-sequence circulating current is calculated by close-loop controller. u_{Ph_ave} is the input-stage-side dc-link capacitor dc mean voltage of the three clusters, while u_{ab_ave} and u_{bc_ave} are the capacitor dc mean voltages of cluster *ab* and cluster *bc*, respectively. After the adjustment by two PI controllers, the required power p_{0ab} and p_{0bc} are determined. Then, the command zero-sequence circulating current is generated by (3) and (8). Equation (8) is derived from (4). The PI controller design process can be found in [30] and [31]

$$\begin{cases} I_o = 1/V_s \sqrt{(p_{0ab})^2 + \dfrac{1}{3}(p_{0ab} + 2 \cdot p_{0bc})^2} \\ \theta = \tan^{-1}[-(1 + 2 \cdot p_{0bc}/p_{0ab})/\sqrt{3}] \end{cases}. \tag{8}$$

C. Individual Balancing Control

With the decoupled current control and cluster balancing control, the cluster dc-link capacitor dc mean voltage in each cluster is controlled and maintained. The command voltage $(u_x^* + u_o^*)$ for each cluster is obtained, where *x* is *ab*, *bc*, or *ca*. The individual balancing control for balancing different dc-link capacitor voltages in one cluster is indispensable due to the power loss difference among the converter cells in one cluster.

In [28], Liu *et al.* reviewed three individual balancing control methods, and proposed a new one based on the small-signal model. As compared with other two methods all implemented by trimming output voltage amplitude, the new one has the biggest power value coefficient with the same module output voltage amplitude increment for STATCOM application. However, this method needs an additional time-variant compensator for each individual module dc-link voltage balancing control loop, which makes it more much complicated. Moreover, it is not analyzed for active rectifier application. In this paper, the comparison of the four individual balancing control methods for active rectifier application is done.

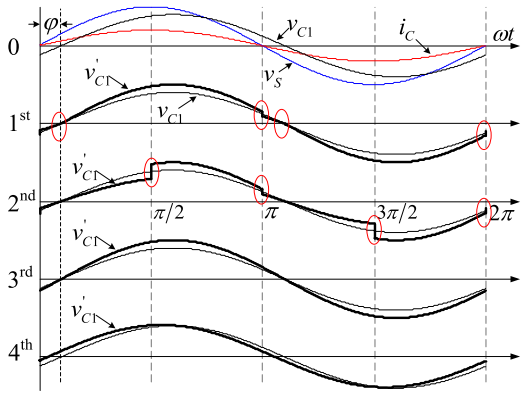

Fig. 6. Waveforms of four individual balancing control methods for active rectifier application with unity power factor.

The detailed operating principle and description of the four methods can be found in [28] and is simply introduced in this paper. Fig. 6 shows the waveforms of four individual balancing control methods for active rectifier application. The first subfigure denoted as 0 depicts the waveforms of the grid voltage, current, and cluster ac voltage. Take the example of the first H-bridge in cluster *ab*, herein it only takes account of the fundamental component of the H-bridge output voltage and cluster current along with neglecting the switching-frequency components. The voltage–current equations could be expressed as follows:

$$\begin{cases} v_S = \sqrt{2}V_S \cdot \sin(\omega t) \\ i_c = \sqrt{2}I_c \cdot \sin(\omega t) \\ u_{c1} = \sqrt{2}U_{c1} \cdot \sin(\omega t + \varphi) \end{cases} \tag{9}$$

$$L_{\mathrm{AC}} = \frac{10\% \times V_S}{\omega \cdot I_c} \tag{10}$$

$$\varphi = \arctan \frac{\omega \cdot I_c \cdot L_{\mathrm{AC}}}{V_S} \approx 0.0997\mathrm{rad} \tag{11}$$

where I_c is the cluster current rms value; and U_{c1} and φ are the H-bridge output voltage rms value and phase angle, respectively. The input-stage interfacing ac inductor could be designed by the empirical equation (10). For active rectifier with unity power factor, the H-bridge output voltage phase angle φ can be estimated by (11), which is very small.

The waveforms in the second figure denoted as 1st depicts the 1st method proposed in [28]: u_{c1} increases ΔU_{c1} when ωt in $[\varphi, \pi]$ or $[\varphi + \pi, 2\pi]$: u_{c1} decreases ΔU_{c1} when ωt in $[0, \varphi]$ or $[\pi, \varphi + \pi]$.

The waveforms in the third figure denoted as 2nd depicts the 2nd method proposed in [27]: u_{c1} decreases ΔU_{c1} when ωt in $[0, \pi/2]$ or $[\pi, 3\pi/3]$; u_{c1} increases ΔU_{c1} when ωt in $[\pi/2, \pi]$ or $[3\pi/2, 2\pi]$.

The waveforms in the fourth figure denoted as 3rd depicts the 3rd method adopted in [29] and [30]: u_{c1} increases ΔU_{c1}.

The waveforms in the fifth figure denoted as 4th depicts the 4th method presented in [32]: u_{c1} have a small phase shift.

The 1st, 2nd, and 3rd methods are implemented by trimming the module voltage amplitude, and the 4th method is implemented by trimming the module voltage phase angle. Assume that the H-bridge needs absorbing active power for balancing dc capacitor voltage. In order to increase the input power, the module output voltage u_{c1} is slightly regulated to be u'_{c1}, which is shown as bold lines in Fig. 6. The average power increment can be calculated by (12). The four average power increment equations of four methods are derived as

$$\Delta P = \frac{1}{2\pi} \int_0^{2\pi} (u'_{c1} - u_{c1}) \cdot i_c d\omega t \tag{12}$$

$$\Delta P_1 = \Delta U_{c1} \cdot I_c \cdot \cos\varphi + 2 \cdot \Delta U_{c1} \cdot I_c \cdot \frac{\sin\varphi - \varphi \cdot \cos\varphi}{\pi} \tag{13}$$

$$\Delta P_2 = 2\Delta U_{c1} \cdot I_c \cdot \frac{\sin\varphi}{\pi} \tag{14}$$

$$\Delta P_3 = \Delta U_{c1} \cdot I_c \cdot \cos\varphi \tag{15}$$

$$\Delta P_4 \approx U_{c1} \cdot I_c \cdot \sin\varphi \cdot \Delta\varphi \tag{16}$$

where

$$\Delta U_{c1} = U'_{c1} - U_{c1} \tag{17}$$

As shown in (11), the phase angle φ for active rectifier application with unity power factor is very small. The first term on the right-hand side of (13) is the same to the one of (15). Moreover, the value of the second term on the right-hand side of (13) is a very small positive one. Therefore, the 1st and 3rd methods have a very small difference on the power value coefficient for active rectifier application with unity power factor. Obviously, the power increment of (14) is very small which means the related 2nd method is not suitable for pure active rectifier application. When the phase angle φ increases, the value of the first term on the right-hand side of (13) decreases, and the value of the second term increases and finally becomes a dominated one. Therefore, the 1st method related to (13) will have a bigger power increment coefficient as compared with the 3rd method related to (15). Moreover, the value of (14) will also increase when the phase angle φ increases. When the phase angle φ is $\pm\pi/2$ which means the system is for ideal STATCOM application, (13) and (14) will have the same equation. Therefore, the 1st and 2nd methods related to (13) and (14), respectively, have the same power increment coefficient for ideal STATCOM application. Therefore, the 1st and 2nd methods are suitable for STATCOM application while the 3rd method is not suitable.

The 4th method related to (16) is implemented by trimming phase angle. Equation (16) is based on phase angle increment $\Delta\varphi$ while (13)–(15) are based on voltage amplitude increment ΔU_{c1}. From this point of view, the author in [28] did not compare it with other methods based on trimming voltage amplitude. Equation (16) could be alternatively expressed as (18). Since the phase angle φ absolute value will be no bigger than $\pi/2$, the phase angle increment $\Delta\varphi$ will also not exceed the range. Moreover, the voltage amplitude increment ΔU_{c1} will also not exceed the voltage amplitude U_{c1}. From this point of view, the assumption of (19) could be made. Based on this assumption,

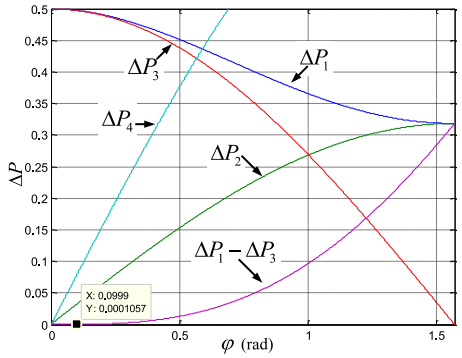

Fig. 7. Comparison of different individual balancing control methods for active rectifier application.

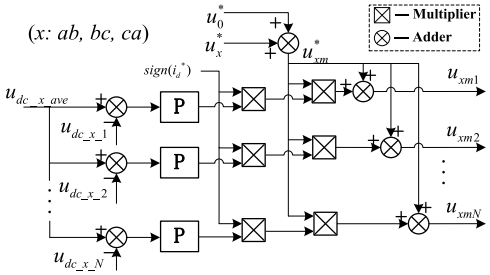

Fig. 8. Block diagram of input-stage individual balancing control.

the 4th method could be compared with other three methods

$$\Delta P_4 \approx \left(U_{c1} \cdot \frac{\Delta\varphi}{\pi/2}\right) \cdot I_c \cdot \sin\varphi \cdot \frac{\pi}{2} \tag{18}$$

$$\Delta U_{c1} = U_{c1} \cdot \frac{\Delta\varphi}{\pi/2}. \tag{19}$$

Based on (13)–(15), (18), and (19), the curves of power increment coefficient with respect to phase angle φ having the same voltage amplitude increment ΔU_{c1} are depicted in Fig. 7. As is shown, the difference on power increment coefficient between the 1st and 2nd methods for active rectifier application is very small and could be neglected. Even when the phase angle is about $\pi/6$ which means the system mainly supplies active power along with certain ratio of reactive power, the power increment coefficient is also small. Moreover, the 1st method [28] needs an additional time-variant compensator for each individual module dc-link voltage balancing control loop, which makes it much more complicated. The 2nd and 4th methods are more suitable for STATCOM application.

Based on the aforementioned analysis and comparison, the 3rd method is selected. Fig. 8 shows the individual balancing control. The idea of the individual balancing control is based on (20). The amplitude of the final command voltage u_{xmh} for each converter cell in one cluster is trimmed by Δu_h, which is the product of the active-power polarity and the adjusted result of the associated closed-loop feedback control. $u_{\mathrm{dc\_x\_ave}}$ is the capacitor dc mean voltage of one cluster, and $u_{\mathrm{dc\_x\_h}}$ is the converter dc-link capacitor voltage. The phase angles of the final command voltages for different converter cells are kept the same. The proportional controller design process can be found

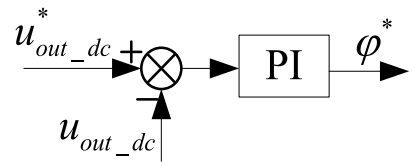

Fig. 9. Block diagram of DAB control.

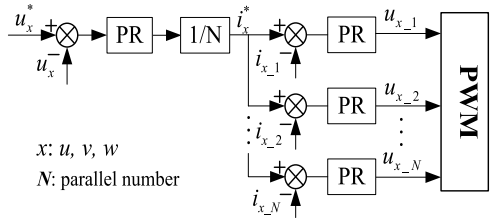

Fig. 10. Block diagram of output-stage control.

in [27]

$$u_{xmh} = (1 + \Delta u_h) \cdot (u_x^* + u_0^*) \quad (h = 1, ..., N). \tag{20}$$

IV. Isolation- and Output-Stage Control Strategy

A. Isolation-Stage Control Strategy

With the input stage control, the input-stage-side dc-link voltages are balanced, and then, the DAB control aims to regulate associated output-stage-side dc-link voltage to track the same voltage reference. Phase-shift control described in detail in [33] is applied for DAB to regulate its associated output-stage-side dc-link voltage. Fig. 9 illustrates the control loop for one DAB. The phase-shift angle is adjusted by PI controller according to the voltage error between output-stage dc-link voltage and the voltage reference

$$P_{\mathrm{DAB}} = \frac{n \cdot V_{\mathrm{in\_dc}} \cdot V_{o\_\mathrm{dc}}}{2\pi f_S \cdot L_S} \beta \left(1 - \frac{|\beta|}{\pi}\right) \tag{21}$$

where $V_{\mathrm{in\_dc}}$ and V_{o_dc} are the input-stage-side and output-stage-side dc-link capacitor voltages, respectively; n is the transformer turn ratio, $n = n_p : n_s$; β is the phase-shifted angle between two H-bridge driving signals; L_S is the leakage inductance; and f_s is the switching frequency.

B. Output-Stage Control Strategy

The output-stage control is responsible for three-phase output voltage regulation and parallel module current-sharing control. Fig. 10 shows the control diagram for one output-stage phase. The overall voltage loop regulates the output voltage, and generates the current reference for N parallel modules in the one phase. The N inner current loops track the same current reference to realize parallel module current-sharing control, where i_{x_N} is inductor current. Proportional-resonant (PR) controller [34] in (22) is applied for the output stage control. P controller could also be used in the current loops. Moreover, the interleaving technique could be applied to the parallel modules in one

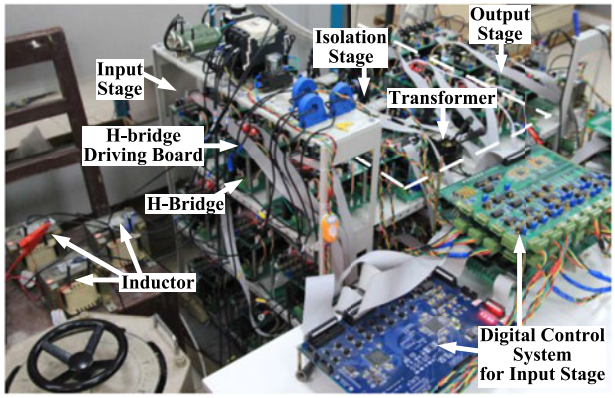

Fig. 11. Photo of the downscaled prototype.

TABLE I
PROTOTYPE PARAMETERS

Line Frequency	50 Hz
Input Inductance	3 mH
Input-Stage Switching Frequency	10 kHz
Isolation-Stage Switching Frequency	10 kHz
Output-Stage switching frequency	20 kHz
DC Capacitor Capacitance	1100 μF
Transformer Ratio	1:2
DAB Inductance	0.1 mH
Output-Stage *LC* inductance	1 mH
Output-Stage *LC* capacitance	60 μF
IGBT/Diode	IRG4 PC50 UD
Load Resistor	5 Ω

phase so that the total harmonic distortion performance could be improved

$$\mathrm{PR}(s) = k_P + \frac{k_I \omega_c s}{s^2 + \omega_c s + \omega^2} \tag{22}$$

where k_P is the proportional gain, k_I is the integral gain, and ω_c is the resonance frequency.

V. EXPERIMENTAL RESULTS

A. Downscaled Prototype

According to the main circuit configuration shown in Fig. 1, a three-phase downscaled laboratory prototype rated at 110-V and 3-kVA is designed, constructed, and tested to verify the aforementioned overall control strategy for the PET topology. Fig. 11 shows the photo of the downscaled prototype. The prototype has total 36 H-bridge converters, which means each input-stage cluster consists of three series-connected H-bridge converters. Table I summarizes the main circuit parameters. The so-called phase-shifted unipolar sinusoidal PWM with a carrier frequency of 1.667 kHz is applied to a cluster of three series-conned H-bridge converters in each input-stage phase. Therefore, the input-stage equivalent switching frequency becomes 10 kHz (1.667 kH $\times$ 2 $\times$ 3), and the ac voltage of each cluster becomes a seven-level line-to-line PWM waveform. The phase-shift control is applied to DAB, and the switching frequency is 10 kHz. The interleaving technique with a carrier frequency of 3.334 kHz is applied to the output-stage parallel modules.

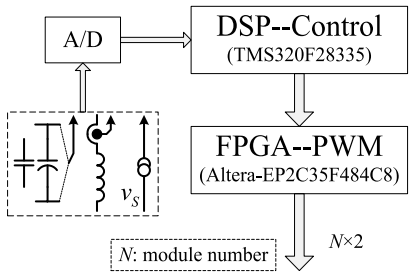

Fig. 12. Block diagram of digital control system.

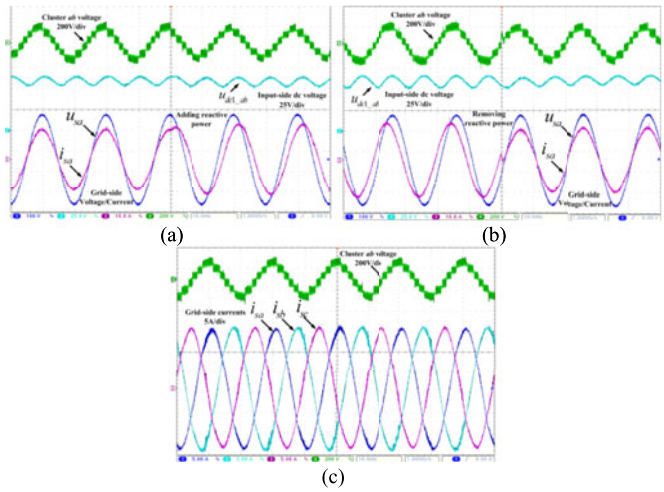

Fig. 13. Experimental waveforms of input-stage grid-side current. (a) Experimental waveform of adding positive reactive power. (b) Experimental waveform of removing negative reactive power. (c) Three-phase grid-side current waveform.

Therefore, the output-stage load-side equivalent switching frequency becomes 20 kHz (3.334 kH $\times$ 2 $\times$ 3).

The downscaled prototype has total 36 H-bridge converters. One H-bridge converter needs two independent PWM signals, where one H-bridge driving circuit would utilize one independent PWM signal to generate two complementary PWM signals for driving one H-bridge leg. Thus, 36 H-bridges need total 72 independent PWM signals, which could not be provided by one DSP chip. Therefore, a DSP + FPGA digital control system shown in Fig. 12 is designed, where DSP and FPGA are responsible for controlling and PWM signal generating, respectively. Each stage has one such digital control system. Thus, three sets of such digital control system serve for the prototype. This digital control system is also suitable for the situation having even more H-bridge converters. If the H-bridge number increases, more FPGA chips may be needed, and some computing work such as voltage–current sampling and converting could be alternatively done by FPGA.

B. Experimental Waveforms

Fig. 13 shows input-stage grid-side current experimental waveforms. As is addressed in the aforementioned input-stage control, unity power factor is normally implemented. Meanwhile, reactive power could be generated or absorbed if the input stage has adequate current capacity. Fig. 13(a) and (b)

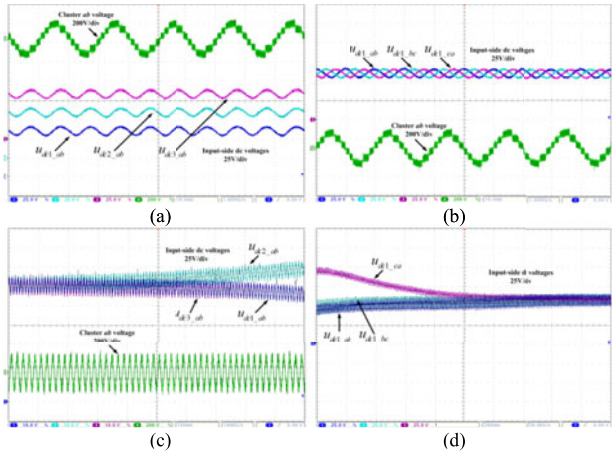

Fig. 14. Experimental waveforms of input-stage-side dc-link voltage. (a) Three dc-link voltage waveforms in one phase. (b) Three dc-link voltage waveforms in three phases. (c) Individual balancing control. (d) Cluster balancing control.

shows the dynamic process waveforms of adding positive reactive power command and removing negative reactive power command, respectively. The seven-level voltage waveform is the one of input-stage cluster *ab* output voltage. In the experiment, the grid voltage is generated by a programmable voltage source, and a line-frequency step-down transformer is connected between the voltage source and prototype to protect the voltage source. The voltage waveforms shown in Fig. 13(a) and (b) are the voltage source output voltage ones. The input-stage-side dc-link capacitor voltage is 60 V. Fig. 13(c) shows the three-phase grid-side current waveform.

Fig. 14 shows the input-stage-side dc-link capacitor voltage experimental waveforms. Fig. 14(a) and (b) shows the three dc-link capacitor voltage waveforms in one phase and three phases, respectively. As is shown, the input-stage dc-link voltages are maintained to reference value 60 V and well balanced in a steady state. Moreover, another two experiments to verify the individual and cluster balancing control are conducted, respectively. For the sake of simplicity, each output-stage-side dc-link capacitor is paralleled with a 40-Ω resistor, and the output stage is cancelled in these two experiments. As shown in Fig. 14(c), three dc-link capacitor voltages become unbalanced when the individual balancing control is removed (cluster balancing control is still working). In order to show the effect of cluster balancing control more obvious, the three DAB output voltages of cluster ca are set only 40 V, which is half of the ones in the other two clusters. As shown in Fig. 14(d), at the beginning of the experiment, the cluster balancing control is removed (individual balancing control is still working), and three dc-link capacitor voltages in three phase are unbalanced; then, the cluster balancing control is added (individual balancing control is still working), and three dc-link capacitor voltages in three phase finally become balanced. The input-stage experimental results verify the input-stage control.

Fig. 15 shows the output-stage-side dc-link capacitor voltage experimental waveforms. With the aforementioned DAB control, the output-stage-side dc-link capacitor voltages track the reference voltage 80 V well and are well balanced in a steady

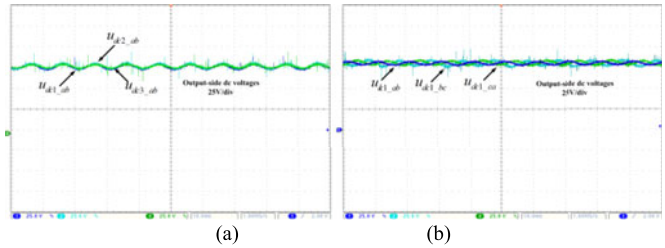

Fig. 15. Experimental waveforms of output-stage-side dc-link voltage. (a) Three dc-link voltage waveforms in one phase. (b) Three dc-link voltage waveforms in three phases

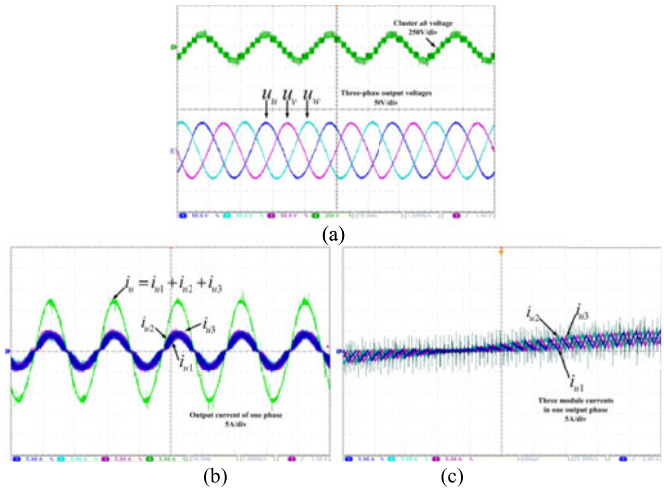

Fig. 16. Experimental waveforms of output voltage and current in output stage. (a) Three-phase output voltage waveforms. (b) Three output current waveforms in one phase. (c) Interleaving effect.

state. Fig. 15(a) and (b) shows the three dc-link capacitor voltage waveforms in one phase and three phases, respectively. These experimental results verify the isolation-stage control.

Fig. 16 shows the experimental waveforms of output voltage and current in the output stage. The output phase voltage reference amplitude is set 70 V. Fig. 16(a) shows the output three-phase voltage waveforms. The inductance tolerance among the output *LC*-filter inductors is about 5%. With the output-stage control, the parallel-connected module currents in one phase are well balanced, which is shown in Fig. 16(b). The current waveform of the 4th channel in Fig. 16(b) is obtained by sensing three inductor currents, which shows the interleaving effect. Fig. 16(c) shows the interleaving effect more obviously among three modules in one phase. These experimental results verify the output-stage control.

VI. Conclusion

In this paper, it is focused on a three-phase three-stage H-bridge-based PET topology, which consists of an input stage with series-connected H-bridge converters, an isolation stage with several independent DAB converters, and an output stage with parallel-connected H-bridge converters. This PET suffers dc-link voltage and power unbalancing issue, and the parallel-connected module current sharing issue. In order to deal with these issues for this PET, a system control structure is proposed,

which is comprised of input-stage control, isolation-stage control, and output-stage control. The input-stage control is responsible for power quality control and input-side dc-link voltage balancing control. The isolation-stage control is responsible for output-side dc-link voltage control. The output-stage control is responsible for output voltage control and parallel-module current-sharing control. This system control structure could be a reference for other three-phase PET topologies having the similar structure. Different individual module dc-link balancing control methods for the input stage are analyzed and compared. Moreover, a three-phase downscaled laboratory prototype is designed, constructed, and tested to verify the control strategy.

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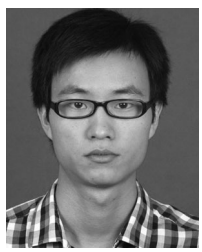

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