Analysis and Design of Modified Half-Bridge Series-Resonant Inverter With DC-Link Neutral-Point-Clamped Cell

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***Abstract*—In this paper, a modified half-bridge (HB) resonant inverter topology with a dc-link neutral-point-clamped cell is proposed. A pseudo asymmetrical voltage-cancellation PWM method and a control strategy are introduced. The proposed topology can maximize the inverter output power factor, and minimize variations in the switching frequency. In addition, most switches are clamped to half of the dc input voltage at turn-off, increasing the overall efficiency of the system for a wide load range. The efficiency of the proposed inverter is improved up to 7% at light-load conditions compared with that of the conventional HB inverter. Informative expressions for performance comparison between the proposed inverter and its counterpart are provided. In addition, the losses in the inverter primary components are analytically analyzed in detail. For validation, a 120-W prototype is implemented, and experimental results are presented.**

***Index Terms*—DC-link neutral-point-clamped cell (NCC), modified half-bridge (MHB), pseudo asymmetrical voltage cancellation (pseudo AVC), series-resonant inverter, zero-voltage switching (ZVS).**

I. Introduction

FULL-BRIDGE (FB) and half-bridge (HB) resonant conversion topologies have been widely applied to dc–dc converters for switched-mode power supply system, photovoltaic power conversion system, and battery chargers of electric vehicles (EVs) [1]–[10]. Along with these applications, induction heating systems are typical examples of dc–ac inverters that use both topologies [11]–[15]. Recently, contactless inductive power transfer systems, mostly developed for low-power applications, have been shifted to higher power levels such as in EV chargers [16]–[20]. The main purpose of the power conversion system is doubtless the efficient energy transfer from the source to the load with little loss. Thus, resonant converter/inverter topologies are a good solution to minimize losses through soft switching for a wide load range. In these fields, recent studies have focused on evenly increasing system efficiency over a wide load range, especially from middle- to low-load ranges [10], [11], [17], [21]. The selection criteria for FB/HB topologies basically depends on the power, control possibilities, and applications. Fig. 1 shows a comparison of the FB and HB inverter topologies in the literature according to the power levels used in practical applications. Considering short-time rating operation with better cooling geometries, the HB topology is allowed to operate at higher power levels of more than 2 kW. In actual practice, HB resonant inverters are suitable for systems of less than 2 kW from the point of view of cost performance. However, the HB resonant inverter suffers from rather limited control possibilities such as frequency modulation (FM) and asymmetrical duty cycle (ADC) controls [1], [11]. In the FM control method, the switching frequency of the inverter is rapidly ramped up under low-load conditions, resulting in increased switching losses. On the other hand, the ADC control method, considered as an alternative solution to reduce switching losses, unbalances the resonant current, resulting in aggravated partial saturation in the magnetic components. To overcome the limitations of the FM and ADC control methods, asymmetrical voltage-cancellation (AVC) control method has been presented [12]. The AVC control method can reduce the phase of the *h*th-order harmonic of a square-wave inverter output voltage in comparison with the ADC control method, resulting in maximization of the phase difference between the voltage and current of the inverter output. The duty cycle can be adjusted for lighter load, while ensuring a zero-voltage switching (ZVS) operation, which implies that the AVC control method can minimize the switching frequency variation according to the load and output power, thus increasing the efficiency. Unfortunately, this control method can be applied only to an FB inverter topology, but not to an HB

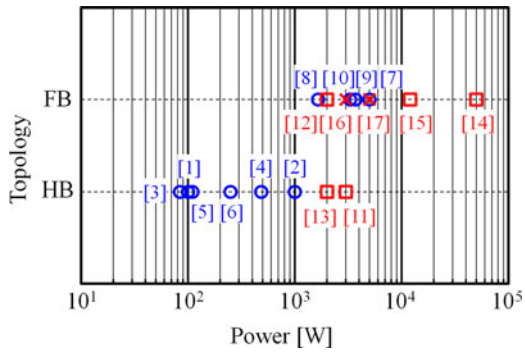

Fig. 1. Comparison of the FB/HB inverter topologies according to power levels.

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inverter topology because of its topological limitation. Moreover, all switches in the HB inverter are stressed by the dc input voltage at turn off. The turn-off switching loss is proportional to the magnitude of the switch voltage during turn-off transition. As the dc-link voltage clamped circuits, the three-level inverter topologies, such as neutral-point-cell inverter, have been widely applied in various industry. Compared with the FB and HB inverters, the three-level inverter is regarded as a good solution for high-power applications, but it could be a reluctant circuit for small and medium power ranges with respect of limited mounting space and implementation cost [22], [23]. Several of the aforementioned drawbacks result in strong motivation for an advanced topology development for small and medium power applications.

In this paper, a modified half-bridge (MHB) resonant inverter topology with a dc-link neutral-point-clamped cell (NCC) is proposed. NCC is realized by a common-drain connection of two MOSFETs. In the proposed topology, two switch pairs exist in which one switch of the bridge leg and one switch of the NCC complementarily operate with each other. One switch pair is controlled by varying the duty cycle during a half-switching period, and the other pair is fixed by a half-duty cycle during one switching period. Because of this operation, the proposed series-resonant inverter topology offers attractive advantages over the conventional HB series-resonant inverter topology. First, the pseudo AVC control method, which shows similar characteristics to the AVC control method of an FB inverter, can be implemented for the HB inverter topology. The proposed control method generates an inverter output voltage step-shaped wave according to the duty cycle ratio. Therefore, the power factor (PF) of the inverter output and the switching frequency variation under load conditions can be significantly improved. Second, because the two switches added to the neutral point and one switch of the HB leg are always clamped to half of the dc input voltage during turn off, the switching turn-off losses can be remarkably reduced. In addition, controlling the HB inverter using the voltage-cancellation control method can alleviate the unbalanced-current problem in a resonant network caused by the ADC control method.

In Section II, detailed analysis about the operating modes and the main derivations of the proposed inverter topology are presented. In addition, along with the design procedure for the resonant parameters, the performance results of the FM-controlled HB, ADC-controlled HB, and the proposed MHB inverters in terms of the inverter output total harmonic distortion (THD) and PF are compared, and the optimum control strategy for the proposed inverter topology is presented in Section III. Section IV shows the analytical results of the various losses. The experimental results are presented in Section V to validate the theoretical analysis.

II. Operating Principle and Analysis of the Proposed Inverter

Fig. 2 shows the circuit diagram of the proposed inverter. It is a combination of the conventional HB inverter with an additional NCC composed of switches S_3 and S_4. The inverter

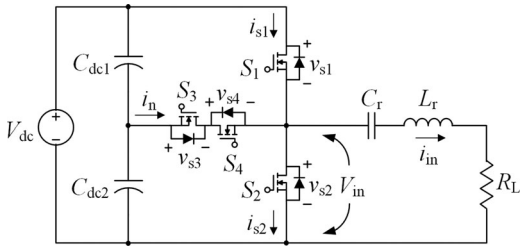

Fig. 2. Circuit diagram of the proposed inverter.

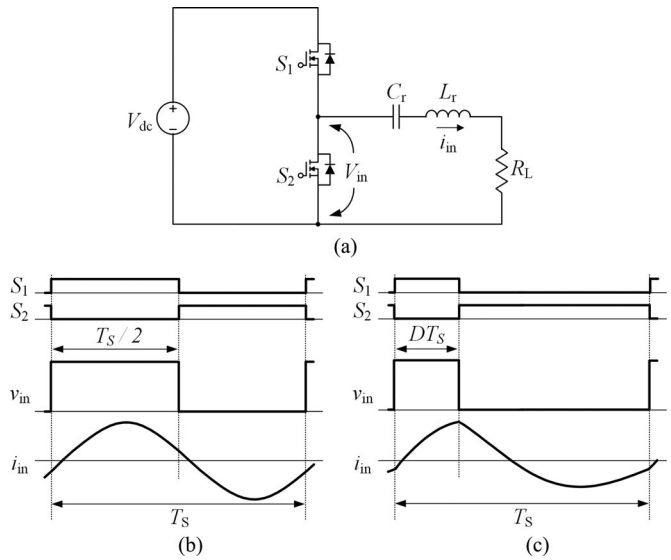

Fig. 3. Conventional HB inverter and main waveforms according to the control schemes. (a) Circuit diagram. (b) FM control scheme. (c) ADC control scheme.

is analyzed in steady state, and for simplicity, several things are assumed which are as follows.

1) The two input capacitors in series, namely $C_{\rm dc1}$ and $C_{\rm dc2}$ are large enough to be considered as two constant voltage sources with a $V_{\rm dc}/2$ value.
2) The resonant current is approximated to be sinusoidal for large loaded quality factor Q.
3) The output capacitances of the MOSFETs have the same values as that of $C_{\rm oss}$ but are ignored in the mode analysis.

A. Operational Principle

Before the operation description of the proposed inverter, the typical operating waveforms of a conventional HB inverter with FM and ADC control schemes are shown in Fig. 3. In the FM-controlled HB inverter, the control variable is the switching frequency with a fixed duty cycle $D = 0.5$, and the ADC-controlled HB inverter changes the switching frequency and duty cycle for the loads. In the proposed inverter, one switch pair is composed of S_1 and S_3, and the other pair is composed of S_2 and S_4. One of both pairs is duty controlled during one-half switching period $T_S/2$, and the other pair is fixed by a 0.5 duty cycle during one switching period T_S. Therefore, two redundant switching states exist in the proposed inverter topology to control the power

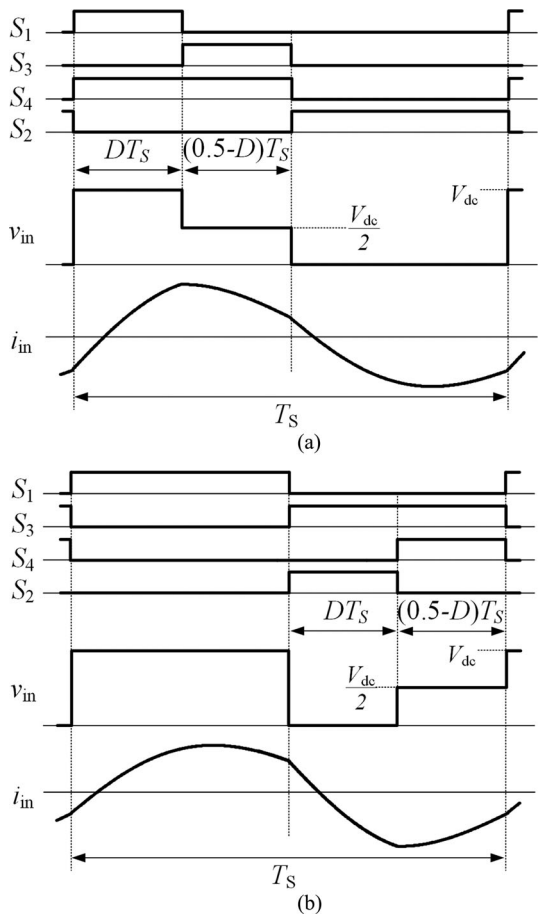

Fig. 4. Operating waveforms for different switching states in the proposed inverter topology. (a) Switching state I. (b) Switching state II.

transferred to the load as shown in Fig. 4. Both switching states I and II are identical in terms of electrical characteristics. This paper focuses on the analysis of switching state I.

The steady-state operation of the proposed inverter topology includes five modes in one switching period T_S. The operating modes and typical waveforms are shown in Fig. 5.

Mode 1 $[t_0, t_1]$ Prior to t_0, switch S_2 is turned OFF. The current through the resonant network $i_{\rm in}$ is conducted through the antiparallel diode of switch S_1. During this interval, switch S_1 can achieve ZVS operation; its turn-on switching loss is eliminated. Even though switch S_4 in the NCC is simultaneously turned on with switch S_1, the resonant current cannot flow through the NCC because the antiparallel diode of switch S_3 in the NCC blocks the switch voltage to $V_{\rm dc}/2$ by turn-off switching.

Mode 2 $[t_1, t_2]$: After t_1, resonance changes the resonant current into the positive direction. Power is transferred from the dc-link voltage $V_{\rm dc}$ to the load. Similar to Mode 1, the resonant current does not flow through the NCC because of the blocking voltage of switch S_3. This mode is the same as that of the conventional HB inverter operation. One difference is that switch S_1 is turned ON during DT_S. Therefore, the conduction loss of switch S_1 can be reduced.

Mode 3 $[t_2, t_3]$: As switch S_1 is turned OFF and switch S_3 is turned ON at t_2, the NCC begins to conduct by dividing the resonant current. It can be observed that the turn-off voltage across switch S_1 is clamped to $V_{\rm dc}/2$ compared with that in the traditional HB inverter, reducing the turn-off loss of switch S_1. During this mode, switch S_3 operates as a synchronous rectifier except for a short dead time. In addition, switch S_4 is turned ON under ZVS condition.

Mode 4 $[t_3, t_4]$: At t_3, all switches in the NCC are turned OFF. The current through the resonant network $i_{\rm in}$ is conducted through the antiparallel diode of switch S_2. During this interval, switch S_2 can achieve a ZVS operation, eliminating its turn-on switching loss. Moreover, because switch S_4 in the NCC can only withstand $V_{\rm dc}/2$, the turn-off switching loss of S_4 remarkably decreases.

Mode 5 $[t_4, t_5]$: The resonant current flows through switch S_2 in the negative direction. The stored energy in the resonant network is transferred to the load. This mode is the same as that in the conventional HB inverter operation.

B. Voltages, Currents, and Power

Fig. 5(b) shows the steady-state operating waveforms of the proposed inverter under an arbitrary load. The time variation and the phase of the *h*th-order harmonic of the square-wave input voltage $v_{\rm in}$ can be expressed through a Fourier series [2], as shown in (1) and (2).

In (1), the dc component is blocked by series capacitor C_r; thus, the ac component of $v_{\rm in}$ contributes to the flow of $i_{\rm in}$ through the resonant network. In addition, although a square-wave voltage is applied to the resonant network, the filtering action of the series resonant network forces the current through the network to become sinusoidal. Therefore, the rms value of the fundamental resonant current is sufficient for power analysis of the proposed inverter. The time-varying expression of the fundamental current of $i_{\rm in}$ through the resonant network results in

$$\theta_{\rm h} = \tan^{-1}\left(\frac{\sin(2\pi Dh)}{2-\cos(\pi h)-\cos(2\pi Dh)}\right) \quad (2)$$

$$i_{\rm in1}(t) = \frac{V_{\rm in1}}{Z_{\rm in1}}\sin(\omega t+\theta_1-\phi_1). \quad (3)$$

In (3), $V_{\rm in1}$ represents the fundamental component of the resonant input voltage, and θ_1 is the phase of the fundamental voltage of $v_{\rm in}$. $Z_{\rm in1}$ and θ_1 represent the resonant network impedance and the phase delay between $v_{\rm in}$ and $i_{\rm in}$ for the fundamental

$$v_{\rm in}(t) = \frac{1}{2}V_{\rm dc}\left(D+\frac{1}{2}\right) + \frac{V_{\rm dc}}{2\pi}\sum_{h=1}^{\infty}\frac{1}{h}\sqrt{6-4\cos(\pi h)-4\cos(2\pi Dh)+2\cos(\pi h)\cos(2\pi Dh)}\sin(h\omega t+\theta_h) \quad (1)$$

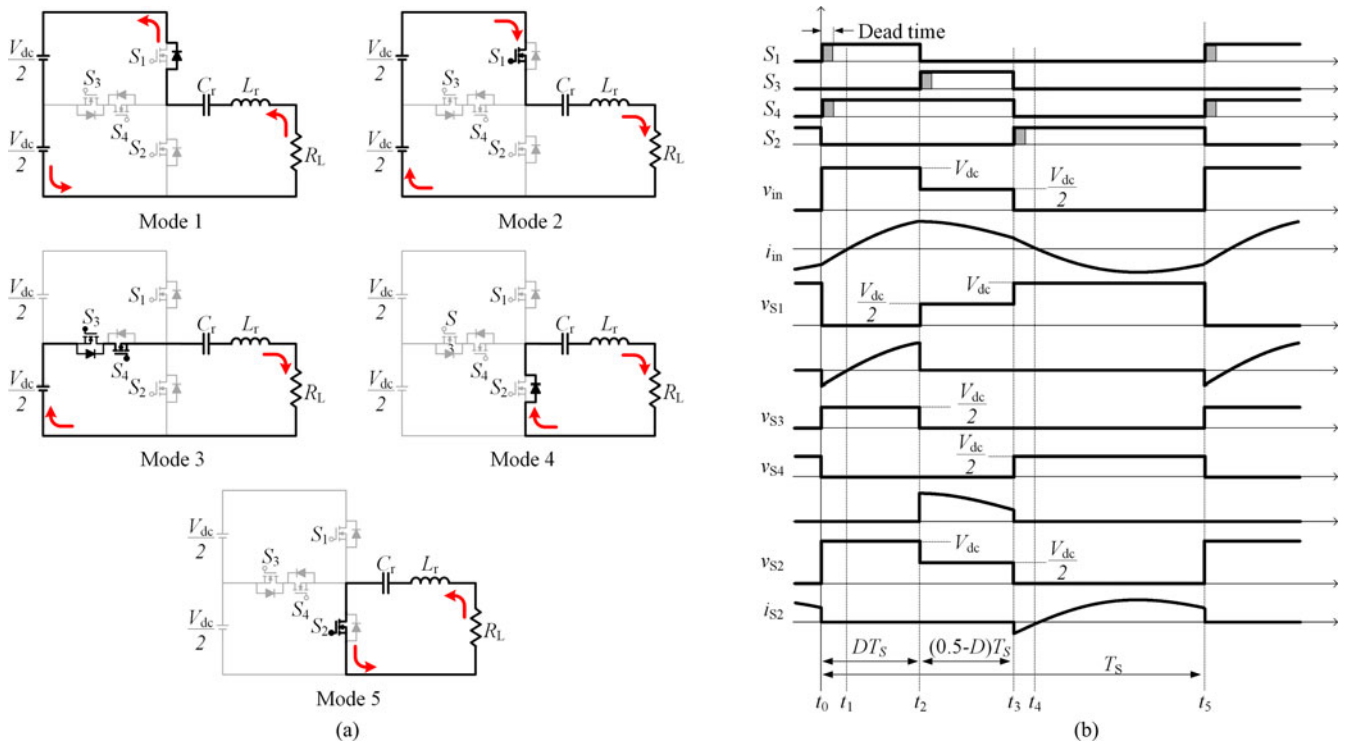

Fig. 5. Proposed inverter operation for switching state I. (a) Operating modes. (b) Typical waveforms.

harmonic, respectively. They are expressed as

$$V_{\text{in1}} = \frac{\sqrt{2}V_{\text{dc}}}{2\pi}\sqrt{5-3\cos(2\pi D)},$$
$$\theta_1 = \tan^{-1}\left(\frac{\sin(2\pi D)}{3-\cos(2\pi D)}\right) \quad (4)$$
$$Z_{\text{in1}} = R\sqrt{1+Q^2\left(\omega_n-\frac{1}{\omega_n}\right)^2},$$
$$\phi_1 = \cos^{-1}\left(\frac{R}{Z_{\text{in1}}}\right) \quad (5)$$

where R_L is the load resistance, $Q(=\sqrt{L_r/C_r}/R_L)$ is the loaded quality factor, $\omega_o(=1/\sqrt{L_rC_r})$ is the angular resonant frequency, and $\omega_n(=\omega_s/\omega_o)$ is the normalized angular switching frequency.

In this section, the detailed analysis of the input and output power is presented, and the related expressions are derived. The maximum value of the resonant current can be obtained by substituting (4) into (3) as

$$I_m = \frac{\sqrt{2}V_{\text{dc}}}{2\pi Z_{\text{in1}}}\sqrt{5-3\cos(2\pi D)}. \quad (6)$$

Using (5) and (6), the output power transferred to the load is expressed as

$$P_o = \frac{I_m^2 R_L}{2} = \frac{V_{\text{dc}}^2(5-3\cos(2\pi D))}{4\pi^2 R_L\left[1+Q^2\left(\omega_n-\frac{1}{\omega_n}\right)^2\right]}. \quad (7)$$

In (7), the output power for $D=0.5$ and $\omega_n=1$ is defined as the peak output power $P_{o,\text{pk}}$

$$P_o|_{\omega_s=\omega_o\ \&\ D=0.5} = P_{o,\text{pk}} = \frac{2V_{\text{dc}}^2}{\pi^2 R_L}. \quad (8)$$

Fig. 6 shows the output power normalized by (8). The decrease in the duty cycle reduces the output power at the same frequency. On the other hand, it can be observed that the switching frequency decreases with the reduction in the duty cycle, while maintaining the same output power. In particular, the decrease in the switching frequency is distinguishable under a light load, which means that the decrease in the switching frequency can alleviate the switching losses and eventually enhance the inverter efficiency. However, the range of the output power transferred through an adjustment in D at a fixed switching frequency is limited.

Fig. 7 shows the relationship of the output power and D, obtained from (7), with certain circuit parameters. Theoretically, the minimum output power, which the proposed MHB inverter can deliver to the load by reducing only the duty cycle from 0.5 to 0 at a fixed switching frequency, is limited to 25% of the maximum output power. It demands a small increase in the switching frequency to deliver power of less than 25%. Nevertheless, implementing the proposed inverter can yield some benefits compared with the conventional HB inverter in terms of efficiency and PF.

The dc input power can be obtained by the integral of the currents through switches S_1, S_3, and S_4 for one switching period, as shown in Fig. 4(a) and (b). The average current through S_1

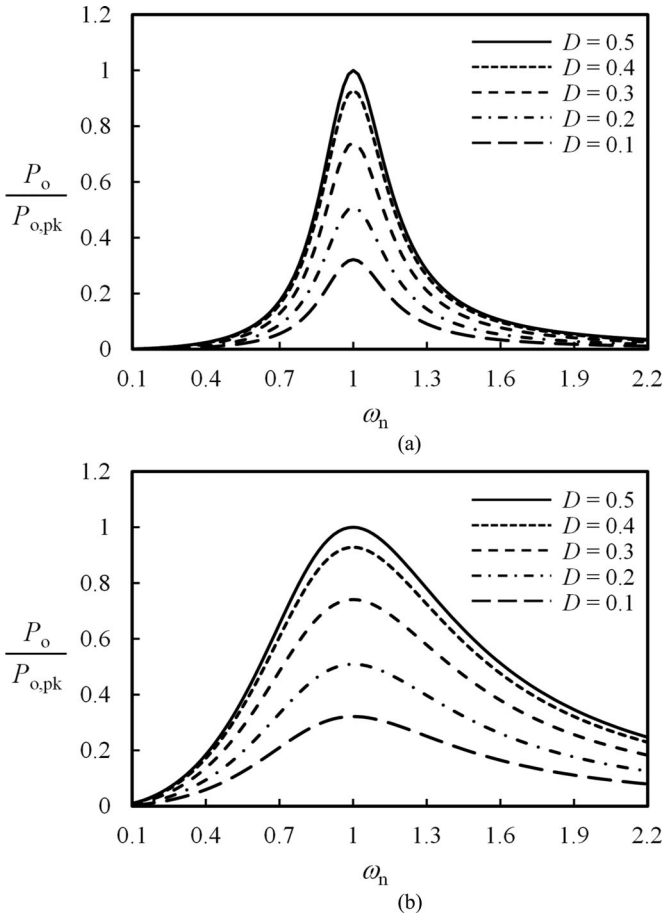

Fig. 6. Normalized output power as function of ω_n and D under different quality factors. (a) $Q = 5$. (b) $Q = 1$.

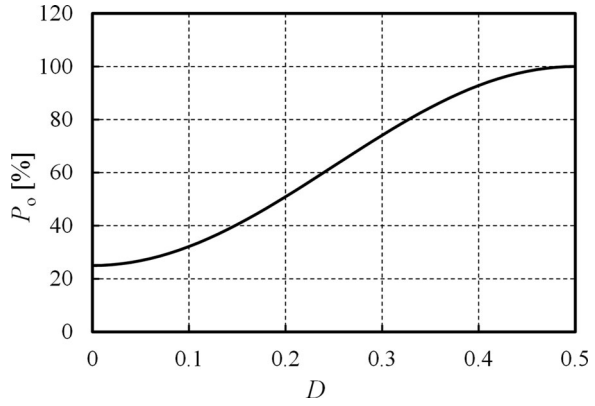

Fig. 7. Output power versus D.

during DT_S and the average current through the NCC during DT_S to $T/2$ are given by

$$I_{\mathrm{S1,avg}} = \frac{I_m}{2\pi}\left[\cos\left(\theta_1 - \phi_1\right) - \cos\left(2\pi D + \theta_1 - \phi_1\right)\right] \quad (9)$$

$$I_{n,\mathrm{avg}} = \frac{I_m}{2\pi}\left[\cos\left(\theta_1 - \phi_1\right) + \cos\left(2\pi D + \theta_1 - \phi_1\right)\right]. \quad (10)$$

TABLE I
GIVEN ELECTRICAL SPECIFICATIONS

Parameters	Values
Rated dc input voltage V_{dc}	48 V
Maximum inverter output power $P_{o,\mathrm{max}}$	120 W
Range of output power	10%–100%
Resonant frequency f_o	80 kHz
Ratio of switching to resonant frequency f_n	1.2

It should be noted that i_n through the NCC (S_3 and S_4) is fed by $V_{\mathrm{dc}}/2$. Thus, the dc input power is expressed as

$$\begin{aligned} P_{\mathrm{in}} &= V_{\mathrm{dc}}\left(I_{\mathrm{S1,avg}} + \frac{1}{2}I_{n,\mathrm{avg}}\right) \\ &= \frac{V_{\mathrm{dc}} I_m}{4\pi}\left[3\cos\left(\theta_1 - \phi_1\right) - \cos\left(2\pi D + \theta_1 - \phi_1\right)\right]. \end{aligned} \quad (11)$$

III. DESIGN OF THE PROPOSED INVERTER

In this section, the optimum control scheme for the proposed inverter that ensures less harmonics, high PF, and high efficiency under ZVS conditions is presented, along with the design of the resonant parameters. Although the scaled 120-W prototype inverter is a relatively low-power model, it is sufficient to show the advantages of the proposed inverter by evaluating several performance results against the conventional HB inverter with FM and ADC controls under the same power.

A. Circuit Parameters for ZVS Conditions

Under given circuit conditions, maximum inverter output power is transferred to the load at duty cycle $D = 0.5$. The operation at $D = 0.5$ is the same as that in the conventional HB inverter because the NCC does not operate. Thus, the circuit parameters under operation at $D = 0.5$ can be determined. The necessary electrical specifications are listed in Table I to obtain the circuit parameters such as the resonant inductance, resonant capacitance, and load resistance.

The minimum switching frequency should preferably have a 20% margin based on the resonant frequency considering parameter variation and stray components.

As mentioned earlier, the inverter overall resistance R consists of R_L and R_{loss}, which is the total parasitic resistance that includes the on-resistances of the MOSFETs, equivalent series resistances of L_r and C_r, and the resistance of the other components. The maximum inverter output power $P_{o,\mathrm{max}}$ from (7) for $D = 0.5$ can be expressed as

$$P_{o,\mathrm{max}} = \frac{2V_{\mathrm{dc}}^2}{\pi^2 R_L\left[1 + \frac{1}{R_L^2} \times \left(\frac{L_r}{C_r}\right) \times \left(\omega_n - \frac{1}{\omega_n}\right)^2\right]}. \quad (12)$$

Rearranging (12) to obtain L_r and C_r yields

$$L_r = \frac{\sqrt{A \cdot R_L - R_L^2}}{\omega_o \times \left(\omega_n - 1/\omega_n\right)}, \quad C_r = \frac{1}{\omega_o^2 L_r} \quad (13)$$

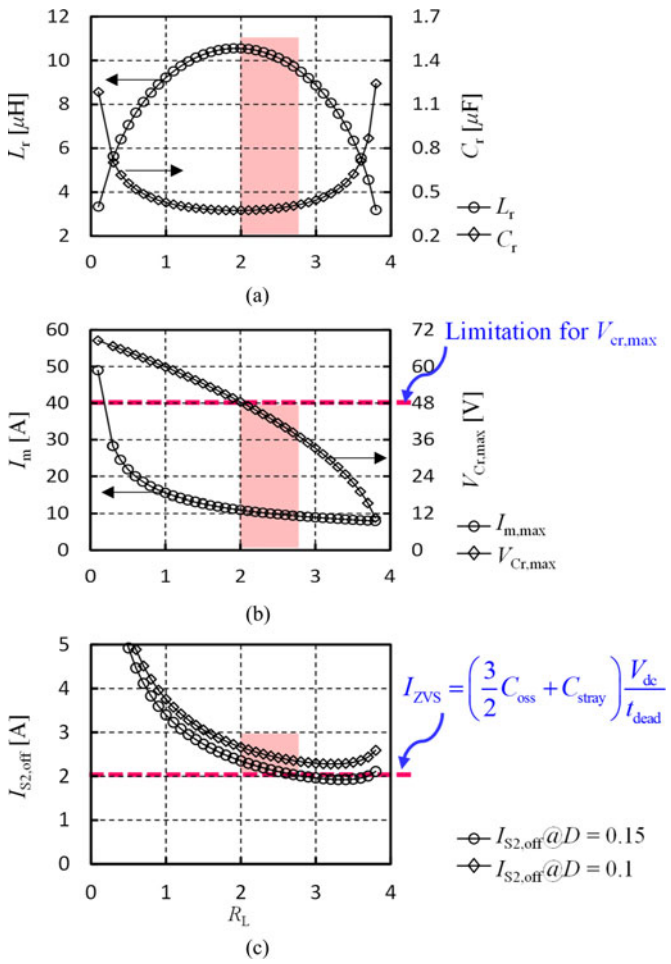

Fig. 8. Range of resonant parameters for ZVS operation. (a) L_r and C_r versus R_L. (b) I_m and $V_{\mathrm{Cr,max}}$ versus R_L. (c) $I_{\mathrm{S2,off}}$ versus R_L according to D for 10% load.

TABLE II
RANGE OF RESONANT PARAMETERS

Parameters	Values
Load resistance R_L	2–2.8 Ω
Resonant inductance L_r	9.5–10.6 μH
Resonant capacitance C_r	375.1–417.4 nF

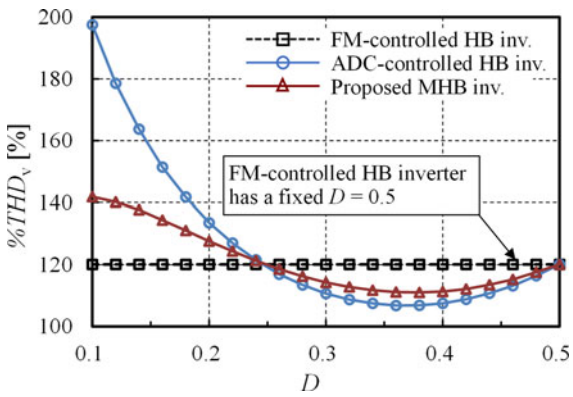

Fig. 9. Percent THD values of the inverter output voltage according to D.

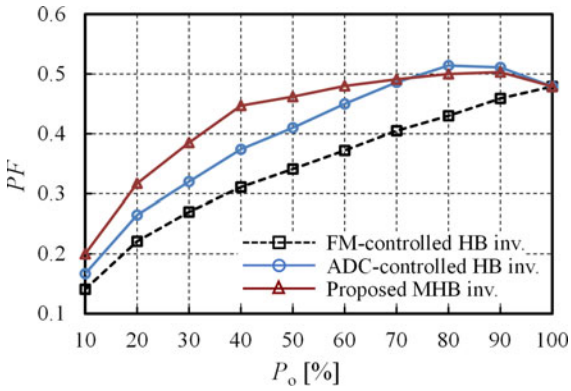

Fig. 10. Inverter output PF versus. P_o.

where $A = (2V_{\mathrm{dc}}^2)/(\pi^2 P_{o,\max})$.

Considering the given specifications, L_r in (13) is a function of the inverter load resistance R_L, where C_r is dependent on L_r. Therefore, L_r and C_r can be lots of values depending on the R_L value. Practically, a constraint on the value of R_L can be derived from the numerator of the formula related to L_r in (13) to satisfy the desired power requirement as given by

$$R_L < \frac{2V_{\mathrm{dc}}^2}{\pi^2 P_{o,\max}}. \tag{14}$$

In the proposed inverter, the load resistance R_L is limited to less than 3.8 Ω for circuit conditions listed in Table I. Evaluating which values are valid among the candidates for the resonant inductance and capacitance corresponding to the R_L values is necessary. The current through the resonant network and the voltage across the resonant capacitor can be good criteria in selecting the optimum parameters. The lower the resonant current is, the smaller is the conduction losses of the components. On the other hand, the lower the resonant capacitor voltage is, the smaller is the physical size of the capacitor. For $D = 0.5$, the maximum resonant current can be derived from (5) and (6) as

$$I_{m@D=0.5} = \frac{2V_{\mathrm{dc}}}{\pi R_L \sqrt{1 + \frac{1}{R_L^2} \times \left(\frac{L_r}{C_r}\right) \times \left(\omega_n - \frac{1}{\omega_n}\right)^2}}. \tag{15}$$

The maximum voltage across the resonant capacitor can be obtained using (15) as

$$V_{Cr,\max} = \frac{I_{m@D=0.5}}{\omega_s C_r} = \frac{2V_{\mathrm{dc}}}{\pi\omega_n \sqrt{\frac{R_L^2 C_r}{L_r} + \left(\omega_n - \frac{1}{\omega_n}\right)^2}}. \tag{16}$$

Satisfying the ZVS operation to increase the efficiency for a wide range of load is most essential. The first condition for ZVS in all switches can be obtained from (3) as

$$\phi_1 - \theta_1 \geq 0. \tag{17}$$

However, (17) is only a necessary condition for ZVS operation but is not sufficient. Parasitic capacitances such as the MOSFET output capacitance C_{oss} and stray capacitance C_{stray}

TABLE III
INVERTER OUTPUT VOLTAGE, CURRENT, AND VOLTAGE PHASE FOLLOWED BY FOURIER SERIES FOR DIFFERENT TOPOLOGIES

FM-HB Inverter	$iv_{in}(t)=\frac{1}{2}V_{dc}+\frac{V_{dc}}{2\pi}\sum_{h=1}^{\infty}\left[\frac{1}{h}\sqrt{4-8\cos(\pi h)+4\cos^2(\pi h)}\sin(h\omega t+\theta_h)\right]$ $i_{in}(t)=\frac{V_{dc}}{2\pi}\sum_{h=1}^{\infty}\left[\frac{1}{Z_{inh}h}\sqrt{4-8\cos(\pi h)+4\cos^2(\pi h)}\sin(h\omega t+\theta_h-\phi_h)\right]$	$\theta_h=0$
ADC-HB Inverter	$v_{in}(t)=V_{dc}D+\frac{V_{dc}}{2\pi}\sum_{h=1}^{\infty}\left[\frac{1}{h}\sqrt{8-8\cos(2\pi hD)}\sin(h\omega t+\theta_h)\right]$ $i_{in}(t)=\frac{V_{dc}}{2\pi}\sum_{h=1}^{\infty}\left[\frac{1}{Z_{inh}h}\sqrt{8-8\cos(2\pi hD)}\sin(h\omega t+\theta_h-\phi_h)\right]$	$\theta_h=\tan^{-1}\left(\frac{\sin(2\pi Dh)}{1-\cos(2\pi Dh)}\right)$
Proposed Inverter	$v_{in}(t)=\frac{1}{2}V_{dc}\left(D+\frac{1}{2}\right)+\frac{V_{dc}}{2\pi}\sum_{h=1}^{\infty}\left[\frac{1}{h}\sqrt{6-4\cos(\pi h)-4\cos(2\pi Dh)+2\cos(\pi h)\cos(2\pi Dh)}\sin(h\omega t+\theta_h)\right]$ $i_{in}(t)=\frac{V_{dc}}{2\pi}\sum_{h=1}^{\infty}\left[\frac{1}{Z_{inh}h}\sqrt{6-4\cos(\pi h)-4\cos(2\pi Dh)+2\cos(\pi h)\cos(2\pi Dh)}\sin(h\omega t+\theta_h-\phi_h)\right]$	$\theta_h=\tan^{-1}\left(\frac{\sin(2\pi Dh)}{2-\cos(\pi h)-\cos(2\pi Dh)}\right)$

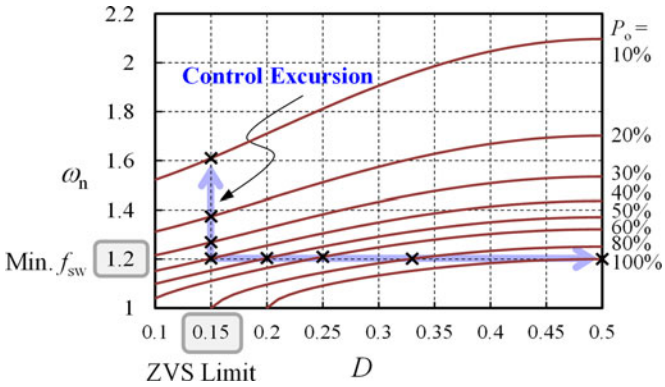

Fig. 11. Normalized angular switching frequency as a function of D for $R_L = 2\ \Omega$.

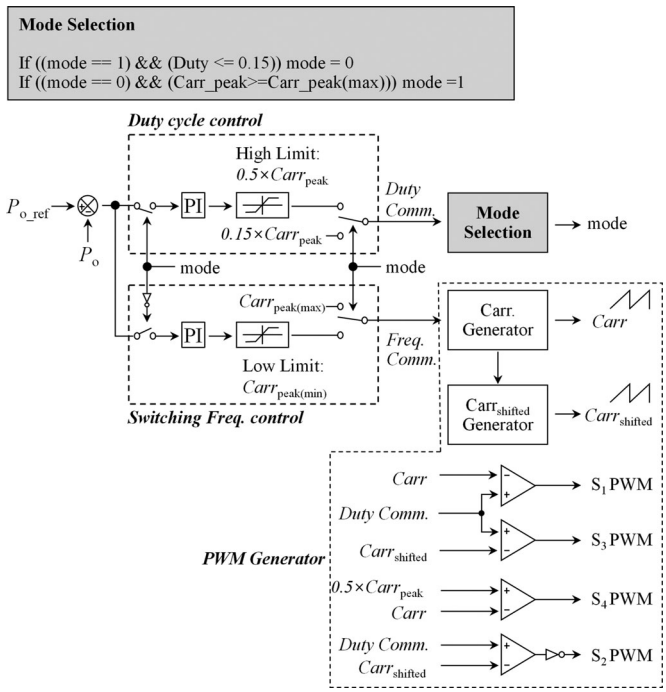

Fig. 12. Control block diagram of the proposed MHB resonant inverter.

require enough energy for charging and discharging during dead time $t_{\rm dead}$ of Modes 1 and 4, as shown in Fig. 5. The other ZVS conditions of the proposed inverter are as follows:

$$I_{\rm S4,off} > (3C_{\rm oss} + C_{\rm stray}) \times \frac{V_{\rm dc}}{2t_{\rm dead}} \tag{18}$$

$$I_{\rm S2,off} > \left(\frac{3}{2}C_{\rm oss} + C_{\rm stray}\right) \times \frac{V_{\rm dc}}{t_{\rm dead}} \tag{19}$$

where $I_{\rm s2,off}$ and $I_{\rm s4,off}$ are the turn-off current values when S_2 and S_4 are turned OFF at $t = T/2$ and T, respectively.

Equations (2) and (5) show that ϕ_1 does not depend on D but is proportional to the switching frequency, where θ_1 is inversely proportional to D. To satisfy (17) for lighter loads, the increment in the switching frequency of the inverter should be minimized by reducing D up to the available limitation value to reduce the switching losses while maintaining ZVS. In addition, determination of the ZVS ranges of all switches is very appropriate by investigating whether the switch turn-off currents satisfy the necessary requirements of (18) and (19) for the loads. Therefore, determining the relationship between the switching frequencies and duty cycles available for the loads is necessary to investigate the switch turn-off currents, and the impedance magnitude of the resonant network has to be calculated from the deduced switching frequencies. The relationship can be derived from (7) and is expressed as

$$\omega_n = \frac{1}{2}\sqrt{\frac{5-3\cos(2\pi D)}{8KQ^2} - \frac{1}{Q^2}} + \frac{1}{2}\sqrt{4+\left(\frac{5-3\cos(2\pi D)}{8KQ^2} - \frac{1}{Q^2}\right)} \tag{20}$$

where $K = \left(\pi^2 P_o R_L\right) / \left(2V_{\rm dc}^2\right)$. Because the values of the resonant inductance and capacitance are dependent on R_L from (13), the value of Q in (20) is fixed according to each value of R_L.

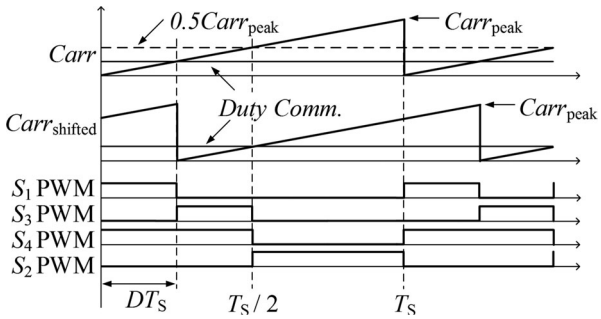

Fig. 13. PWM generation of the gate drive signals.

Fig. 8 shows the resonant inductances and capacitances, maximum inductor current and capacitor voltage, and switch turn-off currents as a function of the load resistance. Fig. 8(a) shows that the resonant inductance and capacitance corresponding to the value of R_L obtained from (14). Fig. 8(b) shows that the maximum capacitor voltage is smaller as the load resistance is larger. On the other hand, the maximum inductor current tends to be saturated. Thus, the limitation for the maximum capacitor voltage is chosen to be the dc input voltage. In particular, Fig. 8(c) shows the switch turn-off currents according to *D* for the lightest load, which is the worst case for ZVS operation. Considering the minimum duty cycle and dead time, the switch turn-off current must satisfy (18) and (19). The available range of values of the resonant parameters to maintain ZVS operation for 10%–100% load is listed in Table II.

B. Comparison of the Harmonic Components and PF

The conventional HB inverter operated by the FM and ADC control schemes and the proposed MHB inverter operated by the pseudo AVC control scheme are compared with respect to the harmonic components and PF of the inverter output. The aim is to determine which topology can produce a lower THD. A lower THD increases the resonant current quality, leading to the reduction in magnetic component losses. Fig. 9 shows the percent THD_v values in the inverter output voltage of both inverters with different control schemes. The percent THD formula is well defined in [24]. In Fig. 9, the dotted line shows the constant percent THD_v values of the HB inverter operated by FM control at $D = 0.5$. Fig. 9 shows that the proposed MHB and ADC-controlled HB inverters have lower percent THD_v values up to $D = 0.25$ compared with the HB inverter with the typical FM control scheme. Although the ADC-controlled HB inverter appears to have a lower THD than the proposed MHB inverter, it is restricted in terms of only the output voltage harmonics. Evaluating the topologies from the perspective of the PF and ZVS operation is essential. The voltage and current of the inverter output become nonsinusoidal periodic waveforms, including the *h*th-order harmonics. In this case, the PF is represented as a ratio of apparent power *S* to active power *P* as

$$\mathrm{PF} = \frac{P}{S} = \frac{V_o I_o + \sum_{h=1}^{\infty} V_h I_h \cos\phi_h}{\sqrt{\sum_{h=0}^{\infty} V_h^2}\sqrt{\sum_{h=0}^{\infty} I_h^2}} \tag{21}$$

where V_o and I_o are the dc offset values and V_h and I_h are the rms magnitudes of each harmonic component.

Fig. 10 shows the PF values when the L_r and C_r values for $R_L = 2\,\Omega$ are selected as resonant parameters from the range of values given in the previous section. The proposed inverter can be distinguished compared with the other inverters for the entire load range. In the ADC-controlled HB inverter, the variable range of the duty cycle is extremely limited up to 80% load for ZVS operation. As a result, phase delay ϕ and the THD should be smaller to maximize the PF. ϕ is strongly dependent on the switching frequency, and the THD is dependent on the duty cycle. A higher PF can increase the active power, enhancing inverter efficiency.

Table III lists the main equations to calculate THD_v and the PFs of the FM and ADC-controlled HB and the proposed MHB inverters. In Table III, $Z_{\mathrm{in}h}$ represents the total resonant network impedance of the *h*th-order harmonic, and ϕ_h represents the phase delay of the *h*th-order harmonic between v_{in} and i_{in}. They are identically applicable to all topologies discussed in this paper owing to the same resonant network as expressed by

$$Z_{\mathrm{in}h} = R_L\sqrt{1 + Q^2\left(h\omega_n - \frac{1}{h\omega_n}\right)^2} \tag{22}$$

$$\phi_h = \tan^{-1}\left[Q\left(h\omega_n - \frac{1}{h\omega_n}\right)\right]. \tag{23}$$

C. PWM and Control Strategy

The greatest advantage of the proposed MHB series-resonant inverter is that the magnitude of the inverter output voltage can be varied with minimum switching frequency variation by adjusting the duty cycle to transfer energy to the load. Fig. 11 shows the normalized angular switching frequency versus the duty cycle for 10%–100% load at $R_L = 2\,\Omega$ using (20). Fig. 11 shows that decreasing the duty cycle can considerably lower the switching frequencies to deliver power corresponding to each load. The optimum control strategy available for the proposed inverter that minimizes the switching frequency variation could be considered. Thus, the control scheme of the proposed MHB resonant inverter consists of two parts: 1) duty cycle control at a fixed switching frequency and 2) frequency control at a fixed duty cycle for ZVS operation under light loads.

The controller consists of reference generators, mode selector, and PWM generators, as shown in Fig. 12. The reference generators generate the command signals for the duty cycle and the switching frequency to regulate the output power. The mode selector determines which one of the two control modes to use according to the power. If mode $= 1$, duty cycle *D* is only adjusted from 0.5 to 0.15 with a minimum switching frequency. If *D* becomes less than 0.15 in this duty cycle control mode, the control mode changes to the frequency control mode. Although the proposed inverter can operate under ZVS conditions as the duty cycle is below 0.15, it is desirable to limit the duty cycle to 0.15 due to dead time and DSP resolution problems when actually implemented. Therefore, the switching frequency is varied by fixed duty cycle $D = 0.15$. If the switching frequency reaches the minimum frequency for the frequency control mode, the mode changes to the duty cycle control mode again, which

TABLE IV
MAIN FORMULAS TO CALCULATE THE SWITCH LOSSES FOR DIFFERENT TOPOLOGIES

FM-controlled HB inverter	ADC-controlled HB inverter	Proposed inverter
Resonant rms current $I_{\text{in,rms}}\left(=I_{\text{m}}/\sqrt{2}\right)$ $\frac{\sqrt{2}V_{\text{dc}}}{\pi Z_{\text{in1}}}$	Resonant rms current $I_{\text{in,rms}}\left(=I_{\text{m}}/\sqrt{2}\right)$ $\frac{V_{\text{dc}}}{\pi Z_{\text{in1}}}\sqrt{1-\cos(2\pi D)}$	Resonant rms current $I_{\text{in,rms}}\left(=I_{\text{m}}/\sqrt{2}\right)$ $\frac{V_{\text{dc}}}{2\pi Z_{\text{in1}}}\sqrt{5-3\cos(2\pi D)}$
Switch-off current $I_{\text{S,off}}$ and voltage stress $S_1, S_2 \Rightarrow \ I_{\text{m}}\sin(\phi_1)\,\&\,V_{\text{dc}}$	Switch-off current $I_{\text{S,off}}$ and voltage stress $S_1 \Rightarrow \ I_{\text{m}}\sin(2\pi D+\theta_1-\phi_1)\,\&\,V_{\text{dc}}$ $S_2 \Rightarrow \ I_{\text{m}}\sin(\phi_1-\theta_1)\,\&\,V_{\text{dc}}$	Switch-off current $I_{\text{S,off}}$ and voltage stress $S_1 \Rightarrow \ I_{\text{m}}\sin(2\pi D+\theta_1-\phi_1)\,\&\,\frac{V_{\text{dc}}}{2}$ $S_2 \Rightarrow \ I_{\text{m}}\sin(\phi_1-\theta_1)\,\&\,V_{\text{dc}}$ $S_4 \Rightarrow \ I_{\text{m}}\sin(\phi_1-\theta_1)\,\&\,\frac{V_{\text{dc}}}{2}$
Switch rms current $I_{\text{S,rms}}$ $S_1, S_2 \Rightarrow$ $\frac{I_{\text{m}}}{2}\sqrt{\left(1-\frac{\phi_1}{\pi}\right)+\frac{\sin(2\phi_1)}{2\pi}}$	Switch rms current $I_{\text{S,rms}}$ $S_1 \Rightarrow$ $\frac{I_{\text{m}}}{2}\sqrt{\left(2D+\frac{\theta_1-\phi_1}{\pi}\right)-\frac{\sin 2(2\pi D+\theta_1-\phi_1)}{2\pi}}$ $S_2 \Rightarrow$ $\frac{I_{\text{m}}}{2}\sqrt{\left(1+\frac{\theta_1-\phi_1}{\pi}\right)-\frac{\sin 2(\theta_1-\phi_1)}{2\pi}}$	Switch rms current $I_{\text{S,rms}}$ $S_1 \Rightarrow$ $\frac{I_{\text{m}}}{2}\sqrt{\left(2D+\frac{\theta_1-\phi_1}{\pi}\right)-\frac{\sin 2(2\pi D+\theta_1-\phi_1)}{2\pi}}$ $S_2 \Rightarrow \frac{I_{\text{m}}}{2}\sqrt{\left(1+\frac{\theta_1-\phi_1}{\pi}\right)-\frac{\sin 2(\theta_1-\phi_1)}{2\pi}}$ $S_3, S_4 \Rightarrow$ $\frac{I_{\text{m}}}{2}\sqrt{(1-2D)+\frac{\cos 2(\pi D+\theta_1-\phi_1)\sin(2\pi D)}{\pi}}$
Body-diode average current $I_{\text{D,avg}}$ $D_1, D_2 \Rightarrow \ \frac{I_{\text{m}}}{2\pi}\left[1-\cos(\phi_1)\right]$	Body-diode average current $I_{\text{D,avg}}$ $D_1 \Rightarrow \ \frac{I_{\text{m}}}{2\pi}\left[1-\cos(\theta_1-\phi_1)\right]$ $D_2 \Rightarrow \ \frac{I_{\text{m}}}{2\pi}\left[1+\cos(2\pi D+\theta_1-\phi_1)\right]$	Body-diode average current $I_{\text{D,avg}}$ $D_1, D_2 \Rightarrow \ \frac{I_{\text{m}}}{2\pi}\left[1-\cos(\theta_1-\phi_1)\right]$

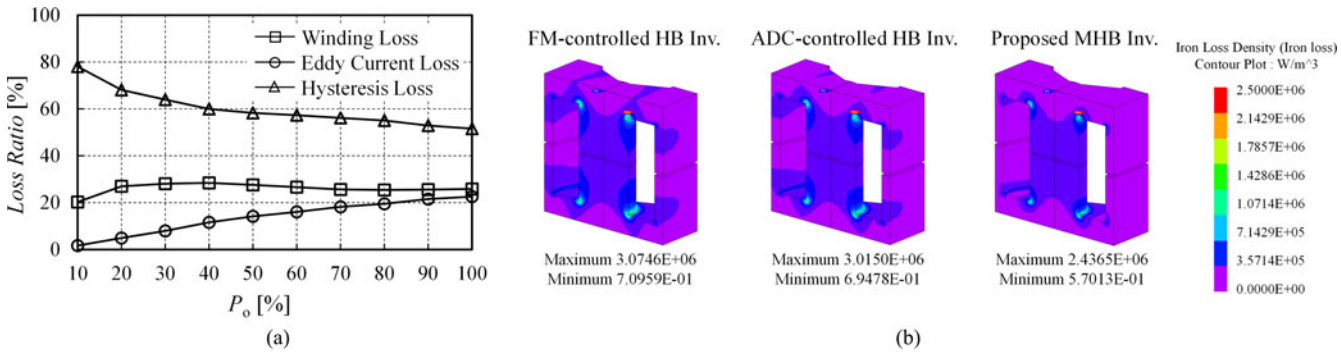

Fig. 14. FEM analysis results. (a) Inductor loss composition of the proposed inverter for the loads. (b) Comparison of core loss distributions for a 40% load.

implies that the load starts to increase. The mode transition is dependent on the load state. Then, gate signals to drive the switches are generated by the PWM generators. Fig. 13 shows the PWM generation of the gate drive signals for switching state I. In this switching state, one switch pair (S_2–S_4) always complementarily operates at fixed duty cycle $D = 0.5$ so that the first ramp signal *Carr* is compared with half of the carrier peak value ($= 0.5 \times \text{Carr}_{\text{peak}}$). On the other hand, another switch pair (S_1–S_3) must be driven by adjusting the duty cycle. Therefore, PWM signals for S_1 and S_3 are generated by comparing the ramp signal with the duty cycle command. It should be noted that another ramp signal $\text{Carr}_{\text{shifted}}$ is utilized for the S_3 PWM signal. The second ramp signal starts when the duty cycle command signal meets the first ramp signal. Finally, the PWM

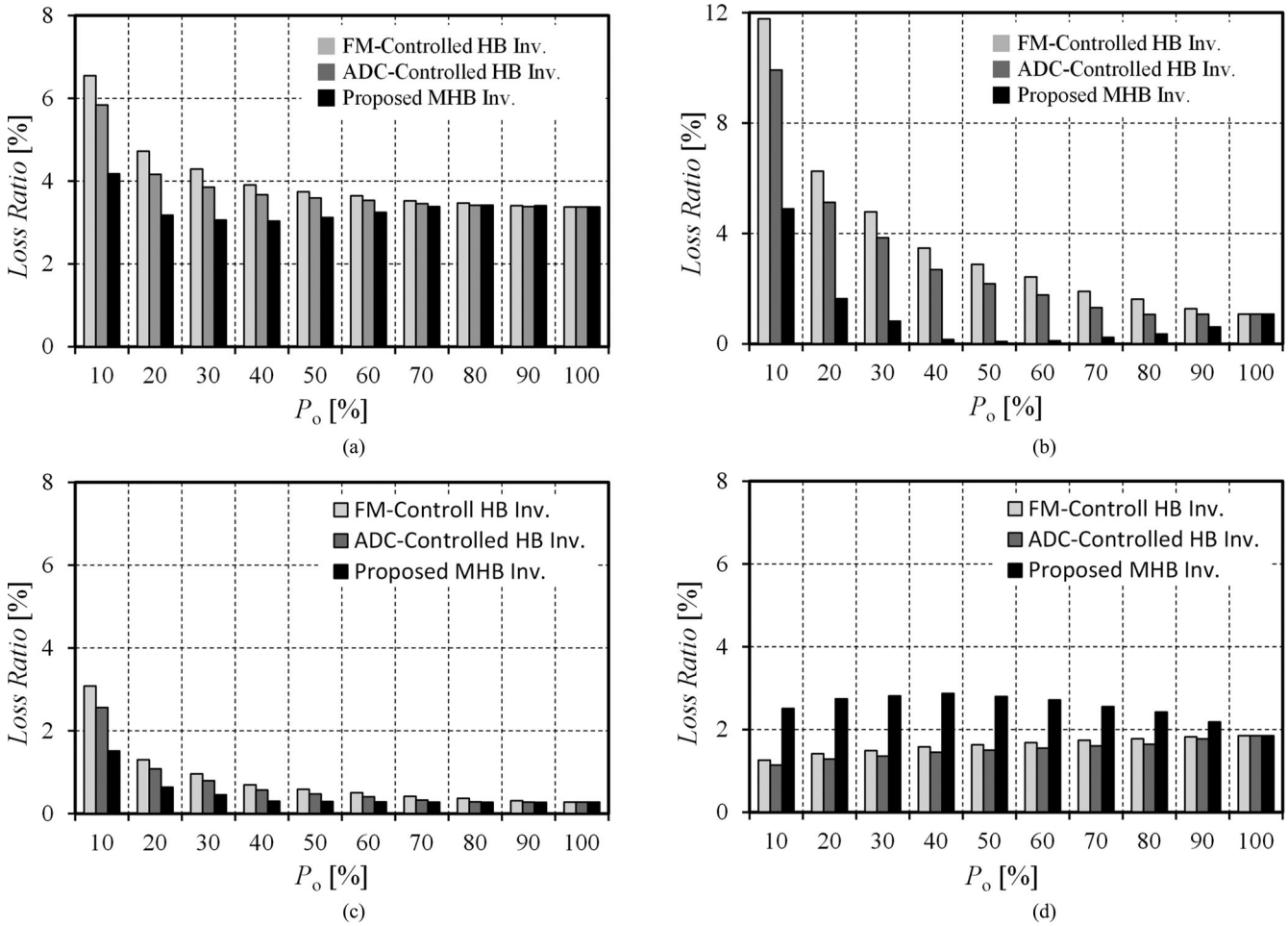

Fig. 15. Loss distributions. (a) Core losses. (b) Body-diode conduction losses. (c) MOSFET switching losses. (d) MOSFET conduction losses.

signals are delivered to the gate circuits for S_1, S_2, S_3, and S_4 through the dead time setting part.

IV. Loss Analysis

In this section, the losses of the proposed inverter are calculated and compared with those of the FM- and ADC-controlled HB inverters. Although the sources of losses in the system are numerous, comparative evaluation of the main sources, such as the MOSFET conduction and switching losses, MOSFET body diode conduction loss, and resonant inductor loss, offers useful estimation of the system efficiency. The dissipated power to drive the switch gate is excluded in the loss analysis.

A. Switch Losses

The switch conduction losses are calculated by the MOSFET approximation of the drain–source on-state resistance. Because of the ZVS operation, only the turn-off loss is considered. The conduction losses of the body diodes are calculated using the diode approximation of the diode on-state voltage and diode average current under a zero-current transition. The adopted switch is the STP36NF06FP 60-V n-channel MOSFET. Table IV lists the related formulas for the calculation of the switch losses derived using the fundamental harmonic component.

B. Magnetics Losses

The resonant inductor loss can be classified into two major categories: core and winding losses. Between them, the core loss has a complex distribution because it depends on the magnetic flux density distribution, which accounts for the core magnetic saturation. In this paper, a magnetic field analysis simulation based on the finite-element method (FEM) using JMAG-Designer v12.0 is performed, while the winding loss considers only the winding dc resistance because the litz wire strand diameter is chosen to reduce the high-frequency effects such as skin-effect losses to a minimum [25]. Therefore, the litz wire winding in the FEM simulation can be modeled as a copper wire with a uniform current density as in the dc case. This prevents the time-intensive calculation of eddy currents in the windings. The specifications of the core and the wire are as follows: Ferrite core PQ3221 PC40 by TDK and USTC $0.1\phi \times 150$ Litz wire. Fig. 14 shows the loss trajectories that compose the inductor loss of the proposed MHB inverter for the load variations: 1) winding loss, 2) core eddy current loss, and 3) core hysteresis loss. Among them, hysteresis loss is crucial in the inductor loss. Its share increases as the load becomes lighter. It can be observed that the FM- and ADC-controlled HB inverters have almost the same loss distributions as the MHB inverter. The hysteresis loss is strongly dependent on the frequency. Therefore, decreasing

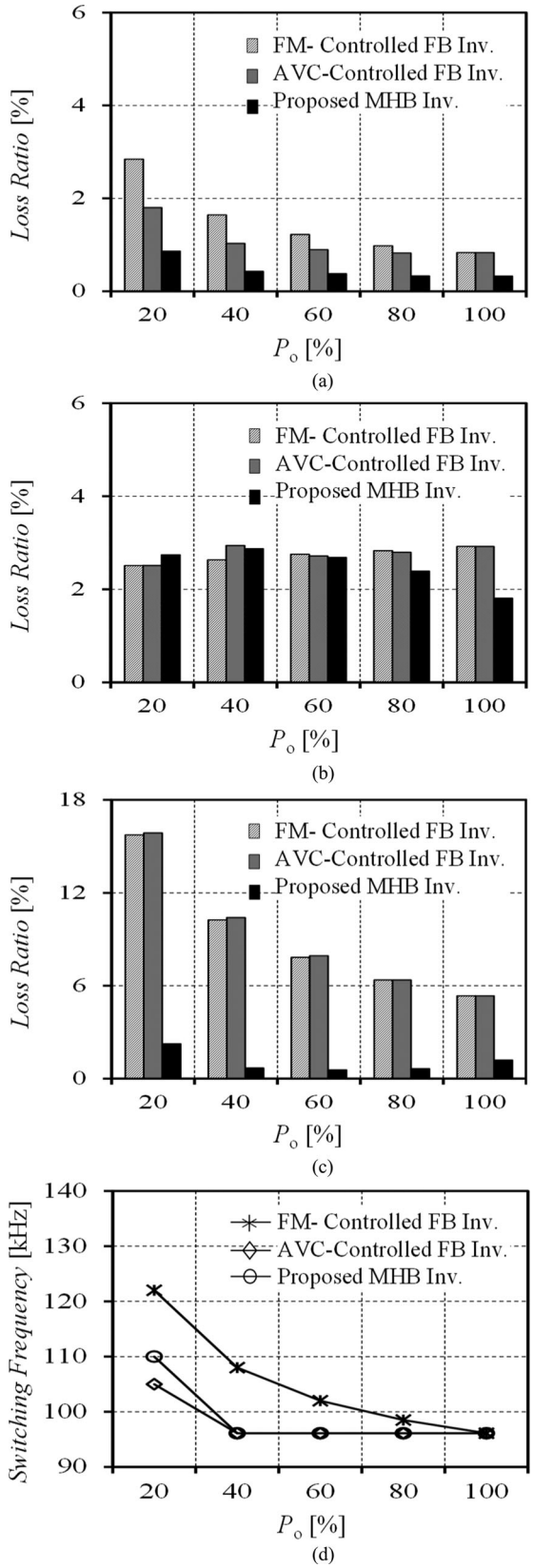

Fig. 16. Comparison of the FB and MHB inverters. (a) MOSFET switching losses. (b) MOSFET conduction losses. (c) Body-diode conduction losses. (d) Switching frequency variations.

TABLE V
CIRCUIT PARAMETERS IN THE EXPERIMENT

Parameters		Values and unit
V_{dc}	DC input voltage	48 V
P_o	Output power	120 W
f_o	Resonant frequency	80 kHz
L_r	Resonant inductance	10.5 μH
C_r	Resonant capacitance	376 nF
R_L	Load resistance	2 Ω
S_1–S_4	Switches	STP36NF06FP

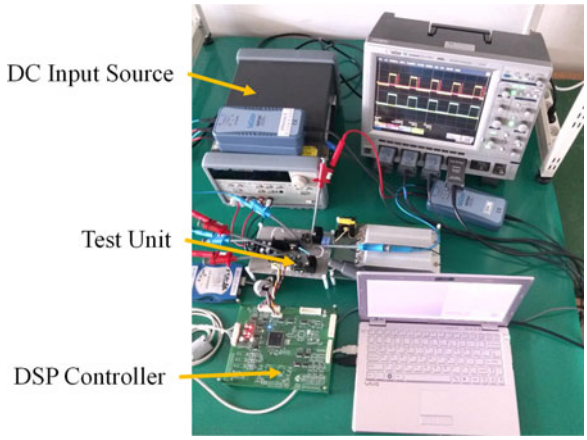

Fig. 17. Experimental setup of the proposed MHB inverter prototype.

the switching frequency is very clearly the most efficient way of reducing the inductor loss, leading to the increase in the overall efficiency. Fig. 14(b) shows the core loss distributions among the proposed inverter and its counterparts for a 40% load.

C. Loss Distributions

The comprehensive loss results in the main components among the different topologies are compared. Fig. 15 shows the ratio of the component loss to the output power for the loads. The component losses of the proposed MHB inverter are lower than those of the FM- and ADC-controlled HB inverters. It is noticeable that the conduction losses of the MOSFET body diodes of the proposed inverter are eliminated by the duty cycle control at a fixed switching frequency in the middle-load range. This can be confirmed by the results of the inverter output PF shown in Fig. 10. In addition, because the switching frequency for light loads can be decreased by a maximum of 24% compared with that of the conventional FM-controlled HB inverter, the MOSFET switching losses are reduced by approximately 50%. However, the MOSFET conduction losses are larger than those of the others because of the use of the NCC switches as a bridge leg, increasing the value of the drain–source on-state resistance of the MOSFET. Nevertheless, the proposed inverter evidently outperforms its competitors. In practical application, because a switch with half of the voltage rating of the bridge leg can be used as an NCC switch, the on-state resistance can be remarkably reduced.

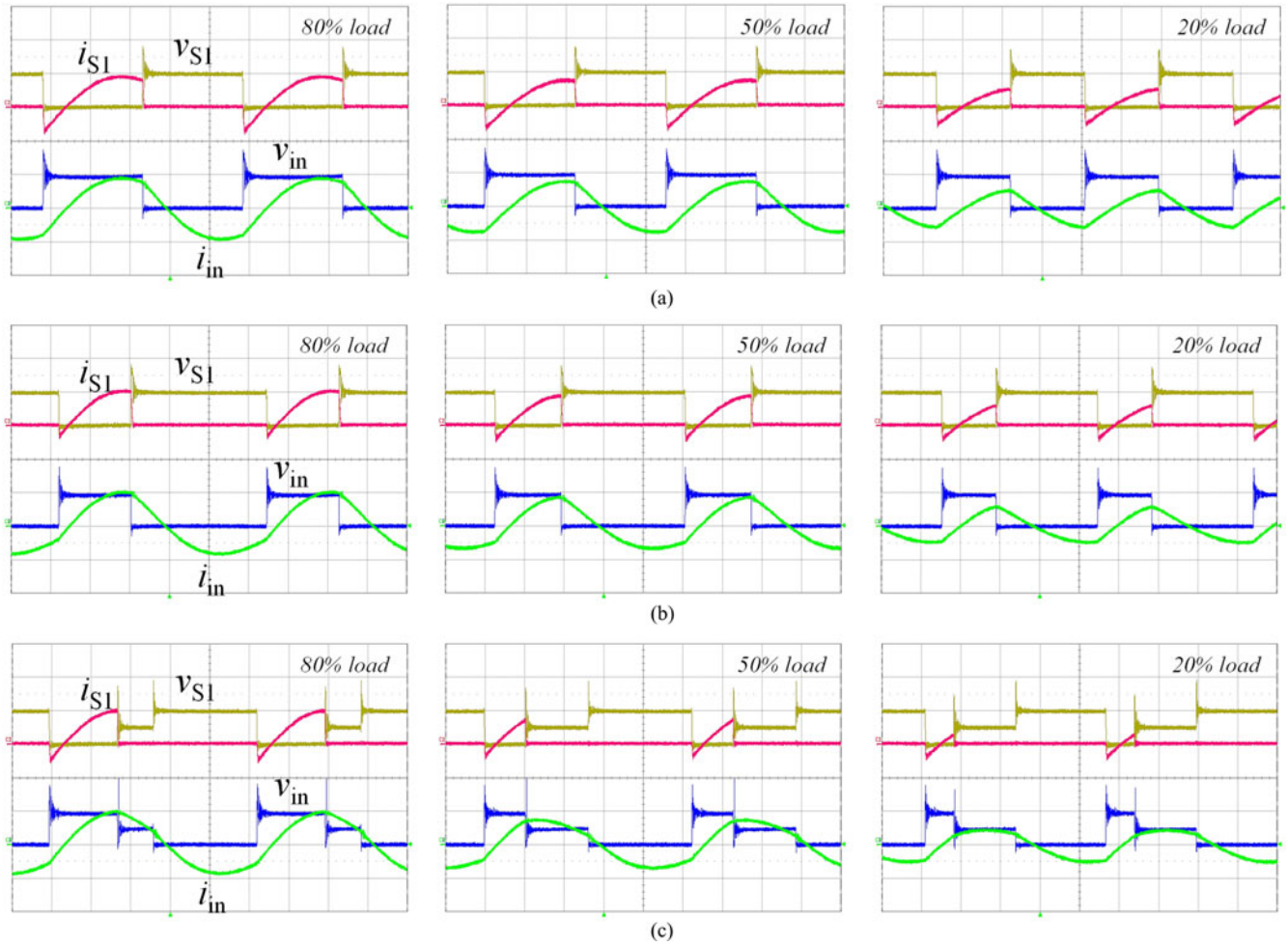

Fig. 18. Experimental waveforms at 80%, 50%, and 20% loads. (a) FM-controlled HB inverter. (v_{S1}: 50 V/div, i_{S1}: 10 A/div, $v_{\rm in}$: 50 V/div, i_r: 10 A/div, tims: 2 μs/div). (b) ADC-controlled HB inverter. (v_{S1}: 50 V/div, i_{S1}: 10 A/div, $v_{\rm in}$: 50 V/div, i_r: 10 A/div, tims: 2 μs/div). (c) Proposed MHB Inverter. (v_{S1}: 50 V/div, i_{S1}: 10 A/div, $v_{\rm in}$: 50 V/div, i_r: 10 A/div, tims: 2 μs/div).

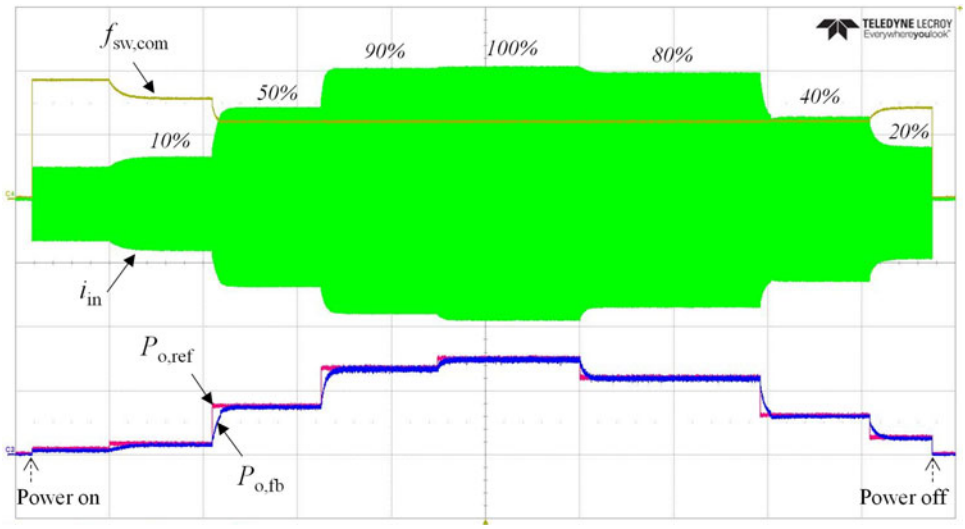

Fig. 19. Dynamic response due to load changes. ($f_{\rm sw,com}$: 2V/div, $i_{\rm in}$: 5 A/div, $P_{o,\rm ref}$: 2 V/div, $P_{o,\rm fb}$: 2V/div, time: 5 s/div).

D. Performance Comparison With the FB Inverter

The FM- and AVC-controlled FB inverters have been theoretically compared with the proposed MHB inverter in terms of switch loss and switch frequency variation, except inductor and capacitor losses. For the clear evaluation, both inverters adopt the same switch (STP36NF06FP 60-V n-channel MOSFET), even though two switches of NCC in the proposed MHB inverter only block half of the dc input voltage. Resonant parameter values of the FB inverter are induced as $R_L = 2\ \Omega$, $L_r = 28.3\ \mu$H, and $C_r = 140.1$ nF in order to have the same rms resonant current value as the proposed MHB inverter at the maximum output power. Fig. 16 shows the ratio of the switch loss to the output power and the range of the switch frequency variation for the loads. As shown in Figs. 16(a)–(c), the switch losses of the proposed inverter are lower than those of the FB inverter, especially MOSFET switching loss and body-diode conduction loss are substantially reduced. Because the voltage stress on three switches in the proposed inverter is half of the dc input voltage at turn off, the turn-off switch loss becomes reduced. In addition, only two body diodes in the proposed inverter conduct the current, while all of body diodes in the FB inverter conduct the current regardless of control methods. Fig. 16(d) shows the switching frequency variations of both inverters for the loads. The switching frequency variation of the proposed inverter is almost the same as that of the AVC-controlled FB inverter. However, when the FB inverter is operated by the FM control method, the switching frequency rapidly increases compared with the proposed inverter as the load is lower.

V. Experimental Results

To verify the proposed inverter, the main performance results are compared using the experimental results. The specifications of the system parameters are listed in Table V, and Fig. 17 shows the test setup of the 120-W prototype inverter. At maximum output power, three topologies are operated by duty cycle D of 0.5 at the minimum switching frequency. Fig. 18 shows the experimental waveforms of the voltage across switch S_1, current through S_1, inverter output voltage, and inverter output current for 80%, 50%, and 20% loads. Fig. 18(a)–(c) shows the waveforms of the FM-controlled HB, ADC-controlled HB, and proposed MHB inverters, respectively, which prove that the experimental results are identical to the theoretical results.

It can be shown that the switching frequencies of the proposed inverter are lower than those of the conventional HB inverter with the FM and ADC control schemes as the load becomes lighter. The proposed inverter can operate with only a duty cycle control at 95 kHz for a fixed switching frequency from a 40% load up to full load. In contrast, the ADC-controlled HB inverter should increase the switching frequency for operation at less than 80% load. For reference, the switching frequency of the proposed inverter is around 136 kHz at about 10% load, a reduction of more than 24% compared with the 179-kHz switching frequency of the FM-controlled HB inverter. Fig. 19 shows the dynamic response of the proposed MHB inverter to a step change from 100% to 10% load. $P_{o,\mathrm{ref}}$ and $P_{o,\mathrm{fb}}$ are command and feedback signals for the output power, respectively, and

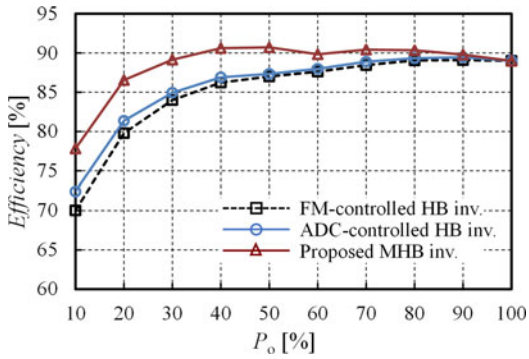

Fig. 20. Efficiency comparison for the different topologies.

$f_{\mathrm{sw,com}}$ is the command signal for the switching frequency. It can be shown that the switching frequency is fixed from 40% to 100% power ranges, and the proposed controller well regulates the output power according to load variations. Fig. 20 shows the measured efficiency comparison among the three different topologies. The efficiency of the proposed inverter is evenly distributed from 100% to 40% load and improved by up to 7% compared with the conventional HB inverter under less than 40% load.

VI. Conclusion

In this paper, an MHB series-resonant inverter topology with dc-link NCC has been proposed. The output voltage of the proposed MHB inverter can have three levels (0, $V_{\mathrm{dc}}/2$, and V_{dc}) according to the switching combinations between the NCC and the HB leg through the proposed pseudo AVC PWM control method. This characteristic implies that the proposed topology has outstanding control possibility with respect to the PF of the inverter output and the switching frequency variation under middle to light loads. The operating characteristics are analyzed in detail, and the design procedure of the resonant parameters is explained. On the basis of the deduced parameters, the performance results between the conventional HB and the proposed inverters are compared in terms of the inverter output PF and overall efficiency. Moreover, the losses in the main components in the inverter are analytically analyzed in detail. In summary, the proposed MHB series-resonant inverter offers the following advantages.

1) The positive and negative resonant currents are approximately balanced by the voltage-cancellation PWM control method.
2) Soft-switching operation of all switches in the inverter is possible.
3) Three switches are always clamped to half of the dc-link voltage at turn off.
4) The variation in the switching frequency can be minimized compared with that of the conventional HB resonant inverter with FM and ADC control methods.

Therefore, the efficiency is increased by more than 3% on average compared with that of the conventional HB inverter from the middle- to the low-load ranges and 7% at the lightest load.

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