An Alternative Approach to LED Driver Design Based on High-Voltage Driving

C. S. Wong, *Student Member, IEEE*, K. H. Loo, *Member, IEEE*, Y. M. Lai, *Senior Member, IEEE*, Martin H. L. Chow, *Member, IEEE*, and Chi K. Tse, *Fellow, IEEE*

***Abstract*—This paper discusses an alternative approach to designing LED drivers based on high-voltage operation. Compared with the conventional approach of driving LEDs with low voltage and high current, the alternative approach aims to deliver the same power to LED load with high voltage and low current so that small and nonelectrolytic capacitor can be used. High-voltage operation also facilitates the use of simple PFC preregulators such as boost or SEPIC converters as single-stage LED drivers. This paper begins with the derivation of the relationship between the nominal output voltage and output capacitor's size of a PFC preregulator for achieving a given output voltage ripple's size, followed by a review of the recently emerged high-voltage LED packages suitable for the proposed application. This paper also discusses the flicker and colorimetric performances of LED light sources under the influence of large current ripple when nonelectrolytic capacitor is used. The method of third-harmonic current injection to the input current of LED drivers is also incorporated as an option for further reducing the output capacitor's size while meeting a specified flicker limit. Finally, a design example of high-voltage LED driver based on a boost PFC preregulator with third-harmonic current injection is presented and verified experimentally.**

***Index Terms*—Harmonic injection, high-voltage LED (HV-LED), light-emitting diode (LED), single-stage LED driver.**

I. Introduction

EVERY year, approximately 20% of electricity is consumed globally by lighting systems for general illumination. In U.S. alone, nearly 186 billion kWh per annum of electricity is consumed for residential lighting and it is forecasted to further increase in the next 20 years [1], [2]. In order to reduce the ever-increasing demand for energy consumption for lighting, many countries have begun to phase out traditional light sources such as incandescent lamps, tungsten lamps, and compact fluorescent lamps that are either highly energy inefficient or environmental unfriendly. They are gradually being replaced by the more energy-efficient and nontoxic light-emitting diodes (LEDs), which are also physically more reliable and possess significantly longer life span. LEDs are expected to become the main candidate for light sources in a nondistant future.

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The authors are with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong (e-mail: chi.shing.wong@connect.polyu.hk; kh.loo@polyu.edu.hk; enymlai@polyu.edu.hk; martin.chow@polyu.edu.hk; michael.tse@polyu.edu.hk).

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TABLE I
EXPECTED LIFETIME OF VARIOUS TYPES OF CAPACITORS [7]

Type of Capacitor	Typical Range of Capacitance	Lifetime (hours)
Electrolytic	1 μF–12 mF	$< 10\,000$
Polyester Film	10 pF–80 μF	$> 100\,000$
Ceramic	10 pF–10 μF	$> 100\,000$

For all lighting systems, the mains power drawn from the power grid is time varying at double-line frequency about a nonzero mean. The conventional approach to minimize its effect on the load is to employ electrolytic capacitors for buffering the difference between the time-varying ac-input power and the time-invariant dc-output power in a power converter [3], [4]. While an LED possesses an expected lifetime of 50 000 h, the relatively short lifetime of electrolytic capacitors, which is typically less than 10 000 h, remains a limiting factor to the overall lifetime of LED lighting systems [5], [6]. Table I compares the expected lifetime of various types of capacitors [7], from which it can be seen that the adoption of nonelectrolytic capacitors can bring the lifetime of LED drivers closer to the lifetime of LEDs. Therefore, the effort to replace electrolytic capacitors with other types of capacitors in LED drivers has become an important research topic in LED lighting system design.

Besides the lifetime issue, offline LED drivers should also comply with the industrial standards for lighting, such as IEC 61000-3-2 or ENERGY STAR, which specify the minimum power factor (PF) or maximum total harmonic distortion of the ac current drawn from the mains power. Consequently, long lifetime and high input PF are two main design objectives for offline LED drivers.

Conventional LED packages are generally characterized by low forward voltage. To enable them to connect directly to the high output voltage that is commonly found in power factor correction (PFC) preregulators, a large number of low-voltage LEDs (LV-LEDs) must be connected in series to form a bulky high-voltage LED (HV-LED) string. Reliability under long operation hours becomes a major concern when LED strings made up of many discrete LEDs connected in series due to, for example, degraded soldering quality. Therefore, a typical LED driver is usually composed of a PFC preregulator stage and a second stage for voltage step-down and current regulation, as shown in Fig. 1. A storage capacitor, usually of electrolytic type, is employed to buffer the energy difference between the PFC stage and the step-down converter stage. To eliminate the use

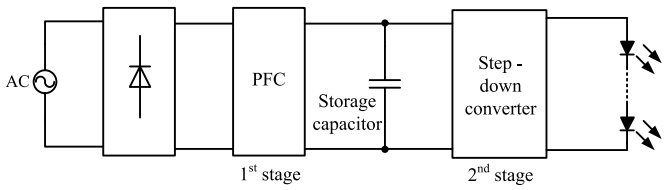

Fig. 1. Block diagram of a classical two-stage LED driver.

of electrolytic capacitor in LED drivers having this architecture, various methods have been proposed. Some researchers suggested that the electrolytic capacitor can be replaced by other types of capacitor by allowing excessive voltage ripple on the nonelectrolytic capacitor having small capacitance value. The excessive voltage ripple is subsequently compensated by the step-down converter that follows the PFC stage [8]–[10]. This architecture usually results in a very high component count and a lower overall energy conversion efficiency. To improve the energy conversion efficiency of typical two-stage LED drivers and to eliminate the use of electrolytic capacitor, a bridgeless-SEPIC-derived PFC coupled to a twin-bus buck converter was proposed [11]. Despite the fact that storage capacitance is reduced and lower component stresses are achieved by the insertion of valley-fill circuit, additional diodes, active switches, and capacitors are used, which lead to increased component count and conduction loss. In order to reduce the component count, integrated converters were proposed to merge PFC preregulators with step-down converters through switch sharing [12]–[14]. In [14], a boost-integrated forward converter was proposed as an integrated single-stage LED driver containing only one controlled switch. Although the two stages are combined, the power flow between the mains power and the LED load is still processed twice as in conventional two-stage drivers. Thus, the overall energy conversion efficiency did not improve significantly. An isolated PFC preregulator was also proposed as a single-stage LED driver to reduce the number of components and to replace electrolytic capacitor with other capacitor types by pulsating LED power [15]. Unfortunately, it still suffers from low energy conversion efficiency due to high voltage conversion ratio. The use of active filters was reported as another way to replace electrolytic capacitor by diverting the current ripple at double-line frequency from the main converter's output to a second converter acting as active filter [3], [16]. However, it involves complicated control, high component count, and reduced efficiency. Even though the open-loop control of the bidirectional dc/dc converter was proposed with the aim of reducing the control complexity while minimizing the size of LED current ripple, high component count and reduced efficiency remain as the main concerns for this type of solution [17]. For the purpose of reducing current ripple size or further reducing the energy storage capacitance, odd harmonic current injection (third or fifth harmonics) was proposed as a solution without a significant increase in control complexity [15], [18], and [19]. However, this method requires a design tradeoff between PF and the size of energy storage capacitor.

In summary, in order to provide low output voltage and eliminate electrolytic capacitor, the aforementioned LED driver solutions mostly suffer from the disadvantages of high component count, complicated control, or low energy conversion efficiency. These disadvantages are the consequences of voltage step-down. Before the emergence of high brightness white LEDs as we have today, incandescent and fluorescent lamps were widely used for general illumination and they are known to operate from high voltage provided by the mains voltage or lamp ballasts. Although high-voltage operation of these conventional light sources have given rise to some safety concerns, these concerns are well addressed by the various existing industrial standards that ensure that the high-voltage areas of these light sources and their drivers are properly sealed and made inaccessible to users. When it comes to driving LEDs, although the common practice is to drive them with low voltage, there is in fact no natural reason for limiting them to a low-voltage operation only. When LEDs are driven by high voltage available from PFC preregulators, the aforementioned shortcomings associated with voltage step-down can be alleviated since the same power can be delivered to LEDs at low current and this renders the use of small output capacitor of nonelectrolytic type sufficient for smoothing the voltage applied on them. Although the elimination of electrolytic capacitor inevitably causes the presence of sizable output voltage ripple, and hence LED current ripple, previous researchers found that flicker percentage in the range of 20% to 40% will not cause perceptible flicker to human eyes [21]–[23]. Therefore, if LED current ripple's size within this range of flicker percentage is acceptable, the realization of HV-LED drivers based on simple and efficient single-stage PFC preregulators with no electrolytic capacitor is not an unrealistic goal.

In this paper, the concept of high-voltage driving of LEDs is introduced as a feasible and simple solution for offline electrolytic capacitorless LED drivers. The advantages of high-voltage driving will be presented in Section II. In Section III, a new family of HV-LED packages will be briefly reviewed. In Section IV, the flicker and colorimetric performances of LEDs in the presence of large current ripple will also be discussed. To further reduce the output capacitor's size for a given output voltage ripple's size, or vice versa, a third-order harmonic current injection technique is introduced and the design guidelines are discussed in Section V. Experimental results will be given in Section VI for verifying the HV-LED driving concept.

II. Advantages of High-Voltage Driving

The advantages of adopting the high-voltage driving approach in LED driver design are demonstrated mathematically below. Assume that the PF of the LED driver is unity such that the input current is perfectly sinusoidal and in-phase with the input voltage, as shown in Fig. 2(a). The mathematical expressions of the input voltage, input current, and instantaneous input power are given below as

$$v_{\rm in}(t) = V_{\rm m}\sin\omega t \tag{1}$$

$$i_{\rm in}(t) = I_{\rm m}\sin\omega t \tag{2}$$

$$p_{\rm in}(t) = v_{\rm in}(t)\times i_{\rm in}(t) = P_{\rm load}(1-\cos 2\omega t) \tag{3}$$

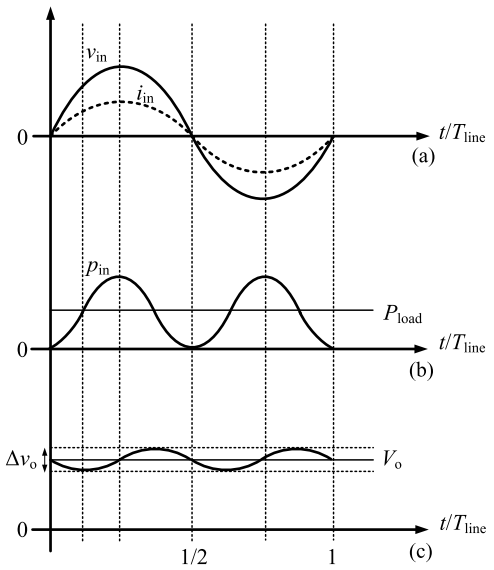

Fig. 2. Typical waveforms of (a) input voltage $v_{\rm in}(t)$ and input current $i_{\rm in}(t)$, (b) instantaneous input power $p_{\rm in}(t)$ and dc load power $P_{\rm load}$, and (c) output voltage $v_{\rm o}(t)$ for a unity-PF LED driver.

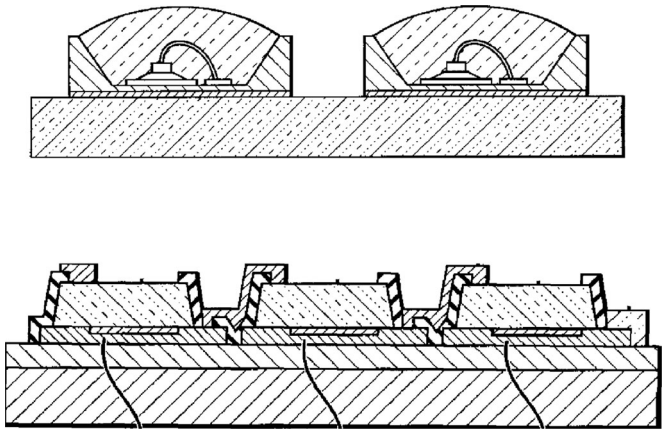

Fig. 3. (Upper) Two single-junction LED package. (Lower) Three sub-LEDs mounted on the same submount. (Extracted from [20]).

where $P_{\rm load} = V_{\rm m} I_{\rm m}/2$.

Since the instantaneous input power $p_{\rm in}(t)$ is pulsating with an average value equal to the dc load power $P_{\rm load}$, the output capacitor is required to buffer the difference between the time-varying input power and the constant load power. The change in the energy stored in the output capacitor ΔE is given by

$$\Delta E = \frac{1}{2} C_{\rm o} \left(v_{\rm o}^2(t) - V_{\rm o}^2 \right) = \int_0^t -P_{\rm load} \cos(2\omega t) dt \qquad (4)$$

where $V_{\rm o}$ is the average output capacitor's voltage. Integrating (4) gives the instantaneous output voltage $v_{\rm o}(t)$ as

$$v_{\rm o}(t) = V_{\rm o} \sqrt{1 - \frac{P_{\rm load}}{\omega C_{\rm o} V_{\rm o}^2} \sin(2\omega t)} \qquad (5)$$

The peak-to-peak output voltage ripple $\Delta v_{\rm o}$ can be obtained by substituting $\sin(2\omega t) = +1$ and $\sin(2\omega t) = -1$ into (5) and computing the difference, i.e.

$$\Delta v_{\rm o} = V_{\rm o} \left| \sqrt{1 + \frac{P_{\rm load}}{\omega C_{\rm o} V_{\rm o}^2}} - \sqrt{1 - \frac{P_{\rm load}}{\omega C_{\rm o} V_{\rm o}^2}} \right|. \qquad (6)$$

When $(P_{\rm load}/\omega C_{\rm o} V_{\rm o}^2) \ll 1$, (6) can be approximated by

$$\Delta v_{\rm o} \approx \frac{P_{\rm load}}{\omega C_{\rm o} V_{\rm o}}. \qquad (7)$$

From (7), it can be readily shown that the output capacitance $C_{\rm o}$ is inversely proportional to the average output voltage $V_{\rm o}$. In other words, if the average output voltage is made high, the output current, and hence, the output capacitor current can be kept small for obtaining the same output power, hence only a small capacitance is sufficient for maintaining a small output voltage ripple. Since the use of electrolytic capacitor is potentially eliminable from such an LED driver and no voltage step-down is required, and given the availability of HV-LED packages, the adoption of high-voltage driving approach implies that a single-stage electrolytic capacitorless LED driver can be realized for the benefits of long lifetime and high efficiency.

III. Emergence of Compact HV-LEDs

To benefit from the advantages of high-voltage driving of LEDs and to comply with the requirements of lighting industry standards, single-stage boost or buck–boost PFC preregulators are natural candidates for HV-LED driver due to their inherent properties that offer high output voltage, good PF, and design simplicity. To match the low forward voltage of LED to the high output voltage of PFC, an intuitive solution would be to connect a large number of LEDs in series for attaining the required forward voltage. Table II lists a selection of conventional LV-LED packages available from the major LED manufacturers, from which it can be seen that all of them are characterized by low forward voltages of about 3 V and forward current capabilities exceeding 300 mA. When a large number of these LEDs are connected in series by means of soldering, the quality of joints or interconnection may lead to degradation in reliability of the LED string, especially when such an LED string is expected to operate for very long hours over its lifetime. Besides, LED strings made of discrete LEDs are also more costly, therefore non-economical and bulky in size.

Instead of utilizing series-connection of discrete LEDs, it is more desirable to implement HV-LED at the chip level. Table III shows a selection of HV-LED packages available from the major LED manufacturers. Each package comprises of a large number of junctions or sub-LEDs mounted on a submount, as shown in Fig. 3. The sub-LEDs are interconnected in series at the chip level, hence the forward voltage required to drive a LED package depends on the number of sub-LEDs and the junction voltages of the sub-LEDs. By changing the number of junctions or sub-LEDs, the forward voltage and current level of an LED package can be adjusted or custom designed to suit various operating voltages and currents [20]. As shown in Table III, the forward

TABLE II
SELECTED CONVENTIONAL LV-LED PACKAGES

Model	Nominal Voltage (V)	Nominal Current (mA)	Size (mm×mm)	Price per 1000 pcs (USD)
CREE XP-E	3.05	350	3.45×3.45	1.110
CREE XM-L	2.9	700	5×5	2.930
Philips LUXEON T	2.8	700	3.7×3.7	1.313
Seoul Z-Power	3.6	400	5×6	1.330

TABLE III
SELECTED COMMERCIALLY AVAILABLE HV-LED PACKAGES

Model	Nominal Voltage (V)	Nominal Current (mA)	Size (mm×mm)	Price per 1000 pcs (USD)
CREE XT-E HVW	46	22	3.45×3.45	1.010
CREE XM-L HVW	46	44	5×5	2.750
Philips LUXEON H	52	20	3×4.5	1.149
Seoul Acrich MJT	63	20	5×5	0.589

Note: All prices are available from Digi-Key Corporation—Distributors of electronic components (http://www.digikey.cn/cn/en/digihome.html?curr=USD)

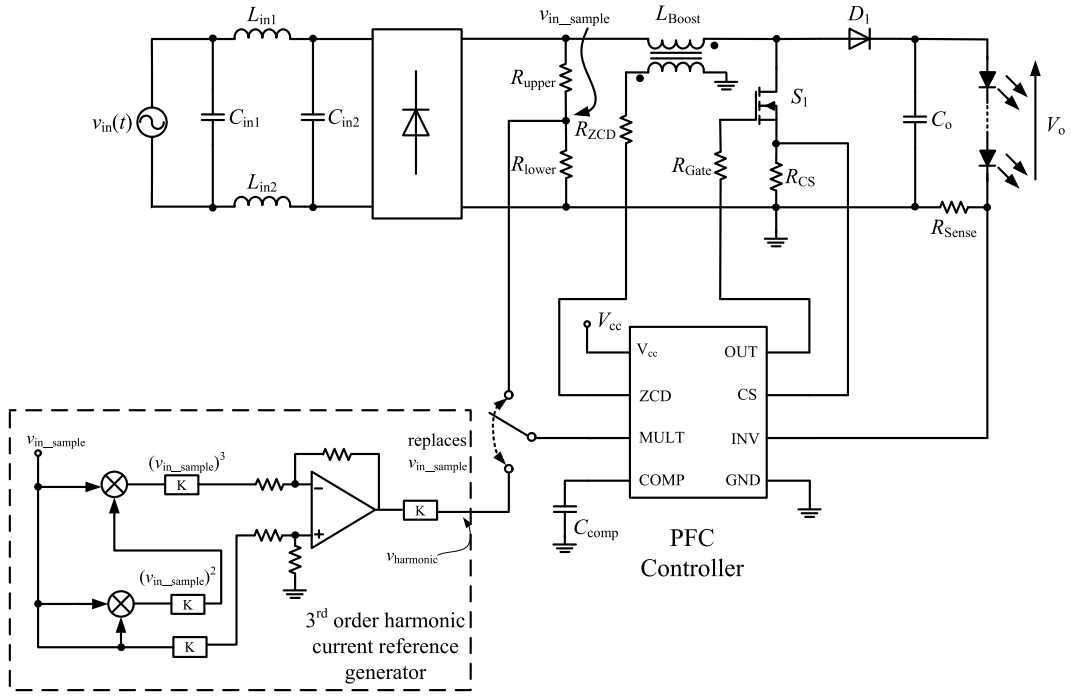

Fig. 4. Schematic diagram of a HV-LED driver based on a boost PFC topology with third-order harmonic current injection.

voltages of HV-LED packages can be made as high as over 60 V, while their forward currents can be as low as several tens of milliamperes while maintaining a small form factor and similar price as their low-voltage counterparts. By utilization of HV-LEDs, high-voltage driving approach can be realized without sacrificing the compactness and cost of single-stage drivers as the series connection of a large number of discrete LEDs is no longer required. Apart from the high forward voltage that is now compatible with the high output voltage of PFC, the chip-level interconnection of LEDs also improves the reliability of the LED load and, hence, the overall lighting systems.

IV. FLICKER AND COLOR STABILITY OF LEDS IN THE PRESENCE OF SIGNIFICANT LED CURRENT RIPPLE

Despite showing the advantages of compactness, high efficiency, high PF, electrolytic capacitorless, and hence, long lifetime, and high reliability, the elimination of electrolytic capacitor as energy buffer from HV-LED drivers inevitably leads to the presence of low-frequency output voltage ripple, which in turn will introduce low-frequency LED current ripple that may cause flicker and color shift in LEDs. This section discusses these issues and establishes design constraints in this respect.

A. Flicker Effect

The presence of low-frequency LED current ripple leads to a time-varying modulation of the luminous flux of LED, which gives rise to the phenomenon of flicker, and its visual impact is commonly measured by the percentage of flicker defined by (8). Despite the general perception that 100 or 120 Hz flicker is invisible to the human eyes, it has been argued that the rapid modulation of light at 100 or 120 Hz is still detectable by human eyes under some environmental conditions or through stroboscopic effect, which may pose risk and adverse biological effects to users [21].

Nevertheless, flicker is not a new issue encountered only in high-voltage driving of LEDs, it also applies to other traditional lighting technologies that are currently in use. In [22], flicker issues associated with traditional lighting technologies were carefully evaluated. In these evaluations, photosensors facilitated by the use of digital signal processing software were used to measure the flicker. It was found that the maximum percentage of flicker encountered in these samples is 40%. In addition, the IEEE Standard P1789 specifies that the percentage of flicker in fluorescent lighting at 100 Hz that is likely to induce headache is approximately 35% [21]. Furthermore, a specialized study on stroboscopic effect involving an LED light source was conducted [23]. In the study, ten subjects were asked to sit in a dark and windowless room and waved a white plastic rod under the illumination of a flickering LED light source in order to evaluate their detection and the level of acceptance toward the induced stroboscopic effects. An empirical model based on the results was developed and used to estimate the level of acceptance of human subjects toward stroboscopic effect. The model estimates that the effect is still acceptable when the percentage of flicker at 100 Hz is below 21%. These figures resulted from the previous studies should be used to define the constraint for the design of HV-LED driver. Taking the worst case into consideration, the percentage of flicker should be kept below 21% which is equivalent to 42% peak-to-peak current ripple

$$Fck_{(\%)} = \frac{F_{\max} - F_{\min}}{F_{\max} + F_{\min}} \times 100\% \tag{8}$$

where $F_{\max}$ and $F_{\min}$ are the maximum and minimum instantaneous luminous flux, respectively.

B. Color-Shift Effect

Most of the conventional low-voltage white LEDs are made from nitride-based blue LEDs coated with yttrium aluminum garnet phosphor [24]. It is found that the color stability and luminous efficacy of these LEDs are influenced by the nature of driving methods and variations of junction temperature [24]. Many experiments were conducted by the previous researchers to show the influences of different driving current waveforms, such as triangular wave, square wave, half- and full-wave rectified wave [25], on the photometric and colorimetric performances of LEDs. In Fig. 5, the results show that there exist different degrees of blue shift under the driving of different current waveforms and the situation becomes more severe when the current ripple's amplitude becomes larger. Since the color-shift

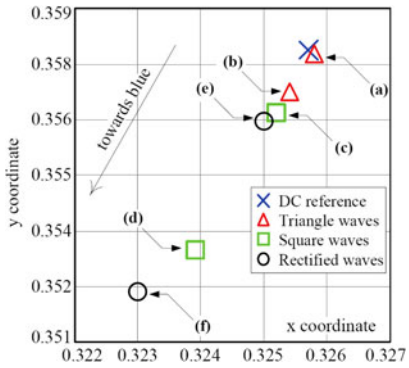

Fig. 5. Measured chromaticity coordinates of conventional low-voltage white LED (Osram LUW W5PM) driven by various current waveforms: (a) 20% ripple; (b) 200% ripple; (c) 70% duty cycle; (d) 35% duty cycle; (e) full-wave rectified; (f) half-wave rectified (Extracted from [25]).

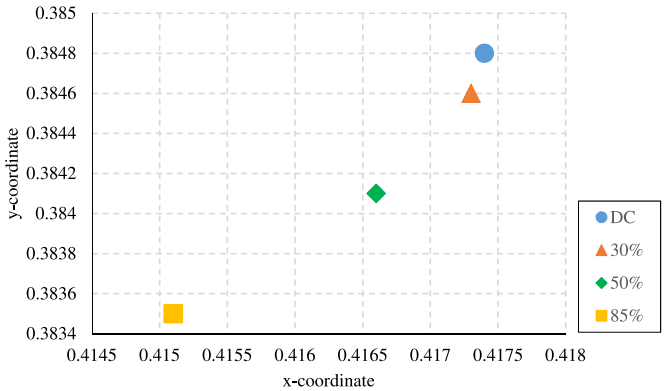

Fig. 6. Measured chromaticity coordinates of CREE XM-L HVW HV-LED driven by dc current having different ripple amplitudes with the average current kept constant at 47 mA.

property of HV-LED has not been studied before, it is necessary to develop a better understanding of it through experimental investigation on the commercial HV-LED package. To quantify the color shift, ΔE^*_{ab} is used to calculate the color difference. For benchmarking, the just noticeable color difference is 2.56 [26]

$$\Delta E^*_{ab} = \sqrt{(L^*_2 - L^*_1)^2 + (a^*_2 - a^*_1)^2 + (b^*_2 - b^*_1)^2}. \tag{9}$$

where L^*, a^*, and b^* are the coordinates in CIELAB color space.

Fig. 6 shows the measured chromaticity coordinates in CIE 1931 color space when a commercial HV-LED package CREE-XM-L was driven by dc current having different ripple amplitudes with the average current kept at 47 mA. The results agree with the findings of the previous researchers [25], [26], where there is an evident of blue-shift when the amplitude of current ripple increases. The CIE 1931 coordinates are converted to CIELAB color space using CIE Illuminant D65 as the reference white point for calculating the color difference. The results are shown in Table IV, from which it can be seen that the color variation remains below the noticeable threshold even for a peak-to-peak current ripple of 50%. The result defines another design constraint for the design of HV-LED driver. By taking

TABLE IV
CALCULATED COLOR DIFFERENCE IN CIELAB COLOR SPACE

Peak-to-peak current ripple	30%	50%	85%
ΔE^*_{ab}	0.178	1.28	4.01

the design constraints for both flicker and color-shift into consideration, the maximum peak-to-peak current ripple should be limited to within 42%.

V. FURTHER CAPACITOR'S SIZE REDUCTION BY A THIRD-ORDER HARMONIC CURRENT INJECTION TECHNIQUE

From the discussions in the previous sections, it is evident that the presence of current ripple is generally acceptable if its amplitude is controlled to within some empirically determined limits, for example, when the peak-to-peak current ripple is less than 42% of the dc current, the resulted flicker is generally imperceptible to human observers and the degree of blue-shift will not cause noticeable color difference. When there is a need to further reduce the ripple amplitude for the same output capacitance, or vice versa, third-order harmonic current injection provides a simple and cost-effective solution. Since it leads to a reduction in PF, the amount of third-order harmonic current introduced must be regulated and this section discusses the design issues related to this method.

A. Third-Order Harmonic Current Injection

With the injection of third-order harmonic current into the input current waveform, the resulting PF can be calculated by (10) and plotted in Fig. 8 based on the percentage of the harmonic current injected I_3^* normalized against the amplitude of the fundamental component $I_{\rm m}$

$$\mathrm{PF} = \frac{1}{\sqrt{1+(I_3^*)^2}}. \tag{10}$$

In the presence of third-order harmonic current, the instantaneous input current waveform $i_{\rm in,1+3}(t)$ and the instantaneous input power $p_{\rm in,1+3}(t)$ are given by

$$i_{\rm in,1+3}(t) = I_{\rm m}\sin(\omega t) + I_{\rm m} I_3^* \sin(3\omega t) \tag{11}$$

$$p_{\rm in,1+3}(t) = 2P_{\rm load}\sin\omega t\left[\sin(\omega t) + I_3^*\sin(3\omega t)\right]. \tag{12}$$

The change in the energy stored in the output capacitor after applying third-order harmonic current injection ΔE_{1+3} can be obtained from (13), assuming that the third-order harmonic current flows through the output capacitor only

$$\Delta E_{1+3} = \int_0^t \left(p_{\rm in}(t) - P_{\rm load}\right) dt \tag{13}$$

which can be simplified to

$$\Delta E_{1+3} = -\frac{P_{\rm load}}{2\omega}\sin(2\omega t)\left(1 - 2I_3^*\sin^2(\omega t)\right). \tag{14}$$

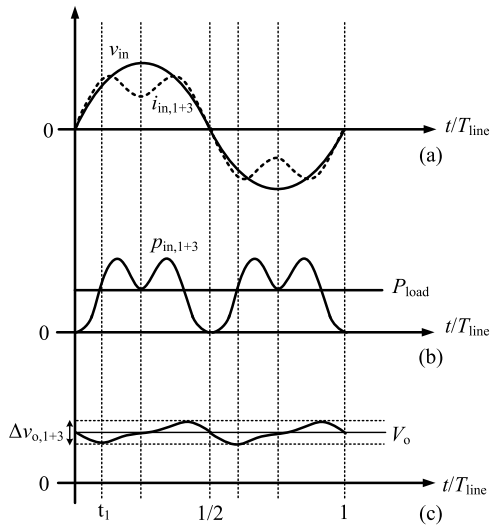

Fig. 7. Typical waveforms of (a) input voltage $v_{\rm in}(t)$ and input current $i_{\rm in,1+3}(t)$, (b) instantaneous input power $p_{\rm in,1+3}(t)$ and dc load power $P_{\rm load}$, and (c) output voltage $v_{\rm o,1+3}(t)$ with third-order harmonic current.

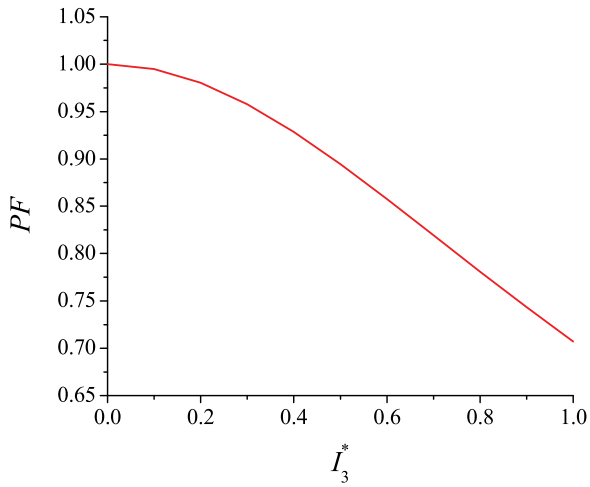

Fig. 8. Variation of PF with I_3^*.

Similar to (4), the instantaneous output voltage in the presence of third-order harmonic current $v_{\rm o,1+3}(t)$ can be derived as

$$v_{\rm o,1+3}(t) = V_{\rm o}\sqrt{1 - \frac{P_{\rm load}}{\omega C_{\rm o,1+3} V_{\rm o}^2}\sin(2\omega t)\left(1 - 2I_3^*\sin^2(\omega t)\right)}. \tag{15}$$

Assuming that the output ripple is small, the peak-to-peak output voltage ripple in the presence of third-order harmonic current $\Delta v_{\rm o,1+3}$ can be approximated by

$$\Delta v_{\rm o,1+3} \approx \frac{P_{\rm load}}{\omega C_{\rm o,1+3} V_{\rm o}}\sin(2\omega t_1)\left(1 - 2I_3^*\sin^2(\omega t_1)\right) \tag{16}$$

where t_1 is the time at which the output voltage ripple reaches its first minimum point, which coincides with the time at which $p_{\rm in,1+3}(t) = P_{\rm load}$, as shown in Fig. 7(b) and (c). By solving

(12), t_1 is given by

$$t_1 = \frac{\cos^{-1}\left(\frac{(I_3^*-1)+\sqrt{\left(1-I_3^*\right)^2+8(I_3^*)^2}}{4I_3^*}\right)}{2\omega}. \quad (17)$$

From (7) and (16), the following ratio can be obtained which when used in conjunction with (10), forms a design guideline for choosing the desired output voltage ripple's amplitude or output capacitor's size for achieving a given input PF

$$\frac{\Delta v_{\mathrm{o},1+3}}{\Delta v_{\mathrm{o}}}\frac{C_{\mathrm{o},1+3}}{C_{\mathrm{o}}} = \sin(2\omega t_1)\left(1-2I_3^*\sin^2(\omega t_1)\right). \quad (18)$$

To realize third-order harmonic current injection, a third-order harmonic current reference should be generated and used to the inductor current. There are a variety of implementation methods for generating the current reference [18], [19] and Fig. 4 shows one of them. It consists of two analog multipliers for generating the $(v_{\mathrm{in\_sample}})^2$ and $(v_{\mathrm{in\_sample}})^3$ signals. By changing the ratio between $(v_{\mathrm{in\_sample}})^3$ and $v_{\mathrm{in\_sample}}$, the amount of injected third-order harmonic current can be controlled. In the case where lower cost or greater control flexibility is required, other methods such as the combination of low-cost microcontroller and one analog multiplier can be used [19].

B. Design Procedure

As for most LED lighting systems, HV-LED drivers also need to face the requirements of safe operation and provision of dimming function. Since this section focuses on capacitor's size reduction by third-order harmonic current injection, these aspects will only be briefly discussed here. The main objective is to outline a procedure for selecting the amount of third-order harmonic current to be injected for a given output capacitance and vice versa.

Commonly luminous control of LEDs is achieved by means of PWM dimming or amplitude dimming. PWM dimming is difficult to achieve with single-stage PFC preregulators due to their slow dynamics. If PWM dimming is desirable, additional stage must be added. For amplitude dimming, considering that if an LED driver works in the European line and the LED current is to be dimmed to a very low level, it is possible for the output voltage to be lower than the input line peak voltage in a single-stage LED driver. In this case, LED driver topologies that can provide a wide output voltage range, such as SEPIC or buck–boost converter, become more suitable due to their capabilities to provide both voltage step-up and step-down. Alternatively, linear regulator can be added in series with each LED string for amplitude dimming although this may introduce additional power loss. However, in comparison to the high output voltage of HV-LED drivers, the voltage drop across the linear regulator and the additional power loss are considered to very small. In addition, if boost-type PFC preregulator is chosen as the HV-LED driver for the advantages of circuit simplicity, fuse should be installed to prevent overcurrent and damage to the LED driver when short-circuit occurs at the output or when the main MOSFET switch fails.

TABLE V
SPECIFICATIONS OF THE PROPOSED SINGLE-STAGE HV-LED DRIVER

Parameter	Symbol	Nominal Value
Input Line Voltage	V_{in}	90–265 V_{rms}
Average Output Voltage	V_{o}	420 V
Average LED Current	I_{o}	47 mA
Peak-to-peak Output Current Ripple	Δi_{o}	14 mA
Output Power	P_{load}	20 W
Minimum Switching Frequency	$f_{\mathrm{sw,min}}$	120 kHz
Type of HV-LED Package	-	CREE XM-L HVW
Number of HV-LED Package	n	9

In the following, the design procedure for a 20-W 420-V HV-LED driver based on boost PFC preregulator is presented. The HV-LED package selected as load is CREE XM-L HVW, the voltage–current characteristic of which is shown in Fig. 11. Other specifications of the LED driver are listed in Table V.

Step 1: From Fig. 11, an average forward current of 47 mA corresponds to an average forward voltage of 46 V for CREE XM-L HVW LED package. Therefore, nine HV-LED packages are connected in series which gives rise to an average output voltage of approximately 420 V.

Step 2: As discussed in Section IV, the maximum peak-to-peak current ripple should not exceed 42% for flicker-free light output. In our design, the limit is set to 30% to allow for some design margin, which is equivalent to 14 mA ($= 47\,\mathrm{mA} \times 30\%$) peak-to-peak current ripple. By referring to Fig. 11, the corresponding peak-to-peak voltage ripple for one HV-LED package is approximately 1 V. A peak-to-peak output voltage ripple of 10 V is chosen for the LED string consisting of nine HV-LED packages.

Step 3: The nominal output capacitance C_{o} is found by using (7) and gives a value of 12 μF. This capacitance can be readily implemented by using film capacitors. The actual implemented value is made up of six 2.2 μF in parallel.

Step 4: ENERGY STAR specifies that PF should be greater than 0.7 and 0.9 for domestic and commercial lighting applications, respectively [28], which limits the maximum allowable amount of third-order harmonic current to 48% calculated based on PF = 0.9. To allow for some design margin, this requires that the maximum amount of third-order harmonic current is 40% which corresponds to a PF of 0.9285.

Step 5: Based on the determined amount of third-order harmonic current injection, the corresponding reduction ratio of output voltage ripple or output capacitor's size can be determined by referring Figs. 9 and 10. For $I_3^* = 0.4$, the output voltage ripple or output capacitor's size can be reduced by 30% from its nominal value.

VI. EXPERIMENTAL VERIFICATION

A boost-type HV-LED driver is constructed to realize the design requirements discussed in the last section. Since the output power is moderate, the LED driver is operated in the boundary conduction mode so that the MOSFET switch can be turned ON at zero current, which gives rise to a higher efficiency. Under

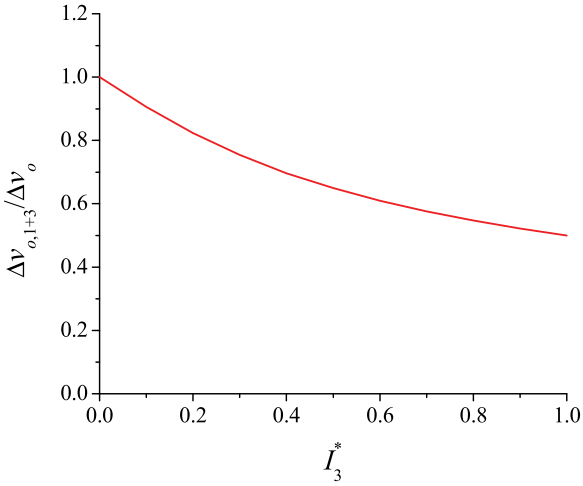

Fig. 9. Variation of $\Delta v_{\mathrm{o},1+3}/\Delta v_{\mathrm{o}}$ with I_3^* for $C_{\mathrm{o},1+3} = C_{\mathrm{o}}$.

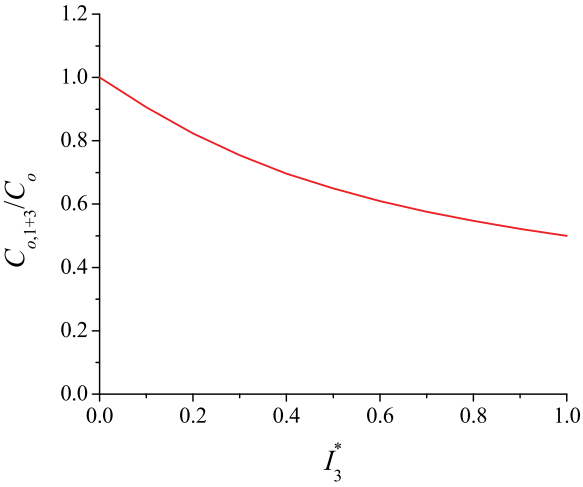

Fig. 10. Variation of $\Delta C_{\mathrm{o},1+3}/\Delta C_{\mathrm{o}}$ with I_3^* for $\Delta v_{\mathrm{o},1+3} = \Delta v_{\mathrm{o}}$.

this condition, the boost inductance is found to be 1.1 mH by using (19). The schematic diagram of the boost-type HV-LED driver is shown in Fig. 4

$$L_{\mathrm{Boost}} = \frac{\eta\left(\sqrt{2}V_{\mathrm{in}}\right)^2}{4f_{\mathrm{sw,min}}P_{\mathrm{load}}\left(1+\frac{\sqrt{2}V_{\mathrm{in}}}{V_{\mathrm{o}}-\sqrt{2}V_{\mathrm{in}}}\right)}. \tag{19}$$

Fig. 12 shows the measured output voltage $v_{\mathrm{o}}(t)$, inductor current reference $i_{\mathrm{ref}}(t)$, and inductor current $i_{\mathrm{L}}(t)$ for the nominal case where no third-order harmonic current is injected to the inductor current reference and $C_{\mathrm{o}} = 13.2\,\mu$F. The measured peak-to-peak output voltage ripple Δv_{o} is 10.5 V, which matches closely the designed value of 10 V. Fig. 13 shows that the percentage of output current ripple is approximately 32% or 16% flicker which, again, matches closely the designed value of 15%. Fig. 14 shows the measured input voltage and input current waveforms with PF $= 0.993$. Under this condition, the measured overall efficiency is 91%.

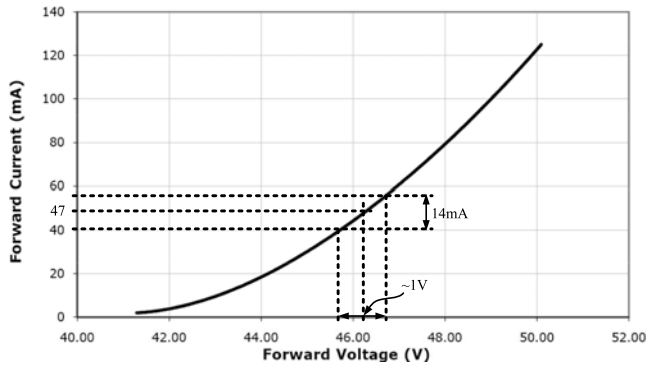

Fig. 11. Voltage–current characteristic of CREE XM-L HVW HV-LED package (Extracted from [27]).

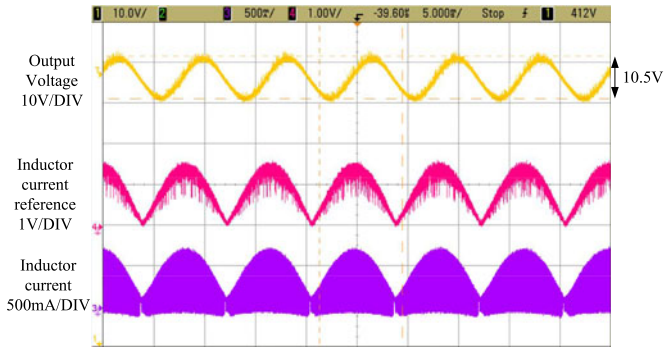

Fig. 12. Measured output voltage $v_{\mathrm{o}}(t)$, inductor current reference $i_{\mathrm{ref}}(t)$, and inductor current $i_{\mathrm{L}}(t)$ with no harmonic injection ($C_{\mathrm{o}} = 13.2\,\mu$F).

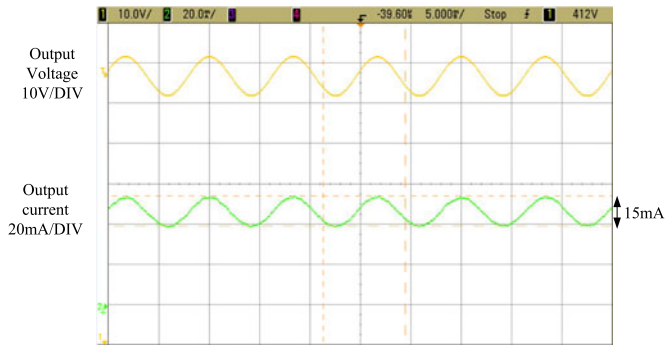

Fig. 13. Measured output voltage $v_{\mathrm{o}}(t)$ and output (LED) current $i_{\mathrm{o}}(t)$ with no harmonic injection ($C_{\mathrm{o}} = 13.2\,\mu$F).

When 40% of third-order harmonic current is injected to the input current, the peak-to-peak output voltage ripple is reduced by 33% with the same output capacitance as the nominal case (13.2 μF). Fig. 15 shows that the new peak-to-peak output voltage ripple is approximately 7V, and Fig. 16 shows that the percentage of output current ripple is approximately 20%, which is equivalent to 10% flicker. Fig. 17 shows the measured input voltage and input current waveforms with PF $= 0.91$, which matches the expected value for $I_3^* = 0.4$.

Alternatively, Figs. 18 and 19 show the measured waveforms when 40% of third-order harmonic current is injected to the input current with 33% reduction in output capacitance.

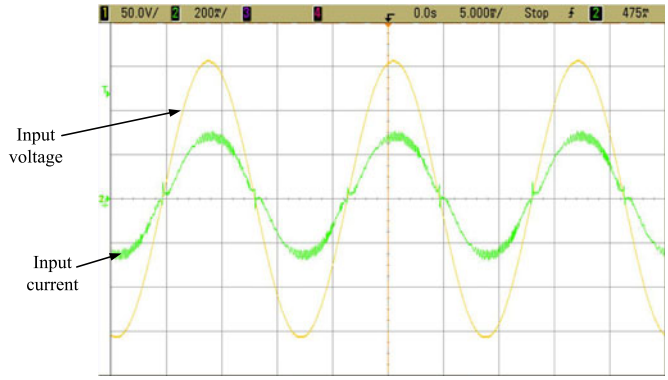

Fig. 14. Measured input voltage and input current with no harmonic injection ($C_{\rm o} = 13.2\,\mu$F).

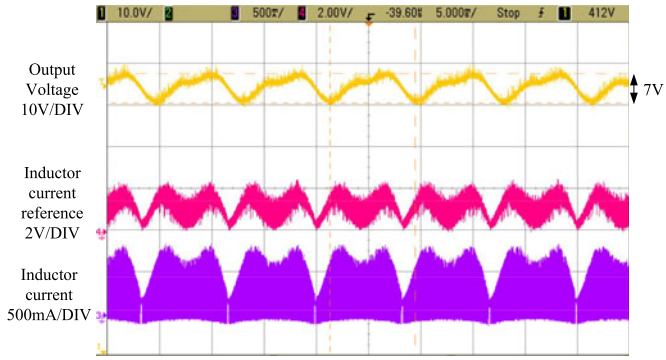

Fig. 15. Measured output voltage $v_{{\rm o},1+3}(t)$, inductor current reference $i_{\rm ref}(t)$, and inductor current $i_{\rm L}(t)$ with $I_3^* = 0.4$ ($C_{{\rm o},1+3} = 13.2\,\mu$F).

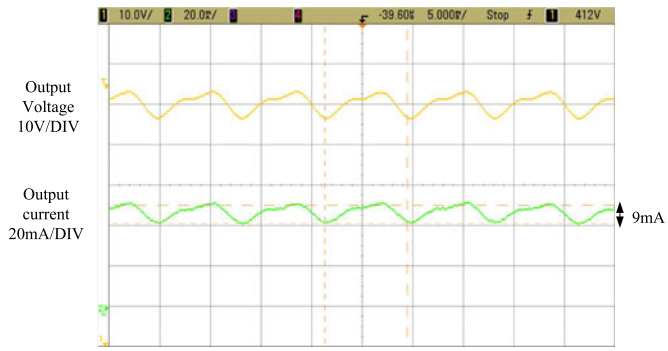

Fig. 16. Measured output voltage $v_{{\rm o},1+3}(t)$ and output (LED) current $i_{{\rm o},1+3}(t)$ with $I_3^* = 0.4$ ($C_{{\rm o},1+3} = 13.2\,\mu$F).

In the experiment, $8.8\,\mu$F is used and the measured PF is also about 0.91. As shown in Fig. 18, the measured peak-to-peak output voltage ripple is similar to that of the nominal case.

Finally,Figs. 20 and 21 show the experimentally measured reduction ratios of output capacitor's size and output voltage ripple for various percentages of third-order harmonic current injection. It can be seen that the measured values generally agree closely with the theoretical values predicted by (18).

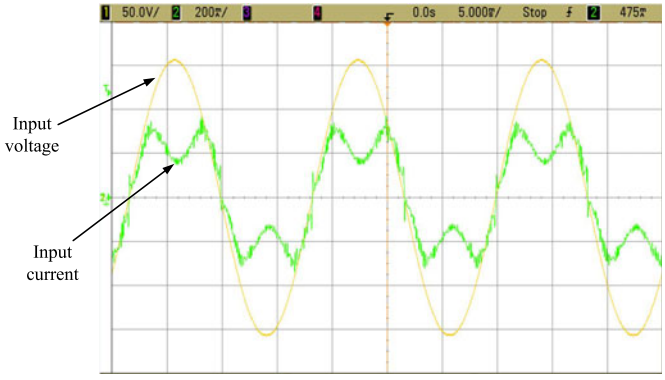

Fig. 17. Measured input voltage and input current with $I_3^* = 0.4$ ($C_{{\rm o},1+3} = 13.2\,\mu$F).

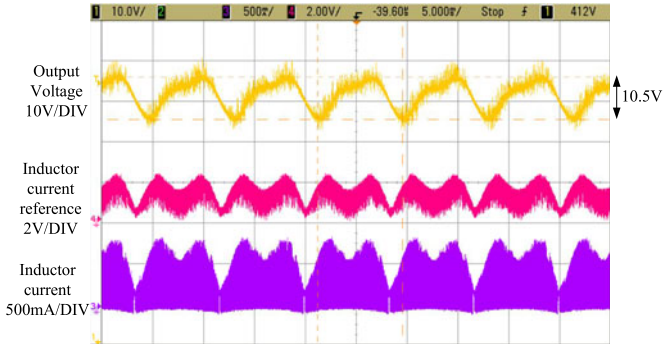

Fig. 18. Measured output voltage $v_{{\rm o},1+3}(t)$, inductor current reference $i_{\rm ref}(t)$, and inductor current $i_{\rm L}(t)$ with $I_3^* = 0.4$ ($C_{{\rm o},1+3} = 8.8\,\mu$F).

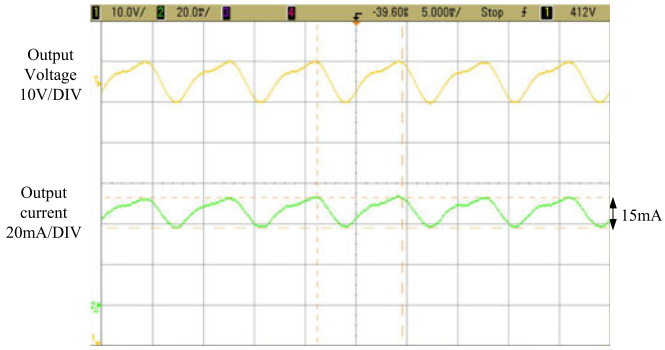

Fig. 19. Measured output voltage $v_{{\rm o},1+3}(t)$ and output (LED) current $i_{{\rm o},1+3}(t)$ with $I_3^* = 0.4$ ($C_{{\rm o},1+3} = 8.8\,\mu$F).

VII. Conclusion

High-voltage driving of LEDs is introduced as a feasible alternative approach to eliminating the use of electrolytic capacitor from LED lighting systems for long-life operation. The proposal is supported by the availability of HV-LED packages that have recently emerged in the market from major LED manufacturers. These compact HV-LED packages are readily driven by high voltage generated by common PFC preregulators without the need for a second stage for voltage step-down, hence the overall efficiency of the lighting systems can be improved. Based on the empirically determined threshold value of human detectable

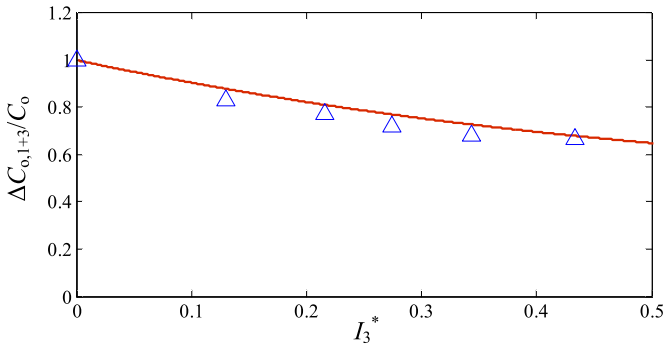

Fig. 20. Experimentally measured $\Delta C_{o,1+3}/\Delta C_o$ with I_3^* for $\Delta v_{o,1+3} = \Delta v_o \approx 10.5$ V.

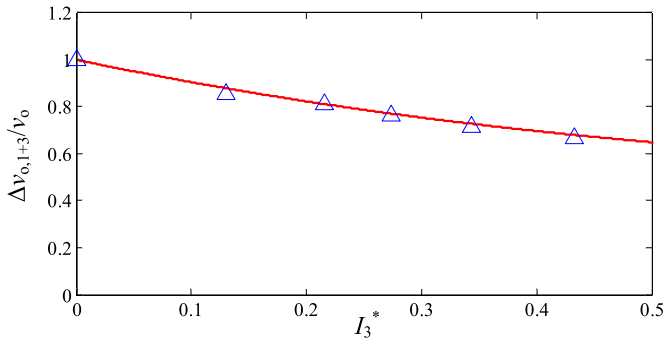

Fig. 21. Experimentally measured $\Delta v_{o,1+3}/\Delta v_o$ with I_3^* for $C_{o,1+3} = C_o = 13.2\,\mu$F.

flicker percentage of 21% and color difference of 2.56, and the voltage–current characteristic of a commercial HV-LED package, a systematic design approach to designing HV-LED drivers for fulfilling both flicker and color-shift requirements is presented. This paper also discusses the use of third-order harmonic current injection as a cost-effective method to further reduce output capacitor's size for a given flicker requirement, or further reduce flicker percentage for a given output capacitor's size. Based on the investigations reported in this paper, it should be appreciated that high-voltage operation of LEDs is a natural approach to achieving electrolytic capacitorless driving of LEDs without complicated circuit and control designs.

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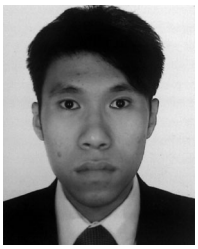
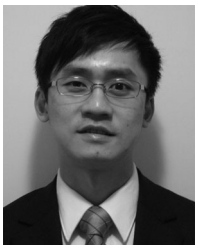


C. S. Wong (S'14) received the B.Eng. (Hons.) degree in electronic and information engineering from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 2013, where he is currently working toward the Ph.D. degree.

His research interests include LED driver circuit design and power factor correction regulators.



K. H. Loo (S'97–M'99) received the B.Eng. (Hons.) degree in electronic engineering and the Ph.D. degree from the University of Sheffield, Sheffield, U.K., in 1999 and 2002, respectively.

From 2002 to 2004, he was the Japan Society for the Promotion of Science (JSPS) Postdoctoral Fellow at Ehime University, Japan. In 2006, he joined The Hong Kong Polytechnic University, Kowloon, Hong Kong, as an Instructor in the Faculty of Engineering, where he is currently an Assistant Professor at the Department of Electronic and Information Engineering. His areas of research interest include power electronics for LED lighting and renewable energy systems.

Dr. Loo has been an Associate Editor for the IEEE TRANSACTIONS ON ENERGY CONVERSION since 2013.

Y. M. Lai (M'92–SM'11) received the B.Eng. degree in electrical engineering from the University of Western Australia, Perth, Australia, in 1983, the M.Eng.Sc. degree in electrical engineering from University of Sydney, Sydney, Australia, in 1986, and the Ph.D. degree from Brunel University, London, U.K., in 1997.

He is an Associate Professor with The Hong Kong Polytechnic University, Kowloon, Hong Kong, and his research interests include computer-aided design of power electronics and nonlinear dynamics.

Martin H. L. Chow (M'98) received the B.Sc. degree in electrical engineering from the University of Hong Kong, Hong Kong, in 1980, the M.Sc. degree in systems engineering from the University of Surrey, Guildford, U.K., in 1984, and the Ph.D. degree in the area of power-factor-corrected switching regulators, from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 1999.

In the course of his career, he has worked on short-wave radio circuit design with Philips, Hong Kong, and in switch-mode power supplies design with Thomson, Singapore. In 1985, he started his teaching career at The Hong Kong Polytechnic University and is currently a Senior Lecturer with the Department of Electronic and Information Engineering.

Dr. Chow received the IEEE Power Electronics Society Transactions Prize Paper Award for 2001.

Chi K. Tse (M'90–SM'97–F'06) received the B.Eng. (Hons.) degree with first class honors in electrical engineering and the Ph.D. degree from the University of Melbourne, Melbourne, Australia, in 1987 and 1991, respectively.

He is presently the Chair Professor at the Hong Kong Polytechnic University, Kowloon, Hong Kong, with which he served as the Head of the Department of Electronic and Information Engineering from 2005 to 2012. He is an author/coauthor of ten books, 20 book chapters, and more than 500 papers in research journals and conference proceedings, and holds five U.S. patents.

Dr. Tse received a number of research and industry awards, including the Best Paper Award by the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2001, the Best paper Award by the *International Journal of Circuit Theory and Applications* in 2003, two Gold Medals at the International Inventions Exhibition in Geneva in 2009 and 2013, and a number of recognitions by the academic and research communities, including the honorary professorship by several Chinese and Australian universities, the Chang Jiang Scholar Chair Professorship, the IEEE Distinguished Lectureship, the Distinguished Research Fellowship by the University of Calgary, Gledden Fellowship, and the International Distinguished Professorship-at-Large by the University of Western Australia. While with The Hong Kong Polytechnic University, he received the President's Award for Outstanding Research Performance twice, Faculty the Research Grant Achievement Award twice, the Faculty Best Researcher Award, and several teaching awards. He serves and has served as an Editor-in-Chief for the IEEE CIRCUITS AND SYSTEMS MAGAZINE, an Editor-in-Chief of the IEEE CIRCUITS AND SYSTEMS SOCIETY NEWSLETTER, an Associate Editor for the three IEEE Journal/Transactions, an Editor for the *International Journal of Circuit Theory and Applications*, and is on the editorial boards of a few other journals. He also serves as a Panel Member of Hong Kong Research Grants Council and NSFC, and a Member of several professional and government committees.