A Single-Phase PV Quasi-Z-Source Inverter With Reduced Capacitance Using Modified Modulation and Double-Frequency Ripple Suppression Control

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***Abstract*—In single-phase photovoltaic (PV) system, there is double-frequency power mismatch existed between the dc input and ac output. The double-frequency ripple (DFR) energy needs to be buffered by passive network. Otherwise, the ripple energy will flow into the input side and adversely affect the PV energy harvest. In a conventional PV system, electrolytic capacitors are usually used for this purpose due to their high capacitance. However, electrolytic capacitors are considered to be one of the most failure prone components in a PV inverter. In this paper, a capacitance reduction control strategy is proposed to buffer the DFR energy in single-phase Z-source/quasi-Z-source inverter applications. Without using any extra hardware components, the proposed control strategy can significantly reduce the capacitance requirement and achieve low input voltage DFR. Consequently, highly reliable film capacitors can be used. The increased switching device voltage stress and power loss due to the proposed control strategy will also be discussed. A 1-kW quasi-Z-source PV inverter using gallium nitride (GaN) devices is built in the lab. Experimental results are provided to verify the effectiveness of the proposed method.**

***Index Terms*—Capacitance reduction, double-frequency ripple (DFR), Z-source (ZS)/quasi-Z-source (qZS).**

I. Introduction

THE voltage-fed z-source inverter (ZSI) and quasi-Z-source inverter (qZSI) have been considered for photovoltaic (PV) application in recent years [1]–[13]. These inverters feature single-stage buck–boost and improved reliability due to the shoot-through capability. The ZSI and qZSI are both utilized in three-phase and single-phase applications [1]–[5]. The single-phase ZSI/qZSI can also be connected in cascaded structure for higher voltage application and higher performance [6]–[12]. In three-phase applications, the Z-source (ZS)/quasi-Z-source (qZS) network only needs to be designed to handle the high-frequency ripples. However, in single-phase application, the ZS/qZS network needs to handle not only the high-frequency ripples but also the low-frequency ripple. The qZSI will be used in this paper to study the low-frequency ripple issue and present the proposed control strategy. A single-phase qZSI system is shown in Fig. 1. Ideally, the dc-side output power is pure dc and the ac-side power contains a dc component plus ac ripple component whose frequency is two times the grid voltage frequency. The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper. In order to balance the power mismatch between the dc side and ac side, the DFR power needs to be buffered by the passive components, mainly the qZS capacitor C_1 which has higher voltage rating than C_2. The DFR peak power is the same as the dc input power, so large capacitance is needed to buffer this ripple energy. To achieve high inverter power density with reasonable cost, electrolytic capacitors are usually selected. Electrolytic capacitors contain a complex liquid chemical called electrolyte to achieve high capacitance and low series resistance. As the electrolytic capacitors age, the volume of liquid present decreases due to evaporation and diffusion. This process is accelerated with higher temperature, eventually leading to performance degradation over time [14]. Therefore, electrolytic capacitors are considered to be the weak component regarding to lifetime, especially under outdoor operation conditions.

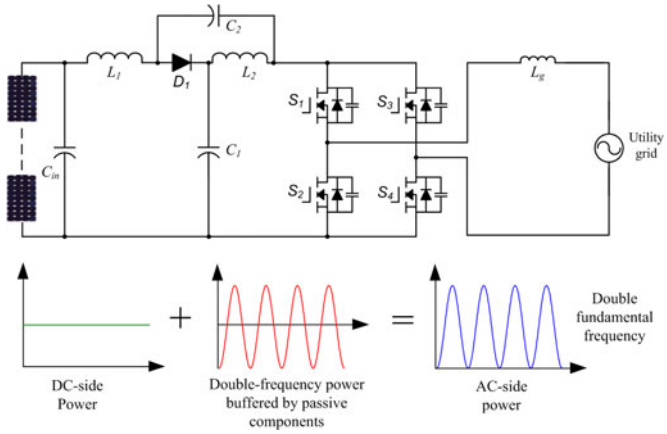

Fig. 1. Diagram of a single-phase qzsi-based PV system.

Accurate analytical models to calculate the DFR for qZSI have been developed in [8], [15], and [16] and the design guidelines for selecting the capacitance to limit the DFR are also provided. Nevertheless, the required capacitance is still large. In [17], two additional smoothing-power circuits are employed to reduce the DFR of dc-link voltage in ZSI. However, the added circuits increase the system cost and complexity. In [18], a low-frequency harmonic elimination PWM technique is presented to minimize the DFR on Z-source capacitors. However, the method

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is used for application with constant voltage input source and DFR current is induced in the inductor and the input side. This is not suitable for the PV application, because the ripple current will decrease the energy harvest from the PV panels.

In some reported single-phase two-stage system which is composed of a dc–dc converter and H-bridge inverter, the dc-link capacitance can be significantly reduced by using dedicated control [14], [19]. However, the qZSI does not have the dc–dc stage, so the reported capacitance reduction methods cannot be applied in the qZSI.

In this paper, a new control strategy is proposed for ZSI/qZSI to mitigate the input DFR without using large capacitance, which enables us to use the highly reliable film capacitors. There is no extra hardware needed to implement the capacitance reduction. The proposed control system incorporates a modified modulation strategy and a DFR suppression controller. In order to apply the capacitance reduction method, it is necessary to study the impact of decreasing the capacitance on system design and performance. This will be covered in Section III. A 1-kW qZSI inverter prototype with the proposed control strategy is built in the laboratory. The gallium nitride (GaN) devices are applied in the inverter to increase the system efficiency at high switching frequency. Finally, experimental results are provided to verify the effectiveness of the proposed control system.

II. Proposed Control System for Capacitance Reducation

The basic principle of the proposed capacitance reduction method can be explained by

$$\Delta E = \frac{1}{2} C \left(v_{C\_\max}^2 - v_{C\_\min}^2 \right) \tag{1}$$

where C is the capacitance, ΔE is the ripple energy that is stored in the capacitor, and $v_{C\_\max}$ and $v_{C\_\min}$ are the maximum and minimum voltages across the capacitor. According to (1), there are two ways to increase ΔE. One is to increase the capacitance C, and the other way is to increase the voltage fluctuation across the capacitor. Instead of increasing the capacitance, the proposed control system will increase the voltage fluctuation across the qZS capacitors to buffer more double-frequency power. A dedicated strategy is needed to impose the DFR on qZS capacitors while preventing the ripple energy from flowing into the input. In order to achieve this, a modified modulation strategy and an input DFR suppression controller are presented.

In conventional single-phase qZSI, the modulation strategy is shown in Fig. 2(a). The two phase legs of the full bridge are modulated with 180° opposed reference waveforms, m and m', to generate three-level voltage output. Two straight lines v_p^* and v_n^* are used to generate the shoot through duty ratio. When the triangular carrier is greater than v_p^* or the carrier is smaller than v_n^*, all four switches $S_1 - S_4$ turn on simultaneously for shoot-through.

In the proposed control system, the shoot-through control lines v_p^* and v_n^* are modified to a line with double-frequency component as shown in Fig. 2(b). By doing so, the dc side and the qZS capacitor DFR can be decoupled. An input DFR

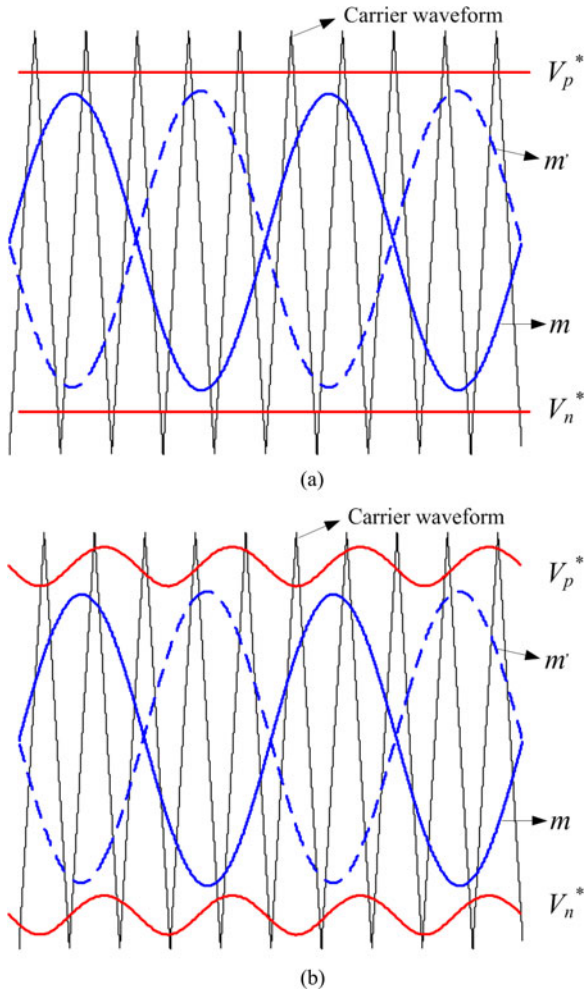


Fig. 2. Modulation strategy of (a) traditional method and (b) proposed method.

suppression controller is added in the control system to generate the double-frequency component in v_p^* and v_n^*.

Fig. 3 shows the detailed control system diagram of the proposed single-phase qZSI. The proposed control contains the maximum power point tracking (MPPT) controller, grid-connected current controller, qZS capacitor voltage controller, and input DFR suppression controller. The MPPT controller provides the input voltage reference v_{IN}^*. The error between v_{IN}^* and v_{IN} is regulated by a PI controller and its output is the magnitude of the grid current reference. The grid current i_g is regulated by controlling the inverter modulation index m through a proportional resonant (PR) controller. The PR controller has a resonance frequency equal to the grid frequency. The qZS capacitor voltage is regulated by controlling d_{SH}. The shoot through lines can be generated as $v_p^* = 1 - d_{\mathrm{SH}}$ and $v_{\mathrm{n}}^* = -1 + d_{\mathrm{SH}}$. It is noted that v_{C2} is used for the capacitor voltage control. This is because v_{C2} signal will be used for the qZS network oscillation damping. As will be explained in Section III-A, the oscillation is mainly caused by the resonance among the C_2 and inductors. If the inverter loss is not enough to damp the oscillation, dedicated active damping is needed to deal with the oscillation and v_{C2} information is required for the implementation.

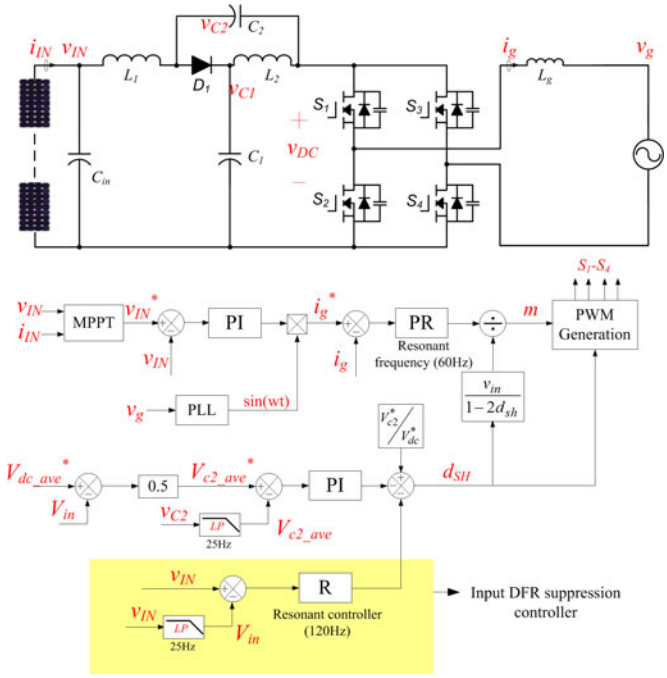


Fig. 3. Diagram of the proposed control system.

Due to the limited space, the detail of the active damping is not presented in this paper and will be covered in future paper. The v_{C2} voltage controller only regulates the average value of v_{C2}, which is V_{c2_ave}, due to the low-pass filter in the signal feedback with a cutoff frequency of 25 Hz. Therefore, the capacitor voltage controller has limited influence on double-frequency component and most DFR energy can be kept in qZS capacitors. The reference $V^*_{c2\_ave}$ is synthesized using the reference value of the average dc-link voltage, $V^*_{dc\_ave}$, and the input voltage average value V_{in}. $V^*_{dc\_ave}$ should be selected carefully so that the value of d_{SH} does not become negative because of the double-frequency swing, and the summation of d_{SH} and m is always smaller than 1. For different input voltages, $V^*_{dc\_ave}$ could be optimized to achieve lowest switching device voltage stress. Selection of $V^*_{dc\_ave}$ will be explained in more detail in Section III-B when we discuss the increased voltage stress across the switching devices. A feed-forward component $V^*_{c2}/V^*_{dc\_ave}$ is added to the output of the capacitor voltage controller to increase the dynamic performance. The DFR suppression controller is composed by one resonant controller whose frequency is designed at two times the grid frequency. The input of the controller is the DFR existed in v_{IN}. It equals to the difference between v_{IN} and V_{in}. The input DFR suppression controller ensures that the DFR in C_1 and C_2 does not flow into the input.

III. Impact of Capacticance Reduction

A. System Stability

In order to apply the proposed control system, it is necessary to study impact of decreasing C_1 on system stability. The possible operation states of voltage fed qZSI have been presented in [13], and it is summarized in the appendix with equivalent circuits, and the averaged model of qZSI can be obtained as

$$\begin{cases} L_1\dfrac{di_{L1}}{dt} = \left(1+\dfrac{T_{AB}+T_{0B}}{T_S-T_{AB}-T_{0B}}\right)(v_{C1}+v_{C2})\,d_{\rm SH} \\ \qquad + \dfrac{T_{\rm SBU}}{T_S-T_{AB}-T_{0B}}(v_{C1}+v_{C2}) - v_{C1} + v_{\rm IN} \\ L_2\dfrac{di_{L2}}{dt} = \left(1+\dfrac{T_{AB}+T_{0B}}{T_S-T_{AB}-T_{0B}}\right)(v_{C1}+v_{C2})\,d_{\rm SH} \\ \qquad + \dfrac{T_{\rm SBU}}{T_S-T_{AB}-T_{0B}}(v_{C1}+v_{C2}) - v_{C2} \\ C_1\dfrac{dv_{C1}}{dt} = i_{L1} - (i_{L1}+i_{L2})\,d_{\rm SH} - \dfrac{T_{\rm SBU}}{T_S}(i_{L1}+i_{L2}) \\ \qquad - \left(\dfrac{T_{\rm AC}}{T_S}+\dfrac{T_{AB}}{T_S}\right) i_{\rm DC} \\ C_2\dfrac{dv_{C2}}{dt} = i_{L2} - (i_{L1}+i_{L2})\,d_{\rm SH} \\ \qquad - \dfrac{T_{\rm SBU}}{T_S}(i_{L1}+i_{L2}) - \left(\dfrac{T_{\rm AC}}{T_S}+\dfrac{T_{AB}}{T_S}\right) i_{\rm DC} \end{cases} \tag{2}$$

where T_s is the switching period, T_{AB}, T_{0B}, $T_{\rm SBU}$, $T_{\rm AC}$, and T_{SBI} are time intervals of different operation states, as listed in the appendix, m is the modulation signal and $d_{\rm SH} = T_{SBI}/T_s$. The small signal model can be derived accordingly as

$$\begin{cases} L_1\dfrac{d\hat{i}_{L1}}{dt} = \left(1+\dfrac{T_{AB}+T_{0B}}{T_S-T_{AB}-T_{0B}}\right)(V_{c1}+V_{c2})\,\hat{d}_{\rm SH} \\ \qquad + \dfrac{T_{\rm SBU}+T_{AB}+T_{0B}}{T_S-T_{AB}-T_{0B}}(\hat{v}_{C1}+\hat{v}_{C2}) \\ \qquad - (1-D_{\rm sh})\hat{v}_{C1} + D_{\rm sh}\hat{v}_{C2} + \hat{v}_{\rm IN} \\ L_2\dfrac{d\hat{i}_{L2}}{dt} = \left(1+\dfrac{T_{AB}+T_{0B}}{T_S-T_{AB}-T_{0B}}\right)(V_{c1}+V_{c2})\,\hat{d}_{\rm SH} \\ \qquad + \dfrac{T_{\rm SBU}+T_{AB}+T_{0B}}{T_S-T_{AB}-T_{0B}}(\hat{v}_{C1}+\hat{v}_{C2}) \\ \qquad -(1-D_{\rm sh})\hat{v}_{C2} + D_{\rm sh}\hat{v}_{C1} \\ C_1\dfrac{d\hat{v}_{C1}}{dt} = \left(1-D_{\rm sh}-\dfrac{T_{\rm SBU}}{T_S}\right)\hat{i}_{L1} - \left(D_{\rm sh}+\dfrac{T_{\rm SBU}}{T_S}\right)\hat{i}_{L2} \\ \qquad + (I_{l1}+I_{l2})\,\hat{d}_{\rm SH} - \left(\dfrac{T_{AB}}{T_S}+\dfrac{T_{\rm AC}}{T_S}\right)\hat{i}_{\rm DC} \\ C_2\frac{d\hat{v}_{C2}}{dt} = \left(1-D_{\rm sh}-\frac{T_{\rm SBU}}{T_S}\right)\hat{i}_{L2} - \left(D_{\rm sh}+\dfrac{T_{\rm SBU}}{T_S}\right)\hat{i}_{L1} \\ \qquad + (I_{l1}+I_{l2})\,\hat{d}_{\rm SH} - \left(\dfrac{T_{AB}}{T_S}+\dfrac{T_{\rm AC}}{T_S}\right)\hat{i}_{\rm DC}. \end{cases} \tag{3}$$

The variables with "^" in (3) denote the small signal perturbations. V_{c1}, V_{c2}, I_{l1}, I_{l2}, and $D_{\rm sh}$ are the steady-state capacitor voltage, inductor current, and shoot-through duty cycle, respectively.

The transfer function from shoot-through duty cycle of $\hat{d}_{\rm SH}$ to capacitor voltage $\hat{v}_{C2}$, denoted as $G^{v_{C2}}_{d_{\rm SH}}$, can be derived as

$$G^{v_{C2}}_{d_{\rm SH}} = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{4}$$

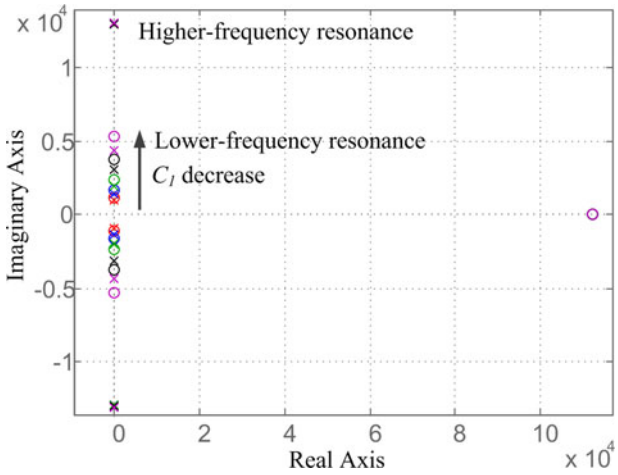


Fig. 4. Root loci of the system with C_1 parameter sweeping.

where

$$a_0 = (1-2D_{\rm sh})^2 - 2(\lambda_1+\lambda_3)(1-2D_{\rm sh}) + 4\lambda_1\lambda_3,$$
$$a_1 = 0, \quad a_2 = (L_1+L_2)(C_1+C_2)(\lambda_1+D_{\rm sh})(\lambda_3+D_{\rm sh}) + (L_1C_1+L_2C_2)(1-2D_{\rm sh}-\lambda_1-\lambda_3),$$
$$a_3 = 0, \quad a_4 = L_1L_2C_1C_2,$$
$$b_0 = (V_{c1}+V_{c2})(1+\lambda_2)(1-2D_{\rm sh}-2\lambda_3),$$
$$b_1 = (I_{L1}+I_{L2})[L_2(D_{\rm sh}+\lambda_1-1) - L_1(D_{\rm sh}+\lambda_1)],$$
$$b_2 = C_1(V_{c1}+V_{c2}) \begin{bmatrix} L_1(1+\lambda_2) \\ -(L_1+L_2)(D_{\rm sh}+D_{\rm sh}\lambda_2+\lambda_3+\lambda_2\lambda_3) \end{bmatrix},$$
$$b_3 = -L_1L_2C_1(I_{l1}+I_{l2}),$$
$$\lambda_1 = \frac{T_{\rm SBU}+D_{\rm sh}(T_{AB}+T_{0B})}{T_S-T_{AB}-T_{0B}},$$
$$\lambda_2 = \frac{T_{AB}+T_{0B}}{T_S-T_{AB}-T_{0B}}, \quad \lambda_3 = \frac{T_{\rm SBU}}{T_S}$$

The root loci of transfer function $G_{d_{\rm SH}}^{v_{C2}}$ are drawn in Fig. 4 by sweeping the value of C_1 capacitance to analyze the dynamic characteristics of the qZSI. When drawing the root loci, other parameters are fixed as $C_2 = 20$ μF, $L_1 = 330$ μH, $L_2 = 215$ μH, $L_g = 600$ μH, $v_{in} = 140$ V, and $D_{\rm sh} = 0.08$. The right-half-hand plane (RHP) zero indicates the qZS network is a nonminimum phase system. This RHP zero will limit the system dynamic response. However, the decrease of C_1 will not significantly change the position of the RHP zero. There are two pairs of conjugated poles located on the imaginary axis, which indicate possible resonances at two different frequencies. The lower frequency resonance is more related to C_1 and the higher frequency resonance is mainly determined by C_2. Therefore, it is seen that the higher resonant frequency does not change much with the C_1 change. The lower resonant frequency increases when C_1 decreases. Because there is always a zero close to the lower frequency pole, the lower frequency resonance is largely damped. Decreasing C_1 does not affect the system stability much.

B. Increased Device Voltage Stress and Power Loss

When the proposed method is applied, the double-frequency voltage ripple across v_{C1} and v_{C2} will be increased intentionally. The dc-link voltage across the H-bridge $v_{\rm DC}$ will also include DFR which could increase the voltage stress of switching devices. Because v_{C1} is much higher than v_{C2}, most double-frequency energy is stored in C_1. The value of v_{C1} can be calculated using the following equation:

$$\frac{1}{2}C_1v_{C1}^2 = \frac{1}{2}C_1V_{c1\_ave}^2 + \int_0^t (P_{\rm in}-p_{\rm AC})dt \tag{5}$$

where V_{c1_ave} is the average value of v_{C1}, $P_{\rm in}$ is the input power, and $p_{\rm AC}$ is the instantaneous ac output power. $p_{\rm AC}$ can be calculated as

$$p_{\rm AC} = V_{g\_p}\sin(\omega t)\times I_{g\_p}\sin(\omega t) = \frac{1}{2}V_{g\_p}I_{g\_p}[1-\cos(2\omega t)] = P_{\rm in}[1-\cos(2\omega t)] \tag{6}$$

where V_{g_p} and I_{g_p} are the peak value of v_g and i_g. Therefore, we can get

$$v_{C1} = V_{c1\_ave}+\Delta v_{c1\_dfr} = \sqrt{V_{c1\_ave}^2+\frac{P_{\rm in}}{\omega C_1}\sin(2\omega t)} = \sqrt{\left(\frac{V_{\rm dc\_ave}+V_{\rm in}}{2}\right)^2+\frac{P_{\rm in}}{\omega C_1}\sin(2\omega t)} \tag{7}$$

where Δv_{c1_dfr} is the DFR component of v_{C1}. In (7), the value of $V_{\rm in}$ and $P_{\rm in}$ are determined by the PV array operating point. $V_{\rm dc\_ave}$ is indirectly controlled by regulating V_{c2_ave} as shown in Fig. 3. Therefore, when $V_{\rm dc\_ave}^*$ is selected and the PV array operating point is determined, $v_{\rm C1}$ can be calculated. It is seen that larger Δv_{c1_dfr} can reduce the size of C_1. $v_{\rm DC}$ during nonshoot period can be obtained as

$$v_{\rm DC} = 2v_{C1}-V_{\rm in} = 2\sqrt{\left(\frac{V_{\rm dc\_ave}+V_{\rm in}}{2}\right)^2+\frac{Pin}{\omega C_1}\sin(2\omega t)}-V_{\rm in}. \tag{8}$$

It is seen from (8), when C_1 and $P_{\rm in}$ are fixed, the switching device voltage stress is mainly determined by $V_{\rm dc\_ave}$ and $V_{\rm in}$. There is an optimized value of $V_{\rm dc\_ave}^*$ for different input voltage conditions to minimize the switching device voltage stress. In order to get the optimized value of $V_{\rm dc\_ave}^*$, $d_{\rm SH}$ and m need to be first calculated as

$$d_{\rm SH} = D_{\rm sh\_ave}+\Delta d_{\rm sh\_dfr} = \frac{v_{C1}-V_{\rm in}}{2v_{C1}-V_{\rm in}} = \frac{\sqrt{\left(\frac{V_{\rm dc\_ave}+V_{\rm in}}{2}\right)^2+\frac{P_{\rm in}}{\omega C_1}\sin(2\omega t)}-V_{\rm in}}{2\sqrt{\left(\frac{V_{\rm dc\_ave}+V_{\rm in}}{2}\right)^2+\frac{P_{\rm in}}{\omega C_1}\sin(2\omega t)}-V_{\rm in}} \tag{9}$$

TABLE I
PARAMETERS OF THE QZSI UNDER STUDY

qZSI Component	Parameters
Input voltage $v_{\rm IN}$	140–180 V
Grid voltage v_g	120 Vrms
C_1	2 mF for conventional system 200 μF for proposed system
C_2	20 μF
L_1	330 μH
L_2	215 μH
L_g	600 μH
Switching frequency	100 kHz

where $D_{\rm sh\_ave}$ and $\Delta d_{\rm sh\_dfr}$ are the average value and double-frequency component of $d_{\rm SH}$, respectively

$$m = \frac{V_{g\_p}\sin(\omega t)}{v_{\rm DC}}. \tag{10}$$

In order to take advantage of the buck–boost feature of the qZSI, the input voltage range is usually selected that V_{g_p} is among the input voltage range. For the proposed method, the maximum switching device voltage stress could happen at maximum or minimum $V_{\rm in}$. When $V_{\rm in}$ is larger than V_{g_p}, no shoot-through is needed in conventional design and $d_{\rm SH}$ equal to zero. However, for the proposed method, certain value of $D_{\rm sh\_ave}$ is needed to make sure $d_{\rm SH}$ does not become negative values because of the double-frequency swing. Higher $V_{\rm in}$ leads to higher peak value of $v_{\rm DC}$. Therefore, one of the worst cases for the increased device voltage stress could happen at maximum $V_{\rm in}$. In this case, according to (9), $V^*_{\rm dc\_ave}$ can be optimized that $D_{\rm sh\_ave}$ is equal to the peak value of $\Delta d_{\rm sh\_dfr}$, so the increased voltage stress can be minimized. On the other hand, when $V_{\rm in}$ is smaller than V_{g_p} and it is at lowest value, large $D_{\rm sh\_ave}$ is needed to guarantee that $v_{\rm DC}$ is always larger than v_g. Therefore, it could be another worst case for the increased device voltage stress. In this case, $V^*_{\rm dc\_ave}$ can be properly selected that the peak value of $d_{{\rm SH}+m}$ is equal to 1, so the increased voltage stress can be minimized. For input voltages between the minimum and maximum, $V^*_{\rm dc\_ave}$ can be selected either when $D_{\rm sh\_ave}$ is equal to the peak value of $\Delta d_{\rm sh\_dfr}$ or the peak value of $d_{{\rm SH}+m}$ is equal to 1. Numeric example will be provided in the prototype design in next section.

For the proposed method, there is a design tradeoff between the demand of decreasing C_1 and the increased voltage stress across the switching devices. This should be considered in the system design. Due to the increased voltage stress and DFR flowing in the qZS network, it is also expected that there is extra power loss compared with the conventional design. This will be demonstrated in the experimental study.

IV. PROTOTYPE DESIGN AND EXPERIMENTAL RESULTS

A 1-kW qZSI prototype was built in the lab. The parameters of the qZSI are provided in Table I. In the qZSI, the voltage across C_1 is higher than the voltage across C_2, so C_1 is designed to handle the DFR. The quasi-Z-source network design can refer to the model developed in [8]. For the conventional design, in order to achieve 5% voltage ripple at the input side, 2 mF capacitor is needed for C_1. By utilizing the proposed control strategy, C_1 can be reduced to 200 μF considering the design tradeoff discussed in Section III-B. C_2 is designed to limit the high-frequency voltage ripple to 1% of the maximum voltage across C_2. The L_1 and L_2 are designed to limit the high-frequency ripple to 20% of the maximum current through L_1 and L_2, respectively.

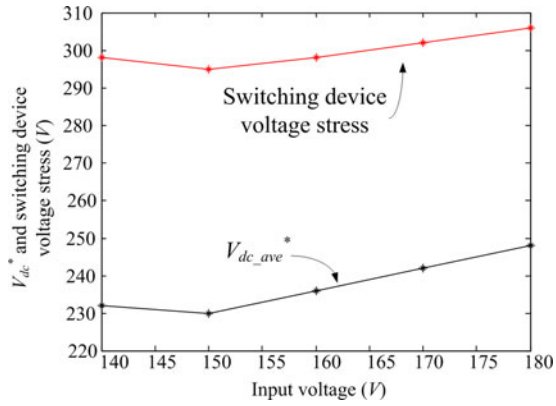


Fig. 5. $V^*_{\rm dc\_ave}$ and switching device voltage stress at different input voltages.

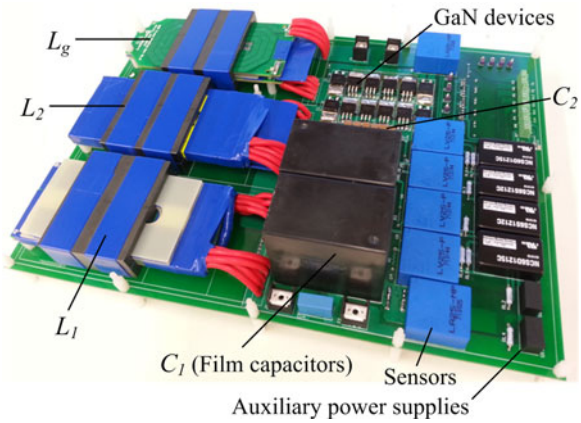


Fig. 6. Prototype of the 1-kW qZSI with minimized capacitance.

In conventional design, the maximum switching device voltage stress equals to 200 V when $V_{\rm in} = 140$ V. For the proposed method, $V^*_{\rm dc}$ and the switching device voltage stress at different input voltages can be calculated based on the analysis in Section III-B. They are provided in Fig. 5. It is seen that the maximum voltage stress across the switching devices happens at $V_{\rm in} = 180$ V in this design. $V^*_{\rm dc\_ave}$ is selected at 248 V, so that $D_{\rm sh\_ave}$ is equal to the peak value of $\Delta d_{\rm sh\_dfr}$. The peak value of $v_{\rm DC}$, also the switching device voltage stress, is increased to 306 V. Therefore, the switching device voltage stress is increased by 53% compared with the conventional design. If the grid voltage is increased to 240 Vrms, the inverter power rating is kept the same and the input voltage is 260–340 V, and C_1 is decreased from 800 μF required in conventional design to 100 μF with the proposed control, the switching device voltage stress is increased by only 15%. Therefore, there is more benefit to apply the proposed method in qZSI with higher output voltage.

The picture of the 1-kW qZSI prototype with minimized capacitance is shown in Fig. 6. TPH3006PS GaN devices from Transphorm are selected as the inverter switches and the switching frequency is selected at 100 kHz. In the experimental study, the Magna Power Electronics XRii 250–16 was used as the

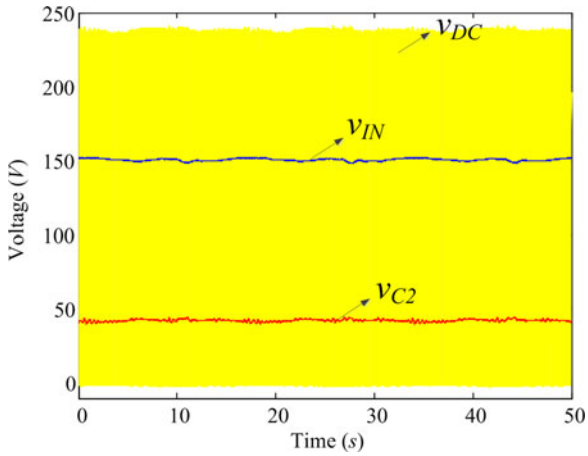


Fig. 7. $v_{\rm DC}$, $v_{\rm IN}$, and v_{C2} waveforms of the qZSI with the conventional control, $C_1 = 2$ mF.

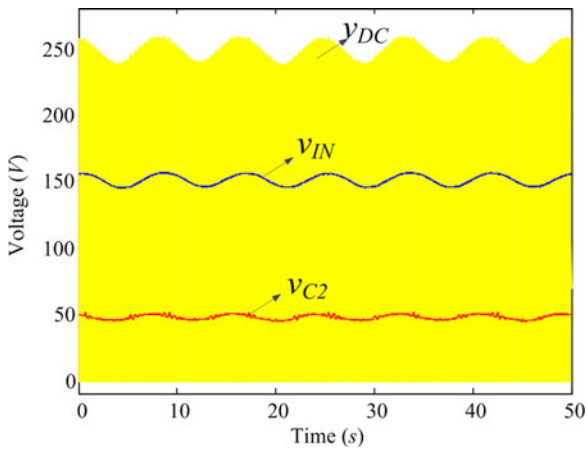


Fig. 8. $v_{\rm DC}$, $v_{\rm IN}$, and v_{C2} waveforms of the qZSI with the conventional control, $C_1 = 200$ μF.

PV emulator. The waveforms of $v_{\rm DC}$, v_{C2}, and $v_{\rm IN}$ for the qZSI system with 2 mF capacitor are shown in Fig. 7. The input voltage was 150 V and the output voltage was 120 Vrms. The inverter was operated at 300 W output power condition. The double-frequency components in $v_{\rm DC}$, v_{C2}, and $v_{\rm IN}$ were 0.72, 0.336, and 0.774 V. The 120-Hz ripple in $v_{\rm IN}$ was limited because of the large capacitance. The waveforms for the qZSI with 200 μF capacitor, but without the proposed control, are provided in Fig. 8. Because the C_1 was significantly reduced, the 120-Hz ripples in $v_{\rm DC}$, v_{C2}, and $v_{\rm IN}$ increased to 7.18, 2.39, and 5.302 V, respectively. The distribution of the 120-Hz ripple largely depends on the impedance network. The conventional control has minor influence on the ripple distribution. The large 120-Hz ripple in $v_{\rm IN}$ could influence the PV energy harvesting. The waveforms of the system with the proposed control strategy are shown in Fig. 9. The 120-Hz ripples in $v_{\rm DC}$, v_{C2} and $v_{\rm IN}$ were increased to 9.186, 8.75 and 0.45 V, respectively. As expected, most 120-Hz ripple energy was imposed on C_1 and C_2. The corresponding output current waveform is shown in Fig. 10 and its total harmonic distortion value is 4.4%.

The efficiency comparison of the conventional qZSI and the qZSI with proposed control at different power outputs is provided in Table II. As expected in the discussion in Section III-B,

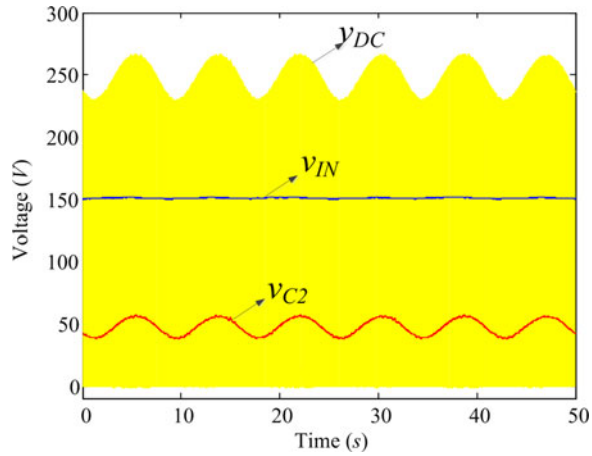


Fig. 9. $v_{\rm DC}$, $v_{\rm IN}$, and v_{C2} waveforms of the qZSI with the proposed control, $C_1 = 200$ μF.

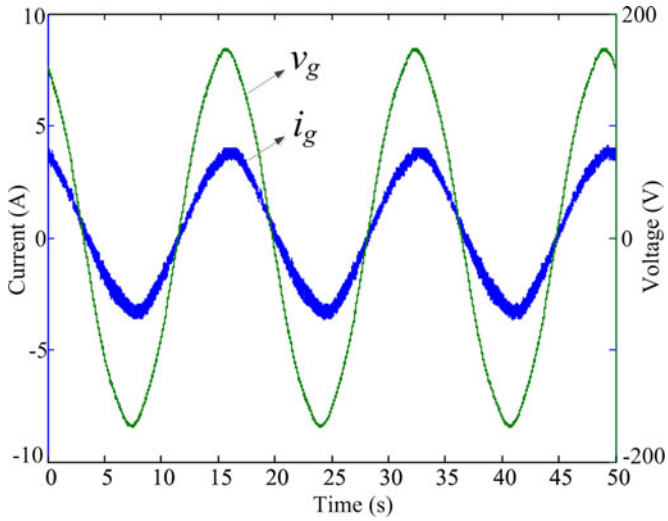


Fig. 10. Output current waveform of the qZSI with the proposed control, $C_1 = 200$ μF.

TABLE II
EFFICIENCY COMPARISON OF THE CONVENTIONAL QZSI AND QZSI WITH THE PROPOSED CONTROL

	300 W	400 W	500 W	600 W
$C_1 = 2$ mF with conventional control	93.05%	93.18%	93.66%	93.76%
$C_1 = 200$ μF with proposed control	92.36%	93.06%	93.48%	93.55%

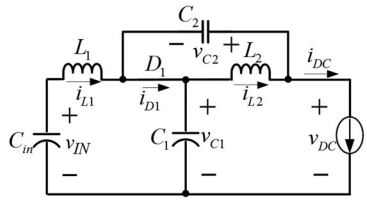
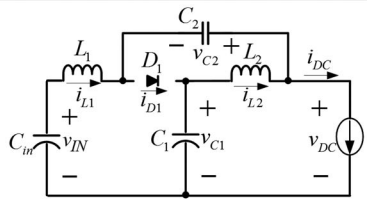
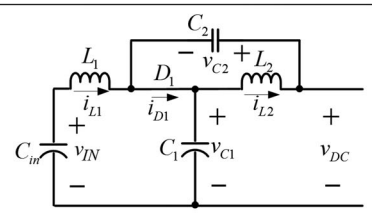
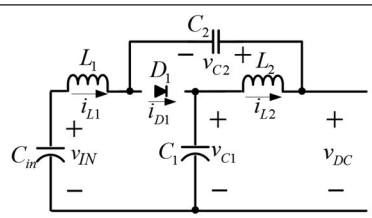
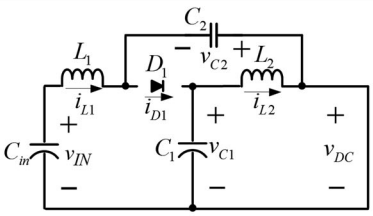
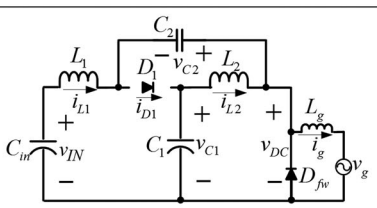
because of the increased voltage stress and 120-Hz ripple flowing in the qZS network, the efficiencies of the proposed system were around 0.12%–0.69% lower than the conventional system. The C_1 capacitance was reduced by ten times, but with the expense of efficiency decrease. Although the efficiency drop was not significant, it should be considered in the design stage if higher efficiency is desired.

V. CONCLUSION

In this paper, a new control strategy is proposed to minimize the capacitance requirement in single-phase qZSI PV system.

Instead of using large capacitance, the qZS capacitors are imposed with higher double-frequency voltages to store the DFR energy. In order to prevent the ripple energy flowing into the input PV side, a modified modulation and an input DFR suppression controller are used to decouple the input voltage ripple from the qZS capacitor DFR. The small signal model is developed and shows that the capacitance reduction does not impact the system stability much. For the developed 1-kW quasi-Z-source PV system, 2 mF capacitor can be replaced with a 200 μF capacitor by using the proposed method. However, the voltage stress across the switching devices was increased by 53% compared with the conventional design. The efficiency was decreased by 0.12%-0.69% at several selected operation points. It is also shown that there is more benefit if the method is applied for 240 Vrms output qZSI. The increase of the switching device voltage stress is only 15% compared with conventional design. This control strategy can also be applied in single-phase ZSI applications.

APPENDIX
OPERATION STATES, EQUIVALENT CIRCUITS, AND DYNAMIC STATE EQUATIONS OF QZSI

Operation States	Equivalent Circuit	Dynamic State Equation
➢ State 1: Active state with conducting diode ➢ Time Interval: T_{AC}		$\begin{cases} L_1\frac{di_{L1}}{dt} = v_{IN} - v_{C1} \\ L_2\frac{di_{L2}}{dt} = -v_{C2} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} - i_{DC} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} - i_{DC} \end{cases}$
➢ State 2: Active state with blocking diode ➢ Time interval: T_{AB}		$\begin{cases} L_1\frac{di_{L1}}{dt} = v_{IN} + v_{C2} - v_{DC} \\ L_2\frac{di_{L2}}{dt} = v_{C1} - v_{DC} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} - i_{DC} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} - i_{DC} \end{cases}$
➢ State 3: Zero state with conducting diode ➢ Time interval: T_{0C}		$\begin{cases} L_1\frac{di_{L1}}{dt} = v_{IN} - v_{C1} \\ L_2\frac{di_{L2}}{dt} = -v_{C2} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} \end{cases}$
➢ State 4: Zero state with blocking diode ➢ Time interval: T_{0B}		$\begin{cases} L_1\frac{di_{L1}}{dt} = v_{IN} + v_{C2} - v_{DC} \\ L_2\frac{di_{L2}}{dt} = v_{C1} - v_{DC} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} \end{cases}$
➢ State 5: Shoot-through state with blocking diode (intended case) ➢ Time interval: T_{SBI}		$\begin{cases} L_1\frac{di_{L1}}{dt} = v_{IN} + v_{C2} \\ L_2\frac{di_{L2}}{dt} = v_{C1} \\ C_1\frac{dv_{C1}}{dt} = -i_{L2} \\ C_2\frac{dv_{C2}}{dt} = -i_{L1} \end{cases}$
➢ State 6: Shoot-through state with blocking diode (unintended case) ➢ Time interval: T_{SBU}		$\begin{cases} L_1\frac{di_{L1}}{dt} = v_{IN} + v_{C2} \\ L_2\frac{di_{L2}}{dt} = v_{C1} \\ C_1\frac{dv_{C1}}{dt} = -i_{L2} \\ C_2\frac{dv_{C2}}{dt} = -i_{L1} \end{cases}$

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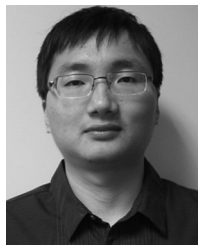

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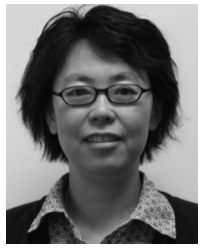

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