A Bidirectional Three-Level *LLC* Resonant Converter With PWAM Control

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***Abstract*—This paper proposes a bidirectional three-level *LLC* resonant converter with a new pulse width and amplitude modulation control method. With different control signals, it has three different operation modes with different voltage gains. Therefore, it can achieve wide voltage gain range by switching among these three modes, which is attractive for energy storage system applications needing wide voltage variation. The proposed topology operates with constant switching frequency, which is easy to implement with digital control, and it can achieve soft switching for all the switches and diodes in the circuit as a conventional *LLC* resonant converter. The performance of the proposed converter is validated by the experimental results from a 1-kW prototype with 20 A maximum output current.**

***Index Terms*—Bidirectional, constant switching frequency, *LLC*, three-level (TL), wide voltage gain.**

I. Introduction

MORE and more research efforts have been focused on how to use the clean energy in an efficient way in recent years for energy saving and environment protection. The distributed generation systems (DGSs) with clean renewable energy resources like photovoltaic, wind power, and fuel cell are widely adopted around the world. However, the intermittent nature of these clean renewable energy resources may cause fluctuation between power generation and consumption [1], [2]. So energy storage systems (ESSs) are required in DGSs to deal with the intermittent outages and make the system more stable and reliable. Batteries and super capacitors are the most popular energy storage components considering the price and performance. Fig. 1 shows a typical DGS with renewable energy resources and ESSs. The ESSs should have bidirectional power flow capability to store the excess energy generated by renewable resources, and release it when the load is heavy or renewable energy is not sufficient [3], [4]. The bidirectional dc–dc converter is a key component in ESSs to enable the bidirectional power flow. Galvanic isolation is usually required for safety consideration. Besides, voltage variation of both the renewable energy resources and energy storage components is wide, so the voltage gain range of the bidirectional dc–dc converter should be as wide as possible.

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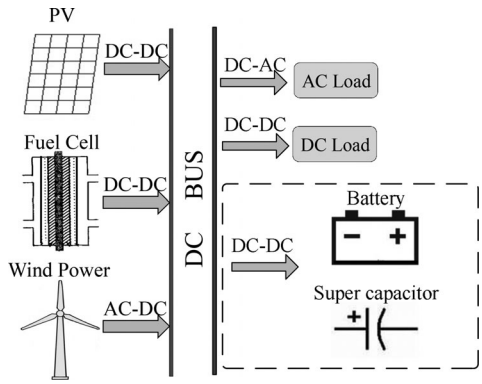

Fig. 1. Typical DG system with ESSs.

Many isolated bidirectional topologies have been proposed and studied in recent years, and the dual-active-bridge converter is one of the most popular topologies for its simplicity and high power density [5]–[19]. However, it suffers from high circulating energy and high turn-off power loss. A lot of control methods have been proposed to minimize the circulating energy or extend its soft-switching range by phase shift or duty cycle control, but the control methods are complex and cannot solve all the disadvantages at the same time [12]–[18].

In order to further improve the efficiency, an *LLC* resonant converter is a promising candidate. It can achieve soft switching for all the power devices and its efficiency is quite high [19]–[22]. A bidirectional *LLC* resonant topology for vehicular applications was proposed in [23]. The topology was still a traditional SRC during backward operation, which can only operate under buck mode. In [24], a symmetrical bidirectional *CLLC* resonant converter with two resonant tanks was proposed. The extra resonant tank increased both the cost and volume of the converter, and the voltage gain was reduced compared with the traditional *LLC* converter especially at heavy-load condition. Furthermore, forward mode and backward mode cannot be switched automatically, and the current in the output side has to flow through the body diodes of the switches which may cause high conduction loss. A bidirectional *LLC* resonant converter with an auxiliary inductor is proposed in [25], which has a symmetrical structure in forward mode and backward mode, and it can automatically change the power flow direction by simply regulating the switching frequency. However, the voltage gain is still limited for reasonable conversion efficiency and switching frequency variation range.

To limit the switching frequency variation and achieve wide voltage gain range, the constant frequency phase shift control method for *LLC* resonant converters are proposed [26]–[32], but the converter will loss zero-voltage switching (ZVS) under low

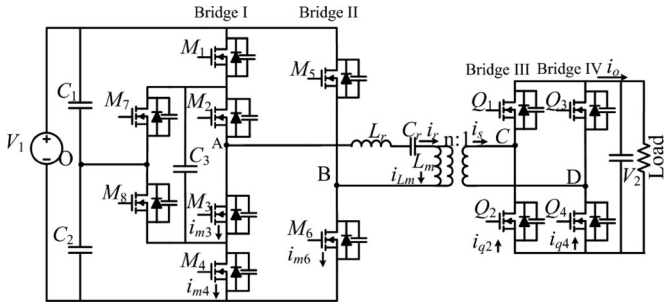

Fig. 2. Proposed bidirectional TL *LLC* resonant converter.

TABLE I
AMPLITUDE OF V_{AB} WITH DIFFERENT ON/OFF STATUS OF M_1–M_6

M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	V_{AB}
1	1	0	0	0	1	0	0/1	V_1
0	1	0	1/0	0	1	1/0	0	$0.5V_1$
1/0	0	1	0	0	1	0	1/0	$0.5V_1$
1	1	0	0	1	0	0	1/0	0
0	0	1	1	0	1	1/0	0	0
0	1	0	1/0	1	0	1/0	0	$-0.5V_1$
1/0	0	1	0	1	0	0	1/0	$-0.5V_1$
0	0	1	1	1	0	1/0	0	$-V_1$

voltage gain or light-load condition [26]–[31]. In [32] and [33], soft switching can always be achieved with extra components, which increases cost and complexity. A unidirectional three-level (TL) constant-frequency *LLC* resonant converter with hybrid full-bridge structure is proposed in [34] to achieve wider voltage gain range. However, duty cycle has to be very small in low voltage gain condition, the ZVS will be lost and the conduction loss is high due to small duty cycle.

To further improve the performance of a bidirectional *LLC* resonant converter, this paper proposes a TL *LLC* converter with a pulse width and amplitude modulation (PWAM) control method. The switching frequency is constant and equal to its resonant frequency, thus the converter can achieve soft switching for all switches easily. With three different control schemes, the converter can achieve a wide voltage gain.

The proposed bidirectional TL *LLC* resonant converter is shown in Fig. 2, which has a hybrid full-bridge structure with MOSFETS M_1–M_6 in the transformer primary side and a full-bridge structure with MOSFETs Q_1–Q_4 in the secondary side, D_1 and D_2 are the body diodes of Q_1 and Q_2, D_5–D_8 are the body diodes of MOSFET M_5–M_8, respectively. MOSFETs M_1 to M_4 are connected in series to form a TL switching leg I, M_5 and M_6 are series connected to form bridge leg II. "A" and "B" are the midpoints of bridge leg I and II. "C" and "D" are the midpoints of secondary-side full bridge. *n* is the transformer turns ratio. In order to achieve bidirectional power flow, MOSFETs M_7 and M_8 are used as clamp switches instead of conventional clamp diodes. The input source V_1 is in the transformer primary side, while the energy storage element V_2 is in the transformer secondary side. L_r is the resonant inductor, C_r is the resonant capacitor, and L_m is the magnetizing inductor of the transformer. Capacitor C_3 is the flying capacitor.

The operation principle in forward mode and backward mode are analyzed in Section II and Section III, respectively. Section IV presents the performance analysis and design considerations for the proposed bidirectional *LLC* converter. A prototype with maximum 20-A output current is built and the experiments results are given in Section V.

To simplify the steady-stage analysis, some assumptions are given as follows:

1) all the MOSFETs with their body diodes and all the passive components are ideal, the dead time between switching signals are neglected;
2) output capacitor C_o is large enough and the output voltage V_2 is constant; C_1 and C_2 are also large enough, the voltage ripple can be neglected, and the dc voltage across them is 0.5 V_1;
3) C_{oss1}–C_{oss8} are the parasitic capacitors of M_1–M_8, which have the same capacitance C_{oss}; the parasitic capacitors of Q_1–Q_4 also have the same capacitance C_{oss} referred to the transformer primary side;
4) current of the MOSFET is assumed to be constant during its ON/OFF transient.

II. FORWARD MODE OPERATION

When the converter is in forward mode operation, the MOSFETs in the primary side can be divided into three pairs: M_1 and M_4, M_2 and M_3, and M_5 and M_6. MOSFETs in each pair turn ON and OFF complementary. M_7 and M_8 are always OFF and their body diodes are used to clamp the voltage of M_1–M_4 to half of the input voltage. Q_1–Q_4 form the rectifier circuit in the secondary side. Since the voltage drop on MOSFETs' body diodes is high, Q_3 and Q_4 are used as synchronous rectifier to reduce the conduction loss, while Q_1 and Q_2 are always OFF to ensure DCM operation.

V_{AB} is the voltage across point "A" and "B", and the equivalent ac voltage of V_{AB} is applied to the resonant tank, and the output voltage is determined by its amplitude and pulse width. Since the switching frequency is constant, duty cycle and phase shift angles between different pairs of MOSFETs are used to regulate the amplitude and pulse width of V_{AB}, so the proposed control method is a kind of PWAM method. With PWAM control, the amplitude of V_{AB} will be different based on the ON/OFF status of M_1–M_6, which is shown in Table I.

It is seen from Table I that V_{AB} can be $0, \pm 0.5V_1$, and $\pm V_1$. There are three control schemes corresponding to three different operation modes. Fig. 3 shows the steady-state waveforms of the three modes. A brief description of these three modes is given below.

A. High Gain (HG) Mode

The peak-to-peak amplitude of V_{AB} shown in Fig. 3(a) is $2V_1$, which is the highest one and the output voltage gain will also be the highest, so it is called the HG mode. Duty cycle of M_1 and M_3 is equal to α, and α is the control variable in HG mode to regulate the output voltage. The duty cycle of M_5 and M_6 is always 0.5. The phase shift time between M_1/M_4 and M_3/M_2 is always equal to $0.5T_s$. The switching frequency is fixed to the resonant frequency f_r formed by L_r and C_r, i.e., $T_s = 1/f_r$.

There are six stages in one switching cycle T_s, and the corresponding equivalent circuits of the first-half switching cycle are shown in Fig. 4(a)–(c).

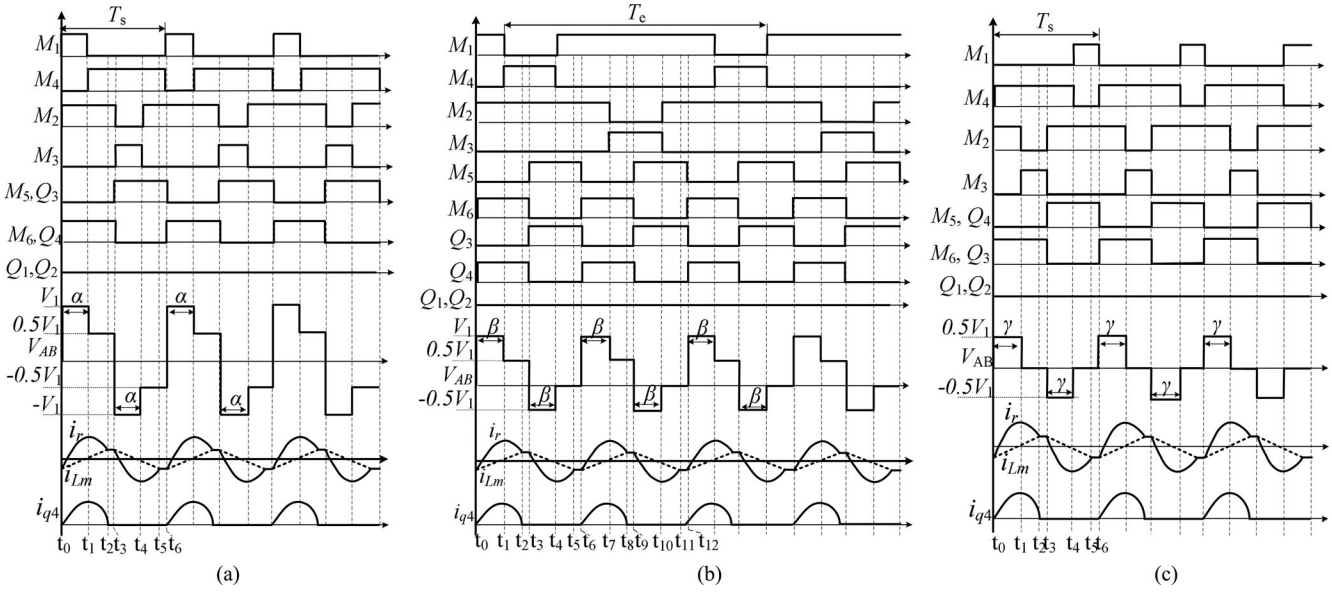

Fig. 3. Control schemes and related waveforms: (a) HG mode, (b) MG mode, (c) LG mode.

Stage 1 (t_0–t_1): In this stage, M_1, M_2, and M_6 in the primary side and Q_1's body diode D_1 and Q_4 in the secondary side are ON, as shown in Fig. 4(a). The resonant current i_r is negative and equal to the magnetizing current i_{Lm} at t_0, and it increases in a resonant mode during this stage.

Stage 2 (t_1–t_2): M_1 turns OFF and M_4 turns ON at t_1, while M_2, M_6, D_1, and Q_4 keep ON during this stage. V_{AB} is equal to $0.5V_1$. The equivalent circuit is shown in Fig. 4(b). Since the resonant current i_r is above zero, it will charge the parasitic capacitor of M_1 until it reaches $0.5V_1$, and M_4 can turn ON with ZVS. Voltage of the flying capacitor C_3 is clamped to $0.5V_1$ through the body diode of M_7. As soon as i_r equals to i_{Lm} at t_2, this stage ends.

Stage 3 (t_2–t_3): Once i_r is equal to i_{Lm} at t_2, the current through D_1 is zero and it turns OFF with ZCS, the converter goes into DCM operation. Since Q_1 is always OFF, the current will not reverse during this mode. The equivalent circuit is shown in Fig. 4(c). The secondary side is separated from the primary side, and load is supplied by the output capacitor. L_r, L_m, and C_r form the resonant tank. Since L_m is much larger than L_r, the resonant period is quite long and the resonant current decreases slowly. This stage ends when M_2 and M_6 turn OFF at t_3, and M_3 and M_5 can turn ON with ZVS in the next stage.

In the next half switching cycle, the operation principle of stages 4–6 is similar to stages 1–3 except the current direction is changed, which is not repeated here.

B. Medium Gain (MG) Mode

The peak-to-peak amplitude of V_{AB} shown in Fig. 3(b) is equal to $1.5V_1$ and its voltage gain will be lower than the HG mode, so it is called the MG mode. In MG mode, V_{AB} is equal to V_1, $0.5V_1$, $-0.5V_1$ and 0 in different stages in a switching cycle, so it is asymmetrical, and the average dc value of V_{AB} is equal to $0.25V_1$, which is blocked by the resonant capacitor C_r and will not affect the operation of converter. The equivalent ac voltage applied to the resonant tank is also a symmetrical TL voltage. The time duration of $V_{AB} = V_1$ in a switching period is βT_s, and β is the phase shift angle between M_4/M_3 and M_6, which is used to regulate the output voltage in MG mode.

Due to the asymmetrical voltage waveforms of V_{AB}, the control signals for the MOSFETs are also asymmetrical, which makes the energy flow through C_1, C_2, and C_3 unbalanced in a switching cycle. In order to solve this problem, the energy flow through the capacitors should be in opposite direction in next switching cycle, thus the energy can be balanced in two consecutive switching cycles. For example, if the capacitors are charged in the first switching cycle, it should be discharged in the next cycle, and vice versa. Therefore, the switching frequency f_e for M_1–M_4 is half the resonant frequency f_r. It should be known that the switching frequency of M_5/M_6 and Q_3–Q_4 is still equal to the resonant frequency. The relationship between f_e, f_s, and f_r is shown in

$$T_e = \frac{1}{f_e} = 2T_s = \frac{2}{f_s} = \frac{2}{f_r}. \tag{1}$$

There are 12 operation stages in an equivalent switching period.

Stage 1 (t_0–t_1): M_1, M_2, M_6, D_1, and Q_4 conduct in this stage, and the equivalent circuit is shown in Fig. 4(a), which is exactly the same as Stage 1 in HG mode.

Stage 2 (t_1–t_2): M_2, M_4, and M_6 conduct in this stage, which is also same as stage 2 in HG mode. The equivalent circuit is shown in Fig. 4(b). Since i_r is above zero, C_3 will be discharged in this stage.

Stage 3 (t_2–t_3): When i_r equals to i_{Lm} at t_2, the converter is in DCM operation, which is same as stage 3 in HG mode. The equivalent circuit is shown in Fig. 4(c).

Stage 4 (t_3–t_4): M_2, M_4, and M_5 in the primary side and Q_2's body diode and Q_3 in the secondary side conduct in this stage. $V_{AB} = -0.5V_1$, and the equivalent circuit is shown in Fig. 4(d). The resonant current i_r is positive at t_3 and will decrease to negative during this stage. So C_3 will be discharged at first and then it will be charged.

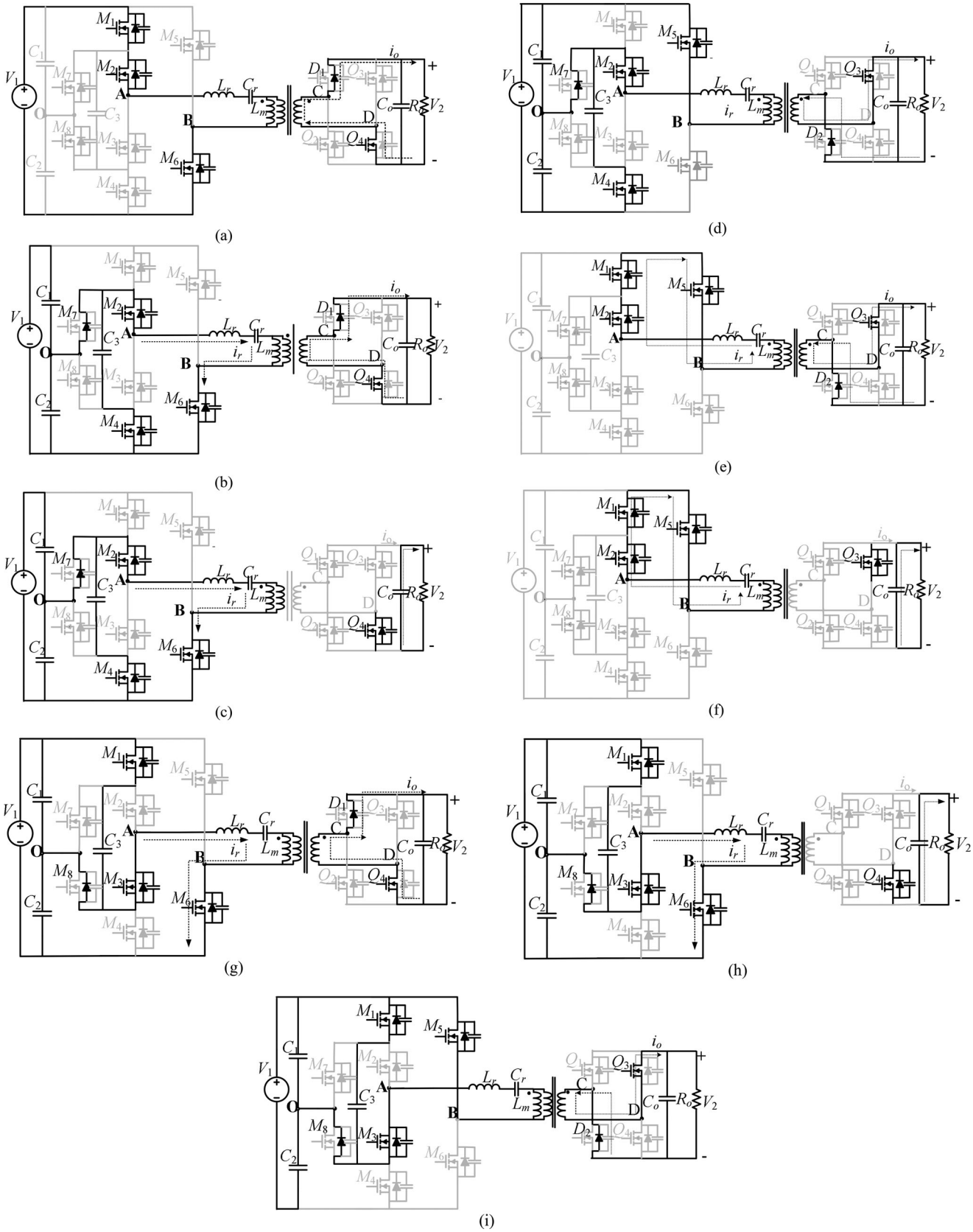

Fig. 4. Equivalent circuits of the converter in different operating stages.

Stage 5 (t_4–t_5): M_4 turns OFF and M_1 turns ON at t_4. $V_{AB} = 0$, and the equivalent circuit is shown in Fig. 4(e). The resonant current decreases to the magnetizing current i_{Lm}, the secondary side keeps the same as previous stage.

Stage 6 (t_5–t_6): Once i_r is equal to i_{Lm}, the secondary-side switches are all OFF, and the converter is in DCM operation. The equivalent circuit is shown in Fig. 4(f).

Stage 7 (t_6–t_7): M_5 turns OFF and M_6 turns ON, the equivalent circuit of stage 7 is same as stage 1 as shown in Fig. 4(a).

Stage 8 (t_7–t_8): M_1, M_3, M_6 in the primary side and Q_1's body diodes and Q_4 in the secondary side conduct. $V_{AB} = 0.5V_1$, the equivalent circuit is shown in Fig. 4(g). Since the resonant current i_r is positive, C_3 will be charged. The amplitude of i_r in stage 2 and stage 8 are same, so the charger variation of C_3 during these two stages is also equal, which can be balanced automatically.

Stage 9 (t_8–t_9): Once i_r is equal to i_{Lm}, the converter is in DCM operation. The equivalent circuit is shown in Fig. 4(h).

Stage 10 (t_9–t_{10}): M_1 and M_3 keep ON, M_6 turns OFF and M_5 turns ON in this stage, and the equivalent circuit is shown in Fig. 4(i). The resonant current i_r is positive at t_9, so C_3 will be charged first. Then, i_r drops to negative and C_3 is discharged. Energy flow through C_1–C_3 is in opposite direction during stage 4 and stage 10, so it can be balanced.

Stage 11 (t_{10}–t_{11}): M_1, M_2, M_5, and Q_3 are ON. The operation principle in stage 11 is same as stage 5, and the equivalent is shown in Fig. 4(e). The resonant current decreases to i_{Lm}.

Stage 12 (t_{11}–t_{12}): Once i_r is equal to i_{Lm}, the converter is in DCM operation. The operation in stage 12 is same as stage 6.

As a conclusion, by adopting the asymmetrical control method, energy of the capacitors C_1–C_3 can always be balanced. Since the switching frequency of M_1–M_4 is half the resonant frequency, the switching loss will also reduce. ZVS can always be achieved for M_1–M_6 and ZCS is achieved for Q_1–Q_4.

C. Low Gain (LG) Mode

The peak-to-peak amplitude of V_{AB} in Fig. 3(c) is equal to V_1, so it is called the LG mode. V_{AB} is equal to $0.5V_1$, 0, –$0.5V_1$, 0 in different stages in this mode. Duty cycle of M_1 and M_3 is equal to (0.5–γ). When γ increases, the pulse width of $V_{AB} = V_1$ also increases. γ is the control variable in LG mode, which is used to control the output voltage.

When the converter is operating in LG mode, it is similar to the traditional phase shift *LLC* resonant converter as proposed in [28], so it is not discussed here. In LG mode, ZVS can be achieved in the primary side and ZCS is achieved in the secondary side.

III. Backward Mode Operation

When the converter is in backward mode operation, the transformer secondary side is the input side. The operation of the converter is similar to a series resonant converter, and the maximum voltage gain is 1.

There are also three operation modes as that in forward mode operation: HG mode, MG mode, and LG mode according to different control schemes. Key waveforms and control schemes of three different modes are shown in Fig. 5. Switching frequency of Q_1–Q_4 is equal to the resonant frequency. M_5 and M_6 are always OFF, and their body diodes are used as rectifier in backward operation. Similar to that in forward operation, the switching frequency of M_1–M_4 is equal to the resonant frequency in HG mode and LG mode, and it will be equal to half the resonant frequency in MG mode.

A. HG Mode

M_5 and M_6 are always OFF and the switching frequency of all the other MOSFETs is equal to f_r. V_{AB} is equal to $0.5V_1$, V_1, –$0.5V_1$, and –V_1 in a switching cycle. α is the duty cycle of M_1 and M_3 which is used to regulate V_1. There are six stages in a switching cycle, which are briefly described as follows.

Stage 1 (t_0–t_1): Q_1 and Q_4 in the secondary side, M_2 M_4, M_7 and D_6 in the primary side are on in this stage, and $V_{AB} = 0.5$ V_1. C_2 and C_3 are charged in parallel.

Stage 2 (t_1–t_2): M_1 and M_8 turn ON, M_4 and M_7 turn OFF at t_1, M_2 and D_6 keep ON. V_{AB} is equal to V_1 in this stage. Current will charge the parasitic capacitor of M_4 and M_7, so M_1 and M_8 can turn ON with ZVS.

Stage 3 (t_2–t_3): i_r is equal to i_{Lm}, so the converter is in DCM operation, D_6 turns OFF with ZCS at t_2. This stage ends when Q_1 and Q_4 turn OFF at t_3, the secondary-side current i_s is positive at t_3, so Q_2 and Q_3 can achieve ZVS in the next stage.

The operation principle for stages 4–6 in the next half switching cycle is similar to stages 1–3 except the current direction, and it is not repeated here.

B. MG Mode

The MG mode in backward operation is similar to that in forward mode operation, and asymmetrical control method is adopted to balance the energy of the capacitors. The key waveforms are shown in Fig. 5(b). Switching frequency f_s of Q_1–Q_4 is equal to the resonant frequency, M_5 and M_6 are always OFF, and the switching frequency f_e of M_1–M_4 and M_7/M_8 is equal to half the resonant frequency. Duty cycle of M_4 and M_7 is 0.25, and β is the phase shift angle between M_4/M_7 and Q_1/Q_4.β is used to regulate the output voltage V_1. There are 12 stages in an equivalent switching cycle T_e, which is from t_0 to t_{12}, as shown in Fig. 5(b). The ON/OFF status of the switches is also given in Fig. 5(b).

V_{AB} is equal to $0.5V_1$, V_1, 0, and –$0.5V_1$ in different stages in a switching cycle. In stage 1 and stage 7 $V_{AB} = 0.5V_1$, the current flow through C_1 and C_2 is balanced in an equivalent switching cycle. In stages 5, 6 and 11, 12, the current flow through C_1 and C_2 is also balanced.

In MG mode, M_5 and M_6 can always achieve ZCS, and all the other MOSFETs can achieve ZVS.

C. LG Mode

Key waveforms and control signals for LG mode operation are shown in Fig. 5(c). V_{AB} in different stages are 0, $0.5V_1$, 0, and –$0.5V_1$. When $V_{AB} = 0.5V_1$ or –$0.5V_1$, output power is supplied by the source in the secondary side; when $V_{AB} = 0$, output power will be supplied by C_1 and C_2. Operation principle in the first-half switching cycle and the second-half switching cycle is

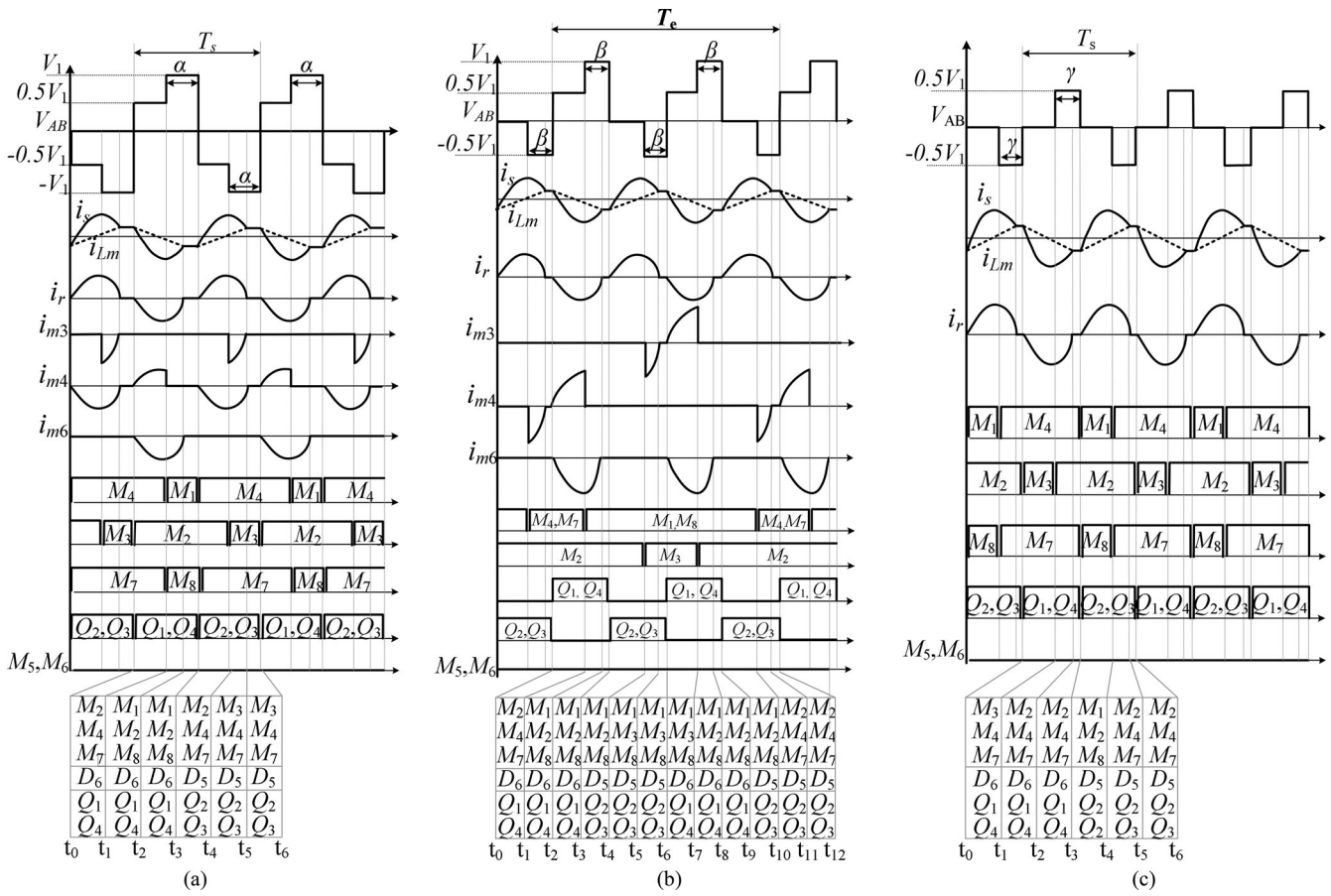

Fig. 5. Waveforms and control schemes in backward operation: (a) HG mode, (b) MG mode, (c) LG mode.

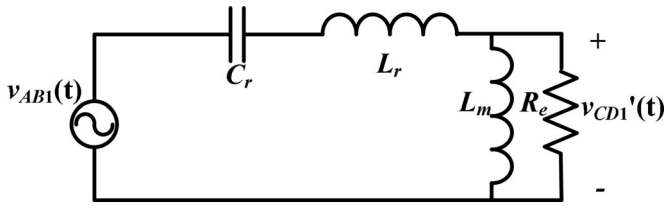

Fig. 6. Simplified equivalent circuit for FHA analysis.

symmetrical. The operation principle of LG mode in backward operation is similar to that in forward operation, which will not repeated here. In LG mode, M_5 and M_6 can always achieve ZCS, and all the other MOSFETs can achieve ZVS.

IV. Performance Analysis

A. Voltage Gain

No matter in forward operation or backward operation, the voltage gain *G* is defined as the ratio of secondary-side voltage referred to the primary side to the input voltage as given in (2), in which *n* is the transformer turns ratio. The fundamental harmonic approximation (FHA) method is used to get the voltage gain expression approximately.

The equivalent circuit based on the FHA method is shown in Fig. 6. $v_{AB1}(t)$ is the fundamental harmonic of $V_{AB}(t)$, R_e is the equivalent ac load which is equal to $8n^2R_o/\pi^2$, R_o is the dc load resistance, $v_{CD1}{}'(t)$ is the fundamental harmonic of the $V_{CD}(t)$ referred to the primary side. Since the switching frequency is equal to the resonant frequency, the amplitude of $v_{AB1}(t)$ is always equal to the amplitude of $v_{CD1}{}'(t)$. So the voltage gain in forward mode and backward mode is same

$$G = \frac{nV_2}{V_1}. \tag{2}$$

1) HG Mode: The expression of V_{AB} in HG mode is shown in (3) according to Figs. 3(a) and 5(a). V_{ABH} is a periodical function which can be expressed as

$$V_{ABH} = \begin{cases} V_1, & (0 \le t \le \alpha T_s) \\ 0.5V_1, & (\alpha T_s \le t < 0.5T_s) \\ -V_1, & (0.5T_s \le t < 0.5T_s + \alpha T) \\ 0.5V_1, & (0.5T_s + \alpha T \le t < T) \end{cases} \tag{3}$$

$$\begin{cases} v_{ABH}(t) = \sum_{n=1}^{\infty} \left[a_n V_1 \cos(2n\pi f_s t) + b_n V_1 \sin(2n\pi f_s t)\right] \\ a_n = \frac{2}{T_s} \int_{-0.5T}^{0.5T} V_{AB}(t) \cos(2n\pi f_s t) dt \\ b_n = \frac{2}{T_s} \int_{-0.5T}^{0.5T} V_{AB}(t) \sin(2n\pi f_s t) dt. \end{cases} \tag{4}$$

Taking (3) into (4), the Fourier decomposition of V_{ABH} is given in (5). $v_{ABH1}(t)$ is the fundamental harmonic of $V_{AB}(t)$, which is given in

$$v_{ABH}(t) = \sum_{n=1,3,5.....}^{\infty} \left(\frac{\sin 2\pi n\alpha}{n\pi} V_1 \sin 2n\pi f_s t + \frac{3-\cos 2\pi n\alpha}{n\pi} V_1 \cos 2n\pi f_s t \right) \tag{5}$$

$$\begin{cases} v_{ABH1}(t) = \dfrac{\sqrt{10-6\cos 2\pi\alpha}}{\pi} V_1 \sin(2\pi f_s t + \theta) \\ \theta = \arctan\left(\dfrac{3-\cos 2\pi\alpha}{\sin 2\pi\alpha}\right). \end{cases} \tag{6}$$

The relationship between $v_{CD1}{}'(t)$ and V_2 is given in (7). Since $v_{CD1}{}'(t)$ is equal to $v_{ABH1}(t)$, taking (6) into (7), the voltage gain can be derived and is given by

$$v'_{CD1}(t) = \frac{4nV_2}{\pi} \sin 2\pi f_s t \tag{7}$$

$$G_H = \frac{nV_2}{V_1} = \frac{\sqrt{10-6\cos 2\pi\alpha}}{4} \tag{8}$$

It is seen from (8) that the voltage gain increases with the increasing of α, and the variation range of α is from 0 to 0.5. When α is 0.5, G_H researches its maximum value 1 and the converter operation is same as a traditional *LLC* converter with input voltage equals to V_1; when α is 0, the voltage gain G_H is 0.5 and the converter operation is same as a traditional *LLC* converter with input voltage equals to $0.5V_1$. The voltage gain range of HG mode is from 1 to 0.5.

2) MG Mode: The voltage gain of MG mode can also be calculated by the FHA method. The dc bias voltage is $0.25V_1$ which is blocked by the resonant capacitor. The actual ac voltage applied to the resonant tank is given in (9). The Fourier decomposition of V_{ABM} is given in (10), and the voltage gain of MG mode is given in (11)

$$V_{ABM}(t) = \begin{cases} 0.75V_1, & (0 \le t \le \beta T_s) \\ 0.25V_1, & (\beta T_s \le t < 0.5T_s) \\ -0.75V_1, & (0.5T_s \le t < 0.5T_s + \beta T_s) \\ -0.25V_1, & (0.5T_s + \beta T_s \le t < T_s) \end{cases} \tag{9}$$

$$v_{ABM}(t) = \sum_{n=1,3,5.....}^{\infty} \left(\frac{\sin 2\pi n\beta}{n\pi} V_1 \sin 2n\pi f_s t + \frac{2-\cos 2\pi n\beta}{n\pi} V_1 \cos 2n\pi f_s t \right) \tag{10}$$

$$G_M = \frac{nV_2}{V_1} = \frac{\sqrt{5-4\cos 2\pi\beta}}{4}. \tag{11}$$

The voltage gain of MG mode will also increase with the increase of β. The variation range of β is also from 0 to 0.5, so the voltage gain range of MG mode is from 0.25 to 0.75.

3) LG Mode: In LG mode, γ is used to regulate the output voltage. The expression of V_{AB} is given in (12). No matter in forward operation or backward operation, the voltage gain equation is same which is given in (13). The range of γ is from 0 to 0.5, so the voltage gain range is from 0 to 0.5

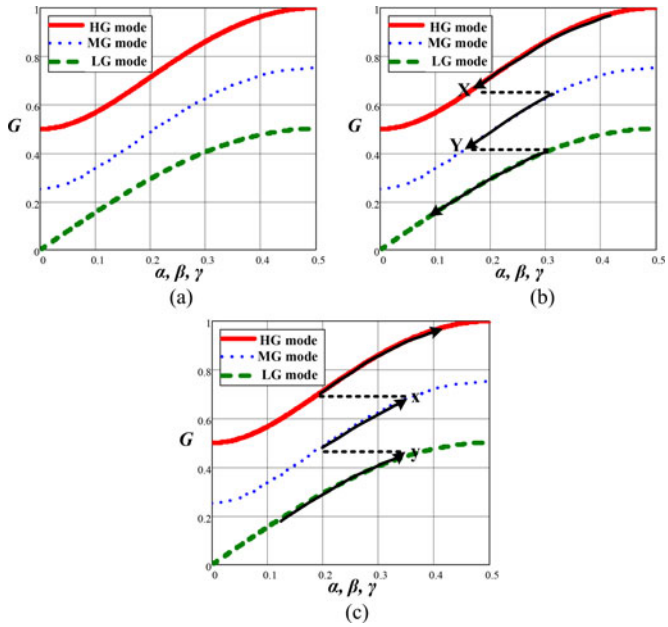

Fig. 7. (a) Voltage gain of HG, MG, and LG mode. (b) Switching process when the voltage gain decreases. (c) Switching process when the voltage gain increases.

$$V_{ABL}(t) = \begin{cases} 0.5V_1, & (0 \le t \le \gamma T_s) \\ 0, & (\gamma T_s \le t < 0.5T_s) \\ -0.5V_1, & (0.5T_s \le t < 0.5T_s + \gamma T_s) \\ 0, & (0.5T_s + \gamma T_s \le t < T_s) \end{cases} \tag{12}$$

$$G_L = \frac{nV_2}{V_1} = \frac{\sqrt{2-2\cos 2\pi\gamma}}{4}. \tag{13}$$

From (8), (11), and (13), the voltage gain is only related to the control variables α, β, and γ, which is not affected by the load condition. The voltage gain curves of HG mode, MG mode, and LG mode are plotted in Fig. 7. It is seen that the voltage gain of HG mode and MG mode are overlapped from 0.75 to 0.5, and the voltage gain of MG mode and LG mode are overlapped from 0.5 to 0.25.

By switching the converter between different operation modes, the total voltage gain range will be very wide, and the voltage gain range in forward operation and backward operation is the same.

It should be noted that the voltage gain given in (8), (11), and (13) are derived based on the FHA method, and it is not very accurate when the converter is in DCM operation like that for a conventional *LLC* converter. Though the switching frequency of the proposed converter always equals to the resonant frequency, the converter can also be in DCM operation as described above, which means the actual voltage gain is still slightly affected by the control variables (α, β, and γ) and load condition.

B. Soft Switching

1) Forward Mode: Since the switching frequency is always equal to the resonant frequency, ZCS can always be achieved

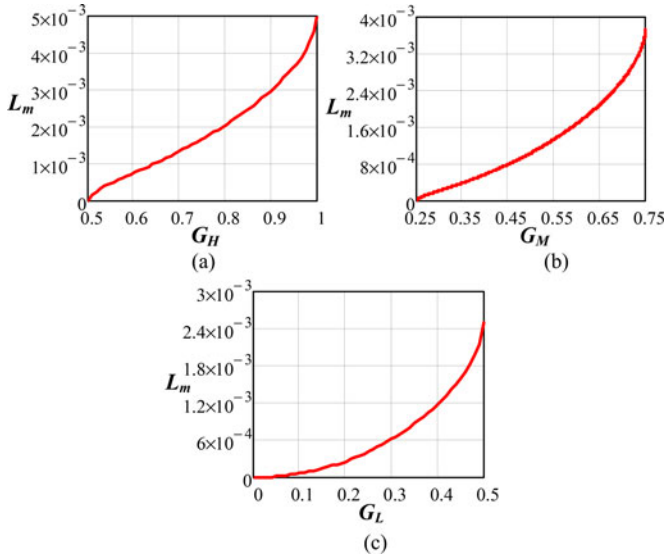

Fig. 8. Maximum inductance of L_m to achieve ZVS versus voltage gain: (a) HG mode, (b) MG mode, (c) LG mode.

for the secondary-side devices. For the primary-side switches, there are two switching point in a half-switching cycle: t_1 and t_3, as shown in Fig. 3. Magnetizing inductor L_m and resonant capacitor C_r will affect the soft-switching condition at these two points.

a) Switching Point t_1: Switching current at t_1 is equal to the resonant current i_r, and the requirement for ZVS is shown in (14), in which $t_{\rm dead}$ is the dead time between the two switching signals. With a given dead time, the soft switching is easy to achieve when the resonant current is large. Since the resonant current i_r is proportional to the load current, it will reach its minimum value at no-load condition. In this condition, i_r is equal to i_{Lm}, so the switching current at t_1 is also equal to i_{Lm}. The expression of i_{Lm} at t_1 at no-load condition is given in (15), and the coefficient (α, β, γ) in the right side of the equation is α for HG mode, β for MG mode, and γ for LG mode

$$i_r(t_1)t_{\rm dead} \geq V_1 C_{\rm oss} \tag{14}$$

$$i_{Lm}(t_1) = (\alpha,\beta,\gamma)\cdot\frac{nV_2}{2L_m f_s}. \tag{15}$$

In order to achieve ZVS in any load condition, the desired magnetizing inductance L_m for the three modes can be derived based on (14) and (15), which is given as

$$L_m \leq \min(\alpha G_H, \beta G_M, \gamma G_L)\cdot\frac{t_{\rm dead}}{2f_s C_{\rm oss}}. \tag{16}$$

Assuming $f_s = 100$ kHz, $C_{\rm oss} = 80$ pF, $t_{\rm dead} = 300$ ns, and $n = 4$, the desired L_m from (16) is shown in Fig. 8. The lower the voltage gain is, the smaller L_m should be to achieve ZVS. For example, when the voltage gain is near 0.5 in HG mode, ZVS cannot be achieved no matter how small L_m is. By switching the converter from HG mode to MG mode when the voltage gain gets lower, the ZVS can still be achieved with a reasonable L_m. When the voltage gain is near 0.25 in MG mode, ZVS will lost too, the converter can be switched from MG mode to LG mode before the voltage gain is too low.

Since γG_L is usually smaller than βG_M and αG_H, therefore if ZVS is achieved in LG mode, it will always be achieved in all the operation modes.

b) Switching Point t_3: The converter is in DCM operation during t_2 to t_3, and the secondary side is separated from the primary side. However, D_2 and Q_3 will conduct and the next half resonant period will begin if the amplitude of v_{Cr} is higher than nV_2, then ZVS cannot be achieved and the converter will operate under capacitive mode. The amplitude of v_{Cr} is related to the load condition; the heavier the load is, the larger the amplitude of v_{Cr} will be. In LG mode, it is the worst case to achieve ZVS at t_3 because there is no input voltage applied to the resonant tank in DCM operation. In order to avoid capacitive switching at heavy load in LG mode, (17) should be satisfied. The approximate value of $V_{Cr\max}$ can be solved according to the equivalent circuit shown in Fig. 6, and the required resonant capacitance of C_r is given in (18)

$$V_{Cr\max} \leq nV_2 \tag{17}$$

$$C_r \geq \frac{\sqrt{\omega^2 L_m^2 + R_e^2}}{\omega^2 L_m R_e}. \tag{18}$$

Besides, another soft-switching condition of LG mode at t_3 is given in (19). The worst case for soft switching occurs at no-load condition because the resonant current i_r reaches its minimum value. For simplicity, the resonant current i_r is assumed to be constant during DCM period at no-load condition, so i_r at t_3 is equal to that at t_2, and the soft-switching condition at t_3 is given in (20)

$$i_r(t_3)t_{\rm dead} \geq 3V_1 C_{\rm oss} \tag{19}$$

$$L_m \leq \frac{\gamma G_L t_{\rm dead}}{6f_s C_{\rm oss}}. \tag{20}$$

2) Backward Operation: In backward operation, Q_1–Q_4 are switched with 50% duty cycle. The soft-switching condition for Q_1–Q_4 is shown in (21), in which $i_s(t_3)$ is the switching current of Q_1–Q_4 at t_3, and $n^2 C_{\rm oss}$ is the parasitic capacitance of switches referred to the transformer secondary side. The secondary-side current $i_s(t_3)$ is equal to $n * i_{Lm}$ at t_3, and the approximate value of i_{Lm} at t_3 is given in (22). Taking (22) into (21), the requirement for L_m to achieve ZVS is given in (23)

$$i_s(t_3)t_{\rm dead} \geq 2n^2 V_2 C_{\rm oss} \tag{21}$$

$$i_{Lm}(t_3) = (\alpha,\beta,\gamma)\cdot\frac{nV_2}{4L_m f_s} \tag{22}$$

$$L_m \leq \min(\alpha,\beta,\gamma)\cdot\frac{t_{\rm dead}}{8f_s C_{\rm oss}}. \tag{23}$$

Based on the analysis given above, we can design the magnetizing inductance and resonant capacitance to achieve soft switching in any operation mode.

C. Mode Switching

In order to achieve ZVS and optimize the operation of the converter during different voltage gain condition, the operation of the converter can be switched between these three modes, and the voltage gain should have overlap for different operation

modes in order to keep the same output. For HG mode and MG mode, the converter can be switched when the voltage gain is between 0.5 and 0.75. For MG mode and LG mode, it can be switched when the voltage gain is between 0.25 and 0.5. It is known that the RMS current in MG mode is smaller than that in HG mode with same voltage gain and load condition, so the conduction loss in HG mode is higher than that in MG mode. Also, the control variables should not be too small in order to achieve ZVS. In order to optimize the efficiency, when HG mode and MG mode can achieve the same voltage gain, MG mode is preferred; when MG mode and LG mode can achieve the same voltage gain, LG mode is preferred. The voltage gain of switching point should be as high as possible, so RMS current will be smaller and ZVS is easier to be achieved.

The control method of different operation modes and the operation modes switching method can be easily implemented by digital control circuit, such as DSP from TI. Taking forward operation as an example, the DSP samples V_2 by its A/D input port and then compares it with the reference voltage $V_{\rm ref}$, after a PI regulator, the error result $V_{\rm err}$ is send to the phase shift register or the duty cycle register of EPWM module. According to the error signal $V_{\rm err}$, the output of phase shift register or duty cycle register varies to change the duty cycle and phase shift angle, which is used to regulate the output voltage. The input voltage V_1 should also be sampled to calculate the actual voltage gain and decide when to switch the operation mode. When the input voltage increases, the voltage gain will decrease. If the voltage gain reaches the mode switching point, control method will be changed and the operation mode is switched, and it is similar when the input voltage decreases. Hysteretic control is adopted to ensure the stability during mode switching. The mode switching process is shown as dash line in Fig. 7(b) and (c). The feedback loop should regulate the phase shift angle to ensure the same voltage gain after mode transition.

V. Experimental Results

A prototype of TL *LLC* converter is built to verify the theoretical analysis. The specifications of the prototype are listed as follows:

1) battery voltage: $V_2 = 30$–60 V;
2) primary side voltage: $V_1 = 240$–480 V;
3) maximum output current in forward operation: $I_o = 20$ A;
4) maximum output current in backward operation: $I_d = 2.5$ A;
5) resonant frequency: $f_r = 100$ kHz.

The 100 kHz resonant is just a reasonable value for dc/dc converter, which is not specially designed. For the proposed converter, switching frequency is same as the resonant frequency. With 100-kHz switching frequency, it is easy to select power devices, magnetic components, and design digital control circuit. IPP65 R110 CFD and IPP200 N15 from INFINEON are used as the primary MOSFETs and secondary MOSFETs, respectively. A brief parameters design description is given below.

1) *Transformer turns ratio:* The minimum primary-side voltage is 240 V, and the maximum secondary-side voltage is 60 V, since the maximum voltage gain of the converter is 1, *n* is set to 4.

TABLE II
Key Parameters of the Prototype

Parameters	Value	Size/Type	Vendor
Resonant capacitor (C_r)	100 nF	MKP4 J023303 C	Vishay
Transformer	$n = 4$	EE42/21/15	TDK
	$L_m = 200\ \mu$H	PC40	
	$n_1 = 32$ turns		
	$n_2 = 8$ turns		
Resonant inductor (L_r)	25.3 μH	PQ32/20	TDK
		PC40	
MOSFETs (Q_1–Q_4)		IPP200 N15 N3 G	Infineon
		TO-220	
MOSFET (M1–M8)		IPP65 R110 CFD	Infineon
		TO-220	
DSP		TMS320 F28335	TI

2) *Mode switching point:* As discussed above, the voltage gain of mode switching point should be as high as possible to optimize the converter operation. In the prototype, the voltage gain for HG and MG mode switching is set to 0.7 with a small hysteresis; and the voltage gain for MG and LG mode switching is set to 0.45 with a small hysteresis. In backward operation and forward operation, the voltage gain for mode switching is the same.
3) *Resonant capacitor C_r:* Considering the soft-switching condition derived for HG mode, MG mode, and LG mode, the minimum capacitance of C_r is given in (18). With the specifications given above, C_r should be larger than 81 nF. In the prototype, C_r is 100 nF considering reasonable margin. So the resonant inductance L_r is 25.3 μH to get the required resonant frequency.
4) *Magnetizing inductor L_m:* The L_m can be designed based on (16), (20), and (23). With the parameters given above, L_m should below 260 μH. In the prototype, L_m is set to 200 μH.

A DSP TMS320 F28335 from TI is adopted as the digital control unit. The output voltage V_2 and the input voltage V_1 are sampled by the A/D input port of the DSP. The conventional digital PI algorithm is adopted to regulate the output voltage, and the gate drive signals are generated by the EPWM module of DSP.

Figs. 9–11 show the waveforms of HG mode in forward operation with $V_2 = 60$ V and $V_1 = 250$, 300, and 400 V, respectively, at $P_o = 1000$ W. It is seen in Figs. 9(a)–11(a) that ZVS is achieved for M_4 and M_6 no matter what the voltage gain is. As shown in Fig. 9(b), V_{AB} is almost a square waveform when α is near 0.5, and when α decreases in Figs. 10(b) and 11(b), the voltage gain decreases correspondingly. The rectifier diodes turn OFF with ZCS as shown in Figs. 9(c)–11(c).

Fig. 12 shows the waveforms of HG mode in forward operation with $V_2 = 60$ V and $V_1 = 300$ V at 10% load, and ZVS and ZCS can also be achieved. The oscillation on the resonant current and secondary-side voltage is caused by the parasitic capacitors of MOSFETs and the resonant inductor due to DCM operation.

Figs. 13 and 14 show the waveforms of MG mode, when $V_1 = 400$ V, and $V_2 = 60$ and 40 V, respectively. Though V_{AB}

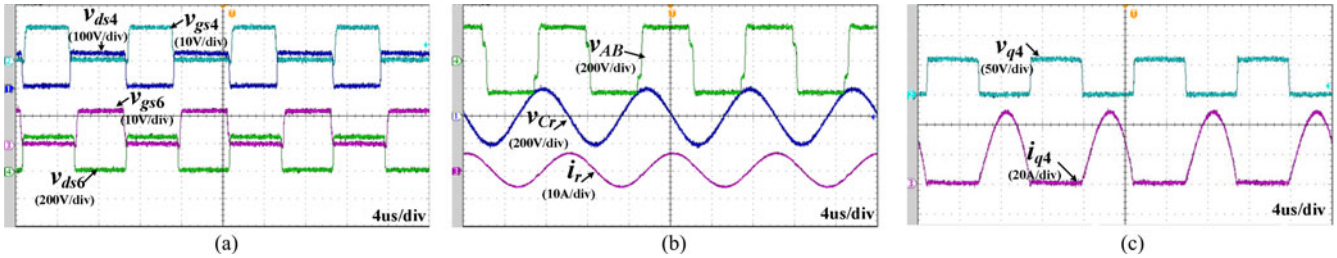

Fig. 9. Waveforms of HG mode when $V_2 = 60$ V and $V_1 = 250$ V at full load in forward operation.

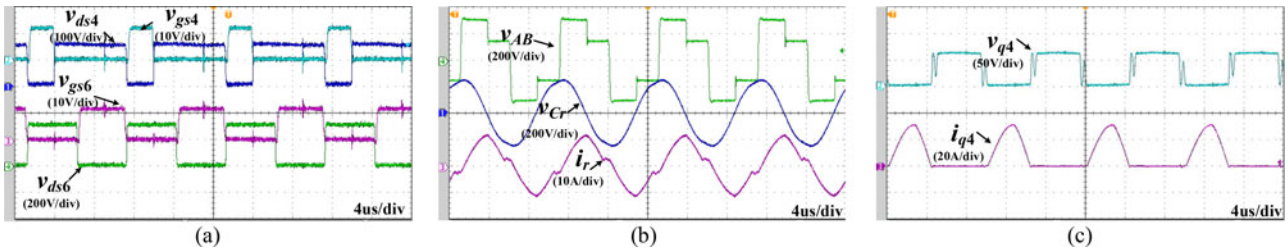

Fig. 10. Waveforms of HG mode when $V_2 = 60$ V and $V_1 = 300$ V at full load in forward operation.

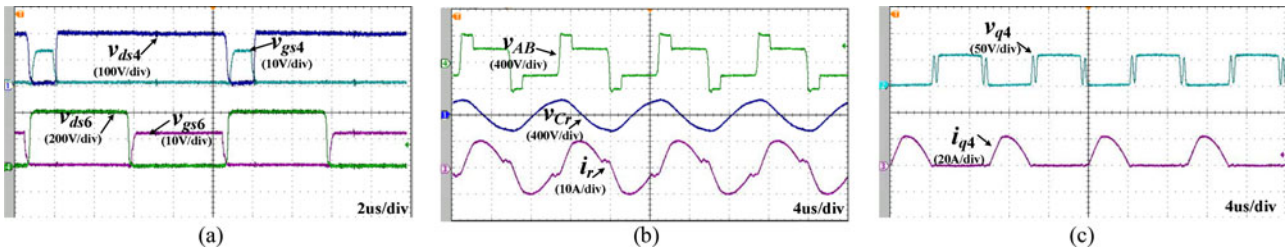

Fig. 11. Waveforms of HG mode when $V_2 = 60$ V and $V_1 = 400$ V at full load in forward operation.

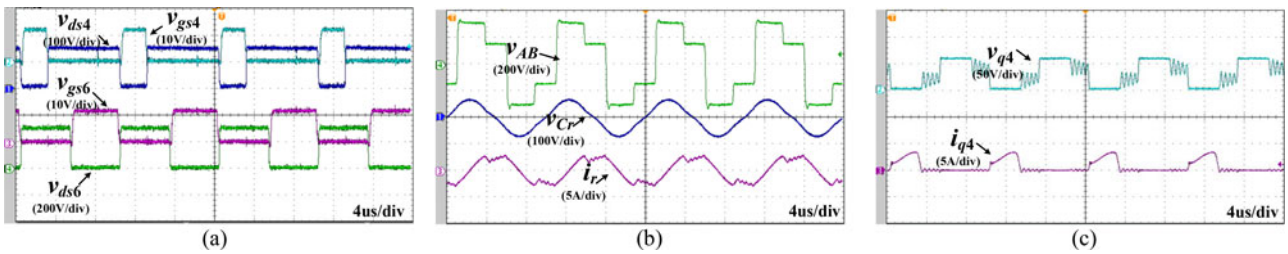

Fig. 12. Waveforms of HG mode when $V_2 = 60$ V and $V_1 = 300$ V at light load in forward operation.

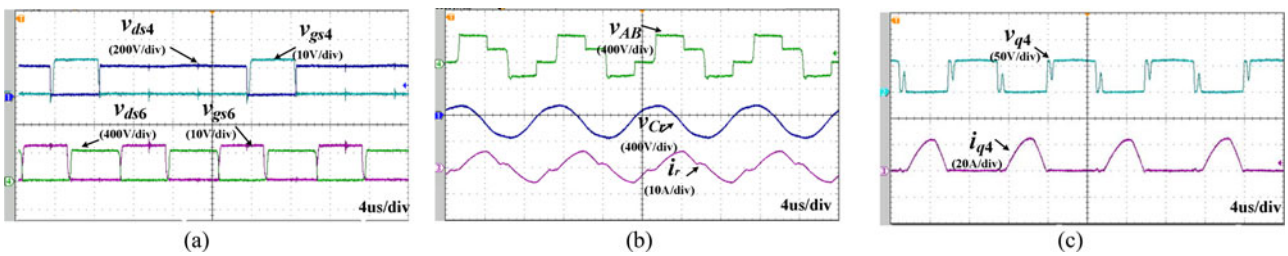

Fig. 13. Waveforms of MG mode when $V_2 = 60$ V and $V_1 = 400$ V at full load in forward operation.

is asymmetrical as shown in Figs. 13(b) and 14(b), energy of capacitors can be balanced. ZVS and ZCS can also be achieved.

Fig. 15 shows the waveforms of LG mode when $V_2 = 30$ V and $V_1 = 400$ V. Since the inductance of L_m is small enough and the capacitance of C_r is large enough, ZVS can also be achieved in LG mode.

Waveforms in backward operation are shown in Figs. 16 and 17, it is seen that ZVS and ZCS are always achieved. Though v_{AB} is asymmetrical in MG mode as shown in Fig. 17, the

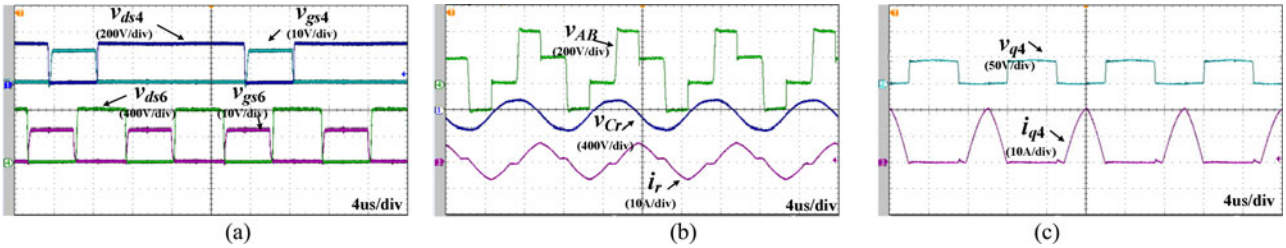

Fig. 14. Waveforms of MG mode when $V_2 = 40$ V and $V_1 = 400$ V at full load in forward operation.

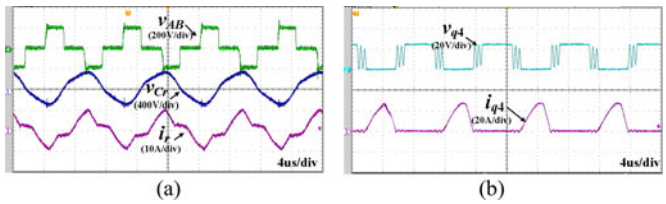

Fig. 15. Waveforms of LG mode when $V_2 = 25$ V and $V_1 = 400$ V in forward operation.

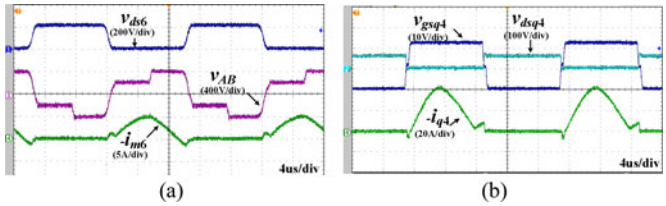

Fig. 16. Waveforms of HG mode when $V_2 = 60$ V and $V_1 = 400$ V at full load in backward operation.

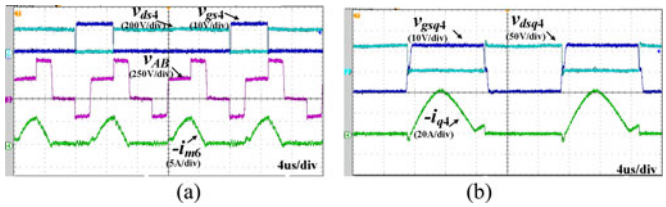

Fig. 17. Waveforms of MG mode when $V_2 = 60$ V and $V_1 = 400$ V at full load in backward operation.

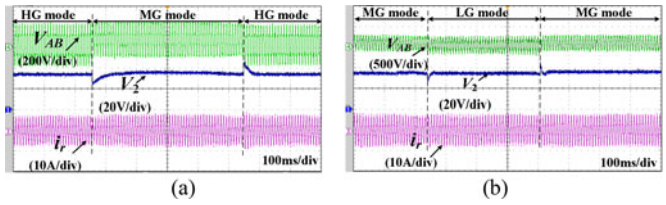

Fig. 18. Dynamic process of operation mode transition.

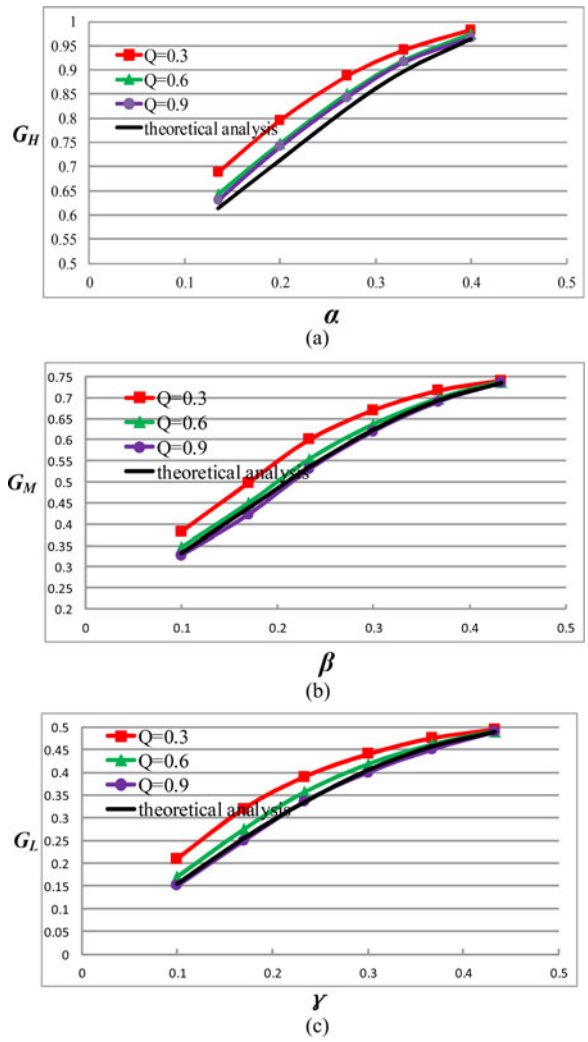

Fig. 19. Measured voltage gain versus control variables: (a) HG mode, (b) MG mode, (c) LG mode.

energy of the capacitor are also well balanced in one equivalent switching cycle.

Fig. 18(a) shows the dynamic transition of mode switching between HG mode and MG mode, the input voltage keeps increasing at first and the converter switches from HG mode to MG mode when the detected voltage gain is beyond the range of HG mode. It is seen that there is a small voltage dip in the output voltage during mode switching and the output voltage will recovery to its steady-state value quickly. When the input voltage decreases and the detected voltage gain is beyond the range of MG mode, the converter is switched from MG mode to HG mode to keep the output voltage constant. There is a small voltage overshoot in the output voltage.

The mode switching between MG mode and LG mode is similar, which is shown in Fig. 18(b). It verifies that the converter can switch between different operating modes smoothly without

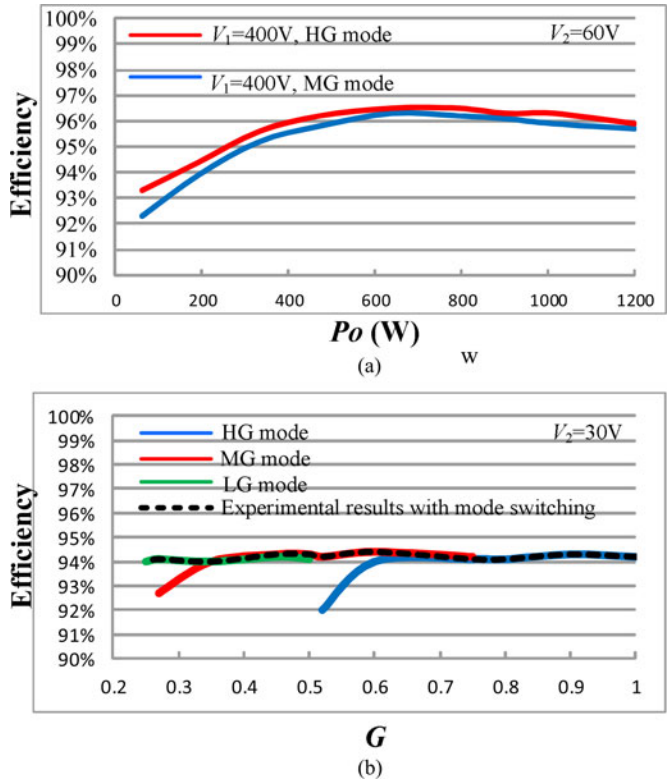

Fig. 20. Efficiency of the prototype: (a) Efficiency versus P_o at HG mode and MG mode. (b) Efficiency versus voltage gain at $V_2 = 30$ V.

any obvious oscillation and the voltage gain can be regulated continuously.

The measured voltage gain of HG mode, MG mode, and LG mode are shown in Fig. 19, the theoretical one is also given for comparison. Based on the theoretical analysis, the voltage gain does not change with the load condition. However, the measured voltage gain is slightly affected by the load resistance. The difference is caused by the FHA analysis method, which is similar to the gain curved deviation of conventional *LLC* converter when the load current is discontinuous.

The measured efficiency of the prototype is shown in Fig. 20. It is seen from Fig. 20(a), the maximum efficiency is about 96.5%. The main power loss is the conduction loss of diodes in the secondary side, and the conduction loss of the primary side MOSFETS with relative high on-state resistance ($0.12\ \Omega$). A further efficiency improvement is still possible with smaller resistance MOSFETs. Efficiency of MG mode is a little higher than HG mode with same voltage gain, since the switching frequency of M_1–M_4 is half the resonant frequency and the switching loss is lower.

From Fig. 20, it is seen that the efficiency when $V_2 = 30$ V is lower than $V_2 = 60$ V because higher output current causes higher conduction loss. It is seen from Fig. 20(b) that the efficiency of each mode will decrease when the voltage gain gets lower, since ZVS will be lost when the voltage gain is too low. However, efficiency of the converter is almost not affected by the variation of input voltage due to the mode change.

VI. Conclusion

This paper proposes a bidirectional TL *LLC* resonant converter with a new PWAM control strategies. The switching frequency is fixed to the resonant frequency and the equivalent amplitude of the voltage is regulated to control the output. With different control schemes, a very wide voltage gain range can be achieved, which overcomes the narrow voltage gain limitation of a conventional *LLC* resonant converter. Bidirectional operation can also be achieved with the proposed control method, and the operation principle in forward mode and backward mode is symmetrical. Finally, a 1-kW prototype is built and verifies the theoretical analysis.

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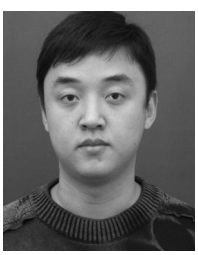

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