Interleaved Dual Buck Full-Bridge Three-Level Inverter

Feng Hong, *Member, IEEE*, Jun Liu, Baojian Ji, Yufei Zhou, *Member, IEEE*, Jianhua Wang, *Member, IEEE*, and Chenghua Wang

***Abstract*—A novel interleaved dual buck full-bridge three-level inverter (IDBFTI) is proposed for the grid-connected system in this paper. It retains the advantages of interleaved parallel technology for inverter as follows: reducing the output ripple current and the total harmonic distortion of the output current, increasing the power density of system, and reducing the current stress and thermal stress of power devices. Besides, it can solve the problem of zero sequence circulation current (ZSCC) in interleaved inverter system by the circuit structure, and it also has the advantages of no shoot-through problem, no reverse recovery of the body diode, and three-level output. The interleaved inverter circuits share two power-frequency switches, which are resized for each specific application, and it is easier to extend the system by improving current capability of the two switches. The working principle of this system is introduced in detail, and a 2-kW experimental prototype has been established and tested. Test results verify the principle and the excellent performance of IDBFTI.**

***Index Terms*—High conversion efficiency, interleaving, low ripple current, three-level inverter, zero sequence circulation current (ZSCC).**

I. Introduction

NEW energy power generation, smart grid, and active power filter put forward higher demand on power quality and power level of grid-connected inverters. Usually, the bridge topology is adopted in traditional inverters with a single output filter inductor L. In this way, with the increase of system power levels, the system switching frequency, which is restricted by the switching loss of power devices, must be reduced. In addition, high-power inverter fails to avoid using large filter inductors, which can reduce the dynamic response of the system and increase the losses. Therefore, how to balance the power level, conversion efficiency, reliability, and ripple is still an important issue we have to concern [1]. High-order filter like *LCL* filter is normally used as a standard interface to the grid to provide the proper attenuation of harmonics around switching frequency. The filter has the advantage of remaining the same performance when the inductance value is much smaller than the single filter inductor L, but as a third-order system, it induces output oscillation easily and therefore reduces system stability. As a result, the resonance of *LCL* filter limits the improvement of both steady state and dynamic performance of grid-connected inverter. Besides, the use of capacitor decreases the power factor of system and increases the THD of output current [2]. Another solution is the technology of parallel inverter, which has the advantages of higher system redundancy [3], higher fault tolerance and reliability [4], and the ability of sharing the power. However, the parallel inverters also need to use large filter inductors, which will cause large losses and cannot meet the requirements of low output ripple current either.

The technology of interleaved parallel inverter is one of the major ways to solve the above problems. The multiply interleaved technology can increase the equivalent switching frequency and decrease switching frequency of each parallel inverter. Besides, the voltage stress of power devices, the switching loss, and the conduction loss can also be reduced. As the power of single inductor reduces by N^2, where N is the number of parallel inverters, the volume and weight of system can be reduced and its dynamic property is improved [5].

In recent years, there are a lot of research works and applications about interleaved parallel inverter. For example, the interleaved half-bridge inverter was used for grid-connected power generation with inductor filter [6]. By interleaved switches, soft-switching was realized and losses of body diode reverse recovery were eliminated [7]. Interleaved modulation strategy was then used in cascade multilevel inverter, which decreases the output ripple and filter [8]. The interleaved control strategy was used in buck/boost converter with double tube, which reduces the magnetic components [9]. In order to further reduce the current ripple, or achieve the goal of optimizing the magnetic parts, the magnetic integration technology and matrix transformation technology of interleaved inverter were studied in [3], [10], and [11]–[13]. Modulation strategies of interleaved inverters [14] include: phase shift, phase disposition (PD) [15], phase opposite disposition, and alternate phase opposite disposition. In view of the nonlinear link for the digital control, a new control method was proposed in [16]. In [17] and [18], the three-route interleaved fixed-frequency quasi-sliding mode control method was proposed for the inverter parallel system to realize zero output ripple (called zero average dynamics in the paper) and three-phase decoupling control. In [19], the method of optimized

Manuscript received September 4, 2014; revised January 29, 2015 and November 20, 2014; accepted March 29, 2015. Date of publication April 9, 2015; date of current version September 29, 2015. This work was supported in part by the National Natural Science Foundation of China (51407089). Recommended for publication by Associate Editor J. Espinoza.

F. Hong, J. Liu, Y. Zhou, and C. Wang are with the Key Laboratory of Radar Imaging and Microwave Photonics, Nanjing University of Aeronautics and Astronautics, Ministry of Education, Nanjing 210000, China (e-mail: hongfeng@nuaa.edu.cn; 704460806@qq.com; zhou_yufei@126.com; chwang@nuaa.edu.cn).

B. Ji is with the School of Automation and Electrical Engineering, Nanjing University of Technology, Nanjing 210000, China (e-mail: ji_baojian@126.com).

J. Wang is with the Jiangsu Provincial Key Laboratory of Smart Grid Technology and Equipment, School of Electrical Engineering, Southeast University, Nanjing 210098, China (e-mail: wangjianhua@seu.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2421295

space vector modulation for interleaved parallel inverter was proposed to minimize ripple current. The disturbance processing method of interleaved inverter with coupled inductor based on a discrete-time decoupling network was proposed in [20]. The repetitive control was used for interleaved parallel inverters in [21].

Yet, there still exists some issues about the inverter interleaved parallel technology to be discussed. Pan and Liao [22] demonstrated that there was a flow path for ZSCC in the parallel inverter system. In some interleaved inverter systems with inductive magnetic coupling, the current of each leg are coupled, and the systems are actually complex multiinput and multioutput systems [23], so the problem of ZSCC becomes more complex. Therefore, Diaz Contreras and Cabaleiro Cortizo [11] proposed and analyzed a decoupled-control method for the interleaved inverter with coupled inductor, but the circulation current was not discussed. Shin *et al*. [12], [13] indicated that: first to eliminate circulation current, some studies used the isolation transformer [24], which increased system size and cost; second, circulation cannot be restrained by isolated method in interleaved system; the complexity of magnetics and control increased in some other studies using interphase reactor, intercell transformer, and common mode coke. From [12] and [13], the inductive coupling method used in 1.5-MW wind power interleaved inverter can restrain the ZSCC, but it is just for the system with 2^N parallel inverters. The circulation current means that there is reverse inductive current in some route. In [25]–[27], the reverse inductive current is used to realize soft-switching, but also increases conduction loss. The authors in [25] and [26] used the method of hysteresis current control to realize soft-switching and limit the reverse inductor current, but the switching frequency was not fixed. Lai *et al*. [27] used phase-shifting angle modulation control, but the experimental verification has not been fully completed.

Existing studies are mostly on bridge-type circuit in parallel, which has the problem of shoot-through phenomenon and also affects the reliability. With the increased number of parallel inverters, the increased number of shoot-through modes, and the more complex control system, the dead-time effect becomes more serious. The NPC inverter with three-phase coupled inductor studied in [28]–[31] has no shoot-through problem, and its output ripple is small because of the interleaved switches of each phase, but the inverter must operate in the mode with dc bias current.

For the above problems, the author in [32] invented the interleaved dual buck full-bridge three-level inverter (IDBFTI). In addition to the common advantages of interleaved inverter, the IDBFTI has the characteristics of no shoot-through problem, three-level output, and no reverse recovery of the body diode. It can cut off the path of ZSCC and eliminate the circulation current between different bridge legs naturally; each bridge leg works independently and do not need the dc bias current. Fixed-frequency sinusoidal pulse width modulation (SPWM) modulation method is used in the inverter. This paper will introduce the inverter in detail.

In Section II, the basic topology of the IDBFTI is presented, and the path of ZSCC of traditional interleaved inverter is analyzed. Comparing IDBFTI with traditional interleaved inverter, it is pointed out that this topology eliminates the circulation path by the circuitstructure. Section III introduces the parameters designing, the analysis of ripple and the control method. In Section IV, theory and simulations are verified with the experiences on a 2-kW IDBFTI prototype.

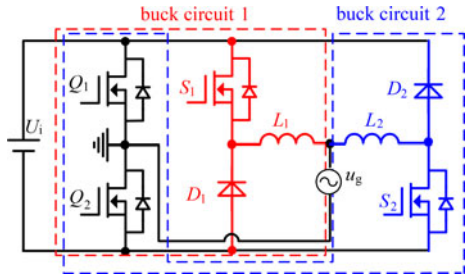


Fig. 1. Dual buck full-bridge three-level inverter.

II. Basic Topology and Analysis of Circulation Current

A. Basic Topology

Fig. 1 shows the topology of DBFTI. The specific system operation is described as follows: The driving signals of power switches Q_1 and Q_2 are produced by the overzero comparing circuit based on the grid voltage. When the grid voltage is greater than zero, Q_2 is turned ON and Q_1 is turned OFF, when it is less than zero, Q_2 is turned OFF and Q_1 is turned ON. The inverter works in half-cycle mode. It means that the buck circuit 1 consisting of power switches S_1, Q_1, Q_2, freewheeling diode D_1, filter inductor L_1, and filter capacitor C_f starts to work when the output current i_o is in the positive half-cycle. While in the negative half cycle, the buck circuit 2 composed of power switches S_2, Q_1, Q_2, freewheeling diode D_2, filter inductor L_2, and filter capacitor C_f works.

The proposed IDBFTI is constructed on the basis of the circuit in Fig. 1 by adopting interleaved parallel technology. The inverter adopts the unipolar frequency doubling SPWM for dual buck circuit to guarantee the waveform of output current, and PI controller is used as the closed-loop control strategy. As shown in Fig. 2, the part 1 is the first inverter circuit I, the part 2 as the second inverter circuit II. The duty cycle of switches S_a and S_b are the same with that of corresponding switches S_1 and S_2 in one switching cycle, but the driving signals of S_a and S_b have half-switching cycle lag, so the ripple frequency of total current is doubled and the total output ripple current is reduced. In addition, the two circuits share two power frequency switches Q_1 and Q_2, which can be resized for each specific application, and it is easy to extend the system by improving current capability of the two switches. The decrease of the current through switches S_1, S_2, S_a, S_b, reduces the conduction loss of the switches and further increases the power levels of the inverter.

B. Analysis of Working Condition of IDBFTI

Key waveforms of IDBFTI are shown in Fig. 3.

1) Stage $t_0 \sim t_1$: During this stage, the grid voltage and grid current are both greater than zero, and Q_2 is turned ON, Q_1 is turned OFF, inductive current $i_{L2} = i_{\mathrm{Lb}} = 0$, $i_{c1} = i_{L1}, i_{c2} =$

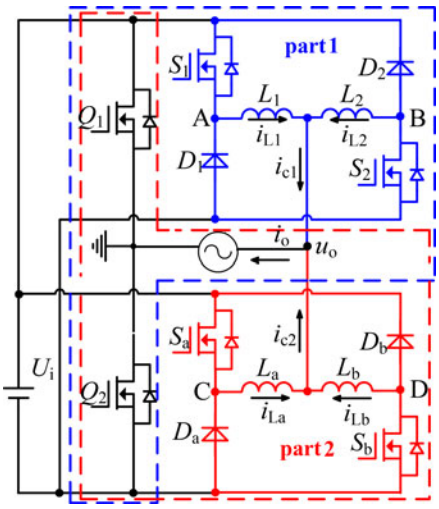


Fig. 2. Interleaved dual-buck full-bridge three-level inverter.

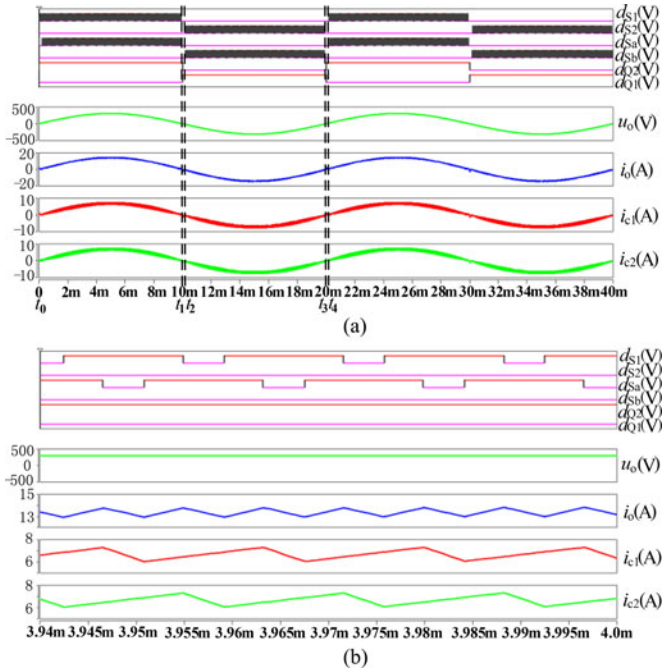


Fig. 3. Key waveforms of IDBFTI at full load.

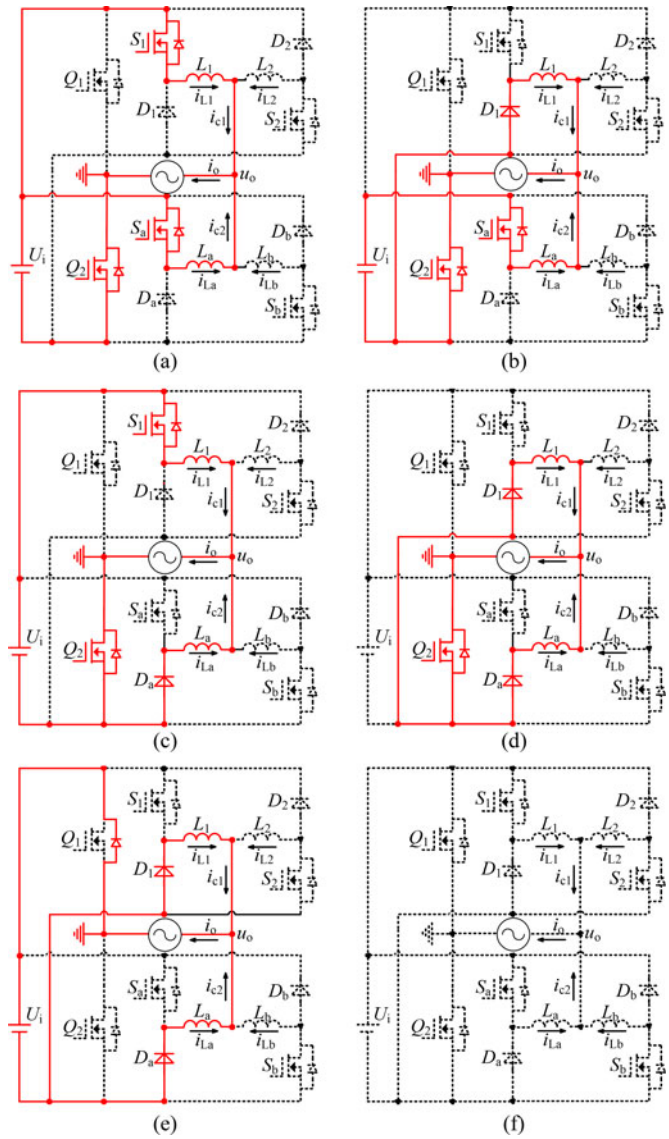


Fig. 4. Operating modes of IDBFTI in positive half-cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

i_{La}, $i_o = i_{c1} + i_{c2}$.The circuit contains four working modes as follows:

Mode 1: As shown in Fig. 4(a), power switches S_1, S_a and Q_2 are turned ON and S_2, S_b and Q_1 are turned OFF, so current i_{L1}, i_{La} rises linearly.

Mode 2: As shown in Fig. 4(b), power switches S_a, Q_2 are turned ON and S_1 is turned OFF. Current i_{L1} flows through D_1 and decreases linearly. Current i_{La} rises linearly.

Mode 3: As shown in Fig. 4(c), power switches S_1, Q_2 are turned ON and S_a is turned OFF. Current i_{La} flows through D_a and decreases linearly. Current i_{L1} rises linearly.

Mode 4: As shown in Fig. 4(d), power switches Q_2 is turned ON and S_1 and S_a are turned OFF. Current i_{L1} flows through D_1 and decreases linearly. Current i_{La} flows through D_a and decreases linearly.

2) Stage $t_1 \sim t_2$: This stage is the dead time between the drive signals of switches Q_1 and Q_2. The dead time is set to avoid shoot-through problem of switches Q_1 and Q_2. The switches are just turned ON and OFF once in a power frequency cycle, so the influence of dead time can be ignored. The shoot-through problem of low frequency legs has only a small impact on the output current. During this stage, Q_2 is turned OFF and Q_1 is not already turned ON. At the time t_1, the inductive current $i_{L1}$and i_{La} are also greater than zero. The circuit contains two working modes as follows:

Mode 5: As shown in Fig. 4(e), power switches S_1, S_a, Q_2, S_2, S_b, Q_1 are turned OFF. $u_0 > 0$, $i_{L1} > 0$, $i_{\mathrm{La}} > 0$. Current i_{L1} flows through D_1 and decreases linearly. Current i_{La} flows through D_a and decreases linearly. Output current i_o flows through the body diode of Q_1 and decreases.

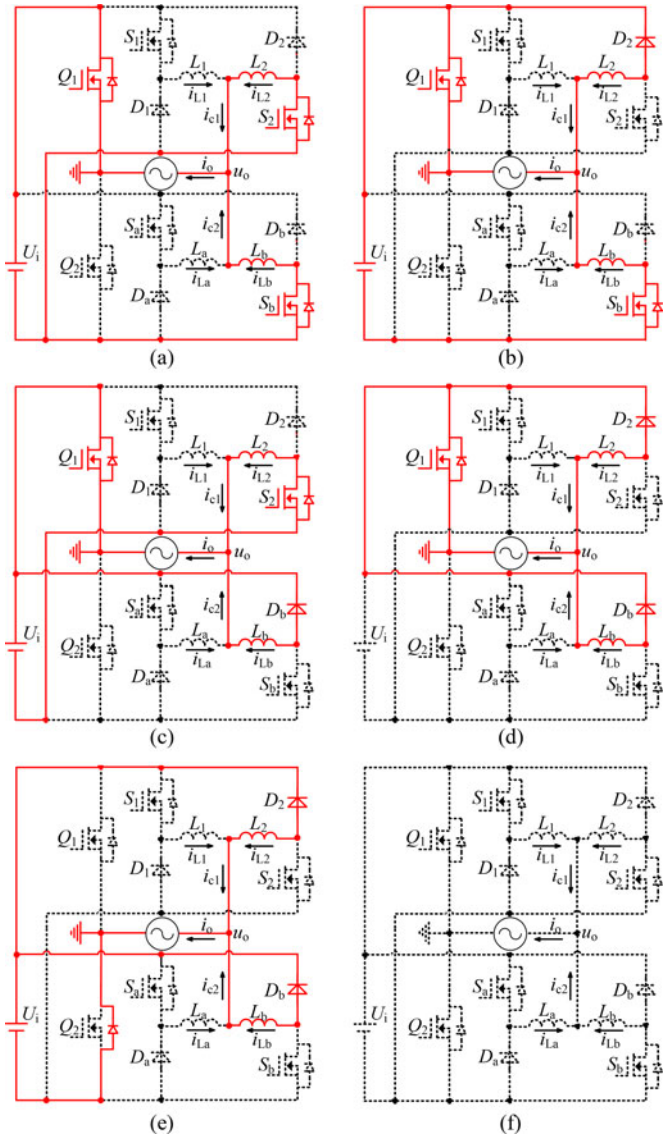


Fig. 5. Operating modes of IDBFTI in negative half-cycle. (a) Mode 7. (b) Mode 8. (c) Mode 9. (d) Mode 10. (e) Mode 11. (f) Mode 12.

Mode 6: As shown in Fig. 4(f), power switches S_1, S_a, Q_2, S_2, S_b, Q_1 are turned OFF. $u_o > 0$. Currents i_{L1} and i_{La} fall down to zero. The inverter does not operate during this time.

During the stage $t_2 \sim t_4$, the grid voltage is in the negative half-cycle. The switch Q_1 is turned ON and Q_2 is turned OFF, and the working process of inverter is symmetrical with the process in the positive half-cycle, which is shown in Fig. 5.

Pan and Liao [22] demonstrate that there is a flow path for zero sequence circulation current (ZSCC) in the inverter parallel system. Here, the interleaved half-bridge inverter is taken for example to analyze the path of circulation current. As shown in Fig. 6, when the interleaved parallel strategy is used, switch S_1 of half-bridge inverter A and the switch S_4 of half-bridge inverter B can conduct during the interval $[t_0, t_1]$ in Fig. 7. When working in discontinuous current mode, the inverter will generate circulation current $i_{\mathrm{bias}}(i_{\mathrm{bias}} = i_{L2})$, which flows through two half-bridge inverters, and the current i_{L2} of half-bridge

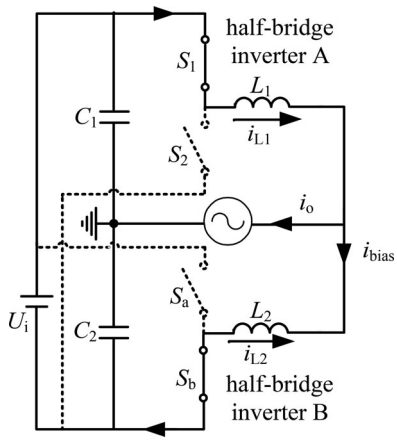


Fig. 6. Diagram of circulation current of interleaved half-bridge inverter.

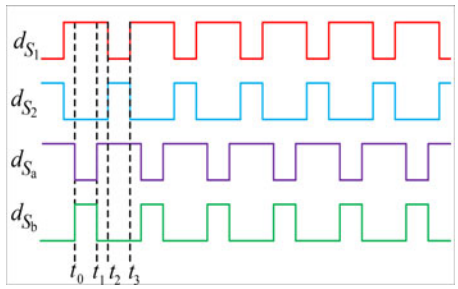


Fig. 7. Driving signals of interleaved half-bridge inverter.

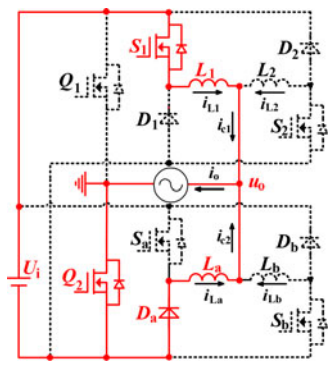


Fig. 8. Diagram of no circulation current of IDBFTI.

inverter B is reversed, so the current flowing through the load $i_o(i_o = i_{L1} + i_{L2})$ will be reduced relatively. Consequently, there will be several problems such as additional power losses, lower efficiency, and increased device stress. However, switch S_1 of IDBFTI just works in the positive half-cycle of output current and switch S_b of IDBFTI is opposite, so they will not be turned ON at the same time and the circulation current will also not be generated. Fig. 8 shows the working modes of the interleaved dual buck inverter, while the top switches are not turned-on simultaneously. The freewheeling current flows through diode, which prevents the reverse current to flow, so there is no circulation current and the polarity of current i_{c2} is the same with that of current i_{c1}.

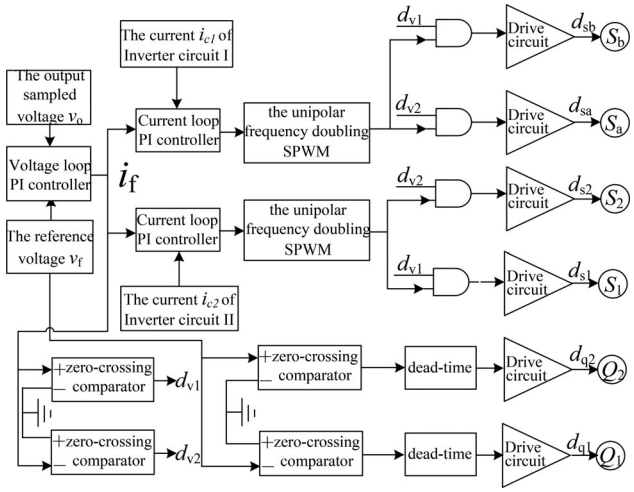


Fig. 9. Control method of IDBFTI.

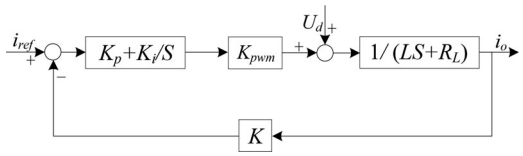


Fig. 10. Control block diagram of the proposed inverter.

III. Simple Analysis of IDBFTI

A. Control Analysis of IDBFTI

Fig. 9 shows the control method of IDBFTI. Power switches Q_1 and Q_2 are controlled by the open-loop strategy. When the grid voltage is greater than zero, Q_2 is turned ON and Q_1 is turned OFF; on the contrary, when the voltage is less than zero, Q_1 is turned ON and Q_2 is turned OFF. All dual buck inverter units adopt SPWM to guarantee the waveform quality of output current. Unipolar SPWM scheme has been successfully applied to the single-phase three-level inverter, and it can effectively improve the quality of output voltage and reduce harmonic content of supply current, so the unipolar SPWM scheme for dual buck inverter unites was chosen. The specific control process is described as follows: The reference current i_f of current loop of two inverter circuits is produced by the phase-locked loop. The unipolar SPWM works following the reference current i_f and the output current of each inverter circuit through current loop PI controller, and the phase difference of the triangular carrier waves of inverter circuit I and II is set as 90°, which will make the current ripple of two inverters interleaved. When the modulation output is processed after the corresponding logical circuits, the drive signals of two inverters are generated.

B. Stability Analysis

From the above analysis, it can be seen that the control methods of two inverter circuits were consistent, so the stability analysis of the proposed inverter can be equivalent to the analysis of one circuit of it. The control block diagram of the proposed inverter was presented in Fig. 10. K is the feedback coefficient

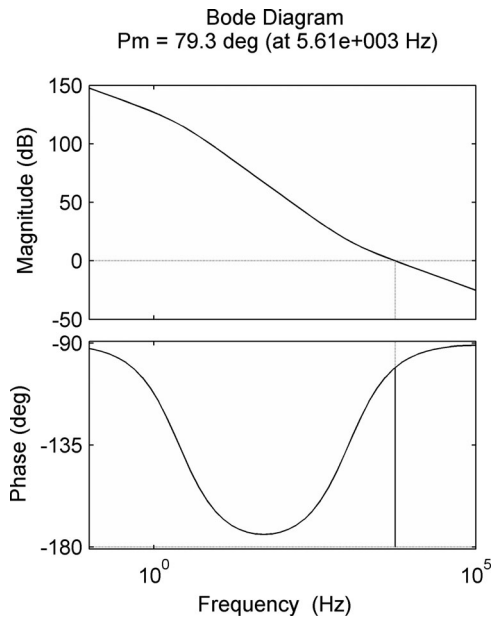


Fig. 11. Bode diagram of the proposed inverter.

of the output current, and K_{pwm} is the equivalent proportionality constant. The open loop transfer function of IDBFTI can be obtained as

$$G(S)H(S) = K \cdot (K_p + \frac{K_i}{S}) \cdot K_{\mathrm{pwm}} \cdot \frac{1}{LS + R_L}. \quad (1)$$

The parameters are as following: $K = 1$, $K_{\mathrm{pwm}} = 30$, $L = 1.3\,\mathrm{mH}$, and $R_L = 0.02\ \Omega$. According to the [33], increasing the phase margin causes the system transient response to be better behaved, with less overshoot and ringing, and the phase margin should be larger than 76°. So the parameters of current loop PI controller are designed as following: $K_p = 1.5$, $K_i = 10000$. By putting these parameters into the (1), bode diagram of IDBFTI can be obtained and was shown in Fig. 11. As can be seen from Fig. 11, the phase margin is 79.3° and is larger than 76°.

C. Filter Inductor Design

In the unipolar SPWM scheme, the output inductor not only filters high-frequency current produced in the switching process, but also suppresses output current fluctuation effectively. So the selection of inductor is directly related to the performance of system.

In this paper, there is no circulation current between inverter I and II of IDBFTI, which has no effect on the inductor design, so the inverter I in Fig. 2 is taken as an example to explain the inductor design. When the output voltage is in the positive half-cycle and the output current i_o is equal to i_{L1}, the voltage and the current of inductor L_1 have the relationship as follows:

$$u_{L1}(t) = L_1 \cdot \frac{di_{L1}(t)}{dt} \quad (2)$$

where the $u_{L1}(t)$ is the voltage of inductor L_1. When the output ripple current reaches the maximum value, setting t_m for this

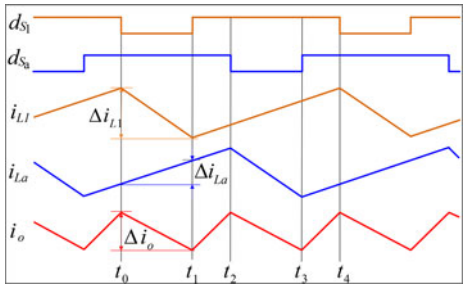


Fig. 12. Analysis of the output ripple current.

moment, T for high-frequency switch cycle, D for the duty of switch cycle, there will be

$$\Delta i_{L1}(t) = \frac{u_{L1}(t_m)DT}{L_1} \tag{3}$$

$$u_{L1}(t_m) = u_i - u_o. \tag{4}$$

By the inductor volt-second balance principle, there will be

$$(U_i - U_o)DT = U_o(1-D)T. \tag{5}$$

By (3)–(5), there will be

$$\Delta i_{L1} = \frac{(U_i - U_o)U_o T}{L_1 U_i}. \tag{6}$$

From (6), it is obvious that when the D equals to 0.5, the output ripple current is maximum. The system bus voltage $U_i = 380\,\text{V}$, the output voltage $U_o = 0.5380 = 190\,\text{V}$, the switching frequency $f = 60\,\text{kHz}$, the single inverter rated output power is $1\,\text{kW}$, the peak rated output current $i_{L1\max} = (1000/220)\times = 6.43$ A, and the actual output ripple current is set as $\Delta i_{L1} < 20\%\ i_{L1\max}$, which cannot be set too low because it needs very large inductor and it also cannot be set too high because it will reduce the efficiency, so the inductance meets the relationship as followed by (6): $L_1 > 1.23\,\text{mH}$. Thus, the value of filter inductor L_1 is selected as 1.3 mH. Inductors L_2, L_a and L_b have the same value as L_1.

D. Analysis of Output Ripple Current

In the *N*th high-frequency switching cycle, when the output current is in the positive half-cycle, the theoretical waveforms of two interleaved inverter circuit currents and system output current are shown in Fig. 12.

In the positive half-cycle, the inductor current i_{L2}, i_{Lb} are equal to zero, $i_{c1} = i_{L1}, i_{c2} = i_{\text{La}}, i_o = i_{c1} + i_{c2}$. The *N*th switching cycle includes four stages $t_0 \sim t_4$, setting Δi_o for output ripple current, ΔT_{off} for the time of the fall of peak current in stage $t_0 \sim t_1$, in which the ripple current of inductor L_1, L_b are Δi_{L1},Δi_{La}. In Fig. 11, the fall time of current i_{L1} is ΔT_{off}, and the ripple is

$$\Delta i_L = \frac{U_o \cos\omega t_N \cdot \Delta T_{\text{off}}}{L_1} \tag{7}$$

where the *D(N)* is the duty cycle at the *N*th switching cycle, $\Delta T_{\text{off}} = [1 - D(N)] \cdot T$. Current i_{La} rises linearly in this stage

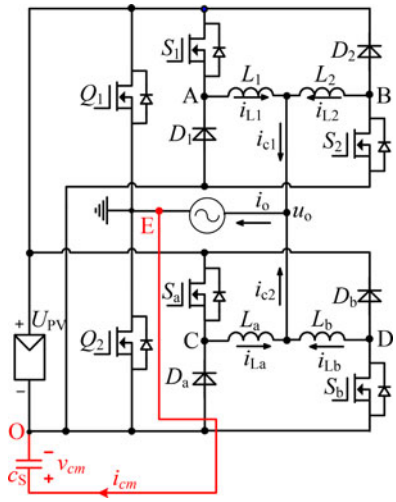


Fig. 13. PV grid-connected inverter.

ΔT_{off} and the ripple of i_{La} is

$$\Delta i_{\text{La}} = \frac{(U_i - U_o \cos\omega t_N) \cdot [1 - D(N)]T}{L_a}. \tag{8}$$

The interleaved output ripple current and Δi_{L1}, Δi_{La} has the following relationship:

$$\Delta i_o = \Delta i_{L1} - \Delta i_{\text{La}}. \tag{9}$$

By (7)–(9), there will be

$$\Delta i_o = \frac{(2U_o \cos\omega t_N - U_i) \cdot \Delta T_{\text{off}}}{L_{1(a)}}. \tag{10}$$

It shows that, the total output ripple current is equal to the difference between the two ripple current of each interleaved circuit, and the frequency of the output ripple current doubles, which reduces the high-frequency harmonic content of output current and the total output current harmonic distortion effectively. In particular, when the duty *D(N)* is equal to 0.5, the Δi_o is equal to zero.

E. Leakage Current Analysis

For the nonisolated grid-connected inverters, the leakage current cannot be ignored and it will reduce the reliability and the security of inverters. The PV grid-connected inverter is shown in Fig. 13, where u_o is the grid voltage and U_{PV} is the output voltage of photovoltaic cells. The system stray capacitors include the parasitic capacitors of PV array C_S. The common voltage of C_S is v_{cm}. According to [34], the common voltage can be defined as

$$v_{\text{cm}} = u_{\text{EO}}. \tag{11}$$

The leakage current of parasitic capacitor C_S can be expressed as

$$i_{\text{cm}} = C_S \frac{dv_{\text{cm}}}{dt}. \tag{12}$$

From Fig. 4, in the proposed inverter, Q_2 keeps turning on in the positive half-cycle, the voltage of parasitic capacitor C_S is clamped to zero, that is

$$v_{\rm cm} = 0. \tag{13}$$

From (12), the leakage current is zero.

While Q_1 keeps turning ON in the negative half-cycle, the voltage of parasitic capacitor C_S is clamped to $U_{\rm PV}$, that is

$$v_{\rm cm} = U_{\rm PV}. \tag{14}$$

From (12), the leakage current is also zero.

F. Analysis of Output Current Harmonic

In the unipolar SPWM scheme adopted in this paper, two sine modulated waves which have the same amplitude and the opposite phase, are used to compare with the same carrier triangular wave, which can get two two-order SPWM waves. By subtracting the two waves, the three-order SPWM can be generated, so the Fourier series expression of output SPWM voltage U_1(t) of inverter circuit I can be given as [35]

$$U_1(t) = MU_i \sin\omega_s t + \frac{4U_i}{\pi} \sum_{m=2,4,6,\ldots}^{+\infty} \sum_{n=\pm1,\pm3,\pm5,\ldots}^{\infty} \frac{J_n\left(\frac{m M \pi}{2}\right)}{m} \cos\frac{m\pi}{2} \sin[(mN+n)\omega_s t] \tag{15}$$

where M is the modulation factor, ω_s is the angular frequency of sine modulated wave, $J_n(x)$ is the *n*-order Bessel function, N is the carrier wave ratio, m is the harmonic order relative to carrier triangular wave, and *n* is the harmonic order relative to sine modulated wave.

The output current of inverter circuit I can be given as

$$i_{c1}(t) = \frac{1}{L}\int [U_1(t) - U_o(t)]d(t). \tag{16}$$

The difference between the triangular carrier phase of inverter circuit I and II is 90 °, so the in the same way the output SPWM voltage U_2(t) of inverter circuit II can be given as

$$U_2(t) = MU_i \sin\omega_s t + \frac{4U_i}{\pi} \sum_{m=2,4,6,\ldots}^{+\infty} \sum_{n=\pm1,\pm3,\pm5,\ldots}^{\infty} \frac{J_n\left(\frac{m M \pi}{2}\right)}{m} \sin[(mN+n)\omega_s t]. \tag{17}$$

The output current of inverter circuit II can be given as

$$i_{c2}(t) = \frac{1}{L}\int [U_2(t) - U_o(t)]d(t). \tag{18}$$

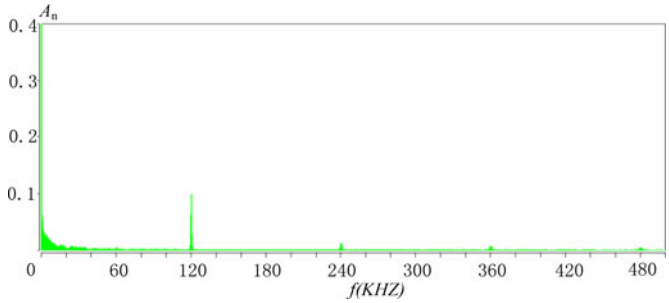


Fig. 14. Spectrum analysis of output current in IDBFTI.

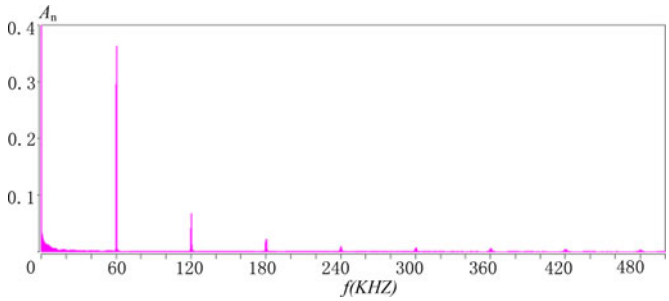


Fig. 15. Spectrum analysis of output current in DBFTI.

The total output current of interleaved inverter circuit can be given as

$$\begin{aligned} i_o(t) &= i_{c1}(t) + i_{c2}(t) \\ &= \frac{1}{L}\int [U_1(t) - U_o(t)]d(t) + \frac{1}{L}\int [U_2(t) - U_o(t)]d(t) \\ &= \frac{1}{L}\int [U_1(t) + U_2(t) - 2U_o(t)]d(t) \\ &= \frac{1}{L}\int \{\{2MU_i \sin\omega_s t + \frac{8U_i}{\pi} \sum_{m=2,4,6,\ldots}^{+\infty} \sum_{n=\pm1,\pm3,\pm5,\ldots}^{\infty} \\ &\quad \frac{J_n\left(\frac{m M \pi}{2}\right)}{m} \left(1+\cos\frac{m\pi}{2}\right) \sin[(mN+n)\omega_s t]\} \\ &\quad -2U_o(t)\}d(t). \end{aligned} \tag{19}$$

From the (19), it can be seen that, in the IDBFTI, the harmonics are around fundamental frequency and the four-times carrier frequency, namely $2mf_c$ ($m = 2, 4, 6 \ldots$, $f_c = 30$ kHz). For example, when the frequency equals to 60 kHz, the m equals to 2,$1 + \cos\frac{m\pi}{2} = 0$, so the harmonic amplitude equals to 0 at the frequency 60 kHz. And from (15), it also can be seen that, in the DBFTI, the harmonics are around fundamental frequency and the even multiple carrier frequency, namely mf_c ($m = 2, 4, 6 \ldots$, $f_c = 30$ kHz). The spectrum of output current of IDBFTI and DBFTI are shown in Figs. 14 and 15 under the same condition by the MATLAB (A_n is the amplitude of *n*-order harmonic). It is obvious that the simulation verifies the correctness of analysis of output current harmonic. With the increase of m ($m = 2, 4, 6 \ldots$), the amplitude of harmonic wave

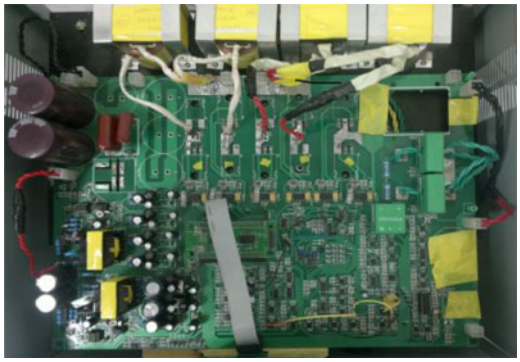


Fig. 16. Prototype of IDBFTI.

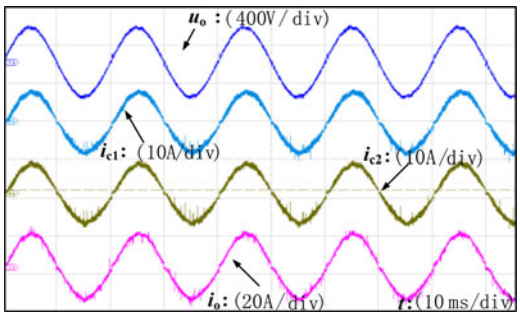


Fig. 17. Experiment waveforms of IDBFTI at full load.

whose frequency is $2mf_c$ in Fig. 14 is obviously less than the amplitude of harmonic wave whose frequency is mf_c in Fig. 15, and the former harmonic content is less than the latter. Therefore, the IDBFTI is more conducive to improving the THD of output current with the same filter.

IV. Experimental Verification

A prototype has been constructed as shown in Fig. 16 with the following parameters: DBFTI: power switch of main circuit is the IGBT FGL35N120FT, power diode is DSEI60-06A, the output filter inductance $L_a = L_b = L_1 = L_2 = 1.3$ mH, the input bus voltage $U_i = 380$ V, and the grid voltage $u_o = 220\text{VAC}/50$ Hz. The output rated power is 2 kW.

Fig. 17 shows the waveforms of IDBFTI at full load: the output current i_{c1}, i_{c2} of two inverter circuits are interleaved, the total output current i_o of the inverter is synchronized with the grid voltage. Fig. 18 shows the waveforms of inverter circuit I, where the current of inductor L_1 is i_{L1} and the voltage of bridge leg A is u_A. It is observed that, when the grid voltage is in the positive half-cycle, the current i_{c1} is equal to the current i_{L1}, and the output of bridge leg A is the SPWM wave; when the grid voltage is in the negative half-cycle, the current i_{c1} is equal to zero and the voltage u_A is equal to the voltage u_o.

Fig. 19 shows the experimental waveforms of the interleaved output current of inverter I and II at full load. Consistent with theoretical analysis, the frequency of total output ripple current doubles and the ripple current is greatly reduced. In addition, the current direction of i_{c1} and i_{c2} is always unchanged and

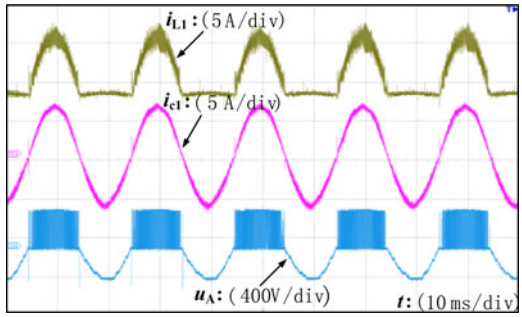


Fig. 18. Experiment waveforms of inverter I at full load.

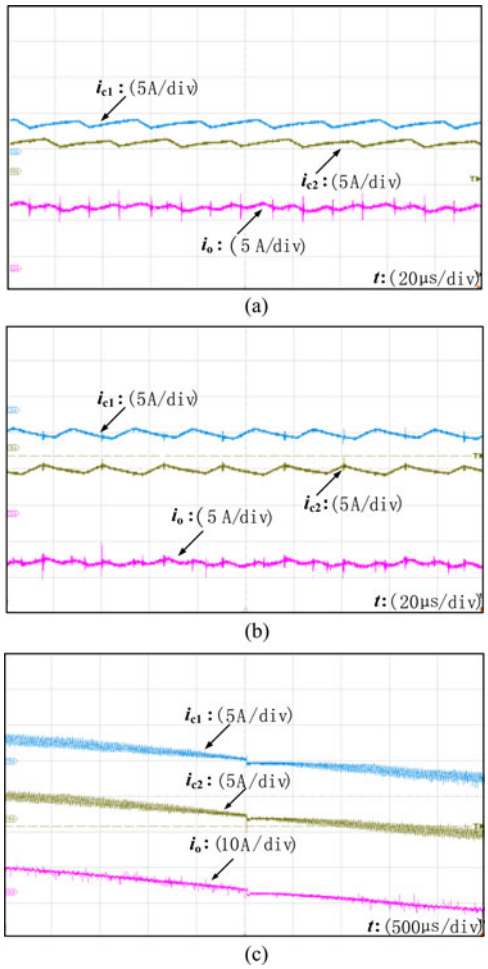


Fig. 19. Experimental waveforms of output current interleaving by inverter I and II of IDBFTI.

there is no circulation current. Fig. 20 shows the experimental waveforms of output current of interleaved half-bridge inverter in Fig. 6, including the waveforms of the current i_{L1}, i_{L2} of two half-bridge inverters and the total output current i_o. When the current is discontinuous, one circuit will produce the reverse current, which is the circulation current according to the above analysis. Comparison with the Fig. 19, there is no circulation current in the proposed inverter.

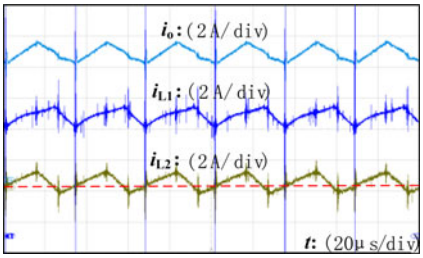


Fig. 20. Experimental waveforms of output current of interleaved half-bridge inverter.

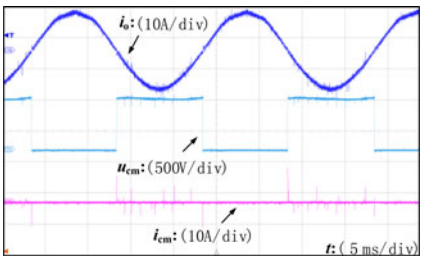


Fig. 21. Experimental result of common mode voltage and leakage current.

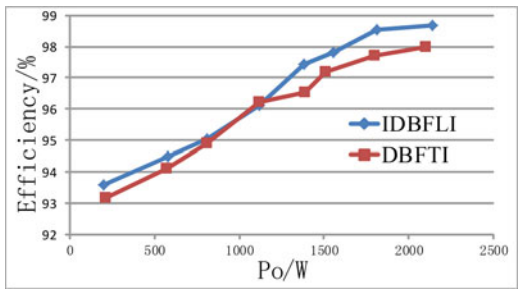


Fig. 22. Comparison of efficiency.

Fig. 21 shows the experimental result of leakage current when the out power P_o is equal to 2137 W. It can be seen that, $u_{\rm cm}$ changes by the power frequency. The voltage is stable at half-cycle, and there is no high-frequency variation, so the leakage current is restrained and it can meet the safety standard.

Fig. 22 shows the comparison of efficiency between IDBFTI and DBFTI at different levels of power delivery to the grid. The input power is measured by Chroma 62024P-600-8 and the output power is measured by Fluke 43B.When the output power is 2137 W, the efficiency of the system is 98.67%. According to the method of inverter loss analysis and calculation proposed in [16], the specific losses of inverter are shown in Fig. 23.The iron loss ($P_{\rm Fe}$) and copper loss ($P_{\rm Cu}$) accounts for only 17.184% of the whole loss, and the inverter losses are mainly conduction losses ($P_{\rm Scon}, P_{\rm Dcon}$) and switch loss ($P_{\rm Son}, P_{\rm Soff}, P_{\rm Don}, P_{\rm Doff}$) of the power switches and diodes. The comparison of output current THD of IDBFTI and DBFTI is shown at resistive load in Fig. 24. Because of the reduced output ripple current of IDBFTI and the double switching frequency, the IDBFTI's THD is lower than that of the DBFTI's.

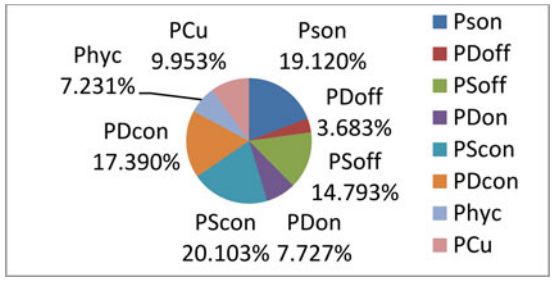


Fig. 23. Forms of losses of IDBFLI.

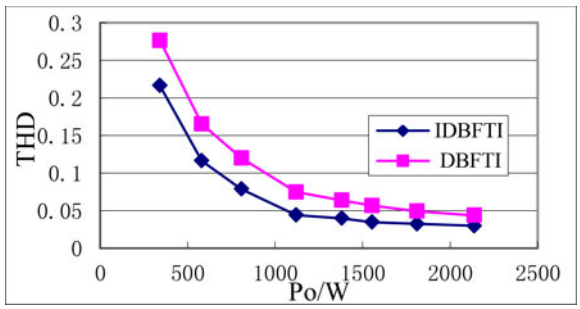


Fig. 24. Comparison of THD.

V. Conclusion

In this paper, a new IDBFTI is proposed, circuit operation is analyzed in detail, and the simulation and experimental verification are conducted. By the theoretical analysis and the experimental results, the proposed topology has the following advantages:

1) It retains the advantages of interleaved parallel technology as follows: promoting the equivalent switching frequency, reducing the switching frequency of parallel unit, reducing the output current ripple, decreasing the total harmonic distortion of the output current.
2) It retains the advantages of dual buck full-bridge three-level inverter as follows: high conversion efficiency, no shoot-through problem, no reverse recovery of body diode. And there is also no circulation current in the inverter, solving the problem of ZSCC in inverter interleaved system by the circuit structure.
3) The interleaved circuits share two power-frequency switches, which can be resized for each specific application, and it is easier to extend the system by improving current capability of the two switches.

The IDBFTI effectively solves the contradiction between the inverter power level and the conversion efficiency, the ripple, the filter of the system, which makes it an excellent candidate in high-reliability and high-efficiency applications, such as grid-connected inverters and new energy power generation.

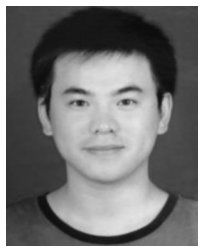
References

[1] M. Prodanovic and T. C. Green, "Control and filter design of three-phase inverters for high power quality grid connection," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 373–380, Jan. 2003.

[2] J. Dannehl and F. Wilhelm Fuchs, "Investigation of active damping approaches for PI-based current control of grid-connected pulse width modulation converters with LCL filters," *IEEE Trans, Ind. Appl.*, vol. 46, no. 4, pp. 1509–1517, Jul./Aug. 2010.
[3] P. Jeannin, D. Frey, Y. Avenas, K. Guepratte, and H. Stephan, "Fault tolerant 24 kVA interleaved inverter," in *Proc. Energy Convers. Cong. Expo.*, 2012, pp. 1733 – 1738.
[4] K. Guepratte, D. Frey, P-O. Jeannin, H. Stephan, and J.-P. Ferrieux, "Fault tolerance on interleaved inverter with magnetic couplers," in *Proc. 25th IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 1817–1824.
[5] D. M. A. Avila, B. Cougo, T. Meynard, and G. Gateau, "Reconfigurable parallel interleaved three-phase inverter for aeronautical applications," in *Proc. Electr. Syst. Aircraft, Railway Ship Propulsion*, 2012, pp. 1–6.
[6] W. Yao, Z. Lu, H. Long, and B. Li "Research on grid-connected interleaved inverter with L filter," in *Proc. 1st Int. Future Energy Electron. Conf.*, 2013, pp. 87–92.
[7] Y. Yisheng, C. Min, and Q. Zhaoming, "A soft-switching interleaved three-level inverter," in *Proc. 25th IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 1503–1507.
[8] B. Johnson, P. Krein, and P. Chapman, "Photovoltaic AC module composed of a very large number of interleaved inverters," in *Proc. 26th IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 976–981.
[9] H. Xiao, S. Xie, W. Chen, and R. Huang, "An interleaving double-switch buck-boost converter for PV grid-connected inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 2642–2646.
[10] C. Gautier, F. Adam, E. Laboure, and B. Revol, "EMC behavior of PWM inverter structure based on coupled interleaved cells using intercell transformers," in *Proc. 14th Eur. Conf. Power Electron. Appl.* 2011, pp. 1–10.
[11] S. A. Diaz Contreras and P. Cabaleiro Cortizo, "Simple control technique for interleaved inverters with magnetically coupled legs," *Power Electron.*, vol. 6, no. 2, pp. 353–363, 2012.
[12] D. Shin, J.-P. Lee, K.-J. Lee, T.-J. Kim, D.-W. Yoo, F. Z. Peng, B. Ge, and H. Cha, "1.5 MVA grid-connected interleaved inverters using coupled inductors for wind power generation system," in *Proc. IEEE Energy Convers. Cong. Expo.*, 2013, pp. 4689–4696.
[13] D. Shin, L. Kyoung.-Jun, K. Hee-Je, L. Jong-Pil, K. Tae-Jin, and Y. Dong-Wook, "Coupled inductors for parallel operation of interleaved three-phase voltage source gridconnected inverters," in *Proc. 28th IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 2235–2239.
[14] D. M. Vilathgamuwa, C. J. Gajanayake, P. C. Loh, "Modulation and control of three-phase paralleled Z-source inverters for distributed generation applications," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 173–183, 2009.
[15] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, Feb. 2012.
[16] Y.-T. Lin and Y.-Y. Tzou, "Digital control of a multi-phase interleaved PWM inverter with minimal total harmonic distortion," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 503–509.
[17] D. Biel, E. Fossas, F. Guinjoan, and R. Ramos, "Interleaving quasi-sliding mode control of parallel-connected inverters," in *Proc. Int. Workshop Variable Struct. Syst.*, 2008, pp. 337–342.
[18] R. Ramos, D. Biel, E. Fossas, and F. Guinjoan, "Interleaving quasi-sliding-mode control of parallel-connected buck-based inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 11, pp. 3865–3873, Nov. 2008.
[19] C. Nemec and J. Roth-Stielow, "Ripple current minimization of an interleaved switched multi-phase PWM inverter for three-phase machine-emulation," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–8.
[20] C. Nemec, J. Wolfle, M. Nitzsche, and J. Roth-Stielow, "Handling of disturbance variables within a multiphase interleaved-switched inverter by a discrete time decoupling network," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
[21] M. A. Abusara, M. Jamil, and S. M. Sharkh, "Repetitive current control of an interleaved grid connected inverter," in *Proc. 3rd IEEE Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2012, pp. 558–563.
[22] C.-T. Pan and Y.-H. Liao, "Modeling and coordinate control of circulating currents in parallel three-phase boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 825–838, Apr. 2007.
[23] S. A. D. Contreras, P. C. Cortizo, and M. A. Severo Mendes, "Analysis of digital controllers for equilibrated current distribution in an interleaved inverter," in *Proc. 9th IEEE Int. Conf. Ind. Appl.*, 2010, pp. 1–6.
[24] C. Zhang, S. Du, and Q. Chen, "A novel scheme suitable for high-voltage and large-capacity photovoltaic power stations," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3775–3783, Sep. 2013.
[25] J. M. Schellekens, J. L. Duarte, M. A. M. Hendrix, and H. Huisman, "Interleaved switching of parallel ZVS hysteresis current controlled inverters," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 2822–2829.
[26] J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Fast-shared current transient response in high-precision interleaved inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3308–3317, Nov. 2011.
[27] R. Lai, L. Wang, and J. Sabate, "A high efficiency two-phase interleaved inverter for wide range output waveform generation," in *Proc. Energy Convers. Congr. Expo.*, 2012, pp. 4533 – 4537.
[28] A. M. Knight, J. Ewanchuk, and J. C. Salmon, "Coupled three-phase inductors for interleaved inverter switching," *IEEE Trans. Magn.*, vol. 44, no. 11, pp. 4119–4122, Nov. 2008.
[29] B. Vafakhah, A. M. Knight, and J. Salmon, "Reducing losses in multilevel coupled inductor inverters using interleaved discontinuous SVPW," in *Proc. 25th IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 2013–2020.
[30] B. Vafakhah, A. M. Knight, and J. Salmon, "Improved interleaved discontinuous carrier-based PWM strategy for 3-level coupled inductor inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2095–2101.
[31] B. Vafakhah, J. Ewanchuk, and J. Salmon, "Multicarrier interleaved PWM strategies for a five-level NPC inverter using a three-phase coupled inductor," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2549–2558, Nov.-Dec. 2011.
[32] Z. Xin, H. Feng and L. Z.-cheng, "Interleaved dual buck full bridge three-level inverter," China Patent 2 012 102 160 646, 2012.
[33] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Kluwer, 2001, pp. 342–347.
[34] H. F. Xiao, X. P. Liu, and K. Lan, "Zero-voltage-transition full-bridge topologies for transformerless photovoltaic grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5393–5401, Oct. 2014.
[35] L. Feng-jun, *Sine Wave Inverter*. Beijing, China: Science and Education Press, 2002, pp. 126–128.

Feng Hong (M'13) was born in Anhui, China, in 1979. He received the B.S., M.S., and Ph.D. degrees from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2001, 2004, and 2008, respectively, all in power electronics and power transmission.

In 2008, he joined the College of Electronic and Information Engineering, NUAA, where he is currently an Associate Professor. His current research interests include renewable energy generation system, high-frequency power conversion, and multilevel power conversion. He has more than 30 journal articles published and accepted, and 18 China patents awarded.



Jun Liu was born in Jiangsu, China, in 1991. He received the B.S. degree in electrical engineering and automation from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2013, where he is currently working toward the M.S. degree in circuits and systems.

His current research interests include renewable energy generation system and high-frequency power conversion.

Baojian Ji received the B.S. degree in automation engineering from Nanjing Normal University, Nanjing, China, the M.S. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, and the Ph.D. degree from Southeast University, Nanjing, in 2002, 2007, and 2012, respectively.

In 2007, he was a Lecturer with Nanjing Tech University, where he is currently the Head of the Department of Electrical Engineering. He has published more than 20 technical papers. His research interests include the digital control technique and the development of a grid-tied inverter for renewable energy applications.

Yufei Zhou (S'10–M'14) was born in Nanjing, China, in 1984. She received the B.S., M.S., and Ph.D. degrees from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, in 2006, 2009, and 2013, respectively.

In 2013, she joined the College of Electric and Information Engineering, NUAA. Her current research interests include renewable energy generation, Z-source converters, and integrated power electronics modules.

Jianhua Wang (M'11) received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2004 and 2010, respectively.

In 2010, he joined the faculty of School of Electrical Engineering in Southeast University, Nanjing, where he is currently a Lecturer. He has published more than 20 technical papers. He is the holder of two China patents. His main research interests include power electronics system integration, general power electronic circuit topologies, modeling and control, high performance power conversions for shipboard, aerospace, and renewable energy applications.

Chenghua Wang was born in Jiangsu, China, in 1963. He received the B.S. and M.S. degrees from the Southeast University, Nanjing, China, in 1984 and 1987, respectively.

In 1987, he joined the College of Electronic and Information Engineering, Nanjing University of Aeronautics and Astronautics (NUAA), and became a Professor in 2001. His current research interests include electronic science and technology, circuit, and system. He has published more than 80 technical papers in journals and conferences, and six books.

Prof. Wang was awarded more than ten Teaching and Research Awards at the Provincial and Ministerial Level.