Integrated Dual Full-Bridge Converter With Current-Doubler Rectifier for EV Charger

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***Abstract*—A novel converter topology for high-power battery charger applications is proposed in this paper. The topology adopts the integration structure of two full-bridge converters, which shares one leg of switching device called center-leg. The two full-bridge converters are placed in parallel on the primary side, and are driven in a phase-shift manner. The integrated form of two current-doubler rectifier is adopted on the secondary side, and it has full-bridge structure. With this structure, the proposed converter can overcome drawbacks of the conventional phase-shift full-bridge converter; narrow zero-voltage-switching range, large duty-cycle loss, and high component counts. The validation of the proposed converter is confirmed by the experiment with a prototype battery charger of 5.7 kW and 13.5 A.**

***Index Terms*—Current doubler rectifier, phase-shift full-bridge, zero-voltage-switching.**

I. Introduction

OVER the last few decades, the global warming and the depletion of natural resources have received increasing attention. Moreover, the abatement of carbon dioxide emissions was strongly required around the world. Accordingly, the sales of eco-friendly electric-powered vehicle such as hybrid electric vehicles (HEVs), plug-in HEVs (PHEVs), pure electric vehicles (EVs), and fuel cell vehicles, are steeply growing. Moreover, the growing trend of EV sales has become the tendency of vehicle market due to the national targets of International Energy Association [1], [2].

These vehicles need necessarily rechargeable batteries as the power source of electric traction system [3]. Among them, PHEVs or EVs require a larger battery with much higher capacity [4], [5]. The battery is typically recharged from public line via an ac–dc converter named as battery charger. In order to meet low current distortion and high conversion efficiency, most of battery chargers have the basic architecture of an ac–dc converter with a power factor correction (PFC) circuit, followed by an isolated dc–dc converter [6]–[11].

For the development of battery charger, it is imperative to reduce its volume and weight in order to facilitate packaging and to highlight the utilization factor of energy. Furthermore, high efficiency is emphasized for the reduction of size and fuel saving. In addition, robust and reliable operation should be satisfied.

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In order to meet the requirements, modern battery chargers adopt the bridgeless boost PFC technology to reduce conduction power loss, which increases the overall efficiency and reduces greatly the size and weight of heat sink. To obtain higher efficiency, especially at high-power levels, interleaving or parallel approaches can be taken into account [12]–[15].

For dc–dc converter part, phase-shift full-bridge (PSFB) converter is the most popular candidate since the converter is a well-researched topology for medium to high power applications where isolation is required [16]. The converter has simple structure, easy controllability, and ZVS capability without the help of any auxiliary components or complex control techniques. However, it has a drawback such as the narrow ZVS range of lagging-leg switches [17]. In order to overcome the drawback, an additional resonant inductor is adopted to extend the ZVS range of lagging-leg switches [18], [19]. The voltage oscillation is caused by the inductor, thus two clamping diodes are used for reduction of the oscillation. However, the converter suffers from an increased duty-cycle loss. In addition, its ZVS operation is still not able to be achieved at a very light load. Several full-bridge converters extending the ZVS range without the increase of duty-cycle loss were introduced in [20]–[23]. In the converters, their operation is based on the one full-bridge converter so that they are not suitable for high output current applications. For high output current applications, the current-doubler rectifier (CDR) is widely applied in various applications [24], [25]. However, the topologies are generally used for low output voltage applications.

This paper suggests a dc–dc converter topology for high-power on-board charger with the capacity of over 6.6 kW in EVs. The application has the maximum output voltage as 420 V. The proposed converter consists of the integration with two full-bridge inverters on primary side, and it is driven in a phase-shifting manner to regulate the output current or voltage. In the rectifier stage, two CDR circuits are integrated by sharing inductors. This architecture makes it possible that the proposed converter features less duty-cycle loss, wide ZVS range, and low number of components.

The proposed converter can easily reflect a trend that the power rating of battery charger will be continuously increased for the purpose of extending the driving range in the EV mode of EVs, because the converter is based on two full-bridge converters.

The circuit configuration, operation principle, and relevant analysis of the proposed converter are described in this paper. In order to confirm the validation of proposed converter, experiment with a prototype converter realized with a 5.7-kW battery charger is carried out. The experimental results show the effectiveness of the proposed converter as battery charger.

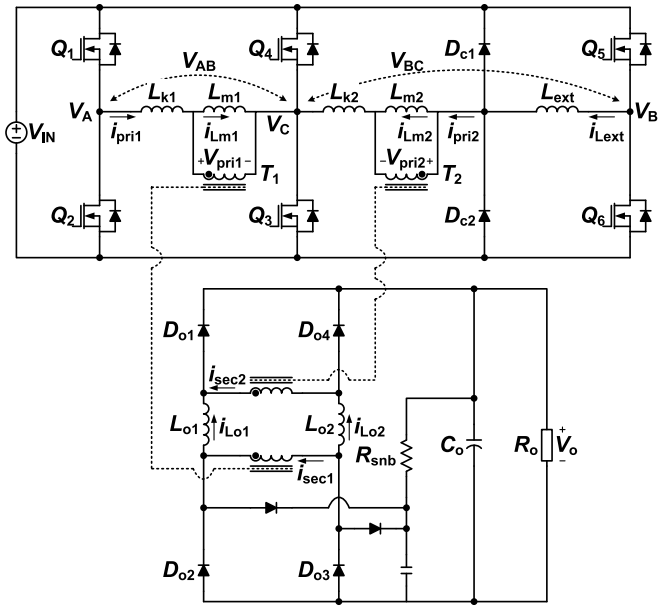

Fig. 1. Circuit configuration of integrated dual full-bridge (IDFB) converter.

II. Description of the Proposed Converter

A. Circuit Derivation

Fig. 1 shows the circuit configuration of the proposed converter. As shown in the figure, the proposed converter is composed of two full-bridge inverter sharing a leg with switches Q_3 and Q_4; a full-bridge inverter consists of switches from Q_1 to Q_4 and a transformer T_1, and the other consists of switches from Q_3 to Q_6 and a transformer T_2. An additional external inductor ($L_{\rm ext}$) is employed in series with T_2. On the secondary side, two transformers and two output inductors (L_{o1} and L_{o2}) are connected in series like as a circle. One CDR circuit is composed of D_{o2}, D_{o3}, L_{o1}, L_{o2}, and the secondary side of T_1. At the each end of T_1, cathode terminal of diodes and output inductors are connected. The other one is composed of D_{o1}, D_{o4}, L_{o1}, L_{o2}, and the secondary side of T_2. At the each end of T_2, anode terminal of diodes and output inductors are connected. In order to clamp voltage stress of rectifier diodes, a RCD clamp circuit is implemented for D_{o2} and D_{o3}, and clamp diodes, D_{C1} and D_{C2}, are employed at the primary side for D_{o1} and D_{o4}.

B. Operation Principle

In order to analyze the operation of the proposed converter, several assumptions are made as follows:

1) A transformer ideally operates according to the primary-side and secondary-side turns; N_p and N_s, respectively. The notation simplifies as $N_{p1} = N_{p2} = N_p, N_{s1} = N_{s2} = N_s$, and $N_s/N_p = n$.
2) The switch devices are ideal MOSFETs except for the parasitic capacitors and the internal body diodes.
3) The rectifier diodes are ideal except for the junction capacitance, $C_{Do1} = C_{Do2} = C_{Do3} = C_{Do4} = C_j$.
4) The capacitance of switch parasitic capacitor, $C_{\rm oss}$, is much larger than the junction capacitance of diode, C_j.

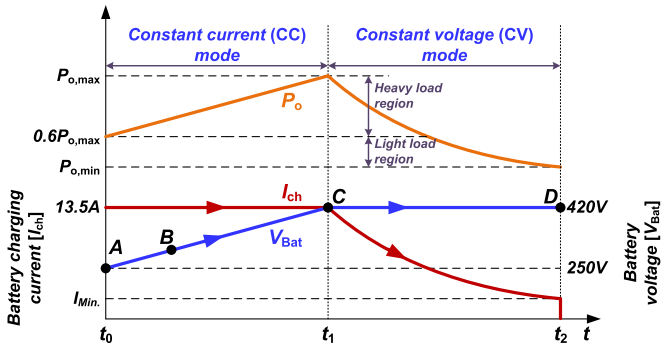

Fig. 2. Battery charging profile.

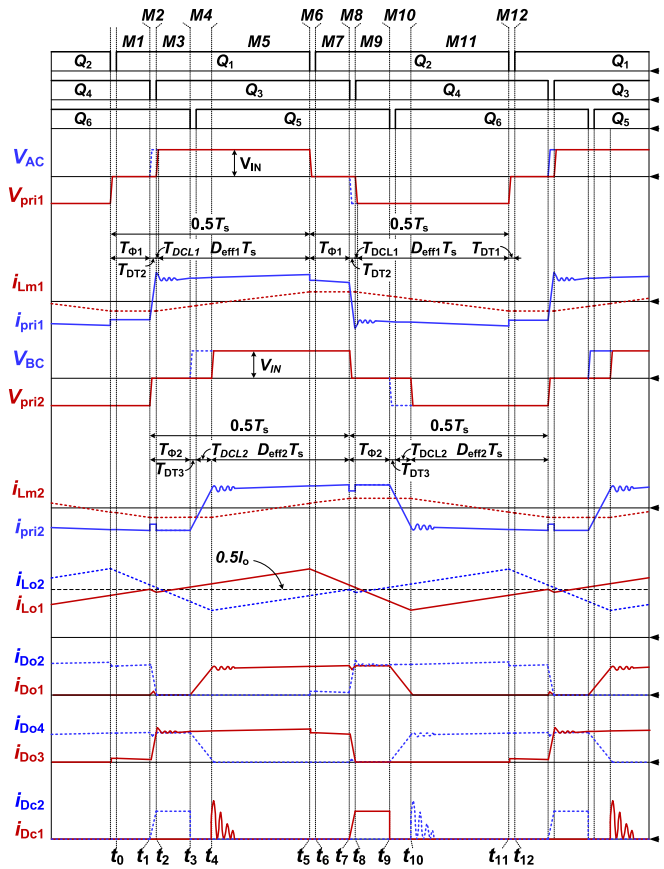

Fig. 3. Key waveforms of proposed converter.

5) The output filter capacitor is large enough to be treated as a constant voltage (CV) source with output voltage, V_o.
6) The output filter inductors have the same magnitude as $L_{o1} = L_{o2} = L_o$, and $\Delta I_{Lo1} = \Delta I_{Lo2} = \Delta I_{Lo}$.

The converter operates under battery charging profile shown in Fig. 2. At the state A in the figure, the phase-delay time, T_Φ, is maximized to regulate low output voltage. With the large phase-delay time, it can be easy to apprehend the operation of the proposed converter. In addition, the controller operates in phase-shift manner as same as the conventional PSFB converter. Thus, the key waveforms are drawn at low output voltage condition as in Fig. 3. Referring to the figure, it can be seen that all the switches are driven with a constant duty-ratio ($D = 0.5$), if

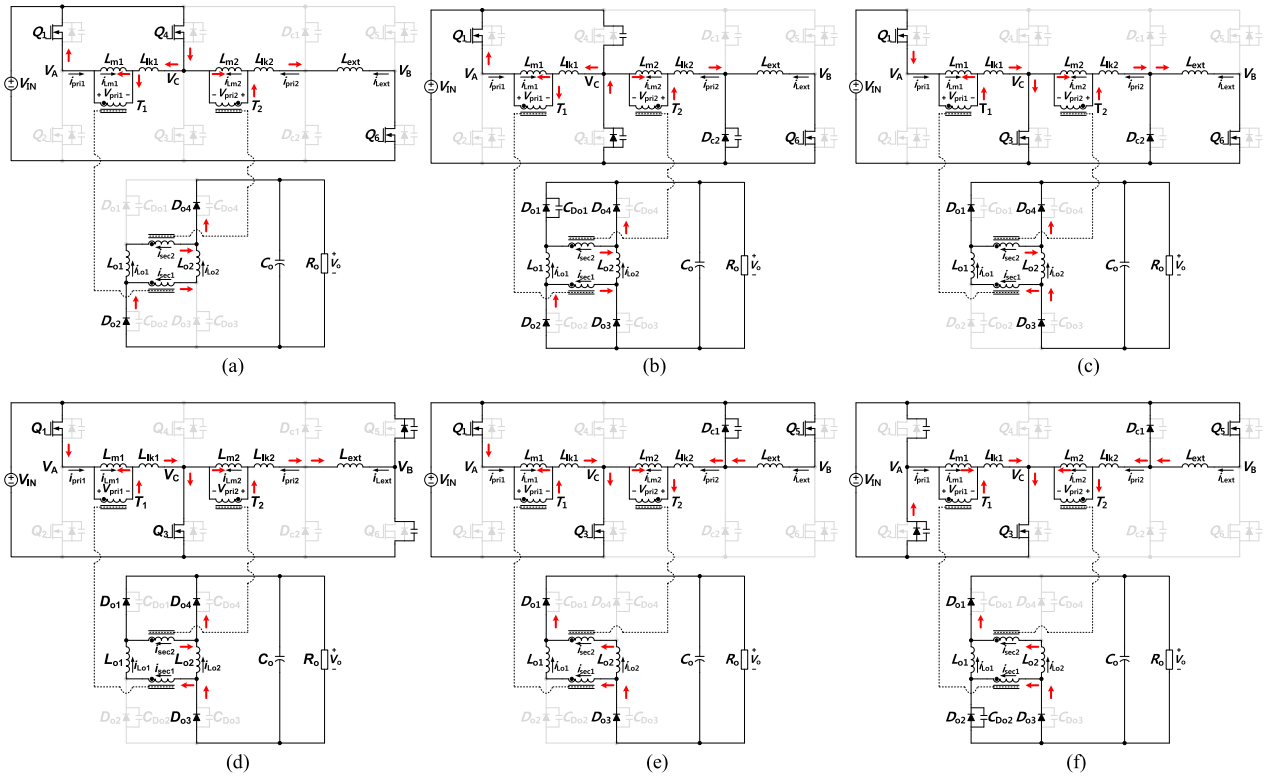

Fig. 4. Operating modes of proposed converter. (a) Mode 1 [$t0-t1$]. (b) Mode 2 [$t1-t2$]. (c) Mode 3 [$t2-t3$]. (d) Mode 4 [$t3-t4$]. (e) Mode 5 [$t4-t5$]. (f) Mode 6 [$t5-t6$].

ignoring the dead times such as T_{DT1}, T_{DT2} and T_{DT3}, which are the dead time between the driving signals for two switches on the same leg; $Q_1 - Q_2, Q_3 - Q_4$, and $Q_5 - Q_6$ in order.

The output power is controlled by adjusting the phase-shift time of $T_{\Phi 1}$ and $T_{\Phi 2}$. They are the same magnitude as T_{Φ}, and it is required to satisfy that the sum of $T_{\Phi 1}$ and $T_{\Phi 2}$ should be smaller than 0.5 T_s at light load condition in CV mode.

In a switching period, there are 12 operating modes that can be divided into two half cycles: t_0-t_6 (from mode 1 to mode 6) and t_6-t_{12} (from mode 7 to mode 12). The operational principles of two half cycles are symmetric, thereby only the first half cycle is described and operating circuits during the cycle are shown in Fig. 4.

Mode 1 [t_0-t_1]: Mode 1 begins when the switch Q_1 is turned ON, and it ends when the switch Q_4 is turned OFF. During this mode, switches Q_1, Q_4 and Q_6 are in ON-state and diodes D_{o2}, D_{o3} and D_{o4} are conducted. Main output current flows through diodes D_{o2} and D_{o4}, and the difference between $i_{Lo2}(t)$ and $i_{\mathrm{sec1}}(t)$ flows through D_{o3} because $i_{Lo2}(t)$ decreases to meet $i_{\mathrm{sec1}}(t)$. The $i_{\mathrm{sec1}}(t)$ has constant value since $i_{\mathrm{pri1}}(t)$ circulates through Q_1 and Q_4 as shown in Fig. 4(a). The power transfers to the secondary side through T_2. Therefore, following equations can be obtained:

$$V_{Lo1} = nV_{\mathrm{IN}} - V_o \tag{1}$$

$$V_{Lo2} = -V_o. \tag{2}$$

Mode 2 [t_1-t_2]: Mode 2 begins when the switch Q_4 is turned OFF, and it ends when the current flowing through output diode, i_{Do2} reaches zero level. During this mode, a commutation occurs between output diodes D_{o2} and D_{o3} and the main powering current flows through D_{o2}, D_{o3} and D_{o4}. The difference between $i_{Lo1}(t)$ and $i_{\mathrm{sec2}}(t)$ flows through D_{o1}. Thereby, all output diodes are conducted, and then the voltages across the secondary side of transformers T_1 and T_2 are zero. The clamping diode D_{C2} is conducted, thus the equivalent circuit can be drawn as Fig. 5. Based on the circuit, following equation can be obtained:

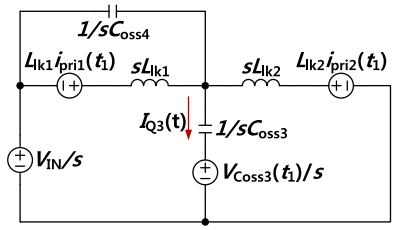

Fig. 5. Equivalent circuit of proposed converter at Mode 2.

$$i_{Q3}(t) = \sqrt{A^2 + B^2}\sin\left[\omega_{\mathrm{o}}(t - t_1) + \alpha\right] \tag{3}$$

$$V_{\mathrm{DS3}}(t) = \frac{L_{lk2}}{L_{lk1} + L_{lk2}}V_{IN} + \sqrt{C^2 + 4z_o^2 B^2}\cos\left[\omega_{\mathrm{o}}(t - t_1) + \beta\right] \tag{4}$$

where

$$A = -\frac{1}{L_{lk2}}\sqrt{\frac{C_{\mathrm{oss}}L_{eq}}{2}}V_{\mathrm{IN}},\ B = \frac{1}{2}\left[i_{\mathrm{pri1}}(t_1) + i_{\mathrm{pri2}}(t_1)\right],$$

$$C = \frac{L_{lk1}}{L_{lk1}+L_{lk2}}V_{\rm IN},\ \alpha = \cos^{-1}\left(\frac{A}{\sqrt{A^2+B^2}}\right),$$

$$\beta = \cos^{-1}\left(\frac{C}{\sqrt{C^2+4z_{\rm o}^2B^2}}\right),\ z_{\rm o} = \sqrt{\frac{L_{eq}}{2C_{\rm oss}}},$$

$$\omega_{\rm o} = \sqrt{\frac{1}{2L_{eq}C_{\rm oss}}},\ \text{and}\ L_{eq} = \frac{L_{lk1}L_{lk2}}{L_{lk1}+L_{lk2}}.$$

The primary current can be calculated with the equations

$$i_{\rm pri1}(t_1) + i_{\rm pri2}(t_1) = i_{Lm1}(t_1) + i_{Lm2}(t_1) + nI_o \quad (5)$$

$$i_{\rm Lm1}(t_1) = -I_{\rm Lm1,peak} = -\frac{D_{\rm eff1}T_{\rm s}V_{\rm IN}}{2L_{\rm m1}} \quad (6)$$

$$i_{Lm2}(t_1) = -I_{Lm2,\rm peak} = -\frac{D_{\rm eff2}T_{\rm s}V_{\rm IN}}{2L_{m2}}. \quad (7)$$

Due to the resonance operation, the switch Q_3 can be turned on with ZVS.

Mode 3 [t_2–t_3]: This mode begins when the commutation between the secondary diodes is completed, and it ends when the switch Q_6 is turned OFF. During this mode, the switches Q_1, Q_3 and Q_6 are in ON-state and diodes D_{o1}, D_{o3}, and D_{o4} are conducted. The input power is transferred to the secondary side by the transformer T_1, and the main output current path is composed of D_{o3} and D_{o4}. The difference between $i_{\rm sec2}(t)$ and $i_{Lo1}(t)$ flows through D_{o1} because $i_{\rm sec2}(t)$ has constant value since the primary current $i_{pri2}(t)$ circulates through Q_3 and Q_6.

Mode 4 [t_3–t_4]: Mode 4 begins when the switch Q_6 is turned OFF, and it ends when the current flowing through output diode, $i_{Do4}(t)$ reaches zero level. During this mode, diodes D_{o1}, D_{o3}, and D_{o4} are conducted, and the resonance of $C_{\rm oss5}$, $C_{\rm oss6}$, L_{lk2}, and $L_{\rm ext}$ occurs in the primary side. In addition, a commutation occurs between D_{o1} and D_{o4}. The voltages across $C_{\rm oss5}$ and $C_{\rm oss6}$ are discharged and charged by the resonance, respectively

$$V_{\rm DS5}(t) = V_{\rm IN} - z_{\rm o}i_{\rm pri2}(t_3)\sin\omega_{\rm o}(t-t_3) \quad (8)$$

where $z_{\rm o} = \sqrt{\frac{L_{lk2}+L_{\rm ext}}{2C_{\rm oss}}}$, and $\omega_{\rm o} = \frac{1}{\sqrt{2C_{\rm oss}(L_{lk2}+L_{\rm ext})}}$.

The primary current is expressed as follows:

$$I_{\rm pri2}(t_3) = I_{Lm2}(t_3) + nI_{Lo2}(t_3) \quad (9)$$

where $i_{Lm2}(t_3) = -I_{Lm2,\rm peak} = -\frac{D_{\rm eff2}T_{\rm s}V_{\rm IN}}{2L_{m2}}$, and $I_{Lo2}(t_3) = 0.5I_o - \frac{V_{\rm o}}{L_{\rm o}}T_\phi$ at $T_{\rm DCL1} \approx T_{\rm DCL2}$.

Due to the resonance operation, the switch Q_5 can be turned on with ZVS.

Mode 5 [t_4–t_5]: Mode 5 is main powering mode. It begins when i_{Do4}(t) reaches zero level, and it ends when the switch Q_1 is turned OFF. During this mode, switches Q_1, Q_3 and Q_5 are in on-state, and diodes D_{o1} and D_{o3} are conducted. Input power transfers to secondary side through T_1 and T_2.

Mode 6 [t_5–t_6]: Mode 6 begins when the switch Q_1 is turned OFF, and it ends when the switch Q_2 is turned ON. During this mode, the resonance of $C_{\rm oss1}$, $C_{\rm oss2}$, and L_{lk1} occurs in the primary side. The voltages across $C_{\rm oss2}$ and $C_{\rm oss1}$ are discharged and charged by the resonance, respectively

$$V_{\rm DS2}(t) = V_{\rm IN} - z_{\rm o}I_{\rm pri1}(t_5)\sin\omega_{\rm o}(t-t_5) \quad (10)$$

where $z_{\rm o} = \sqrt{\frac{L_{lk1}}{2C_{\rm oss}}}$, and $\omega_{\rm o} = \frac{1}{\sqrt{2C_{\rm oss}L_{lk1}}}$.

The primary current is expressed as follows:

$$I_{\rm pri1}(t_5) = I_{Lm1}(t_5) + nI_{Lo1}(t_5) \quad (11)$$

where $i_{Lm1}(t_5) = -I_{Lm1,\rm peak} = -\frac{D_{\rm eff1}T_{\rm s}V_{\rm IN}}{2L_{m1}}$, and $I_{Lo1}(t_5) = 0.5(I_o + \Delta I_{Lo})$.

The operation is the same as conventional PSFB, so that the output current has the highest value and it is reflected to primary side. Thereby, the switch Q_2 is easily turned on with ZVS condition.

III. Analysis of Steady-State Operation

A. Relation of Input-to-Output Voltage

The dc conversion ratio of the proposed converter can be derived by using the principle of volt-second balance on the output inductor. The conversion ratio equation is expressed as follows:

$$M = V_o/V_{\rm IN} = n(D_{\rm eff1} + D_{\rm eff2}) \quad (12)$$

where $D_{\rm eff1}$=$(0.5T_{\rm s} - T_\phi - T_{\rm DCL1})T_{\rm s}^{-1}$, and $D_{\rm eff2}$ = $(0.5T_{\rm s} - T_\phi - T_{\rm DCL2})T_{\rm s}^{-1}$ are effective duty cycle.

It is noted that the output voltage of the proposed converter can be modulated by adjusting phase delay at a fixed switching frequency, like the conventional PSFB converter.

B. Duty-Cycle Loss

In general, it is known that the method applying a large resonant inductor for extending ZVS range increases duty-cycle loss [16]. To compensate for the increased duty-cycle loss, a large turn-ratio transformer with high secondary turns should be applied. However, it generates the conduction power losses, and increases the voltage stress of rectifier.

In the proposed converter, output inductor current can be negative value in light load condition so that the reflected current from secondary side can be used as soft switching energy for lagging-leg switches, Q_5 and Q_6. Thereby, ZVS range for Q_5 and Q_6 can be extended with small external inductor. Compared to the conventional PSFB converter with the same ZVS range, it can reduce the duty-cycle loss, $T_{\rm DCL2}$. Since the ZVS operation of switches Q_1 to Q_4 is easily achieved without external inductor, the duty-cycle loss, $T_{\rm DCL1}$ is never increased. The equations of duty-cycle losses, $T_{\rm DCL1}$ and $T_{\rm DCL2}$ are expressed as follows [1]:

$$T_{\rm DCL1} = \frac{2L_{lk1}n}{V_{\rm IN}}\left[I_{\rm o} - \frac{V_{\rm o}}{L_{\rm o}}(1-2D)T_{\rm s}\right] \quad (13)$$

$$T_{\rm DCL2} = \frac{2L_{lk,\rm total}n}{V_{\rm IN}}\left[I_{\rm o} - \frac{V_{\rm o}}{L_{\rm o}}(1-2D)T_{\rm s}\right] \quad (14)$$

where $L_{lk,\rm total} = L_{lk2} + L_{\rm ext}$, and D is ideal duty-ratio generated by the controller ($0 < D < 0.5$).

C. ZVS Condition

The ZVS characteristic of leading-leg switches, Q_1 and Q_2, is similar to that of the conventional PSFB converter. It is easy

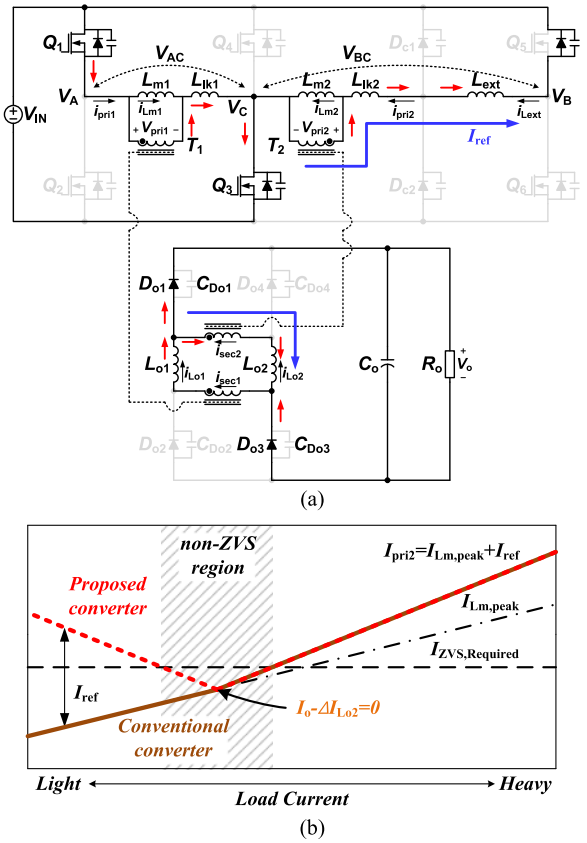

Fig. 6. ZVS condition analysis of lagging-leg switches, $Q5$ and $Q6$. (a) Circuit diagram of Mode 4 with $\Delta ILo2 > Io$, and (b) ZVS characteristic as per load current.

to achieve ZVS condition since the reflected current from output inductor has the highest value.

The ZVS condition of lagging-leg switches, Q_5 and Q_6, is affected by i_{pri2}. It is the same as the conventional PSFB converter, but the reflected current is not the same in light load condition. For easy understanding, the analysis is performed in the Mode 4. At light load condition, the current ripple of output inductor is higher than average output current, then $i_{Lo2}(t)$ becomes negative value. As aforementioned, the output inductors and secondary side of transformers are connected as a circle. The structure is derived from the integration of two CDRs. A current circulates in this loop as shown in Fig. 6(a), then i_{pri2} have higher ZVS energy. Therefore, wide ZVS range can be achieved with small external inductor. Especially, it is possible to achieve ZVS condition in very light load condition. In order to ensure ZVS operation in whole range, magnetizing current ($I_{\mathrm{Lm,peak}}$) of T_2 should have higher current than required current ($I_{\mathrm{ZVS,required}}$) for ZVS in the worst condition as shown in Fig. 6(b).

The ZVS condition of center-leg switches, Q_3 and Q_4, is achieved by the sum of two primary currents, $i_{\mathrm{pri1}}(t)$ and $i_{\mathrm{pri2}}(t)$. Before these switches are turned ON, the output inductor currents are equal to a half of output current. These currents are reflected through transformers, and they help to achieve ZVS operation. Namely, the ZVS condition is directly affected by load condition.

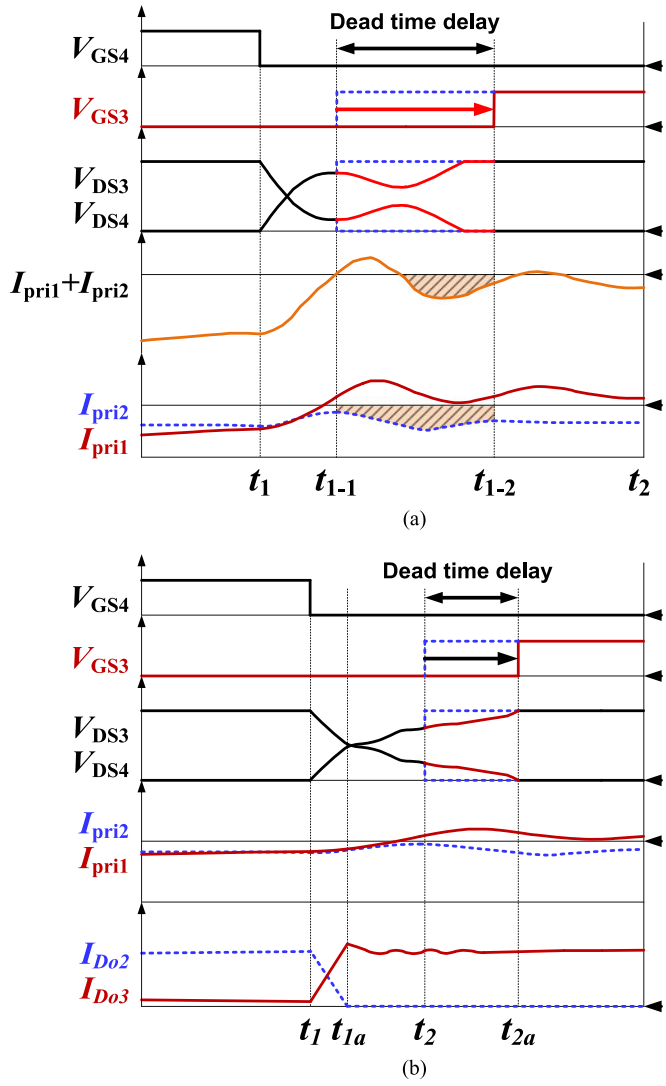

Fig. 7. Voltage and current waveforms of center-leg switches w/ VDT control (a) in normal light load condition, and (b) in non-ZVS region.

Since the Q_3 and Q_4 are the same status, the analysis is performed about Q_3 on Mode 2. From (4), it is noted that the relation between leakage inductances and the magnitude of primary currents affects drain-to-source voltage. In case of very light output-load condition, the primary currents can be regarded as zero value, and drain-to-source voltage of Q_3 can be expressed as follows:

$$V_{\mathrm{DS3}}(t) = \frac{L_{eq}}{L_{lk1}} V_{\mathrm{IN}} + \frac{L_{eq}}{L_{lk2}} V_{\mathrm{IN}} \cos\left[\omega_{\mathrm{o}}(t - t_1)\right] \qquad (15)$$

where $\omega_{\mathrm{o}} = \sqrt{\frac{1}{2L_{eq}C_{\mathrm{oss}}}}$, and $L_{eq} = \frac{L_{lk1}L_{lk2}}{L_{lk1}+L_{lk2}}$.

From the above equation, the drain-to-source voltage fluctuates even though the primary current is zero. Thereby, the switching loss can be reduced. However, when I_{Do2} reaches zero level at t_{1a} as shown in Fig. 7(b), the circuit diagram is changed as Fig. 8. Then, the parasitic capacitance (C_j) on secondary rectifier diodes starts to be involved in the resonance. Until Q_3 is turned ON, the resonant frequency is changed as

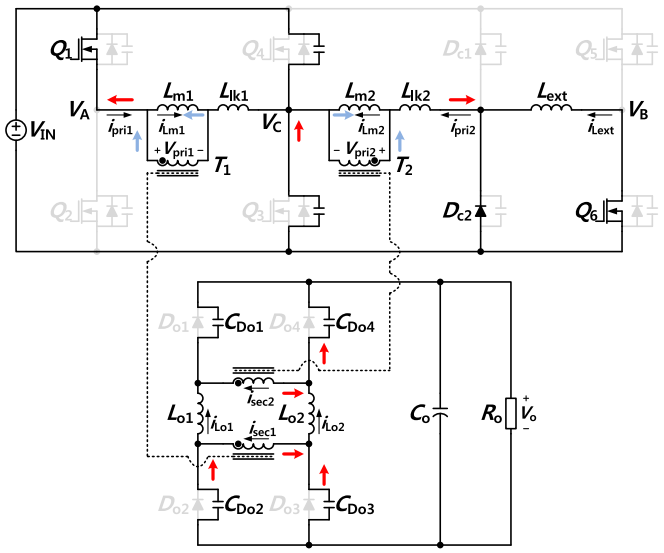

Fig. 8. Circuit diagram of additional mode between Mode 2 and Mode 3.

follows:

$$\omega_{\mathrm{o}} = \sqrt{\frac{1}{2L_{eq}C_{\mathrm{oss}}} + \frac{1}{4L_{eq}n^2C_{\mathrm{j}}}}. \tag{16}$$

Although i_{pri1} changes direction and the drain-to-source voltage of Q_3 increases again, the i_{pri2} is maintained as negative value as shown in Fig. 7(a) and (b). Thereby, ZVS condition is barely achieved, but it is possible to achieve ZVS condition if sufficient time is allowed.

D. Variable Delay Time (VDT) Control

For achieving ZVS condition of lagging-leg and center-leg switches, VDT control scheme modifying dead time T_{DT2} and T_{DT3} is implemented in controller. Since i_{pri2} maintains negative value as mentioned above, the ZVS can be achieved in light load condition for center-leg switches. And also, ZVS condition can be achieved for lagging-leg switches [26].

For lagging-leg switches, the worst point of ZVS condition is non-ZVS region shown in Fig. 6(b). For center-leg switches, ZVS is barely achieved in lower load. The dead time is controlled as per the following equations:

$$I_{\mathrm{o}} < \frac{V_{\mathrm{IN}}}{nL_{m2}}\left(D_{\mathrm{eff2}}T_{\mathrm{s}} - \frac{2\pi}{\sqrt{1/2L_{lk2}C_{\mathrm{oss}} + 1/4L_{lk2}n^2C_{\mathrm{j}}}}\right) \tag{17}$$

$$I_{\mathrm{o}} < \frac{V_{\mathrm{IN}}}{n\left(L_{m1}+L_{m2}\right)} \left(D_{\mathrm{eff1}}T_{\mathrm{s}} - \frac{2\pi}{\sqrt{1/2L_{eq}C_{\mathrm{oss}} + 1/4L_{eq}n^2C_{\mathrm{j}}}}\right). \tag{18}$$

If the condition is satisfied, the dead time should be increased. However, the dead time has limitation as follows: $T_{\mathrm{DT2}} < T_{\Phi}$, $T_{\mathrm{DT3}} < 0.5T_s - 2T_{\Phi}$.

TABLE I
COMPARISON OF COMPONENT COUNTS

	Proposed converter	Single PSFB converter	Interleaved or Parallel PSFB converter
Switches	6	4	8
Rectifier Diodes	4	4	8
Transformers	2	1	2
Output Inductors	2	1	2
Resonant Inductors	1	1	2
Total	15	11	22

E. Component Counts

In the condition that the converter handles high power over 6.6 kW, the interleaved or parallel PSFB converter is commonly used. In the conventional converter, two external inductors are required for wide ZVS operation of lagging-leg switches in each full-bridge inverter circuit. However, the soft switching energy is obtained from one external inductor in the proposed converter as aforementioned. Moreover, the primary-side is integrated so that it can reduce the number of switches, and the number of rectifier diodes is equal to the single PSFB converter. Therefore, the less number of components are used in the proposed converter. The comparison of component counts is summarized in Table I.

IV. Design Considerations

A. Component Design

The required turns-ratio for transformer can be designed with the equation of dc conversion ratio and delay time. Based on those equations, the equation of turns-ratio is expressed as follows:

$$n = \frac{\mathrm{DV_{IN}} \pm \sqrt{\left(\mathrm{DV_{IN}}\right)^2 - I_{\mathrm{o}}f_{\mathrm{s}}L_{lk,\mathrm{total}}V_{\mathrm{o}}}}{I_{\mathrm{o}}f_{\mathrm{s}}L_{lk,\mathrm{total}}} \tag{19}$$

where $D = 0.5 - T_{\phi}/T_{\mathrm{s}}$.

The design of switches and diodes are based on the voltage and current stresses. In case of primary switches, the voltage stress is equal to input voltage, and current stress of Q_3 and Q_4 is nI_o and the others are a half of it.

The clamping diodes reduce voltage ringing on upper side diodes of rectifier, D_{o1} and D_{o4}, by regenerating the ringing energy. For the other two diodes, RCD clamp circuit is used.

It is typical that the output capacitor is designed as per the consideration of voltage ripple. However, the current ripple is the key factor to design the output capacitor of converter with high output current. In the proposed converter, the ripple can be calculated as follows:

$$i_{Co,\mathrm{rms}} = \frac{\Delta I_{Lo1} + \Delta I_{Lo2}}{2}. \tag{20}$$

The design of output inductor can be done with the equation expressed as follows:

$$L_o = \frac{V_oT_s}{\Delta I_{Lo}}\left(1 - \frac{V_{\mathrm{o}}}{nV_{\mathrm{IN}}}\right). \tag{21}$$

The current ripple (ΔI_{Lo}) is the main factor of optimal design.

TABLE II
PROTOTYPE COMPONENT LIST

Component	Description
Switches ($Q_1 - Q_6$)	IPP60R074C6 (600 V, 31.6 A)
Rectifier diodes ($D_{o1} \sim D_{o4}$)	IDH15S120 (1200 V, 15A, $V_f = 2.5$ V)
Transformers (T_1, T_2)	Core : EE7066 Turns-ratio (n) : 1.33
	For T_1, For T_2
	L_{m1} : 2.35 mH L_{m2} : 2.35 mH
	L_{lk1} : 7.6 μH L_{lk2} : 7.6 μH
External inductor ($L_{\rm ext}$)	8.8 μH, MPP core (229060, 2 ea)
Output inductor (L_{o1}, L_{o2})	250 μH, HF core (330060, 3 ea)
Output capacitor (C_o)	270 uF/450 V
Controller	TMS320F28069

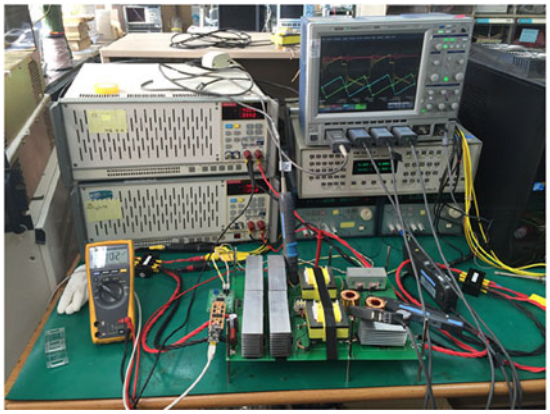

Fig. 9. Photograph of the experiment setup.

B. Relation Between ZVS Condition and Output Inductor

In this section, the ZVS condition of the switch Q_5 on lagging leg will be mainly discussed, thus the analysis is performed in Mode 4. As aforementioned, the reflected current becomes higher in very light load condition because the equation of reflected current ($I_{\rm ref}$) is as follows:

$$I_{\rm ref} = \frac{n\,|I_o - \Delta I_{Lo2}|}{2}. \tag{22}$$

Based on the design of output inductor, the magnitude of ripple is settled by the inductance of output inductor. Therefore, the reflected current can be decided by circuit design.

When the reflected current is equal to zero, namely the current ripple of i_{Lo2} is the same as output current, the magnetizing current is only source for achieving ZVS condition. During Mode 4, the magnetizing current has peak value so it is in proportion with duty cycle.

From the above, the relation between ZVS condition and primary current can be drawn as Fig. 6. In order to achieve ZVS condition in whole load range, i_{Lm} current should be higher than $I_{\rm ZVS,required}$ which is expressed as follows:

$$I_{\rm ZVS,required} = V_{\rm IN}\sqrt{\frac{2C_{\rm oss}}{L_{\rm ext} + L_{lk2}}}. \tag{23}$$

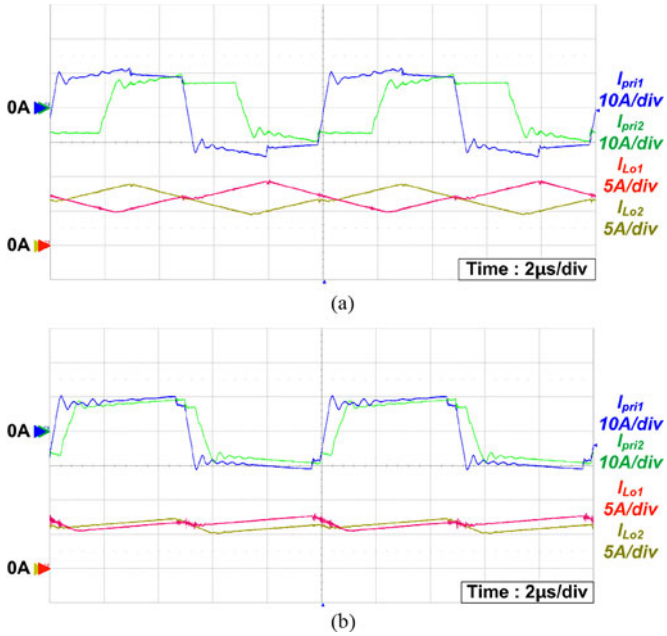

Fig. 10. Operation waveforms of proposed converter with load-share (a) at $Vo = 250$ V and $Io = 13.5$ A, and (b) at $Vo = 420$ V and $Io = 13.5$ A.

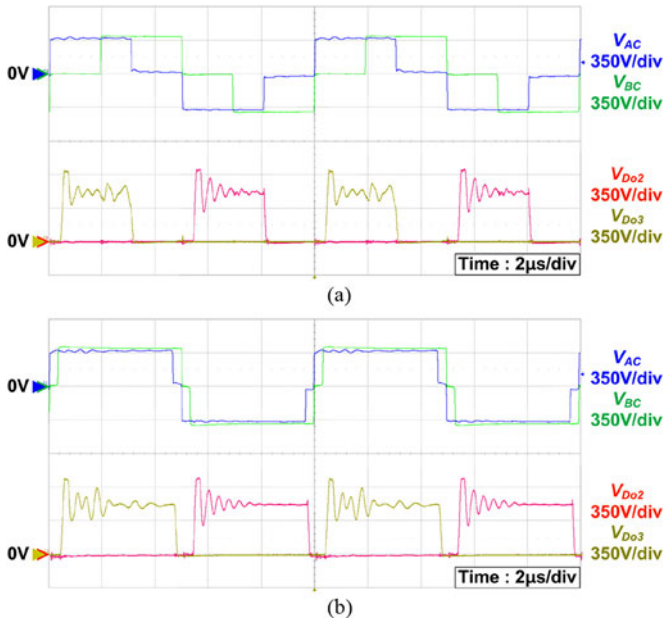

Fig. 11. Primary voltage of transformers and rectifier voltage (a) at $Vo = 250$ V, and (b) at $Vo = 420$ V.

Based on the analysis of magnetizing current and reflected current, primary current equation can be expressed as follows:

$$I_{\rm pri2} = 0.5nI_{\rm o} + \frac{A}{L_{m2}} + \frac{B}{L_{\rm o}} \tag{24}$$

where $A = \frac{D_{\rm eff2}T_{\rm s}V_{\rm IN}}{2}$, and $B = \frac{V_{\rm o}T_{\rm s}}{2}\left(n + \frac{V_{\rm o}}{V_{\rm IN}}\right)$.

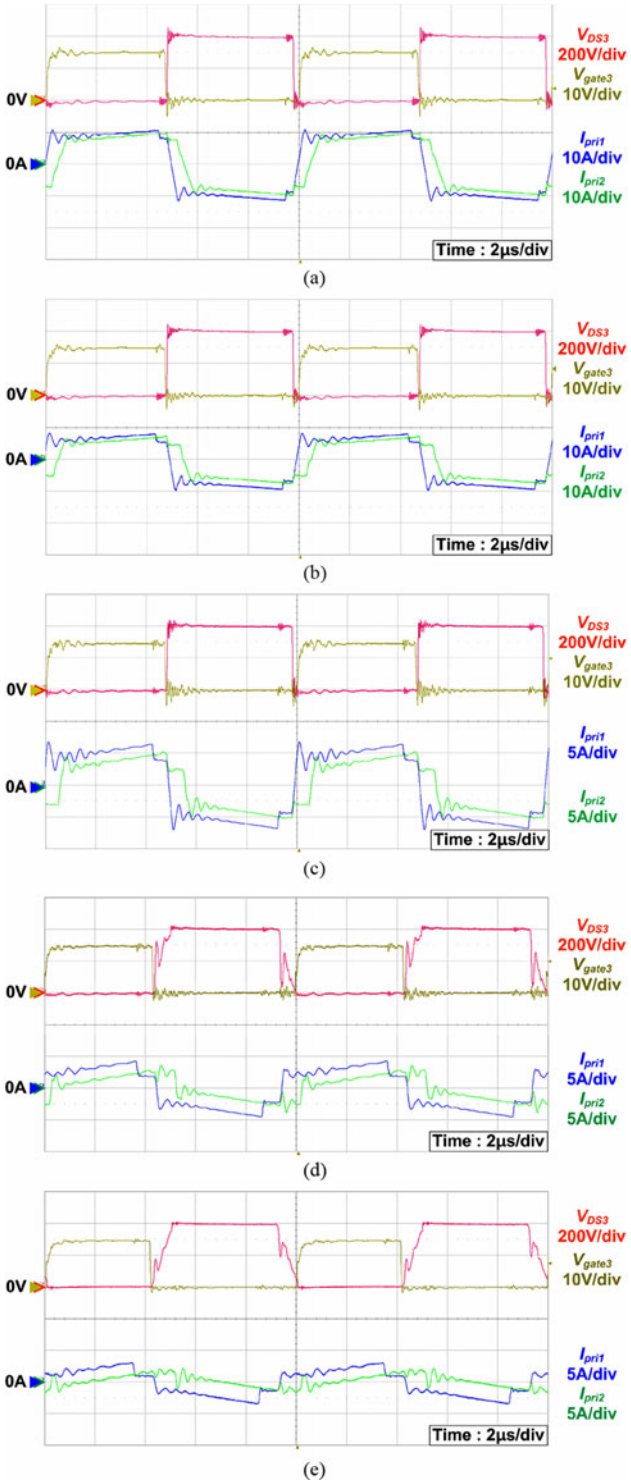

Fig. 12. ZVS operation of center-leg switches, $Q3$ and $Q4$ at (a) 100%, (b) 75%, (c) 50%, (d) 25%, (e) 10% load condition.

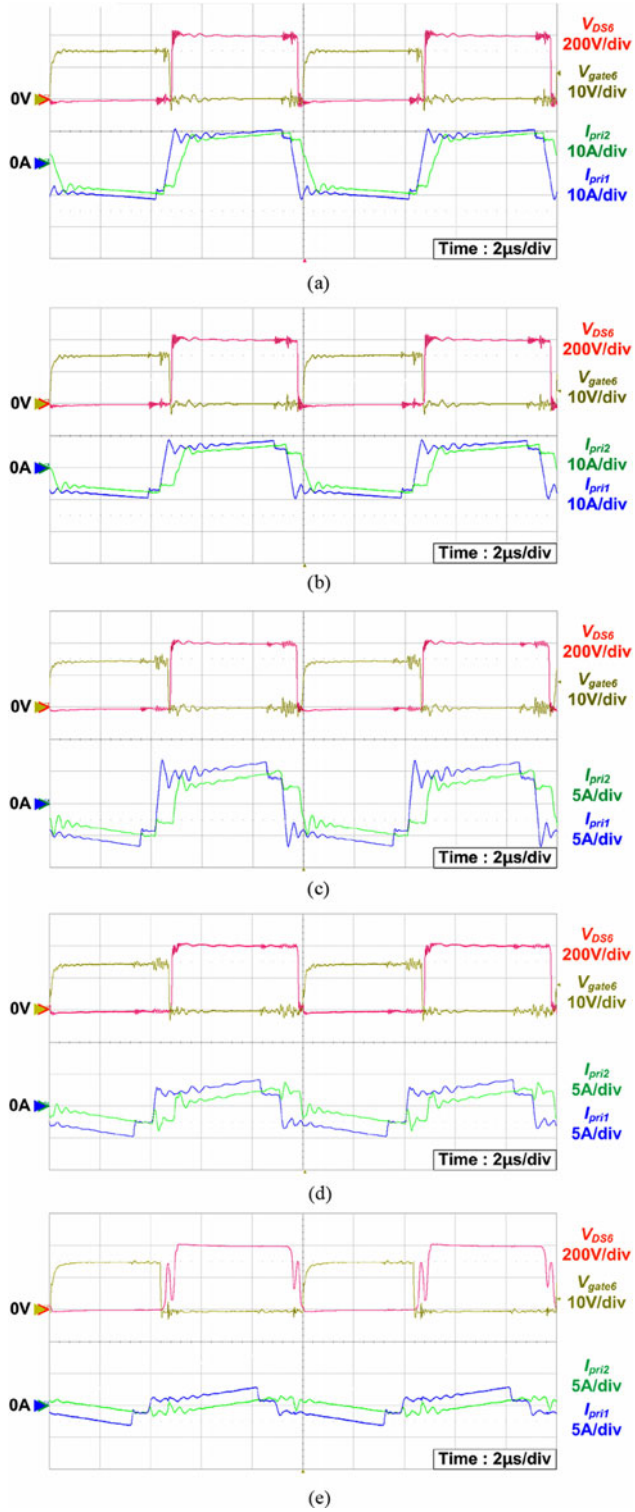

Fig. 13. ZVS operation waveforms of lagging-leg switches, $Q5$ and $Q6$, at (a) 100%, (b) 75%, (c) 50%, (d) 25%, (e) 10% load condition.

V. Experimental Results

In order to verify the effectiveness of the proposed converter, the prototype with 5.7 kW is realized with the battery charger specification given below:

1) Input voltage (V_{IN}) 385 V
2) Output voltage (V_o) 250–420 V
3) Maximum output current ($I_{o,\max}$) 13.5 A
4) Switching frequency (f_s) 100 kHz
5) ZVS range Full-load to 25% load

The prototype converter for the experiment was built using the components listed in Table II, and the photograph of the experiment setup is shown in Fig. 9.

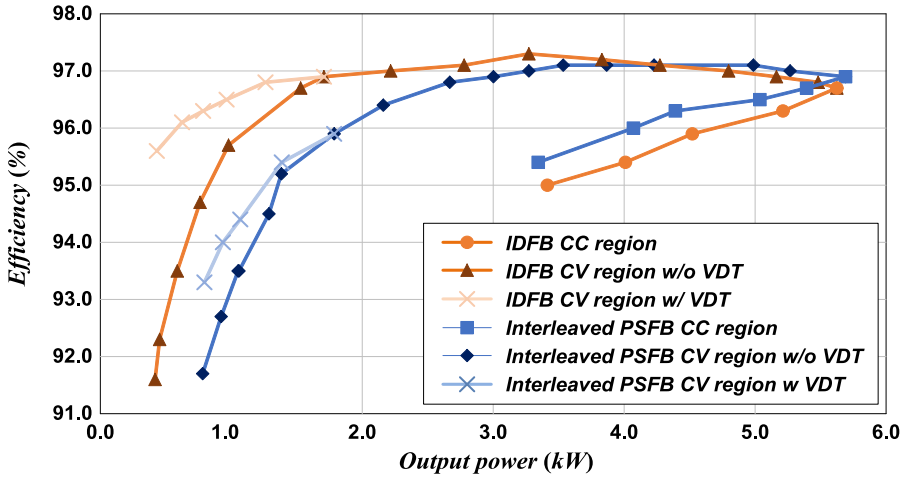

Fig. 14. Measured efficiency of the proposed converter.

Although the smaller external inductor is adopted, the proposed converter can achieve wider ZVS operation range than the conventional PSFB converter. The transformer turns-ratio and filter inductors were designed as per the procedure outlined in Section IV. The magnetizing inductance and external inductor are designed to have ZVS characteristic until 10% load. In order to alleviate the voltage ringing problem of rectifier diodes, clamp diode circuit and RCD snubber circuit are employed in the secondary side ($R = 100$ kΩ/10 W, $C = 33$ nF, $D =$ ES1M).

The conventional PSFB converters built for the comparison have ZVS range with 50–100% of full load. This is because it needs a very large resonant inductor to ensure the ZVS operation under light load condition.

Fig. 10 shows the primary currents and output inductor currents during constant current (CC) charging mode. From the primary current waveforms, the proposed converter well operates with phase-shift manner. Also, the output inductor currents show that load-share operation is properly performed without other technique.

Fig. 11 shows the voltage between two inverter legs and voltage stress of rectifier diodes, corresponding to the minimum and maximum output voltage. To charge the battery, the controller changes phase delay as shown in this figure. Also, the diode voltage is clamped under 830 V as designed.

Figs. 12 and 13 show the gate-to-source and drain-to-source voltages of center-leg and lagging-leg switches, respectively.

As seen, the drain-to-source voltage reduces to zero level before gate voltage reaches threshold, demonstrating ZVS turn-on. At higher load condition, ZVS is achieved easily.

The efficiency curves versus output power for charging the battery are shown in Fig. 14. The figure shows the efficiency when the proposed and conventional interleaved converters operate in CC and CV region. At light load region defined in Fig. 2, the proposed converter has higher efficiency than conventional one.

With VDT control method, the efficiency can be improved and it maintains over 95%. Under heavy load condition, conventional converter has a little higher efficiency due to conduction power loss. However, it can be said that the proposed converter is more suitable for high power applications in terms of efficiency and the number of components than single PSFB or interleaved (or parallel) PSFB converters.

VI. Conclusion

In this paper, a soft-switching dc–dc converter topology for high-power on-board charger with the capacity of over 6.6 kW has been proposed. It is based on the integration of dual full-bridge converter. In the rectifier stage, two CDR circuits are integrated by sharing inductors. The operating principles and the ZVS characteristics of the proposed converter are analyzed for EV charger applications. Experimental results were obtained from a 5.7 kW (13.5 A) prototype converting from the input dc link of 385 V to an output voltage range of 250–420 V. The efficiency is higher than 95% in whole output power range, and it achieves 97.3% peak efficiency. The main features of the proposed circuit are summarized as follows:

1) less component counts than interleaved or parallel PSFB converter, only six switches and one external inductor;
2) wide ZVS range with VDT control scheme, and with its reflected current from output inductor;
3) less duty-cycle loss due to only one external inductor and small inductance of it; and
4) output load-share on output filter inductors without specific control.

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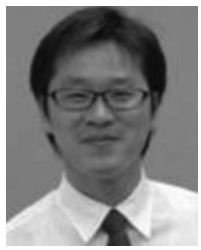

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