Full-Range Soft-Switching-Isolated Buck-Boost Converters With Integrated Interleaved Boost Converter and Phase-Shifted Control

Hongfei Wu, *Member, IEEE*, Tiantian Mu, Hongjuan Ge, and Yan Xing, *Member, IEEE*

***Abstract*—A new method for deriving isolated buck-boost (IBB) converter with single-stage power conversion is proposed in this paper and novel IBB converters based on high-frequency bridgeless-interleaved boost rectifiers are presented. The semiconductors, conduction losses, and switching losses are reduced significantly by integrating the interleaved boost converters into the full-bridge diode-rectifier. Various high-frequency bridgeless boost rectifiers are harvested based on different types of interleaved boost converters, including the conventional boost converter and high step-up boost converters with voltage multiplier and coupled inductor. The full-bridge IBB converter with voltage multiplier is analyzed in detail. The voltage multiplier helps to enhance the voltage gain and reduce the voltage stresses of the semiconductors in the rectification circuit. Hence, a transformer with reduced turns ratio and parasitic parameters, and low-voltage rated MOSFETs and diodes with better switching and conduction performances can be applied to improve the efficiency. Moreover, optimized phase-shift modulation strategy is applied to the full-bridge IBB converter to achieve isolated buck and boost conversion. What's more, soft-switching performance of all of the active switches and diodes within the whole operating range is achieved. A 380-V output prototype is fabricated to verify the effectiveness of the proposed IBB converters and its control strategies.**

***Index Terms*—Bridgeless rectifier, dc–dc converter, interleaved boost converter, isolated buck-boost (IBB) converter, soft-switching.**

I. Introduction

ISOLATED dc–dc converters are widely required in various applications to meet the requirements of input/output voltage range and galvanic isolation. Generally speaking, isolated converters can be classified into three categories: buck converters [1]–[3], boost converters [4]–[6], and buck-boost converters [7]–[9]. Voltage step-down can be implemented with an isolated buck converter, and the efficiency decreases with the decreasing of the voltage conversion ratio. Contrarily, voltage step-up is achieved with an isolated boost converter, and the efficiency decreases with the increasing of the voltage conversion ratio. Therefore, the isolated buck or boost converters are not flexible in terms of conversion efficiency and voltage range [8], [9]. Take the maximum power point tracking converters for renewable power generation systems as an example. Since the open-circuit voltage of renewable sources, such as photovoltaic [10], fuel-cell [11], and thermoelectric generator [12], is much higher than the maximum power point voltage, the highest conversion efficiency is usually achieved at the open-circuit voltage if an isolated boost converter is employed. In this case, high efficiency at the maximum power point, which is very important for the renewable power system, cannot be ensured. For the applications of battery charging and discharging [1], [13], high conversion efficiency over the entire operating range is needed. Therefore, achieving high-efficiency power conversion in a wide-voltage range is an important research topic, especially for the power systems that are sourced by batteries and renewable energy sources.

From the view of conversion efficiency, an isolated buck-boost (IBB) converter would be a promising approach. Unfortunately, in the past decades, a lot of work has been done for the isolated buck and boost converters, but the research on the IBB converters is still insufficient. The flyback converter is a typical IBB converter [14], but the efficiency is still lower because of the high voltage/current stresses on components and hard-switching of the active switch and rectifying diode. In fact, an IBB converter is an isolation version of a corresponding nonisolated buck-boost converter. Therefore, an IBB converter can be derived easily by inserting a transformer into a nonisolated buck-boost converter, for example the Cuk, SEPIC, and ZETA converters. However, similar to the flyback converter, the isolated Cuk [15], ZETA [16], and SEPIC [17] converters still suffer from the disadvantages of high component stress, hard-switching, and low efficiency. Moreover, these single-switch IBB converters can be used only in small-power applications. For nonisolated buck-boost conversion, the two-switch buck-boost converter shown in Fig. 1(a), which is composed by a buck cell, a boost cell, and an inductor, is an attractive and popular solution due to its flexible control and high efficiency[18]–[20]. Based on this topology, a family of IBB converters is derived in [8] by replacing the nonisolated buck cell in the nonisolated two-switch buck-boost converter with an isolated buck cell; the structure of the IBB converters presented in [8] is illustrated in Fig. 1(b). Although wide-voltage gain range with flexible control can be achieved, it should be noted that the conversion efficiency

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The authors are with the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: mutiantian@nuaa.edu.cn; allenge@nuaa.edu.cn; xingyan@nuaa.edu.cn; wuhongfei@nuaa.edu.cn).

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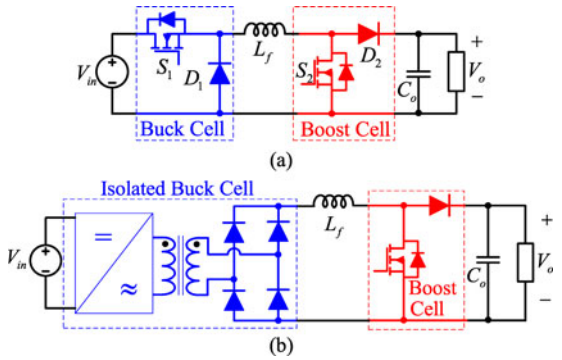

Fig. 1. (a) Nonisolated two-switch buck-boost converter. (b) IBB converters presented in [11].

will be hurt by the cascaded two-stage conversion architecture of Fig. 1(b) due to the additional conduction and switching losses. Moreover, the active switches and rectifying diodes on the secondary side of Fig. 1(b) are hard-switching, which has negative influence on the conversion efficiency as well. From the view of conversion efficiency, how to implement IBB converters with single-stage and soft-switching power conversion characteristics is an interesting and valuable research topic.

From Fig. 1(b), it can be seen that the secondary-side circuit of the cascaded IBB converter is very similar to a conventional boost power factor corrector [21], which is composed of a rectifying bridge and a nonisolated boost converter. In the research area of power factor correctors, it has been demonstrated that the rectifying bridge and the boost power factor correction circuit can be integrated to build a bridgeless power factor correction circuit topology, which features higher efficiency, less power loss, and component count [22], [23]. The research results of the bridgeless power factor correction circuit drop a hint that we may build an IBB converter featuring single-stage power conversion if the rectifying bridge and the nonisolated boost converter are merged in a cascaded IBB converter.

The major contribution of this paper is to propose novel IBB converters with single-stage power conversion based on integration of nonisolated-interleaved boost converters and isolated buck converters. Novel IBB converters are harvested. Moreover, optimized phase-shift modulation strategy is presented and applied to the proposed converter to achieve soft-switching operation of all of the switching devices within the entire operating range. This paper is organized as follows. In Section II, the basic ideas used to generate IBB converters are proposed. In Section III, the operational principles of a full-bridge IBB converter with presented optimized phase-shift modulation is analyzed in detail. The performance of this converter and design guidelines are presented in Sections IV and V, respectively. Experimental results are provided in Section VI. Finally, conclusions will be given in Section VII.

II. Derivation of the IBB DC/DC Converters

A. High-Frequency Bridgeless-Interleaved Boost Rectifier

As an example, a traditional two-phase-interleaved boost converter [24] cascaded with a full-bridge rectifier of an isolated buck converter, as shown in Fig. 2(a), is used to illustrate the integration concept. For simplicity, only the secondary-side circuit of the isolated buck converter is shown in Fig. 2(a). Referring to the circuit topology of the bridgeless power factor corrector [22], the interleaved boost converter and the high-frequency full-bridge diode rectifier can be integrated to build a bridgeless-interleaved boost rectifier, as shown in Fig. 2(b). Compared to the conventional cascaded topology shown in Fig. 2(a), four diodes have been removed, and the inductor current only flows through two semiconductors, resulting in reduced conduction losses. Moreover, the switching losses can be reduced as well with the bridgeless-interleaved boost rectifier shown in Fig. 2(b). It should be noted that L_{f_1} and L_{f_2} of Fig. 2(b) are both high-frequency inductors. The two high-frequency inductors can be merged into one inductor because they are always in series. Then, the final version of the bridgeless-interleaved boost rectifier is derived and shown in Fig. 2(c). The functions of the original full-bridge diode-rectifier and boost converter, rectification and regulation of the output voltage/power, can be realized with the integrated bridgeless-interleaved boost rectifier.

Following the integration concept illustrated in Fig. 2, almost all of the interleaved boost-type converters and high-frequency full-bridge diode–rectifier can be integrated to derive novel high-frequency bridgeless-interleaved boost-type rectifiers. For example, based on the interleaved boost converter with a voltage multiplier [25], as shown on the left-hand side of Fig. 3(a), a novel high-frequency bridgeless-interleaved boost rectifier with voltage multiplier can be derived and shown on the right-hand side of Fig. 3(a). Similarly, a high step-up boost rectifier with a coupled inductor, as shown in Fig. 3(b), can be derived based on the topology presented in [26]. Obviously, in comparison with the rectifier shown in Fig. 2(c), the bridgeless boost rectifiers shown in Fig. 3 are more suitable for high-output-voltage applications because the output voltage ratio can be enhanced with the help of voltage multiplier and coupled inductor. Moreover, the voltage stresses of the semiconductors and the turns ratio of transformers can be reduced significantly as well.

B. Novel IBB Converters

Based on the proposed bridgeless boost rectifiers, novel IBB converters can be derived by employing the input stage of an isolated buck converter as the primary-side circuit of the IBB converters. The primary-side circuit can be full-bridge, half-bridge, or three-level half-bridge, etc., as shown in Fig. 4. Since the focus of this paper is the boost rectifiers, only the IBB converter topologies with full-bridge input stage are shown in Fig. 5. Obviously, the input stage of the IBB converter is a buck-cell, the output stage is a bridgeless boost cell, and the two cells are linked by a high-frequency inductor and transformer. This structure is similar to the nonisolated two-switch buck-boost converter.

Although the concept of the high-frequency bridgeless boost rectifier is first presented in this paper, some of the derived topologies have been presented before. For example, the feasibility of the topology shown in Fig. 5(a) has been studied and verified in [27]. But, it should be noted that, this topology is only used as an isolated boost converter in [27], and

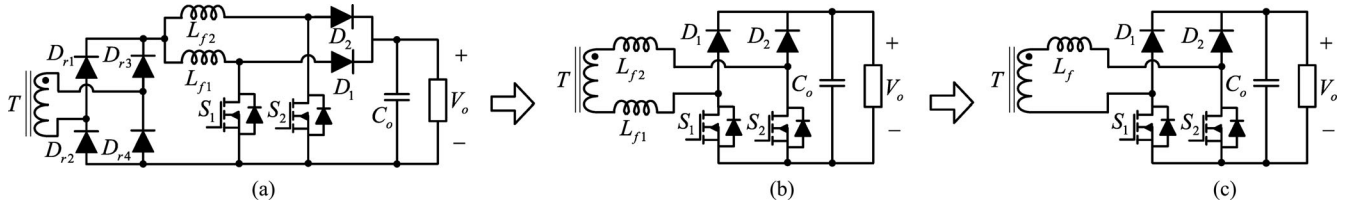

Fig. 2. (a) Interleaved boost converter cascading with a full-bridge rectifier. (b) High-frequency bridgeless-interleaved boost converter with two inductors. (c) High-frequency bridgeless-interleaved boost converter with one inductor.

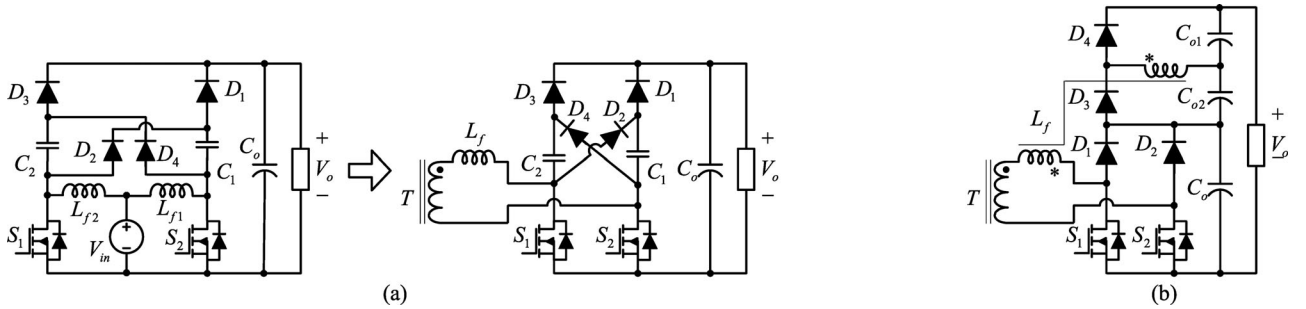

Fig. 3. (a) Bridgeless boost rectifier derived from an interleaved boost converter with a voltage multiplier. (b) High step-up bridgeless boost rectifier with a coupled inductor.

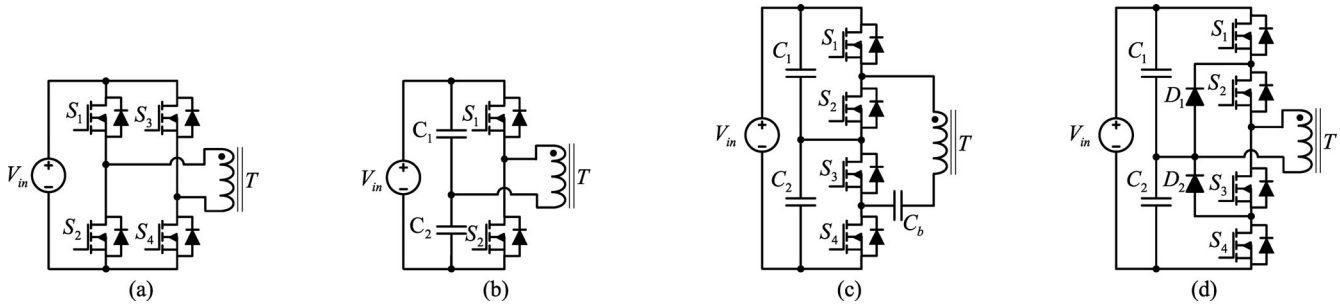

Fig. 4. Primary-side circuits of isolated buck converters: (a) full-bridge, (b) half-bridge, and (c) and (d) three-level.

soft-switching within the full operating range cannot be achieved by only employing secondary-side phase-shift control. Because the operation principles, control strategy, and performance of these IBB converters are similar with each other, the full-bridge IBB converter with voltage-multiplier (FB-IBB–VM), as shown in Fig. 5(b), with optimized phase-shift control strategy will be analyzed in the following sections to validate the feasibility and advantages of the proposed converters.

III. Operational Principles of the Proposed FB-IBB Converter

The FB-IBB converter taken as an example to be analyzed is redrawn in Fig. 6. v_{DS1}, v_{DS4}, and v_{DS6} are the drain to source voltages of S_1, S_4, and S_6, respectively. ν_{NP} and v_{S56} are the voltages of the primary side and secondary side of the transformer. And i_{Lf} is the current flowing through the inductor L_f. A proper dead-time is necessary for the primary-side switches to achieve ZVS and avoid shot-through of the switching bridges, but dead-time is not needed for the secondary-side switches S_5 and S_6. To simplify the analysis, the parasitic capacitance of the MOSFET is ignored.

The normalized voltage gain *G* is defined as

$$G = \frac{NV_o}{2V_{\text{in}}} \tag{1}$$

where V_{in}, V_o, and *N* are the input voltage, output voltage, and transformer turns ratio n_P/n_S, respectively. The secondary-side phase-shift angle φ is defined as the phase difference between S_6 gate signal and S_4 gate signal. Because this phase shift serves the same function as duty cycle in the PWM converter, we define duty cycle D_s as

$$D_s = \frac{\varphi}{\pi}. \tag{2}$$

And the primary-side phase-shift angle α is defined to be the phase difference between the gate signals of S_1 and S_3. So, the duty cycle D_p is defined as

$$D_p = \frac{\alpha}{\pi}. \tag{3}$$

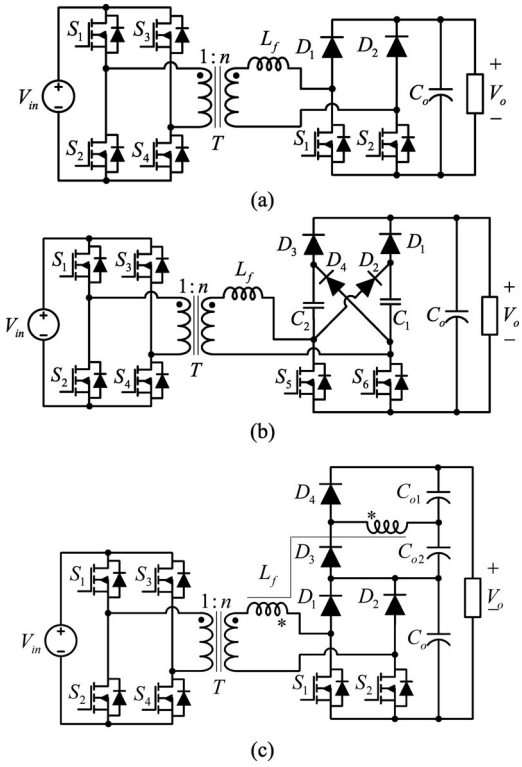

Fig. 5. Novel full-bridge IBB converters with (a) bridgeless boost rectifier, (b) bridgeless boost rectifier with voltage multiplier, and (c) bridgeless boost rectifier with a coupled inductor.

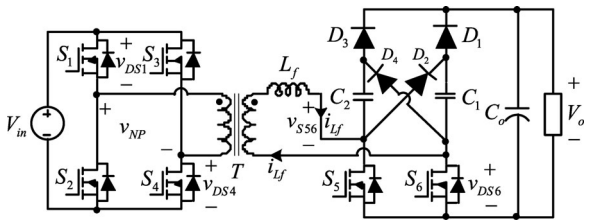

Fig. 6. Proposed FB-IBB converter.

The converter can work either in the buck mode ($G < 1$) or the boost mode ($G \geq 1$). According to the waveform of the secondary-side current i_{Lf}, each operation mode can be further divided into continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

A. Boost-CCM Operation

In the boost mode, the primary-side MOSFETs S_1 and S_4, and S_2 and S_3 conduct simultaneously which means $D_p = 1$. The secondary-side phase-shift angle is employed to regulate the output power. If the primary-side switches commute before the secondary-side current decreases to zero, the converter operates in the boost-CCM mode. The key waveform of this mode is shown in Fig. 7, where D_0 is defined as the equivalent duty cycle during which the inductor current returns to zero after the primary side switches turn OFF, and T_S is the switching period. There are eight stages in one switching period. Due to

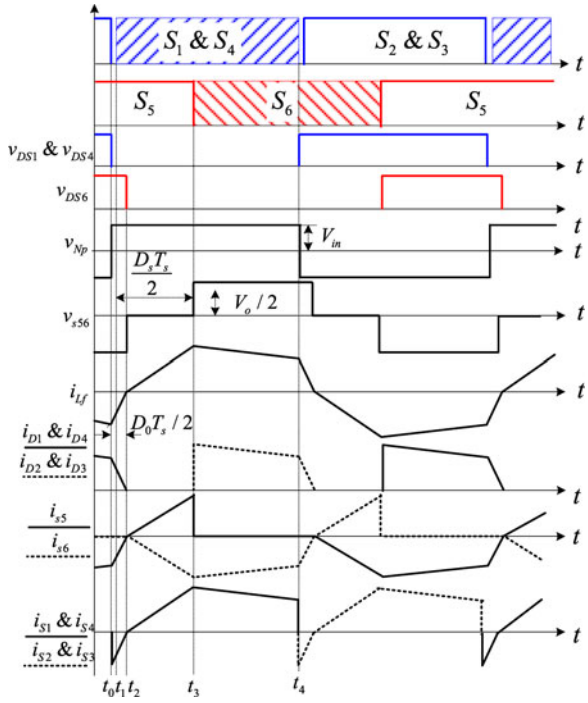

Fig.7. Key waveform of the proposed converter in the boost- CCM mode.

the symmetry of the circuit, only four stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 8.

Stage 1—[t_0, t_1] [see Fig. 8(a)]: Before t_0, S_2, S_3, S_5, D_1 and D_4 are ON. On the secondary side, S_5, D_1 and C_1 make up for one current loop, while D_4 and C_2 make up for another one. At t_0, S_2 and S_3 turn OFF. Body diodes of S_1 and S_4 begin to conduct due to the energy stored in L_f, which results in ZVS of S_1 and S_4. Due to the negative voltage across L_f, the current i_{Lf} decreases rapidly

$$i_{Lf}(t) = i_{Lf}(t_0) + \frac{\mathrm{V}_o/2}{L_f}(1/G + 1)(t - t_0). \tag{4}$$

Stage 2—[t_1, t_2] [see Fig. 8(b)]: At t_1, S_1 and S_4 are turned ON with ZVS. This stage ends when i_{Lf} returns to zero, and D_1 and D_4 are OFF naturally without reverse recovery.

Stage 3—[t_2, t_3] [see Fig. 8(c)]: At t_2, i_{Lf} returns to zero. The body diode of S_6 begins to conduct and L_f is charged by the input voltage

$$i_{Lf}(t) = i_{Lf}(t_2) + \frac{V_o/2}{GL_f}(t - t_2). \tag{5}$$

Stage 4—[t_3, t_4] [see Fig. 8(d)]: At t_3, S_5 turns OFF, and S_6 turns ON with ZVS. D_2 and D_3 are ON and the power is transferred to the load during this stage

$$i_{Lf}(t) = i_{Lf}(t_3) + \frac{V_o/2}{L_f}(1/G - 1)(t - t_3). \tag{6}$$

At the end of this stage, i_{Lf} has the same absolute value but in the reverse direction as that in the beginning of Stage 1, which

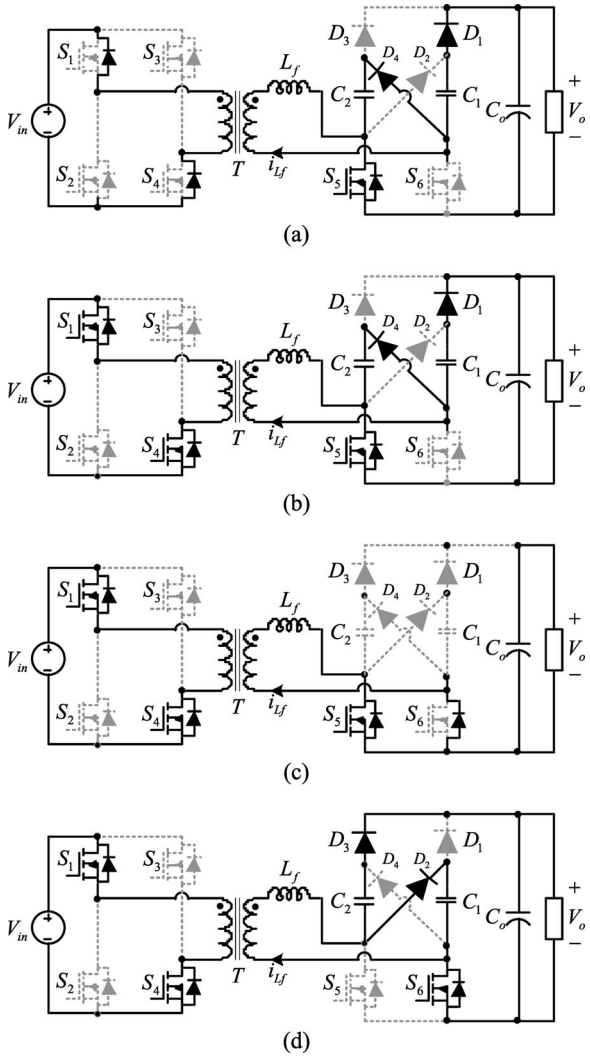

Fig. 8. Equivalent circuits for each operation stage in the boost-CCM mode: (a) Stage 1 $[t_0, t_1]$, (b) Stage 2 $[t_1, t_2]$, (c) Stage 3 $[t_2, t_3]$, and (d) Stage 4 $[t_3, t_4]$.

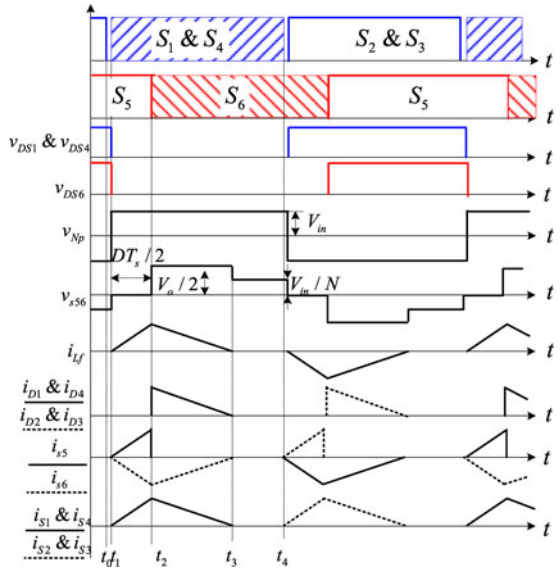

Fig.9. Key waveform of the proposed converter in the boost-DCM mode.

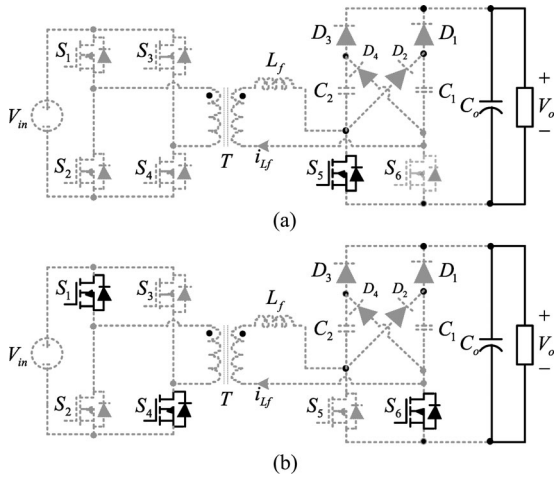

Fig. 10. Equivalent circuits for each operation stage in the boost-DCM mode: (a)Stage 1 $[t_0, t_1]$ and (b) Stage 4 $[t_3, t_4]$.

is expressed as

$$i_{Lf}(t_4) = -i_{Lf}(t_0). \tag{7}$$

A similar operation works in the rest stages of a switching period.

B. Boost-DCM Operation

In the boost mode, if the secondary-side current has decreased to zero before the primary-side switches commutate, the converter enters the boost-DCM operation. The key waveform of the converter operating in the boost-DCM mode is shown in Fig. 9. There are also eight stages in one switching period. Due to the symmetry of the circuit, only four stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 10.

Stage 1—$[t_0, t_1]$ [see Fig. 10(a)]: Before t_0, S_2, S_3, and S_5 are ON. Since $i_{Lf} = 0$, there is no energy transferred between the input and output. At t_0, S_2 and S_3 turn OFF with zero voltage and zero current.

Stage 2 $[t_1, t_2]$ and Stage 3 $[t_2, t_3]$: At t_1, S_1 and S_4 are turned ON with ZCS. The operation principles of Stages 2 and 3 of the boost-DCM mode are the same as that of the Stages 3 and 4, respectively, in the boost-CCM mode.

Stage 4—$[t_3, t_4]$ [see Fig. 10(b)]: At t_4, i_{Lf} reaches zero. i_{Lf} will stay in the zero state in this stage and there is no energy transferred between the input and output.

A similar operation works in the rest stages in a switching period.

C. Buck-CCM Operation

In the buck mode, a dual-phase-shift control scheme is employed. In the buck-CCM mode, the primary phase-shift angle α is fixed and the phase-shift angle between the primary- and

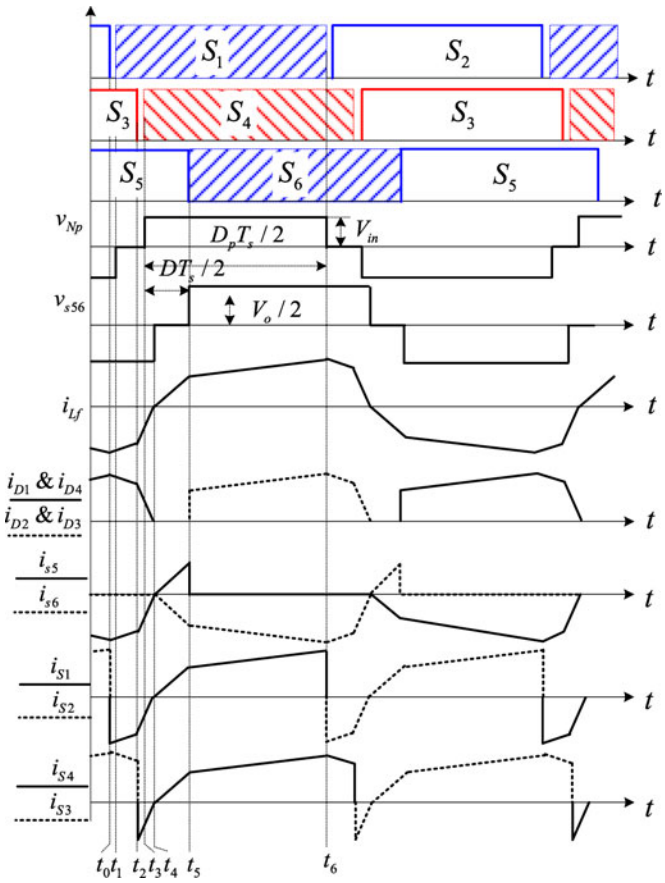

Fig. 11. Key waveform of the proposed converter in the buck-CCM mode.

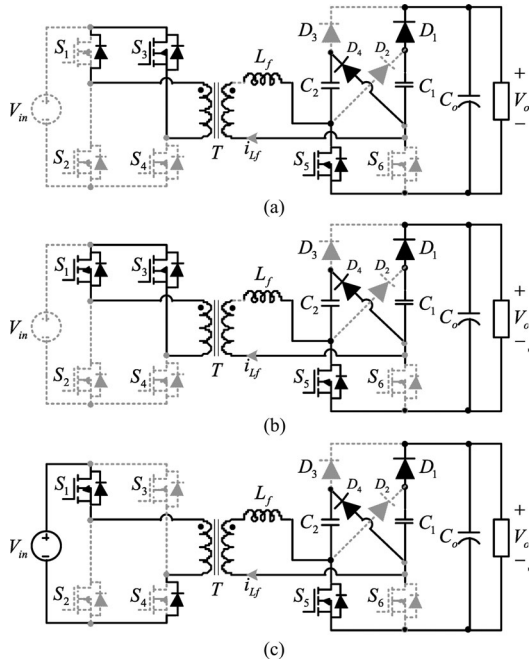

Fig.12. Equivalent circuits for each operation stage in the buck-CCM mode: (a) Stage 1 $[t_0, t_1]$, (b) Stage 2 $[t_1, t_2]$, and (c) Stage 3 $[t_2, t_3]$.

secondary-side MOSFETs φ is employed to regulate the output power and voltage. The key waveform is shown in Fig. 11. There are twelve stages in one switching period. Due to the symmetry of the circuit, only six stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 12.

Stage 1—[t_0, t_1] [see Fig. 12(a)]: Before t_0, S_2, S_3, S_5, D_1 and D_4 are ON. At t_0, S_2 turns OFF. The body diode of S_1 begins to conduct due to the energy stored in L_f, which results in ZVS of S_1. The energy stored in L_f is delivered to the output

$$i_{Lf}(t) = i_{Lf}(t_0) + \frac{V_o/2}{L_f}(t - t_0). \tag{8}$$

Stage 2—[t_1, t_2] [see Fig. 12(b)]: At t_1, S_1 is turned ON with ZVS. This stage ends when S_3 turns OFF.

Stage 3—[t_2, t_3] [see Fig. 12(c)]: At t_2, S_3 turns OFF. The body diode of S_4 begins to conduct. Due to the negative voltage across the inductor, the current i_{Lf} decreases rapidly

$$i_{Lf}(t) = i_{Lf}(t_2) + \frac{V_o/2}{L_f}(1/G + 1)(t - t_2). \tag{9}$$

Stage 4 [t_3, t_4], Stage 5 [t_4, t_5], and Stage 6 [t_5, t_6]: At t_3, S_5 turns OFF, S_6 is turned ON with ZVS. The operating principle of this state is the same as that of Stage 2 in the boost-CCM mode, whereas the operating principles of Stages 5 and 6 of the buck-CCM mode are the same as that of the Stages 3 and 4, respectively, in the boost-CCM mode.

At the end of this stage, i_{Lf} has the same absolute value but in the reverse direction as that in the beginning of Stage 1. A similar operation works in the rest stages of a switching period.

D. Buck-DCM Operation

When φ decreases to zero, the converter enters in the buck-DCM mode, in which φ is fixed at zero while α begins to decrease. In order to achieve ZVS of the secondary-side MOSFETs, a dead-time between the primary-side and the secondary-side MOSFETs is needed. The key waveform is shown in Fig. 13. There are twelve stages in one switching period. Due to the symmetry of the circuit, only six stages are analyzed here and corresponding equivalent circuits for each operation stage are shown in Fig. 14.

Stage 1 [t_0, t_1] and Stage 2 [t_1, t_2]: Before t_0, S_2, S_3, S_5, D_1 and D_4 are ON. At t_0, S_2 turns OFF. The operating principles of Stages 1 and 2 of the buck-DCM mode are the same as that of the Stages 1 and 2, respectively, in the buck-CCM mode.

Stage 3—[t_2, t_3] [see Fig. 14(a)]: At t_2, i_{Lf} reaches zero. i_{Lf} will stay in the zero state in this stage and there is no energy transferred between the input and output.

Stage 4—[t_3, t_4] [see Fig. 14(b)]: At t_3, S_5 and S_3 turn OFF.

Stage 5—[t_4, t_5] [see Fig. 14(c)]: At t_4, S_4 turns ON. L_f is charged by the input voltage

$$i_{Lf}(t) = i_{Lf}(t_2) + \frac{V_o/2}{GL_f}(t - t_2). \tag{10}$$

Stage 6—[t_5, t_6]: At t_5, S_6 turns ON. The operating principle of this stage is the same as that of the Stage 4 in the boost-CCM mode.

A similar operation works in the rest stages of a switching period.

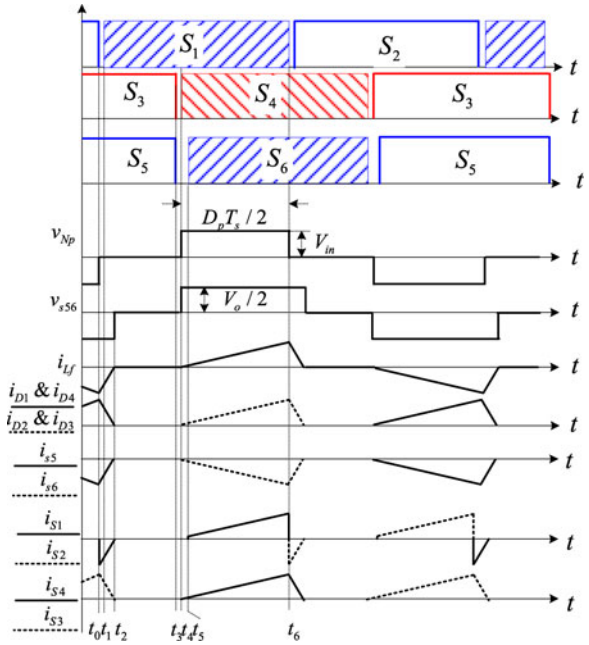

Fig. 13. Key waveform of the proposed converter in the buck-DCM mode.

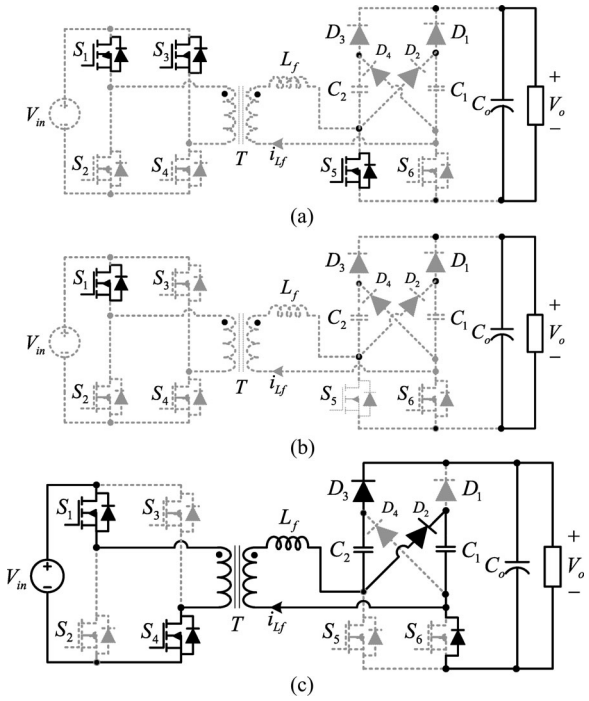

Fig. 14. Equivalent circuits for each operation stage in the buck-DCM mode: (a) Stage 3 $[t_2, t_3]$, (b) Stage 4 $[t_3, t_4]$, and (c) Stage 5 $[t_4, t_5]$.

IV. Performance Analysis and Discussion

A. Soft-Switching Performance

According to the operating principles of different modes, the ZVS performance of the active switches will be analyzed in this section.

When the converter operates in the boost mode, ZVS turn-on can always be achieved for the secondary-side switches, because the operation of the secondary-side switches is the same as that of a synchronous rectifier. The direction of the current flowing through the secondary-side switches is negative before and after the driving voltage applied to the switches. Besides, ZCS soft-switching of rectifier diodes can be always obtained because the diode current decreases to zero naturally. For the primary-side switches, ZVS turn-on can be achieved in the CCM mode because their body diodes conduct before the gate signal thanks to the reverse current. But, once the converter enters the DCM mode, the ZVS performance is lost and ZCS can be achieved for the primary-side switches.

In the buck-CCM mode, the ZVS turn-on of all the MOSFETs can be achieved when the current of the inductor meets the following requirements:

$$\begin{cases} i_{Lf}(t_1) < 0 & S_1 - S_2 \\ i_{Lf}(t_3) < 0 & S_3 - S_4 \\ i_{Lf}(t_5) > 0 & S_5 - S_6 \end{cases} \tag{11}$$

in which the current value can be calculated according to (1)–(9) and expressed as follows:

$$\begin{cases} i_{Lf}(t_1) = -\dfrac{V_o}{4fL_f}\dfrac{D_p - (D_p - D_s)G^2 + (1 + D_s - D_p)G}{2G + G^2} \\ i_{Lf}(t_3) = -\dfrac{V_o}{4fL_f}\dfrac{D_p - (1 - D_s)G^2 + (1 + D_s - D_p)G}{2G + G^2} \\ i_{Lf}(t_5) = \dfrac{V_o}{4fL_f}\dfrac{2D_s - D_p + G}{2G + G^2} \end{cases} \tag{12}$$

where f is the switching frequency. According to (11) and (12), the range of duty cycle for ZVS can be inferred

$$\begin{cases} D_s > \dfrac{1}{2}[D_p - G] \\ D_s > 1 - \dfrac{1}{G} + (1 - D_p)\dfrac{1}{G} \end{cases}. \tag{13}$$

According to (13), it is obvious that if $D_p = G$, the ZVS turn-on of all the MOSFETs can be always achieved, because D_s always satisfies $D_s > 0$ when the converter operates in the buck-CCM mode.

In the buck-DCM mode, the ZVS turn-on of the primary-side MOSFETs in the leading leg and the secondary-side MOSFETs can be achieved and the ZCS turn-on of the primary-side MOSFETs in the lagging leg can also be obtained.

Based on the analysis above, the optimized primary-side duty cycle D_p is summarized as follows:

$$D_p = \begin{cases} G, & \text{if } (G < 1 \text{ and } \mathrm{D}_s > 0) \\ 1, & \text{if } (G \geq 1 \text{ and } \mathrm{D}_s > 0) \end{cases}. \tag{14}$$

With the optimized duty cycle and phase-shift control strategy, soft-switching of all of the switching devices can be

realized within the whole operating range. Moreover, ZVS turn-ON of the secondary-side switches can be always achieved in the entire operation range, because these switches always operate like a synchronous rectifier before and after applying driving voltages.

B. Output Characteristics

According to the operational analysis of the boost-CCM mode, the average input current can be given by

$$I_{\text{in}} = \frac{i_{Lf}(t_0)}{2} D_0 + \frac{i_{Lf}(t_3)}{2}(D_s - D_0) + \frac{i_{Lf}(t_3) + i_{Lf}(t_4)}{2}(1 - D_s). \tag{15}$$

Then, based on (1)–(7), the values of $i_{Lf}(t_0)$, $i_{Lf}(t_3)$, and D_0 can be derived as

$$\begin{cases} i_{Lf}(t_0) = \dfrac{V_o T_S}{4L_f} \dfrac{(1+G)[(1-D_s)G-1]}{G(G+2)} \\ i_{Lf}(t_3) = \dfrac{V_o T_S}{4L_f} \dfrac{2D_s+G-1}{G(G+2)} \\ D_0 = \dfrac{1+G(D_s-1)}{G+2} \end{cases}. \tag{16}$$

Ignoring the power losses, then, the output power can be derived as

$$P_o = V_{\text{in}} I_{\text{in}}. \tag{17}$$

From (1)–(6), the output power can be obtained as

$$P_{o\_\text{Boost-CCM}}(G, D_s) = \frac{V_o^2}{16 f L_f} \frac{(1+G-2G^2) + 4D_s(1+G+G^2) - 2D_s^2(2+2G+G^2)}{G(2+G)^2}. \tag{18}$$

In the boost-DCM mode, the analysis is similar while the current value is given as

$$i_{Lf}(t_2) = \frac{V_o}{4 f L_f} \frac{D_s}{G} \tag{19}$$

and the output power is

$$P_{o\_\text{Boost-DCM}}(G, D_s) = \frac{V_o^2}{16 f L_f} \frac{D_s^2}{G(G-1)}. \tag{20}$$

Letting $i_{Lf}(t_0) = 0$, the boundary between the boost-CCM mode and the boost-DCM mode can be obtained as

$$D_{B1} = \frac{G-1}{G}. \tag{21}$$

The same analysis process can be performed for buck-CCM and buck-DCM modes. The output power can be obtained as, Eq. (22) as shown at the bottom of the next page.

Based on the analysis, the output characteristics of the converter are depicted in Fig. 15 (the boost mode) and Fig. 16 (the

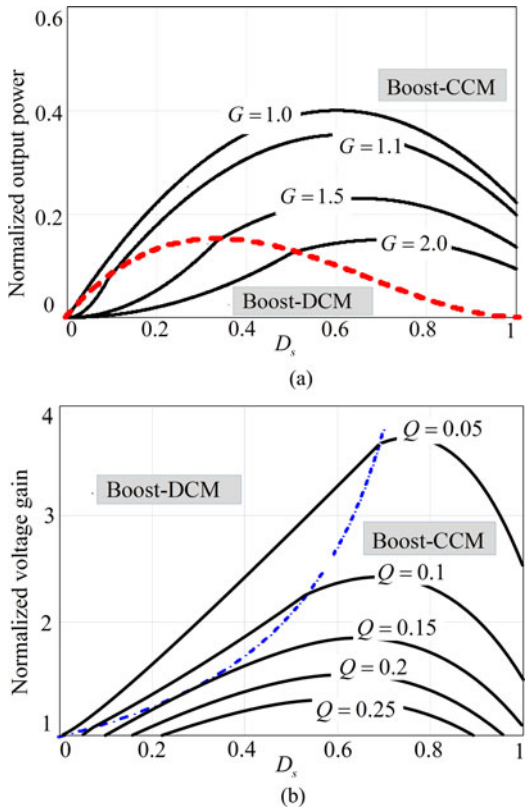

Fig. 15. Output characteristics in the boost mode: (a) normalized output power versus duty cycle and (b) voltage gain versus duty cycle.

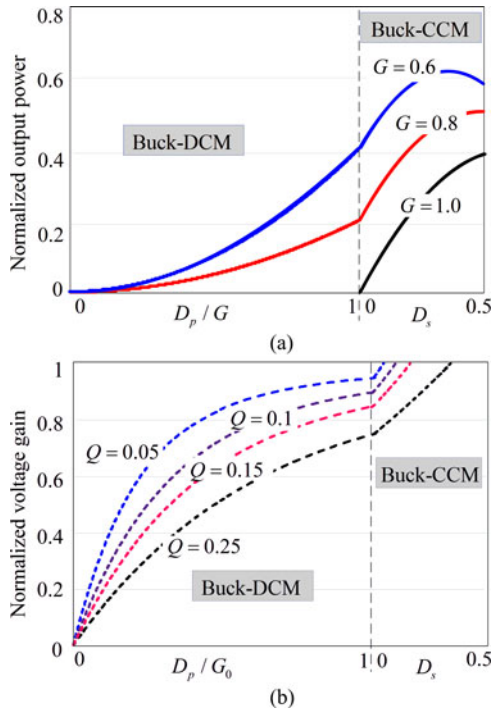

Fig. 16. Output characteristics in the buck mode: (a) normalized output power versus duty cycle and (b) voltage gain versus duty cycle.

buck mode). Fig. 15(a) shows the curves of the normalized output power versus the duty cycle D_s, where the output power is normalized with power base P_{base}

$$P_{\text{base}} = \frac{V_o^2}{16 f L_f}. \tag{23}$$

Fig. 15(b) shows the curves of the voltage gain G versus the duty cycle. In these curves, the characteristic factor is defined as

$$Q = \frac{16 L_f f}{R_o} \tag{24}$$

where R_o is the load resistance. From these curves in Fig. 15, it can be seen that the output power in the boost-CCM mode is greater than the boost-DCM mode when the gain is the same. On the other hand, comparing to the conventional PWM converters, the gain curves, which are affected mainly by the duty cycle and Q value, are more similar to a resonant converter.

Fig. 16 shows the curves of the output power with different voltage gains and the curves of the voltage gain with different characteristic factors in the buck mode. G and G_0 are used to normalize the duty cycle of the primary-side switches

$$G_0 = 1 - Q. \tag{25}$$

From Fig. 16, it can be seen that the output power in the buck-CCM mode is greater than the buck-DCM mode. Besides, when the duty cycle and output voltage are fixed, the output power decreases with the increase in the voltage gain. From the curves of Figs. 15 and 16, it is obvious that isolated buck conversion with $G < 1$ and boost conversion with $G \geq 1$ can be achieved with the proposed converter.

V. Design Considerations and Implementation of Control

A. Design Considerations

As analyzed above, the performance of the proposed IBB converter is mainly affected by the value of characteristic factor Q. A 500-W prototype operating at 100 kHz with 40–60-V input voltage and 380-V output voltage for renewable power system applications is adopted as an example to explore the main design considerations of the characteristic factor Q.

As the gain curves shown in Fig. 15 and Fig. 16, G is designed to be $0.83 \sim 1.25$ with $G = 1$ setting on 50-V input. So, the transformer turns ratio can be designed to be $N = n_P : n_S = 1 : 3.8$. According to the above analysis, soft-switching of all MOSFETs can be achieved in all the operating modes, so the estimation of efficiency should focus on conduction losses. Therefore, the root-mean-square (RMS) current of the high-frequency inductor L_f normalized with the load current is calculated to indicate the conduction losses. The RMS current of the inductor normalized with the load current for different Q values is calculated and illustrated in Fig. 17. It can be seen that when G is close to 1, a smaller Q value stands for less conduction losses and is better for efficiency. However, small Q will lead to high conduction loss if G is away from 1. When G is smaller or greater than 1, a larger Q value leads to a better efficiency. However, if the Q reaches a certain point, such as $Q = 0.3$ shown in Fig. 17, the conduction loss gets worse in the range of $G > 0.9$. Taking these factors into consideration and to achieve high conversion efficiency within a wide operating range, $Q = 0.2$ is a recommended choice. As shown in Fig. 17, the line with $Q = 0.2$ ends at $G = 1.6$, which is the maximum voltage gain when $Q = 0.2$ as shown in Fig. 15(b). Therefore, smaller Q is desired to achieve higher and wider voltage gain.

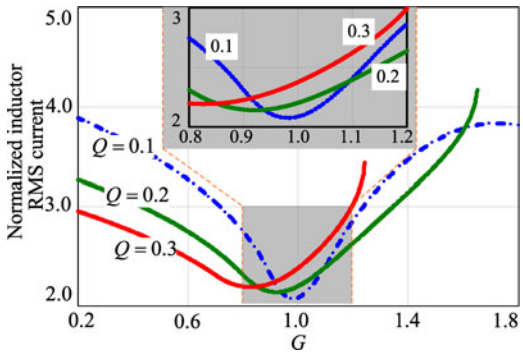

Fig. 17. Normalized inductor RMS current versus normalized voltage gain under different characteristic factors.

B. Implementation of Control

As analyzed in Section III, the control strategy of the proposed converter is similar to the dual-phase-shift control, which is presented for a dual-active-bridge converter to reduce the reactive power and improve efficiency [28], [29]. However, the control of the dual-active-bridge converter is rather complicated in comparison with the proposed converter, because the dual-active-bridge converter has higher degree of control freedom due to the active switches on both the primary and secondary sides, and the bidirectional power flow. Complicated calculations based on the output power, input and output voltages, and parameters of the converter have to be made to derive the optimized phase-shift angle. In contrast, the implementation of the control is very simple. It is because the power flow of the proposed converter is unidirectional. The rectifying diodes are

$$\begin{cases} P_{o\_\text{Buck}-\text{CCM}}(G, D_s, D_p) = \dfrac{V_o^2}{16 f L_f} \dfrac{\left(4D_p - 4D_s^2 + 4D_s D_p - 3D_p^2\right)(G+1) - \left(2D_s^2 - 2D_s + 1 - 2D_s D_p + D_p^2\right) G^2}{G(2+G)^2} \\ P_{o\_\text{Buck}-\text{DCM}}(G, D_s) = \dfrac{V_o^2}{16 f L_f} \dfrac{D_p^2 (1-G)}{G^2} \end{cases}. \tag{22}$$

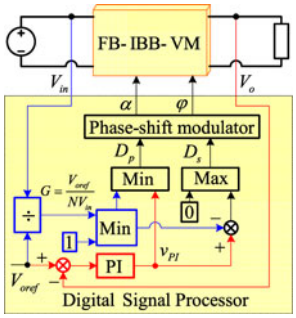

Fig. 18. Control block diagram of the proposed converter.

TABLE I
COMPONENTS AND PARAMETERS OF THE PROTOTYPE

Components	Parameters
Input voltage ($V_{\rm in}$)	40–60 V
Output voltage ($V_{\rm o}$)	380 V
Maximum output power ($P_{\rm o}$)	500 W
Switching frequency	100 kHz
Turns ratio of transformer (nP:nS)	8:30
Inductor L_f	40 μH
Primary side MOSFETs	IPP037N08N
Secondary side MOSFETs	FQA38N30
Secondary side diodes (D1/D3)	DPG20C300PB
Secondary side diodes (D2/D4)	DSEC30-06A
Output capacitors (Co1, Co2)	330 μF

OFF naturally once the inductor current decreases to zero. So, the reactive power in the proposed converter can be minimized inherently.

The control block diagram of the proposed converter is shown in Fig. 18, where only one proportional-integral (PI) regulator and some logic operation are used to realize the control. The phase-shift angles are determined only by the output of the PI regulator, $\nu_{\rm PI}$, and the normalized voltage gain. In the steady state, if $\nu_{\rm PI} > 1$, the converter works in the boost mode with $D_p = 1$ and $D_s = \nu_{\rm PI} - 1$. If $G \le 1$, the converter works in the buck mode. In this scenario, once $G < \nu_{\rm PI}$, then $D_p = G$ and $D_s = \nu_{\rm PI} - G$. Once $\nu_{\rm PI} \le G$, the primary-side duty cycle D_p will be equal to $\nu_{\rm PI}$, while the secondary-side duty cycle $D_{\rm s}$ will be kept at 0. The detailed operation principle of the control is exactly in agreement with the control strategy. And, obviously, the output voltage can be regulated continuously by using this control, and the transition between the buck mode and the boost mode is accomplished automatically.

VI. EXPERIMENTAL VERIFICATION AND ANALYSIS

A 500-W prototype is built to verify the theoretical analysis. The specifications are listed in Table I. The input voltage is 40 V–60 V and the output voltage is 380 V.

Fig. 19 shows the voltage ν_{Np}, ν_{S56}, and current i_{Lf} waveforms of the converter under boost-CCM, boost-DCM, buck-CCM, and buck-DCM modes, respectively. As shown in Fig. 19(a) and (b), the primary current decreases linearly when the input power is transferred to the output side through the filter inductor, because the normalized voltage gain G is greater than

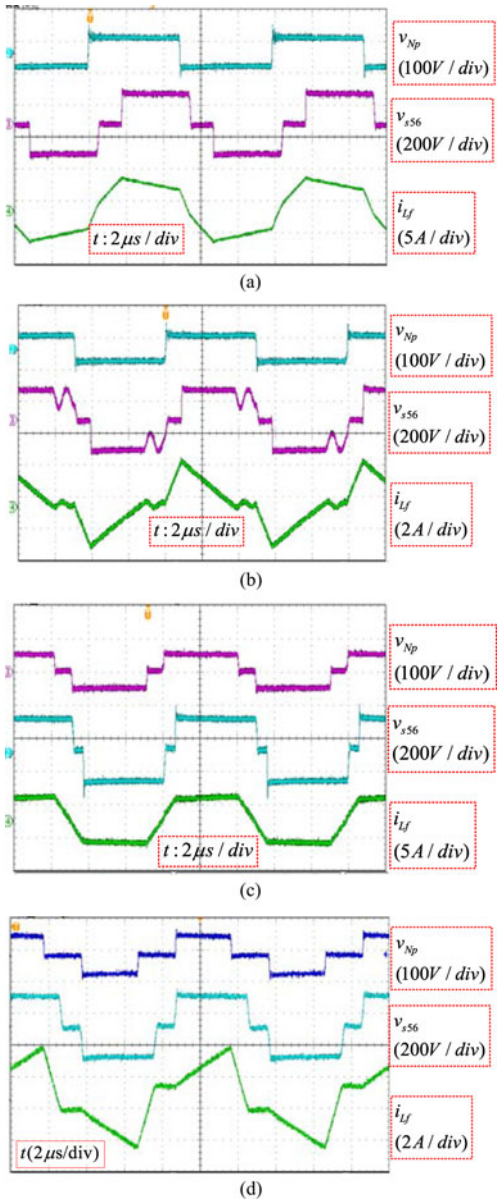

Fig. 19. Voltage ν_{NP}, ν_{S56}, and current i_{Lf} waveform in (a) boost-CCM mode, (b) boost-DCM mode, (c) buck-CCM mode, and (d) buck-DCM mode.

1 and the converter works in the boost mode. In Fig. 19(b), when the inductor current decreases to zero, a small voltage ringing can be seen on the secondary winding of the transformer, which is caused by the parasitic parameters. On the other hand, the primary current increases linearly during the power transferring state, as shown in Fig. 19(c) and (d), with the voltage gain $G < 1$. The waveform in Fig. 19 satisfies the theoretical analysis pretty well.

The soft-switching waveforms of the switches under different operation modes are shown in Figs. 20–23. v_{GS1}, v_{GS4}, and v_{GS6} are the driving voltages of the switches S_1, S_4, and S_6, while v_{DS1}, v_{DS4}, and v_{DS6} are corresponding drain-to-source voltages. The waveform shown in Fig. 20 indicates that ZVS turn-on can be achieved for all the primary-side and secondary-side switches when the converter operates

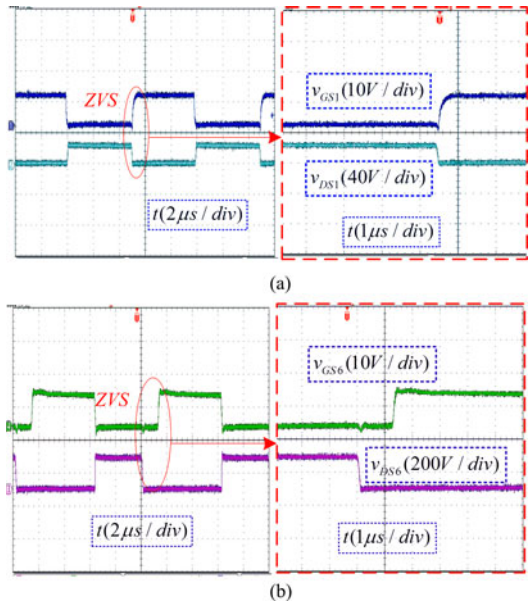

Fig. 20. Switching waveform of (a) primary-side switch and (b) secondary-side switch under the boost-CCM mode.

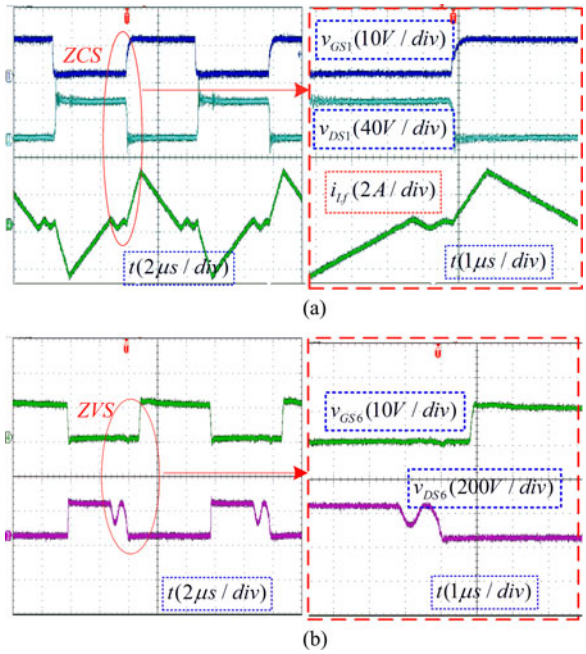

Fig. 21. Switching waveform of (a) primary-side switch and (b) secondary-side switch under the boost-DCM mode.

in the boost-CCM mode. As shown in Fig. 21, when the converter works in the boost-DCM mode, the ZVS performance is lost for the primary-side switch but ZCS performance can be accomplished for the primary-side switch, and the ZVS performance is achieved for the secondary-side switch. It can be concluded that soft-switching can be achieved for all the switches when the converter works in the boost mode.

In the buck-CCM mode, as shown in Fig. 22, ZVS turn-on of all the primary-side and secondary-side switches can be obtained. While in the buck-DCM mode shown in Fig. 23, ZVS

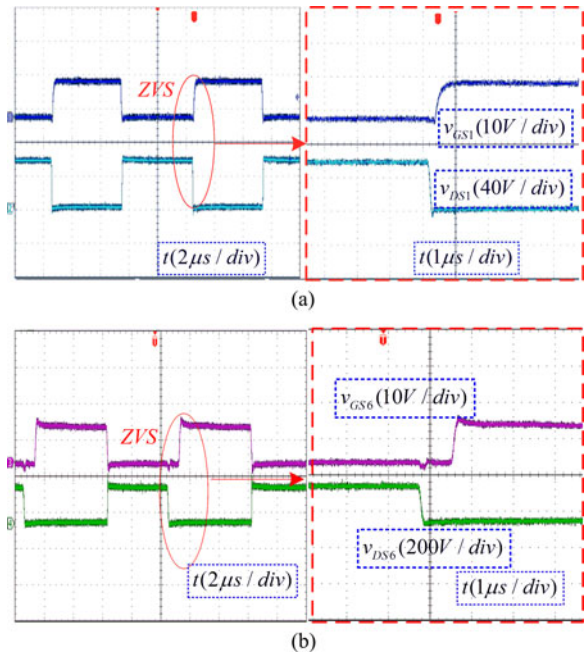

Fig. 22. Switching waveforms of (a) primary-side switch and (b) secondary-side switch under the buck-CCM mode.

turn-on of the primary-side switches in the leading leg and ZCS turn-on of the primary-side switches in the lagging leg can be achieved. ZVS of the secondary-side switches can also be realized. It can be seen that in the buck mode, the soft-switching of all the switches can also be obtained.

The experimental waveforms when the operation mode transits from the boost mode to the buck mode are shown in Fig. 24, where smooth and autonomous mode transition is realized by using the control shown in Fig. 18. When the input voltage increases, the output voltage is always kept constant no matter which mode the converter works in.

The curves for efficiency versus output power under 40-, 45-, 55-, and 60-V input voltages are shown in Fig. 25. When the input voltage is 40 and 45 V means the proposed converter operates in the boost mode, the peak efficiency is about 97.8%. When the input voltage is 55 and 60 V means the proposed converter operates in the boost mode, the peak efficiency is about 97.4% and the efficiency at full load is above 96%. Meanwhile, efficiency higher than 94% has been achieved in a wide load and voltage range. The experimental results indicate that high efficiency over a wide operating range has been achieved with the proposed IBB converter and control strategies due to the single-stage power conversion, soft-switching performance, and reduced conduction losses.

VII. Conclusion

Novel IBB converters with single-stage power conversion based on high-frequency bridgeless-interleaved boost rectifiers have been proposed and investigated in this paper. The concept of high-frequency bridgeless-interleaved boost rectifiers, which are built by integrating a full-bridge diode-rectifier and interleaved boost converters, are rooted in the bridgeless

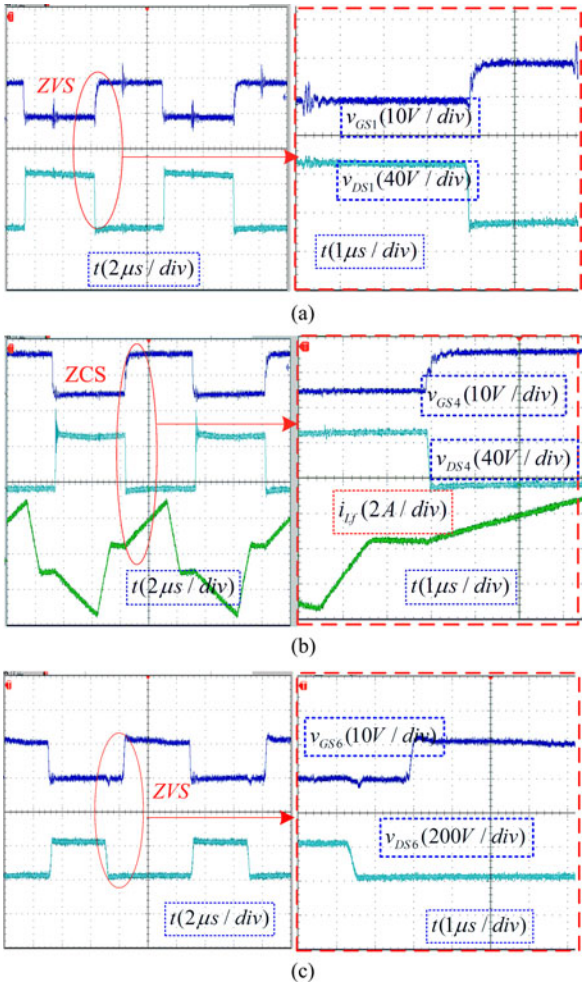

Fig. 23. Switching waveform of (a) primary-side switch in the leading leg, (b) primary-side switch in the lagging leg, and (c) secondary-side switch under the buck-DCM mode.

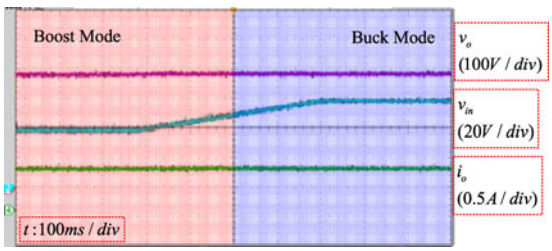

Fig. 24. Operation mode transition waveforms.

ac–dc power factor corrector circuit. A full-bridge IBB converter with a voltage multiplier on the secondary-side bridgeless boost rectifier has been investigated. The voltage stresses of the semiconductors in the boost-rectifier are reduced significantly due to the voltage multiplier; hence, low-voltage-rated devices with better conduction and switching performance can be used to improve efficiency. In other words, this converter is more attractive for high-output-voltage applications. Optimized phase-shift control strategy is applied to the proposed converter to realize isolated buck and boost conversion. Moreover, soft-switching

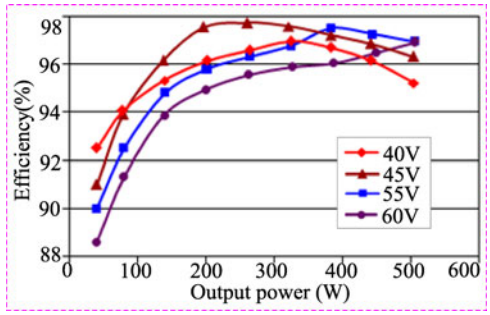

Fig. 25. Measured efficiency versus output power.

within the whole operating range have been achieved for all of the active switches and diodes, respectively, by adopting the optimized phase-shift control. The analysis and performance have been fully validated experimentally on a 40–60 V-input, 380-V-output hardware prototype. Experimental results demonstrate that the proposed IBB converter is an excellent candidate for high-efficiency IBB conversion.

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Hongfei Wu (S'11–M'13) was born in Hebei Province, China, in 1985. He received the B.S. and Ph.D. degrees in electrical engineering and power electronics and power drives from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2008 and 2013, respectively.

From June 2012 to July 2012, he was a guest Ph.D. student at the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. Since 2013, he has been with the Faculty of Electrical Engineering, NUAA, and is currently a Lecture with the College of Automation Engineering, NUAA. He has authored and co-authored more than 80 peer-reviewed papers published in journals and conference proceedings. He holds more than ten Patents. His research interests are power converters, distributed power generation, and spacecraft power system.

Dr. Wu received the Presentation Award at IEEE Energy Conversion Conference and Exposition 2011, and also the Outstanding Reviewer of IEEE TRANSACTIONS ON POWER ELECTRONICS (2013).

Tiantian Mu was born in Jiangsu Province, China, in 1991. She received the B.S. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2014, where she is currently working toward the M.S. degree in electrical engineering and power drives.

Her research interests include topology and control of soft-switching dc–dc converters.

Hongjuan Ge was born in Jiangsu Province, China, in 1966. She received the B.S. and M.S degrees in engineering from Southeast University, Nanjing, China, in 1985 and 1988, respectively, and the Ph.D. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2007.

She joined the Faculty of Electrical Engineering, NUAA, in 1988, and is currently a Professor at the Electrical Engineering Department, College of Automation Engineering. Her research interests include topology and control for AC-AC Matrix Converters, and PMSM drive and Control. She has authored more than 30 technical papers published in journals and conference proceedings.

Yan Xing (M'03) was born in Shandong Province, China, in 1964. She received the B.S. and M.S. degrees in automation and electrical engineering from Tsinghua University, Beijing, China, in 1985 and 1988, respectively, and the Ph.D. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2000.

Since 1988, she has been with the Faculty of Electrical Engineering, NUAA, and is currently a professor with the College of Automation Engineering, NUAA. She has authored more than 100 technical papers published in journals and conference proceedings and has also published three books. Her research interests include topology and control for dc-dc and dc-ac converters. She is an Associate Editor of the IEEE Transactions on Power Electronics.

Dr. Xing is a member of the Committee on Renewable Energy Systems within the IEEE Industrial Electronics Society.