Dynamic Modeling Method of Electro-Thermo-Mechanical Degradation in IGBT Modules

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***Abstract*—A degradation model investigating the electro-thermo-mechanical fatigue, experienced by insulated gate bipolar transistors modules, is presented. To illustrate the concept, a specific case of power modules subjected to active power cycling which induce failure through bond wire lift-off is considered. Bond wire lift-off is believed to be due to thermally induced stress arising from a mismatch in the coefficients of thermal expansion between the wires and the given substrate. Overall, the theoretical evaluation is based on determining the thermo-mechanical stress around the bond wire/substrate interface through multiphysics-based models. The simulation detail and included equations are specified according to the region of interest and their complexity. In common, however, is the use of the finite element method combined with empirical equations. The final result is a numerical approach to evaluate the damage accumulated by a given load which may be used for prediction of lifetime or optimization of work points and module geometry.**

***Index Terms*—Accelerated testing, degradation mapping, IGBT modules, lifetime estimation, thermal modelling.**

I. Introduction

DEMANDS of increased use of renewable energy sources as well as changes in the structure of the power grid toward a more distributed system makes the global electrical energy consumption increase steadily. Accordingly, reliable and efficient power electronics is essential [1]. In wind power systems failures in the power converters account for as much as 15% of all failures. Degradation assessment of individual elements as well as accurate lifetime estimation of power modules is thus vital. Presently, insulated gate bipolar transistor (IGBT) modules are used widely, with applications ranging from a few 100 W to several MW. Accordingly, a modeling method needs to be developed which is usable in a wide application range. This requires a detailed model of the physics-of-failure of the device of interest [2], [3].

In this paper, the problem of power modules employed in high power conversion, especially wind power converters, is regarded. Thermo-mechanical fatigue accounts for several severe failure modes of IGBT modules, e.g., solder creep, bond wire lift-off/heel cracking, metalization reconstruction, etc. [2], [4]. This is normally induced by time varying loads (alternating currents, pulsed conditions, etc.) which causes local heating in active components followed by cool-down during passive periods. In this paper, a model for degradation analysis of high power IGBT modules is presented. A common approach for testing robustness of power module packaging is to simulate the before mentioned temperature cycling, either through power- (active thermal) or passive thermal cycling [3]. In both cases, the test is a simulation of real world conditions, in this paper a power module subjected to so-called active power cycling [5] is regarded. The motivation for this particular case is its resemblance to real world application. Under these conditions, the dominant failure mechanism observed is bond wire lift-off [6], [7].

Given the highly varying loads experienced by this type of component, it is not surprising that thermo-mechanics play an important role on its lifetime. If the primary load of the overall module is the applied current and the switching of it, then the dominating heating occurs in the active components - transistors and diodes. Due to the vast difference in the volume of the chips and the remaining part of the module one distinguishes between two types of loads, namely long and short load times. In both cases, the diodes and transistors are heated up followed by the surrounding layers. But in the latter case the short time between heat-up and cool-down of regions ensures that only active elements and immediate contacts are significantly heated [3], [8].

So far the common approach in degradation and lifetime assessment of IGBT modules failing due to bond wire lift-off has been based on the Coffin–Manson (CM) or CM-Arrhenius model with a parameter corresponding to the load inserted [9], [10] [see (1)–(2)]. Often the change in temperature ΔT is used as the load and the model parameters are fitted to accelerated test data to take shape, environment, degree of damage, etc., into account (see [3], [6], [7], [11], [12]).

$$N_f = \beta (\Delta T)^{\alpha} \tag{1}$$

$$N_f = \beta (\Delta T)^{\alpha} \exp\left\{\frac{E_A}{k_B T}\right\} \tag{2}$$

where N_f is number of cycles to failure, α and β are fitting parameters, and E_A is an activation energy.

The simplicity of the models is both an advantage and disadvantage. In principle, they can be applied to any element failing from thermo-mechanical-induced degradation; however, one needs to obtain component specific parameters from fitting

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to test data. In high power electronics the expected component lifetime often exceeds ten years, accordingly, one needs accelerated conditions to obtain lifetime information within a reasonable time frame. This is also the normal approach, were the component of interest is subjected to highly accelerated test conditions, e.g., a high ΔT, that normally cause a failure in a shorter time frame (days-weeks). α and β are afterwards obtained by fitting the model to accelerated test data, and the lifetime at nonaccelerated conditions are obtained through extrapolation. While this approach has been useful for more than a decade, it has begun to be problematic in recent years. There are several reasons for this:

1) The simplicity of the model does not take the effect of geometry and material composition into account. It has been reported that changes of, e.g., wire curvature alone as well as bond footprint affect the lifetime directly [13], [14]. Accordingly, accurate fitting of empirical models is paramount.
2) With ΔT as only input parameter and only one set of fitting parameters attached to the stressor, the model assumes the eventual failure is either a single mechanism or a series of mechanisms connected to ΔT with a constant grouping.
3) Failure mechanisms observed under accelerated conditions are not necessarily occurring at normal operation.
4) Variation in production quality requires a very large quantity of wear-out tests [11].
5) ΔT is often based on thermal networks or the V_{CE} which corresponds to the average chip temperature. Due to the geometrical shape and the change of the load over time and space it is fair to assume that the temperature field is not constant everywhere. On the contrary, it has been noted that depending on the load, a very inhomogeneous field might be the case [13], [15].

The first problem has in later years been sought solved by increasing the number of fitting and input parameters in the same way the Arrhenius factor was added in (2) (see [10], [11], [16]). However, this still only delivers a functioning lifetime model at accelerated conditions as well as for the particular module tested.

In the following, a dynamic 3-D degradation model which can be used for design optimization, specification of load limitations, and lifetime estimation is presented. The model presents possibilities for large scale 3-D electro-thermo-mechanical simulations with only geometry and electrical/environmental load as input. In all steps physical-based models are used in the simulation with realistic boundary conditions corresponding to actual application.

II. Model Structure

In principle, all degradation models in cyclic systems are based on the same steps: *load, damage, recovery*. These process steps run simultaneously and do so until reaching a given failure criteria. To construct a degradation model for electro-thermo-mechanical degradation of interconnects in high power IGBT modules, one need to understand the load conditions, relevant

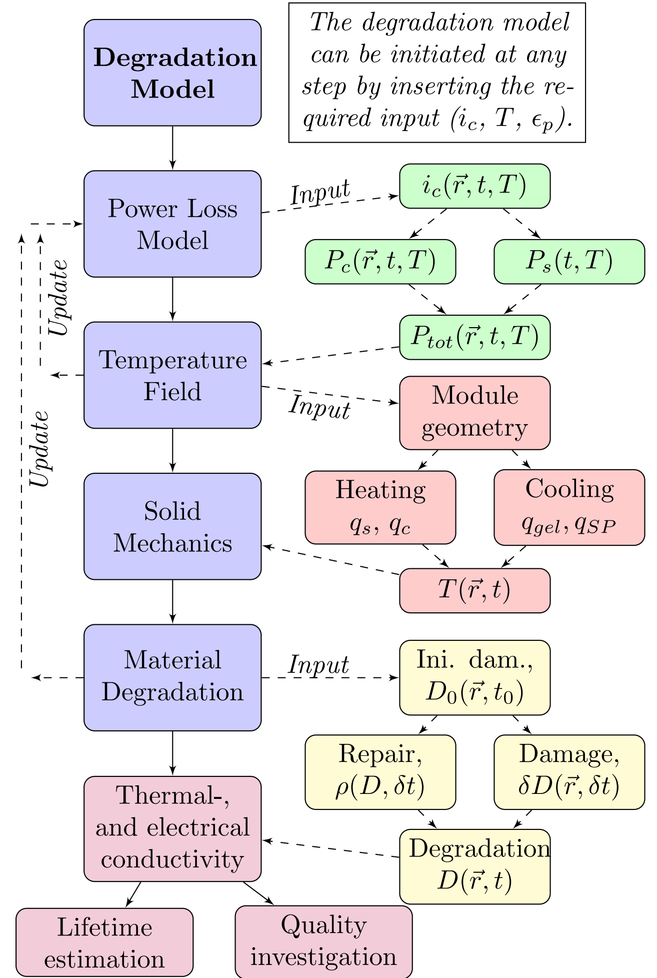

Fig. 1. Flow chart of electro-thermo-mechanical degradation model of power module interconnects.

subcomponents, and degrading elements. The power modules of interest are primarily used for power conversion in high power application fields, e.g., wind mills or automotive. Based on this, the model presented in Fig. 1 is proposed.

Due to the complexity of the regarded system, the model is as far as possible sought divided into steps. In Fig. 1, four primary sections constitute the model: *1) power loss, 2) temperature field, 3) solid mechanics*, and *4) material degradation*. These are all directly connected as illustrated by the lines in the flow chart.

III. Geometry and Test Conditions

The proposed model can be utilized on any geometry, however, in order to validate the simulation results an actual IGBT module is regarded which in [5] and [17] is subjected to accelerated testing.

A. Power Module Geometry

The considered module consists of six identical sections with two IGBT chips and two diodes. Each section is rated at 1700 V

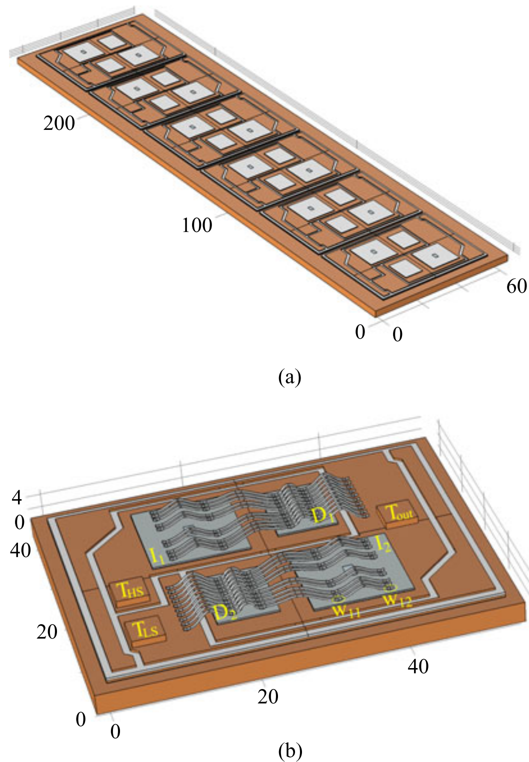

Fig. 2. CAD illustration of (a) full power module and (b) single section. The power module consist of six identical sections running in parallel. Units are in millimetre. (a) Full power module with limited elements included. (b) Detailed illustration of single module section.

TABLE I
LAYER COMPOSITION AND THICKNESS OF THE DCB BASED IGBT MODULE

Layer	Material	d_i [μm]
Bond wire	Al	400
Metalization	Al	6
Chip	IGBT/Diode	200
Solder	$SnAg(3.5)$	100
Copper	Cu	300
Ceramic	Al_2O_3	380
Copper	Cu	300
Solder	$SnAg(3.5)$	100
Baseplate	Cu	3000

and a total current of 1000 A of all six. The geometry is depicted in Fig. 2(a) and (b) with the layer thickness' specified in Table I.

B. Sinusoidal Test Conditions

The specific test conditions are presented in Table II and a detailed description of the setup is outlined in [17]. A sinusoidal current load is applied at 6 Hz and switched at 2.5 kHz. Water cooling is applied directly to the backside of the baseplate using Danfoss ShowerPower (see [18]). The high load current combined with a high cooling temperature and low fundamental frequency is a common approach for causing accelerated wear in this type of power module.

TABLE II
ACCELERATED TEST CONDITIONS

Parameter	Symbol	Value
Dc-link voltage	V_{DC}	1000 V
Peak load current	I_{tot}	922 A
Fundamental frequency	f_{out}	6 Hz
Switching frequency	f_s	2.5 kHz
ShowerPower temperature	T_{SP}	80° C

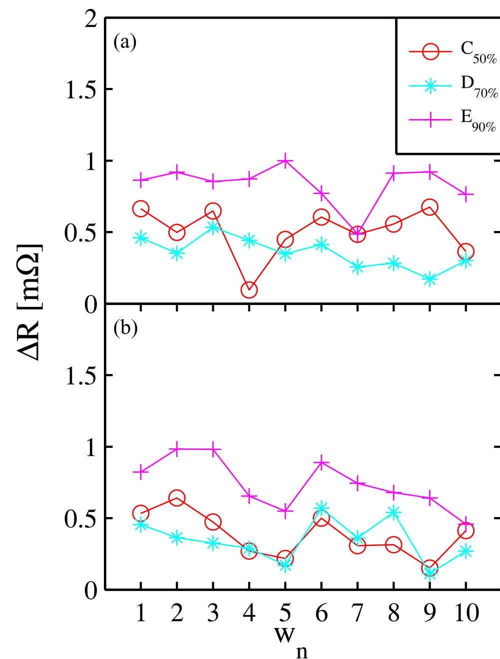

Fig. 3. Four-point probing of change in effective resistance of IGBT (a) LS and (b) HS wire bonds, figure is presented and discussed in detail in [21]. The first axis numbering is the wire from the section edge and inwards.

C. Test Results

To experimentally investigate the degradation evolution of the regarded module several samples were power cycled to different states of lifetime: A_{New}, $B_{25\%}$, $C_{50\%}$, $D_{70\%}$, $E_{90\%}$, and $F_{100\%}$. Here the subscript denotes the relative state on a lifetime curve compared to the $F_{100\%}$ module run until catastrophic failure. Detailed information on online monitoring methodologies, power cycling setup, and visual inspection results are available in [5], [17], and [19]. Following power cycling the modules were experimentally investigated by four-point probing [20], [21] of electrical parameters and microinvestigation using SEM/FIB and microsectioning [14]. No significant degradation was observed in the chip or baseplate solder in any of the samples, accordingly, further investigation was centred on chip topside interconnects.

1) Four-Point Probing: In Fig. 3, a plot of the change in effective resistance of the IGBT (a) LS and (b) HS wire bonds is presented. As would be expected, the degree of wear is seen to increase gradually with state in lifetime, however, no chip hotspot effects are observed around the center wires. The latter

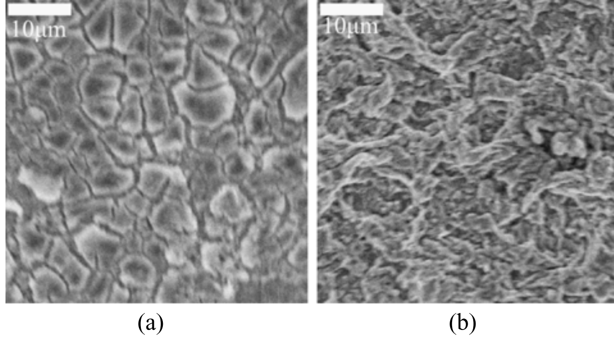

Fig. 4. Topographic SEM images of $E_{90\%}$ diode. Clear metalization reconstruction is observed with a tendency of increased degradation near the center. (a) Diode edge. (b) Diode center.

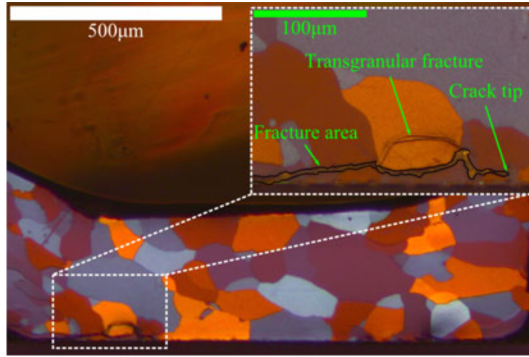

Fig. 5. Cross-sectional image of an end IGBT wire bond from $D_{70\%}$, Al grain contrast is obtained by electro-etching (see [14]).

is in contrast to previous presented results [6], [7] where the chip center tend to trap heat due to geometry. This effect is observed in the diode wire bonds, however, where the middle wires are observed to degrade at a highly increased rate.

From both visual inspection and four-point probing the diode LS wire bonds are observed to fail at a highly increased rate (see [21], [22]).

2) SEM/FIB and Microsectioning: The before mentioned hot spot effects on the module diodes are easily observed by topographic SEM images (see Fig. 4). Here, the metalization near the center is clearly observed to degrade at an increased rate compared to the edge. Similarly, the depth of the cavities created by the grain extrusion is observed to increase depending on position by FIB milling (see [22]).

In Fig. 5, a cross-sectional image of an end IGBT wire bond from $D_{70\%}$ is presented. The cross-sectional view is obtained by several steps of grinding and fine grade polishing combined with electro-etching (see [14]). Electro-etching creates color contrast between different grains when using polarized light which makes it possible to distinguish different types of fracture processes: delamination, intergranular, and transgranular. By investigation of microstructure a clear tendency of increased degradation in stitch bondings compared to edge bondings is observed and center wires on diodes are displaying significant wear. For additional information, see [19] and [22].

IV. Theory

This section contains the fundamental theory behind the degradation model. As discussed in Section II, the model is separated into a number of blocks, the theory is outlined similarly.

A. Power Loss

In Section III-A, a typical power module design is presented. This consists of several active and passive components. While power losses in passive components (Cu pads, Al bond-wires, solders, metalizations) can be limited to standard conduction losses the active semiconductor components have several other contributing effects. The power loss in the semiconductor components far exceed the conduction losses of the remaining elements, accordingly the power loss calculation is centered around the semiconductor chips.

The total power loss in a power module is normally separated into static (P_{static}), switching (P_s), and driving losses (P_{driving})

$$P_{\text{tot}} = P_{\text{static}} + P_s + P_{\text{driving}} \tag{3}$$

$$\approx P_c + P_s. \tag{4}$$

In (4), P_{static} includes conduction losses (P_c) and blocking losses. As the forward blocking and driving losses are often small compared to the remaining, these are normally left out [23]–[25].

In the test system regarded, a well-defined current load is applied (see [5], [17]). Accordingly, conduction losses in all passive components are calculated by deriving the current distribution $[i_c(\vec{r}, t)]$ and using the local electrical conductivity. However, for the active components switching losses has to be included as well. As explained in [5], the load is switched between IGBTs and diodes and similarly it changes between interconnects. This is handled through the system modulation function (m)

$$P_c^{\text{IGBT}} = i_c(\vec{r}, t) v_{CE}(\vec{r}, t, T) \left(\frac{1-m}{2}\right) \tag{5}$$

$$P_s^{\text{IGBT}} = f_s \left[E_{\text{on}}(T) + E_{\text{off}}(T)\right] \left(\frac{V_{\text{DC}}}{V_{\text{ref}}}\right)^{K_v^I} \tag{6}$$

$$P_c^{\text{Diode}} = i_F(\vec{r}, t) v_D(\vec{r}, t, T) \left(\frac{1+m}{2}\right) \tag{7}$$

$$P_{\text{rec}}^{\text{Diode}} = f_s \left[E_{\text{rec}}(T)\right] \left(\frac{V_{DC}}{V_{\text{ref}}}\right)^{K_v^D} \tag{8}$$

where i and v denote the forward current and voltage of the semiconductor components and K_v is the shape difference [25] of the switch-loss curve (E) at V_{DC} compared to V_{ref} in the data-sheet.

As introduced through the arguments of the power losses in (5)–(8) the switching and recovery loss is assumed homogeneously distributed according to temperature.

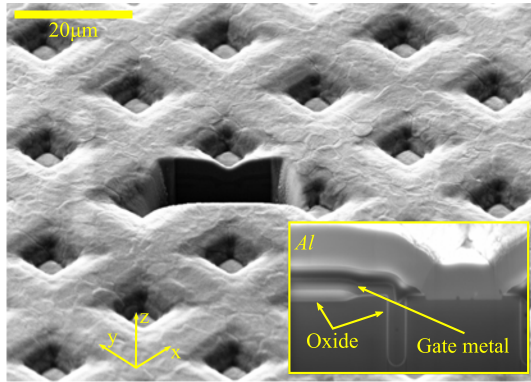

Fig. 6. SEM image of the topological layout of an IGBT chip with an FIB obtained cross-sectional view of the trench gate structure.

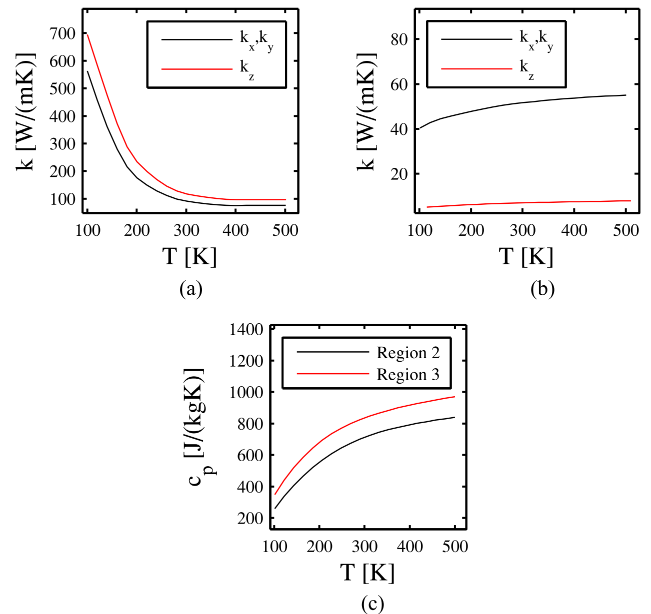

Fig. 7. Thermal conductivity and specific heat capacity of regions 2 and 3 as a function of direction and temperature. The parameters are derived using an EMA (a) Thermal conductivity of region 2. The components in the direction parallel to the chip surface are identical due to symmetry (b) Thermal conductivity of region 3 (c) Pressure specific heat capacity of regions 2 and 3.

B. Electro-Thermal Model

The electro-thermal modeling may be divided into the actual power loss presented in Section IV-A which heats up the component and the following transfer of heat. Accordingly, the physical parameters of the geometry as well as the geometrical structure is important for the temperature field [15].

1) Transient Temperature Fields: As earlier discussed, the initial problem is to calculate the temperature field for a given load. This problem is fundamentally governed by the diffusion-convection-reaction partial differential equation (PDE), which is, when neglecting mass transport, given as [26], [27]

$$\vec{\nabla} \cdot (k\vec{\nabla}T(\vec{r},t)) + \frac{\partial q(\vec{r},t)}{\partial t} = \rho c_p \frac{\partial T(\vec{r},t)}{\partial t}. \tag{9}$$

Here, ρ is the density, c_p is the specific heat capacity, k is the thermal conductivity, and q is the heat flux. In the stationary case this problem is ideal for a finite element (FE) approach. However, as the load fluctuates with the applied current the problem is far from stationary. It may still be solved using an FE analysis, but with significantly higher demands on computational power and solution time. As mentioned in the previous section, the power loss fluctuates in time and space when the load switches to either one of the diodes or the other transistor.

2) Physical Parameters: In order to accurately calculate $T(\vec{r},t)$ for the power module presented in Section III-A temperature dependent parameters are needed [15], [28]. For pure materials like Al and Cu these are catalogued data if one assumes the materials as continua (see [28] or [29]). However, for the semiconductor devices the situation is different which is clearly seen in Fig. 6.

Fig. 6 presents a topographic view and an FIB cut of a new IGBT chip. In the topographic image a channel like structure of the IGBT is observed with a spacing of app. 18 μm. In the FIB cut the vertical layout near the chip surface is observed. From the top down the first 6 μm is Al metalization. Beneath the metalization two regions are observed: the current channel and the gate area. The current channel consists of doped Si (see the dark gray region at the bottom of the FIB cut in Fig. 6) and the gate area includes the gate metal region surrounded by a thin white oxide layer.

The gate structure seen in the IGBT chip in Fig. 6 is far from a continuous medium and accordingly a different approach needs to be applied with regard to physical parameters. Presently, an effective medium approach (EMA) is applied for the calculation of the thermal conductivity tensor and the specific heat capacity. A similar approach is applied in [15] for a trench-based structure. Here, a channel type transistor is considered as seen in Fig. 6. Most of the materials in the composition are well known with regard to thermal conductivity and specific heat capacity. For the doped silicon, the temperature dependent parameters are obtained from [30].

The IGBT geometry is separated into three regions, the first region includes all layers from the solder to the beginning of the trench in Fig. 6. This is the major part of the chip, and due to its simple structure its physical parameters may be derived directly from the doping. Region 2 extends from the bottom of the trench to the beginning of the horizontal oxide layer, resulting in identical coefficients in two directions. This leaves the remaining layers in region 3 including the horizontal oxide and gate layer. The simulated thermal conductivity and specific heat capacity of regions 2 and 3 are presented in Fig. 7(a)–(c).

Due to symmetry considerations the thermal conductivity in the plane of the chip surface are identical. The clear difference between regions 2 and 3 is generated by the volume fraction of the oxide layer which has a much lower thermal conductivity. With the amount of silicon present, the heat capacity naturally comes close to that of bulk silicon. With EMA obtained physical parameters simulation of the chip junction temperature has been observed to be in good agreement with online temperature estimation results both in magnitude and time (see [5]).

3) Boundary Conditions: The bottom of the baseplate is in this example directly water cooled and the topside is cooled through the gel. Both of these imply a convection surface, the water cooling externally forced and the gel passively. The convection surface on the gel side is not to be confused with the assumption that mass transport are occurring inside the silicone gel. It is merely an approach to model the flux through the gel without including its vast volume into the model. The convection surfaces are approached using a BC with Newton's law of cooling

$$q_n = -h_s(T - T_\infty) \tag{10}$$

where q_n is the flux normal to the surface, h_s is the mean coefficient of convection of the surface, and T_∞ is the stationary temperature of the ambient beyond the thermal layer. The convection parameter for the Danfoss ShowerPower system is obtained from [18] and the gel is modeled as passive cooling in air.

C. Thermo-Mechanical Modeling

In the same way, the calculation of the temperature field depends heavily on the electro-thermal parameters, the derivation of the plastic strain field depends highly on the CTE, elastic parameters, and yield strength. However, the primary damage assessment is carried out in the degradation calculation based on sample specific experimental data. Accordingly, textbook parameters are used in the stress derivation and corrected afterwards.

With the simulated temperature field $T(\vec{r},t)$ the thermal expansion may be derived directly. The created strain is uniform leaving out shear contributions

$$\vec{\epsilon}_{th} = \Delta\vec{\alpha} \cdot \Delta T \tag{11}$$

where $\vec{\alpha}$ is the CTE vector which reduces to α for linear isotropic materials [26, Ch.7]. For two continuous slabs connected to each other the three strain components $\epsilon_x, \epsilon_y, \epsilon_z$ are easily calculated through the difference in CTE and the fundamental constraints between the three directions. From these components the generated plastic strain for a single cycle may be derived analytically from a 1-D approximation presented in [31]. This approach, however, neither takes the geometry or an inhomogeneous temperature field into account. The difference will be clear in the results section where results from the detailed 3-D dynamical simulation is presented together with the simplified.

By combining (11) with the before mentioned temperature field, the resulting displacement field $u(\vec{r},t)$ may be calculated everywhere. To identify when the strain moves from the elastic to the plastic regime the stress needs to be derived. In the elastic region this is solved through the elasticity tensor. In the inelastic regime, the solution is more problematic. In the present case, the plastic potential function $[F(\vec{\sigma})]$ is used to calculate changes in the plastic deformation

$$\frac{d\epsilon_p}{dt} = \frac{d\lambda}{dt}\frac{\partial F(\vec{\sigma})}{\partial \sigma} \tag{12}$$

where λ is the plastic multiplier and $F(\vec{\sigma})$ for a Von Mises type isotropic strain-hardening material is

$$F(\vec{\sigma}) = \sigma_{VM}(\vec{r}) - \sigma_y(\vec{r}) \tag{13}$$

where σ_{VM} is the Von Mises stress, and σ_y is the yield strength of the material. To account for material hardening over time $\sigma_y(\vec{r})$ needs to be modified continuously. However, in the present model, the material hardening is included in the degradation step, meaning that material hardening is in the structural mechanics calculation assumed perfectly plastic [32].

D. Degradation Modeling

The thermal and mechanical analysis presented in Section IV-B and C in principal yields all the primary stressors relevant for modeling degradation in power module interconnects. However, the derivation of the actual material degradation as a function of position and time $[D(\vec{r},t)]$ induced by the stressors is nontrivial. The primary failure mechanism experienced in the presently regarded module placed under the conditions shown in Table II has been identified as bond wire lift-off and metalization reconstruction (see Section III-C or [20]). Accordingly, the degradation model is centered on low cycle fatigue damage in the Al/Si interfaces. To incorporate degradation effects elsewhere, e.g., chip or baseplate solders, one would need to specify relevant models, which for solders could be time-induced effects like creep or diffusion.

In [9] and [33], a 1-D approach for modeling the bond wire lift-off failure mechanisms is presented. The model is a time-domain-based degradation approach where T and ϵ_p are inputs and the fracture propagation criteria is obtained from shear tests

$$\begin{aligned} \delta D &= f(D,\epsilon,T)\delta T - \rho(D,T)\delta t \\ &= f_\epsilon f_D f_T \delta T - \rho_D \rho_T \delta t. \end{aligned} \tag{14}$$

In (14), the first term on the right hand side includes the created damage during loading and the second term the damage removal. In the following two sections, the terms applied in (14) in this paper are presented for damaging and repairing effects, respectively. The main function $D(\vec{r},t)$ of the differential equation in (14) is a unitless degradation parameter. Any physical interpretation of the absolute value of $D(\vec{r},t)$ has to be obtained by comparing to specified criteria, e.g., fracture propagation by comparison to experimental data or design quality by comparison to damage generated at other positions.

The method suggested in this study is to utilize the changes in on-state voltage induced by material degradation. This is already a commonly monitored parameter through power module Kelvin terminals [34]. Using the Kelvin terminals, however, is problematic as these include all interconnections in the module. This has been sought solved by introducing new monitoring methodologies [17] and four-point probing of individual interconnects [20].

1) Damage Functions: The first term on the right hand side of (14) is the damage generated at time t. As indicated in the equation, this is separated into four contributions: strain concentration function $f_\epsilon(\vec{r},t)$, hardening function $f_D(\vec{r},t)$, thermal

load $f_T(\vec{r},t)$, and a local displacement strain $d\epsilon_d$

$$f_\epsilon(\vec{r},t) = G_0 {\epsilon_p}^e(\vec{r},t) \quad (15)$$

$$f_D(\vec{r},t) = 1 + a_H D(\vec{r},t)^{B_H} \quad (16)$$

$$f_T(\vec{r},t) = \left(\frac{T_{\text{eq}}}{T(\vec{r},t)}\right)^{B_T} \quad (17)$$

$$d\epsilon_d = \Delta\alpha\delta T \quad (18)$$

where G_0, a_H, B_H, and B_T are computational coefficients and ${\epsilon_p}^e$ is the effective plastic strain. The physical explanation for each term is in principle explained by the stressor input. The strain concentration and thermal load function makes accumulated damage proportional to the absolute plastic strain and temperature increase, respectively. This is similar to the original low cycle fatigue law, the CM. The same can be stated regarding the local displacement strain which include elastic effects describing the damage created during the solver time steps. Finally, the hardening functions are included to account for material hardening effects in order to correct for the perfect elasto-plastic assumption in the mechanical analysis.

2) Restoration Functions: The second term on the right hand side of (14) is the recovery part. ρ_D is the already existing damage and $\rho_T \delta t$ is a temperature-activated annealing term depending on the amount of time at the given temperature and the strain hardening experienced prior

$$\rho_T(\vec{r},t) = \kappa_2 \exp\left(-\frac{E_A}{k_B T(\vec{r},t)}\right) \quad (19)$$

where E_A is the activation energy and κ_2 is a computational coefficient. The recovery term is simply a standard Arrhenius contribution normally used for describing temperature dependent reaction rates.

V. Results

As is clear from Sections III and IV, the regarded geometry and theory combined compose a complicated problem which was the motivation for separating the modeling into multiple blocks as illustrated in Fig. 1. Apart from separating the simulation into multiple steps, the detail level of the applied theory also depends on the regarded geometry. An example of this is that thermal simulations are initially carried out on a full module as presented in Fig. 2(a) to obtain information on thermal interactions between sections. In this simulation, the wire bonds are not included as the local effect, they are observed to have on the chip surface temperature, only has limited influence on the thermal overlap of the sections. Accordingly, in the initial step of the temperature field calculation a function of the baseplate surface temperature $[T_{BP}(\vec{r},t)]$ is obtained and used as input in the detailed simulation of the chip temperature. Similarly, the detail level of the strain field and degradation function calculation is also increased when regarding a more specific region.

Computationally, the different steps are solved depending on type regarded. Current distribution between module sections, illustrated in Fig. 2(a), is obtained using standard electrical circuit-based software. The local current distribution on a module section, the temperature field, and the strain field is derived using finite element (FEM) simulations based on COMSOL multiphysics. Finally, the PDE in (14) yielding the degradation parameter is solved using standard solvers as available in Matlab.

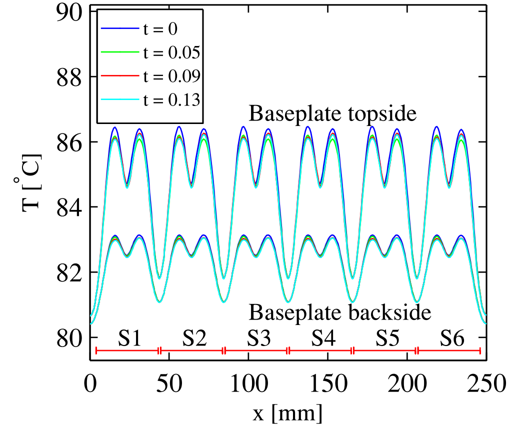

Fig. 8. Baseplate mean temperature of topside and backside plotted along a line placed at the module center. The position and width of the different sections are marked with red lines.

The results section is separated into individual model steps and module/section/bond wire analysis.

A. Temperature Field

With the sinusoidal applied load the temperature field of the geometry presented in Fig. 2 varies highly in time and space. If the simulation is initiated at the same temperature as the cooling water (T_{SP}) the applied power loss initially increases the mean temperature of the four active components until reaching a steady level. With a sinusoidal load more than 30 power cycles are needed to reach a steady level. The regarded power module was tested under same conditions with online monitoring of on-state voltage and load current in [17]. Accordingly, the simulated power loss could at all-time be compared to real life data.

1) Module Temperature Field: In Fig. 8, the mean temperature of the topside and backside of the baseplate is plotted along a line placed at the center running parallel to the module long side. The curve is plotted at four time steps during a power cycle, where $t = 0$ notes the beginning of a steady cycle.

The flow rate in the Danfoss ShowerPower during power cycling is specified so the temperature of the cooling water varies less than 0.5°C. Accordingly, the baseplate backside temperature is seen to be close to T_{SP} even near the middle of the plate where the majority of heat dissipates. Similarly, the baseplate topside is close to the backside temperature with limited effect of the chosen time during a power cycle. The baseplate topside temperature is validated by comparison to images obtained by infrared thermography of an open black painted module subjected to similar power cycling conditions [35]. With a homogeneous convection approximation on the baseplate backside, as introduced in Section IV-B, the section position is seen to have limited effect on the baseplate surface temperature. An effect

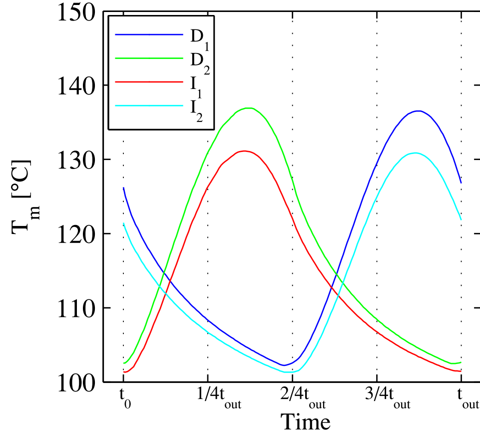

Fig. 9. Junction temperature of the four semiconductor components subjected to sinusoidal load conditions after reaching a steady cycle.

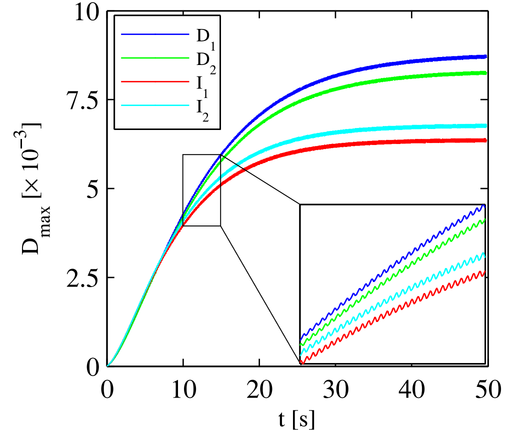

Fig. 11. Degradation evaluation near heel of end wire bond experiencing mean temperature as plotted in Fig. 9.

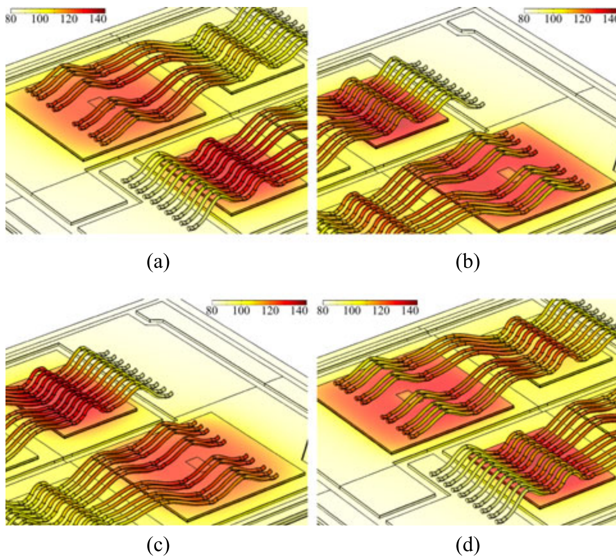

Fig. 10. Temperature surface plots of the active elements at selected points during one power cycle after reaching a stable mean junction temperature. Units are in $^\circ C$ (a) $T(\vec{r}, t_0)$. (b) $T(\vec{r}, t_0 + \frac{1}{4}t_{\rm out})$. (c) $T(\vec{r}, t_0 + \frac{2}{4}t_{\rm out})$. (d) $T(\vec{r}, t_0 + \frac{3}{4}t_{\rm out})$.

is observed when regarding the situation in 3-D. Here, due to the homogeneous boundary condition, the distribution is mirrored around the center of the module and small edge effects are observed in Sections I and VI.

2) Junction Mean Temperature: With the parameters presented in Table II, the mean junction temperature of the four chips are as presented in Fig. 9 .

In Fig. 10, the temperature distribution around the active components is presented at time t_0 and three time steps one fourth of the output time after: $t_0 + \frac{1}{4}t_{\rm tout}$, $t_0 + \frac{2}{4}t_{\rm tout}$, and $t_0 + \frac{3}{4}t_{\rm tout}$. The time t_0 notes the beginning of a power cycle after the mean junction temperature T_m of the different chips have reached a steady cycle. The sinusoidal load is naturally at its peak for I_1 and D_2 at $\frac{1}{4}t_{\rm tout}$ and I_2 and D_1 at $\frac{3}{4}t_{\rm tout}$. However, as presented in Fig. 9, the junction temperatures are still increasing after the peak power loss has been reached. This is due to the power loss still being higher than the outward flux due to water and passive cooling. As before mentioned, the junction and component surface temperature is in good agreement with experimental results obtained by online temperature estimation and infrared thermography of black painted modules, respectively (see [5], [35]).

3) Section Temperature: Fig. 10 shows a clear tendency of uneven temperature fields across the surface of the chips as reported on numerous occasions (see [5], [13], [15]). However, the majority of these results were obtained without including bond wires in the actual thermal simulations. The difference observed by including the bond wires on this particular geometry is significant. Power loss on both LS and HS chips are initially identical, however, due to the bond wires the LS and HS diode are not experiencing the same thermal reservoir. This is also visible in Fig. 2(b) were the Cu pad beneath the Al wire connection to the DCB is of noticeable less volume. This in total means the thermal impedance is not identical for the LS and HS diodes.

B. Simplified Degradation Model

From $T_m(t)$ in Fig. 9, a quick simplified simulation of the degradation function $D(\vec{r}, t)$ in a given region can be carried out. As presented in Fig. 1, the simulation of $D(\vec{r}, t)$ requires the plastic strain as input. Accordingly, an analytical equation is needed which, as discussed in Section IV-C, can be done from a 1-D assumption. Furthermore, a specific geometry needs to be specified for the degradation evaluation. From [5], it was clear that bond wire related issues was the primary concern, accordingly, a typical wire end bond is regarded. In Fig. 11, the peak degradation value (near the heel) is plotted against time for identical bond wire interfaces placed on the four chips.

In the accelerated test, the diodes are supposed to be stressed most severely, which is clearly seen in Fig. 11. Furthermore, as discussed in Section V-A, the LS components are experiencing a higher ΔT than the HS. This increased load is even more clear in this simplified degradation evaluation.

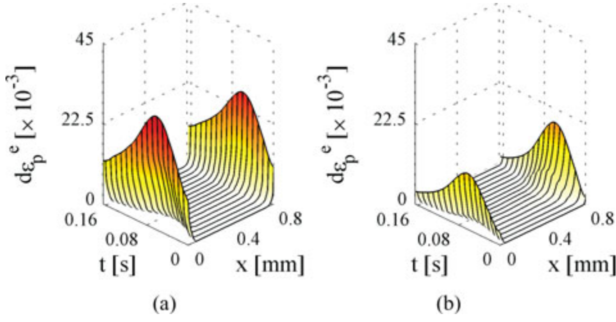

Fig. 12. Effective plastic strain plotted along a line x, placed in the center of the wire bond, for a complete power cycle t_{out}. (a) w_{11}. (b) w_{12}.

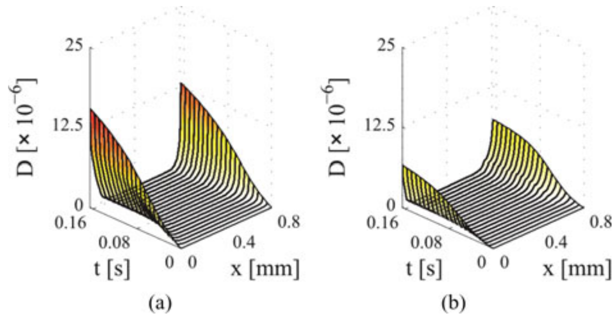

Fig. 13. Degradation function of (a) stitch bond and (b) end bond of w_1. (a) w_{11}. (b) w_{12}.

C. Detailed 3-D Degradation Simulation

1) Plastic Strain Field: Based on the temperature field the thermo-mechanical analysis is carried out as described in Section IV-C. As mentioned in the section, material hardening is presently included in the degradation assessment, but not the strain calculation. In Fig. 12, surface plots of the increase in effective plastic strain $d\epsilon_p^e$ in two interfaces are plotted for a line across the interface for a full power cycle. The interfaces regarded are w_{11} and w_{12} which are illustrated in Fig. 2(b). To limit the data presented only the effective plastic strain along a line from the beginning to the end of the bond is presented. The line is parallel to the wire curve placed in the center of the bond in the wire/metalization interface. To summarize, when following the plot along the first axes the spatial variation along the line is observed at a fixed time. Similarly, when moving along the second axes the time-resolved variation at a fixed position is observed. The motivation for plotting the change in effective plastic strain is to highlight the critical regions versus time.

As were expected $d\epsilon_p^e$ is highest, when the local temperature reach peak value, at the heel and toe of the interface. Heel and toe provide natural areas for crack propagation and are the main regions limiting expansion of the wire curvature.

From the derived temperature field and effective plastic strain (14)–(19) can be utilized for derivation of the degradation parameter $D(\vec{r}, t)$. In Figs. 13–17, surface plots of $D(\vec{r}, t)$ are presented in the same way as the effective plastic strain was in Fig. 12. The numbering in the figure captions is identical to

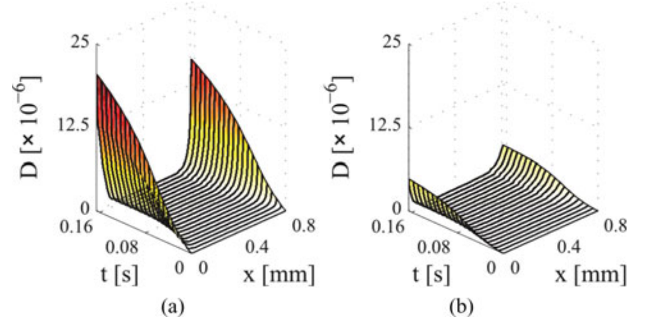

Fig. 14. Degradation function of (a) stitch bond and (b) end bond of w_2. (a) w_{21}. (b) w_{22}.

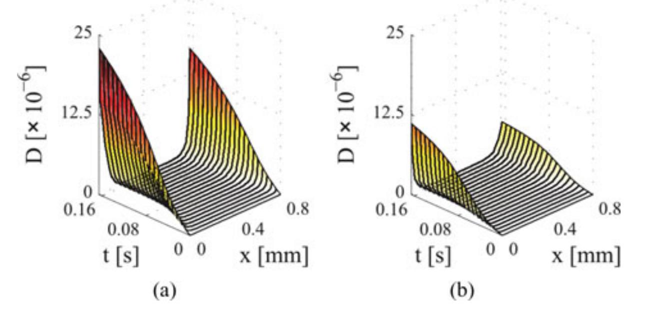

Fig. 15. Degradation function of (a) stitch bond and (b) end bond of w_3. (a) w_{31}. (b) w_{32}.

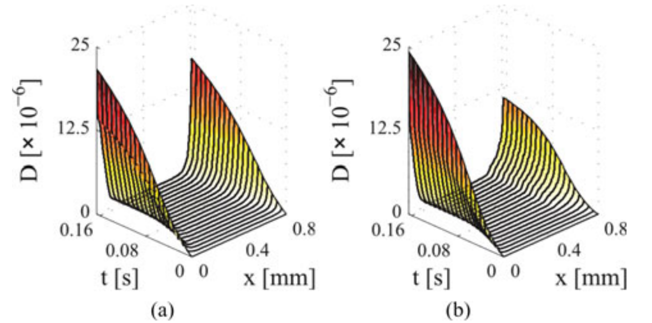

Fig. 16. Degradation function of (a) stitch bond and (b) end bond of w_4. (a) w_{41}. (b) w_{42}.

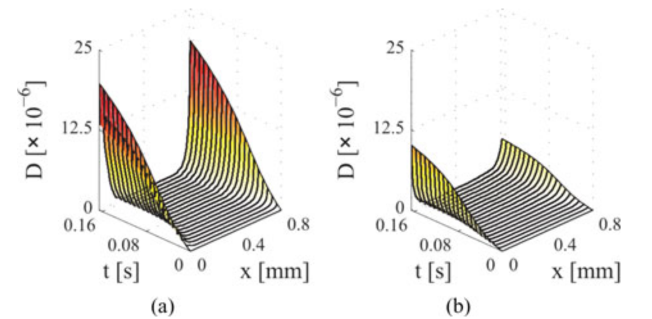

Fig. 17. Degradation function of (a) stitch bond and (b) end bond of w_5. (a) w_{51}. (b) w_{52}.

the concept presented earlier, the initial number denote the wire and the second the interface. Keep in mind that the degradation parameter is a unitless quantity and as such the absolute value of it is only relevant when compared to other positions, times, or failure criteria.

A clear tendency of the fastest degradation of the first interface (stitch bond) is observed in a majority of the images. Similarly, the degree of degradation is the largest near the beginning of the bond footprint. Finally, performing the same simulation for the remaining wire interfaces in the section indicates an uneven degradation rate between bonds. These can be divided into specific groups with some bonds being in multiple groups. The enumeration is ordered after degree of damage in a rising manner:

1) Wire interfaces facing another chip, in this example $w_{11}, w_{21}, ..., w_{91}, w_{101}$.
2) Clustered interfaces, in this example w_{31}/w_{32} and w_{41}/w_{42}.
3) Interfaces facing a wire curvature - End bonds are in general less damaged than stitch bonds.

VI. Discussion

From the simulated temperature fields, strain, and degradation function, it is clear that the sample chosen to illustrate the modeling approach shows nonhomogeneous wear in numerous ways: on module level with difference between sections, on section level with changing load between chips, and on chip level with differently affected wire bondings.

A. Parallel Sections in Power Modules

Calculation of the temperature field is the initial step to indicate problems in component design. In Fig. 2(a), a full module with six identical sections is illustrated. Even with a constant convection parameter and water-cooling temperature as a boundary condition, the mean temperature of the DCB ceramic depends on the section position. This is a commonly reported problem, even with water-cooling systems, and in this case the temperature difference is not critical.

B. High and Low Side Configuration

In numerous applications, the HS and LS problem with regard to active components is common. However, the present situation should not display such tendencies. The accelerated test setup was designed to apply a sinusoidal load similar to real life conditions with equally distributed power loss between similar components - which initially was the case. Over time, however, the LS diode displayed clear tendencies of increased stress - increase in forward voltage, and material changes from visual inspection after testing, see [17] and [19], respectively. This problem was through the temperature simulation alone (see Fig. 9) identified to be directly related to local temperature. The thermal reservoir experienced by the LS diode chip is simply not identical to the HS. As is clear from the degradation calculations this also accelerates the degradation of the interconnects, as indicated in the mean degradation parameter in Fig. 11. Temperature differences in between chips are, however, more critical. The accelerated test is designed to stress and damage the freewheeling diodes and this is also clear from the junction temperature plotted in Fig. 9. Initially, the power loss is identical in the HS and LS components which is also supported by measurements of the forward voltage in [5]. However, over time the forward voltage is observed to increase steadily on the LS diode (D_2) which is consistent with thermal simulations.

C. Bond Wire Degradation

Nonhomogeneous temperature distributions on the chip level is in the same way as on the module level a common problem. The center of the chip experiences a higher thermal impedance than the edge of the chips resulting in additional heating. This creates a tendency of faster material degradation near the center wire bonds compared to edge bonds.

The observed degradation behavior is to some degree consistent with experimental data. In general, the LS diode in this geometry under these load conditions has been reported on several occasions to be the failing part (see Section III-C and [17], [19], [21]). However, separating the individual wire bonds from each other is only carried out in [21]. On the diodes a tendency of center wire bonds to be degrading faster is clear, however, the variation in production seems to overpower the difference in wire bond position with regard to comparing individual bonds. This could be handled by inspecting additional samples. Regarding the first group presented in Section V-C a clear tendency with lifted wires is that bonds facing another chip are more inclined to fail (see [19]).

D. Fracture Analysis and Change in Electrical Parameters

The next step in this degradation evaluation would be to derive the fracture speed from the degradation function. In Fig. 11, one would specify a parameter D_{FC} as a fracture criteria and as a plane in Figs. 13–17. When $D(\vec{r}, t) > D_{FC}$ the region would be marked as fractured. The main approach for specifying the fracture criteria D_{FC} would be through experimental investigation of interface degradation using four-point probing. However, as mentioned above, additional data are needed.

From the mapping of the fracture parameter, however, it would be possible to plot the change in effective resistance of the individual bond wires through the method in Section V-C and a mean wire bond from Section V-B. This would enable either a very clear image of the module wear-out process or an approach for end-of-life assessment.

VII. Conclusion

A detailed 3-D modeling approach for simulation of thermomechanical degradation of interconnects in high power IGBT modules is presented. The model allows for simplifications speeding up the simulation process for end-of-life estimation as well as detailed mapping of the degradation distribution on individual wire level.

The model is built in a structured manner allowing for simulation of individual elements like power loss, temperature fields,

mechanical analysis, and material degradation (see Fig. 1). By separating these steps on an acceptable level, it is possible to initiate the model at any level by simply supplying the previous one as an external load. This allows for a stepwise increase in model detail to ensure the right information in the end. Presently, this has been utilized in many ways. The effect of the position of the individual sections on the baseplate is handled only in the thermal analysis. Similarly, the plastic strain field calculation, which is very time consuming, is limited in 3-D to specific wire bonds and on the large scale derived from a simplified 1-D slab model.

By applying the model to a specific case, a high power IGBT module subjected to a sinusoidal load under accelerated conditions, an image of the possibilities is outlined. From the thermal analysis design problems were found at both the module, section, and chip level (see Section V-A). While the module level distribution issues are common, and limited in the present situation, the section problem between LS and HS components is substantial. In Fig. 9, the average junction temperature is plotted for the four semiconductor components and while the difference on this scale seems marginal the difference in degradation speed is more pronounced (see Fig. 11). This problem is also consistent with experimental results as presented in [5] and [19].

Similar to the module level distribution issue, the temperature distribution on a power transistor or diode is commonly known. Wires placed near the center of a chip often delaminate or lift-off sooner than edge wires. This is also illustrated in Figs. 13–17 with the presented degradation fields, however, additional groupings of higher stressed bonds are possible. Wires closer to other active components are more stressed due to additional heating, and edge bonds are stronger than stitch bondings due to lack of wire curvature. All in all this illustrates the inadequacy of the commonly used lifetime estimation methods based on a standard CM or CM-A approach, and highlight the necessity of new more detailed multiphysics-based approaches.

Acknowledgment

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