Distributed Auxiliary Inverter of Urban Rail Train—The Voltage and Current Control Strategy Under Complicated Load Condition

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***Abstract*—With increasingly prominent role of rail transit in the entire urban transport system, an auxiliary inverter is used increasingly. The complicated and fluctuating load condition of the auxiliary inverter implies special designs about structure and control strategy are necessary. For this purpose, a comprehensive control strategy is proposed. First of all, this paper proposes a structure that is capable of suppressing unbalanced voltage. Second, the control strategy based on the resonant controller is proposed, which can balance split capacitors voltage, is capable of suppressing the effect of unbalanced load and nonlinear load. This paper introduces the design method of the control system in detail. Then, this paper simulates the proposed comprehensive control strategy in MATLAB. Finally, experimental results are presented, which fully demonstrate the excellent performance of the comprehensive control strategy.**

***Index Terms*—Nonlinear load, rail transportation, resonant controller, unbalanced load.**

I. Introduction

With urbanization of China, the role of rail transit is becoming more and more significant, because of outstanding advantages such as less pollution, larger capacity, and higher security. The rail transportation has become one of the most effective way in eliminating the limitations of urban traffic. As an indispensable part of the rail transit vehicle, an auxiliary inverter has been paid more and more attention. The function of the auxiliary inverter is to transform DC1500V or DC750V to AC380V, to supply the on-board electrical equipment.

On-board electrical equipment usually contains compressor, lighting device, electric heater, and computer, etc. These equipment can be divided into five categories:

1) unbalanced load (electric heater or single-phase load);
2) nonlinear load (inverter air conditioning, power supply of computer, and power electronic devices);
3) pump load (air conditioner, compressor, etc.);
4) sensitive load (contactor coil, computer, etc.);
5) ordinary load (lighting devices, etc.).

It can be found from the classification that the load of an auxiliary inverter covers almost all load types. However, a high quality output voltage is still required for protecting sensitive load. For example, dc bias in output voltage is highly possible to mistrigger or even burns the contactor coil. The demand for higher quality output voltage requires more advanced control strategy.

Because auxiliary inverter must support unbalanced load, a three-phase four-wire structure has to be employed. These three-phase four-wire structures can be divided into two categories normally: one is four-leg inverter [1]–[4], as shown in Fig. 1(a), which possesses superior performance with unbalanced load. However, the forth leg increases complicacy and costs and decreases stability. Another category is the conventional three-leg inverter structure, which is applied more widely. The three-leg inverter structure can be divided into "inverter with transformer" (△/Y0 transformer [5]–[7] and neutral point forming transformer inverter—NFTI [8]) and split capacitors inverter (SCI) [9], as shown in Fig. 1(b)–(d). As the control strategy of the △/Y0 transformer inverter is relatively simple, because the primary side of the transformer cannot provide the zero-sequence

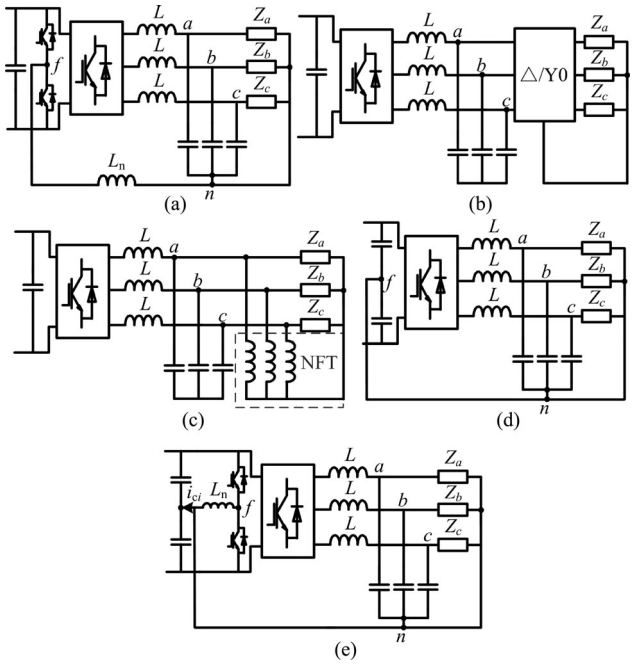

Fig. 1. Inverter topologies. (a) Four-leg inverter. (b) Inverter with △/Y0 transformer. (c) NFTI. (d) SCI. (e) Combination of (a) and (d).

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route, the structure does not need special control strategy to deal with zero-sequence component. However, owing to the Δ/Y0 transformer, volume, weight, and costs are larger or more than other structures. The split capacitors of an SCI not only acts as support capacitors but also provides the route of unbalanced current and ripple current, which means that split capacitors require larger volume and weight. Because there is pathway between point *f* and *n*, the ripple current in support capacitors and filter capacitors is larger than other structures, which makes the capacitors be vulnerable to ripple current. What is worse, an SCI needs special control strategy to eliminate neutral voltage bias of split capacitors. The most obvious advantage of the NFTI is that the pressure of the filter and support capacitors can be reduced. But the NFT still increases the costs, size, and weight. A topology of combining Fig. 1(a) and Fig. 1(d) has been proposed recently [10], [11], as shown in Fig. 1(e). The fourth leg is introduced to control neutral potential of split capacitors [10], the topology possesses the merits of less space occupation, less weight, and less capacitance of the split capacitors, however, the fourth leg makes the inverter more complex, and it is necessary for the application of extra transducers, as well as complicated control schemes [10].

Taking the existing and related achievements into consideration, the PID scheme [12], repetitive control [13]–[17], deadbeat control [18], $H\infty$ theory [13], and resonant controller [6], [19]–[23] have been all applied in the auxiliary inverter. The PID scheme has the merit of simply realization and the shortcoming of limited harmonic suppression capability. Repetitive control has the merit of theoretically full-band harmonic suppression capability, but stability is questionable. The deadbeat control designed for the digital system, has the merit of one beat delay tracking reference signal and the shortcoming of limited harmonic voltage suppression capability, as well as the $H\infty$ theory. Because of infinite gain in resonant frequency, the resonant controller is capable of suppressing harmonic and unbalanced voltage. However, complicated realization and the existence of digital control delay [24], [25] and discrete coupling [26] lead to unstable characteristic, especially high-order resonant controller.

This paper proposes a comprehensive control strategy, which can effectively provide excellent output characteristics even in complicated load condition. The comprehensive control strategy includes a topology and double-loop control strategy, as shown in Fig. 2. The topology introduces neutral inductance to SCI, and takes advantage of neutral inductance to eliminate disadvantages of the SCI. The topology has three advantages, first of all, neutral inductance can decrease ripple current of filter capacitors [2]. Limited by volume and the need for impedance matching, filter inductance value of high-power auxiliary inverter cannot be high enough to restrict ripple current of filter capacitors, therefore, filter capacitors are relatively easy to be damaged. Neutral inductance can restrict ripple current effectively and extend the lifetime of filter capacitors. Second, neutral inductance can suppress unbalanced voltage, because potential of point *n* can be smoothed by accurately designed neutral inductance value, which will be described in Section II in detail. Finally, volume and weight of neutral inductance are small and

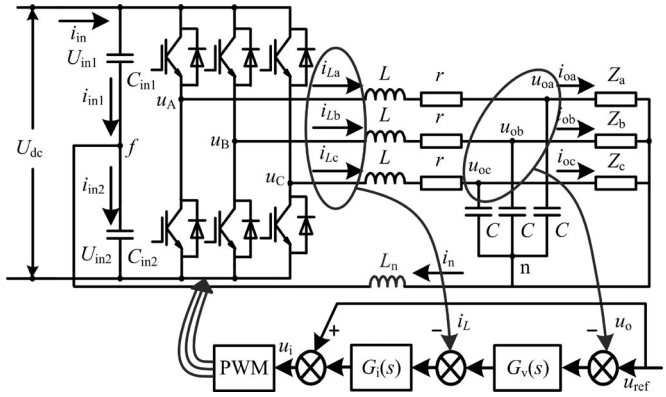

Fig. 2. Proposed structure.

light, because there is only unbalanced current and ripple current flows on neutral inductance. However, since the topology cannot completely eliminate the effect of complicated load, the cooperation with control strategy is necessary. This paper adopts the voltage and current double-loop control strategy; current loop adopts a simply proportional controller, the paper considers the effect of control delay and introduces design method in detail. Voltage loop adopts resonant controller, the paper synthesizes the demand of dynamic performance and stability, and proposes the design method of resonant controller. The control strategy based on a resonant controller not only eliminates the effect of complicated load condition but also balances split capacitors voltage automatically.

II. Advantages of the Proposed Structure

It is mentioned previously that neutral inductance is capable of suppressing ripple current and unbalanced voltage. According to the Kirchhoff Law, the model of the proposed structure can be derived

$$\begin{bmatrix} u_{\rm oa} \\ u_{\rm ob} \\ u_{\rm oc} \end{bmatrix} = G_{\rm op}(s) \begin{bmatrix} u_{\rm A} \\ u_{\rm B} \\ u_{\rm C} \end{bmatrix} - Z_{\rm op}(s) \begin{bmatrix} i_{\rm oa} \\ i_{\rm ob} \\ i_{\rm oc} \end{bmatrix} - Z_{\rm on}(s) \begin{bmatrix} i_{\rm n} \\ i_{\rm n} \\ i_{\rm n} \end{bmatrix} \tag{1}$$

$$G_{\rm op}(s) = \frac{1}{LCs^2 + rCs + 1} \tag{2}$$

$$Z_{\rm op}(s) = \frac{Ls + r}{LCs^2 + rCs + 1} \tag{3}$$

$$Z_{\rm on}(s) = \frac{L_{\rm n}s}{LCs^2 + rCs + 1} \tag{4}$$

where *L*/*C* is filter inductance/capacitor, *r* is parasitic resistance of filter inductance, $u_{\rm oa\sim oc}$ are the output voltage of the inverter, $u_{\rm A\sim C}$ are the output voltage of the leg, $i_{\rm oa\sim oc}$ are the output current of the inverter, $i_{\rm n}$ is the neutral current, which is equal to sum of inductance current. $Z_{\rm op}(s)$ is internal impedance of the inverter.

Equation (1) adequately considers impact of unbalanced load. In unbalanced load condition, potential of point *f* is fluctuant and voltage drop upon internal impedance is unbalanced, these two reasons result in unbalanced output voltage together. In

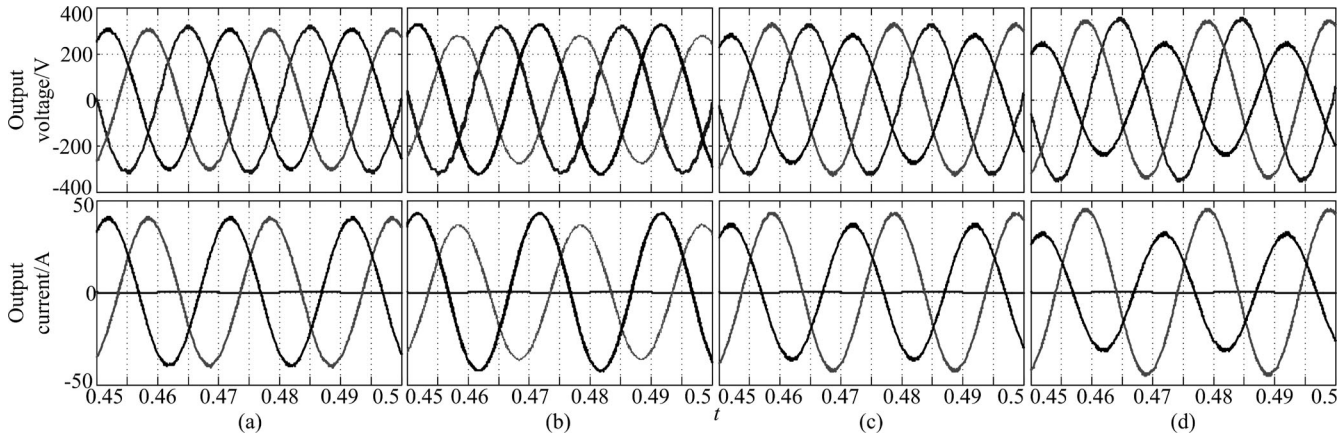

Fig. 3. Output waveforms of open-loop condition with unbalanced load. (a) $L_n = 2.3$ *m*H. (b) $L_n = 0$ *m*H. (c) $L_n = 4.6$ *m*H. (d) $L_n = 8$ *m*H.

order to eliminate the effect of unbalanced load, fluctuant potential of point *f* should be smoothed and unbalanced voltage drop should be balanced. Optimal neutral inductance value can smooth potential of neutral point, but eliminating unbalanced voltage drop should depend on the control strategy.

Assuming that unbalanced load $Z_{\rm a} = Z_{\rm b} = Z$ and $Z_{\rm c}$ is infinity. Take load condition into account and rewrite (1) as

$$\begin{bmatrix} u_{\rm oa} \\ u_{\rm ob} \\ u_{\rm oc} \end{bmatrix} = \begin{bmatrix} \dfrac{ZG_{\rm op}(s)}{Z+Z_{\rm op}(s)}u_{\rm A} \\ \dfrac{ZG_{\rm op}(s)}{Z+Z_{\rm op}(s)}u_{\rm B} \\ G_{\rm op}(s)u_{\rm C} \end{bmatrix} - \begin{bmatrix} \dfrac{ZZ_{\rm on}(s)}{Z+Z_{\rm op}(s)}i_n \\ \dfrac{ZZ_{\rm on}(s)}{Z+Z_{\rm op}(s)}i_n \\ Z_{\rm on}(s)i_{\rm n} \end{bmatrix}. \quad (5)$$

Neutral current can be derived as

$$i_n = sC(u_{\rm oa}+u_{\rm ob}+u_{\rm oc}) + \frac{u_{\rm oa}+u_{\rm ob}}{Z}. \quad (6)$$

By substituting (5) into (6), the neutral current can be expressed finally as

$$i_{\rm n} = \frac{[sCZ_{\rm op}(s)-1]G_{\rm op}(s)}{3sCZZ_{\rm on}(s)+sCZ_{\rm on}(s)Z_{\rm op}(s)+2Z_{\rm on}(s)+Z+Z_{\rm op}(s)}u_{\rm C}. \quad (7)$$

Whether balanced or unbalanced load, split capacitors voltage can be expressed as

$$\begin{aligned} U_{\rm in1} &= \frac{U_{\rm dc}}{2} + \frac{1}{C_{\rm in}}\int i_{\rm in1}dt \\ U_{\rm in2} &= \frac{U_{\rm dc}}{2} + \frac{1}{C_{\rm in}}\int i_{\rm in2}dt \end{aligned} \quad (8)$$

where $U_{\rm in1/2}$ are split capacitors voltage, $U_{\rm dc}$ is dc bus voltage, $C_{\rm in}$ is split capacitor ($C_{\rm in1} = C_{\rm in2} = C_{\rm in}$), and $i_{\rm in1/2}$ are split capacitors current.

For the Kirchhoff law, it gives

$$\begin{aligned} i_{\rm in1} + i_n &= i_{\rm in2} \\ U_{\rm dc} &= U_{\rm in1} + U_{\rm in2}. \end{aligned} \quad (9)$$

Combining (7), (8), and (9), potential of point *f* can be given as

$$u_f = \frac{U_{\rm dc}}{2} + \left[\frac{1}{2sC_{\rm in}} \cdot \frac{(sCZ_{\rm op}(s)-1)G_{\rm op}(s)u_{\rm C}}{3sCZZ_{\rm on}(s)+sCZ_{\rm on}(s)Z_{\rm op}(s)+2Z_{\rm on}(s)+Z+Z_{\rm op}(s)}\right]. \quad (10)$$

The aforementioned equation indicates that potential of point *f* oscillates around $0.5U_{\rm dc}$ and the oscillation has relationship with $u_{\rm C}$ and *Z*. According to (10), potential of point *n* can be derived as

$$u_n = \frac{U_{\rm dc}}{2} + \left[\left(\frac{1}{2sC_{\rm in}}+sL_n\right) \cdot \frac{(sCZ_{\rm op}(s)-1)G_{\rm op}(s)u_{\rm C}}{3sCZZ_{\rm on}(s)+sCZ_{\rm on}(s)Z_{\rm op}(s)+2Z_{\rm on}(s)+Z+Z_{\rm op}(s)}\right]. \quad (11)$$

Potential of point *n* is reference of $u_{\rm oa\sim oc}$, if potential of point *n* is more stable than potential of point *f*, which means that effect of unbalanced load can be suppressed partly. Comparing (10) and (11), the objective can be realized as long as (12) is satisfied

$$\left|\frac{1}{2sC_{\rm in}}+sL_n\right| < \left|\frac{1}{2sC_{\rm in}}\right| \quad (12)$$

Because fundamental component is the main part of the output voltage, unbalanced voltage mainly refers to fundamental voltage and harmonic component has little effect on unbalanced output voltage. Therefore, fundamental component is considered in (12) and the following equation can be derived:

$$0 < L_n < \frac{1}{(100\pi)^2 C_{\rm in}}. \quad (13)$$

If

$$L_{\rm n} = \frac{1}{2(100\pi)^2 C_{\rm in}}. \quad (14)$$

TABLE I
PARAMETERS TABLE

Sampling time t_s/s	1e-4	Current Loop K_p	5.35
Switching Period/Hz	5k	Voltage Loop K_{pr1}	0.058
Filtering inductance L/m H	1	Voltage Loop K_{ir1}	90
Parasitic resistance r/m Ω	100	PID strategy current loop K_p	5.35
Neutral inductance L_n /m H	2	PID strategy voltage loop K_p	0.11
Filtering capacitor C/u F	10	PID strategy voltage loop K_i	1
Split capacitor C_{in} /u F	2200	PID strategy voltage loop K_d	0.0001
PADE approach parameter a	1.33e4		

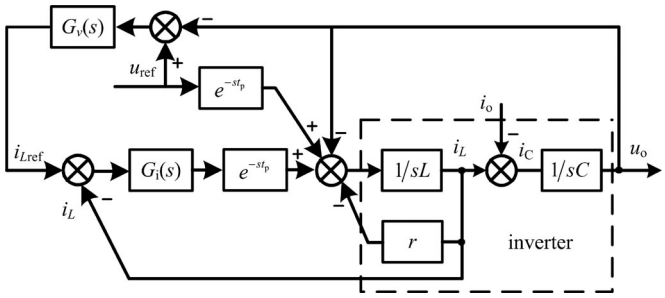

Fig. 4. Block diagram of inverter.

Potential of point n is equal to $0.5U_{dc}$ and unbalanced voltage can be immensely eliminated.

This paper simulates the aforementioned theory and the results are shown in Fig. 3; the control strategy adopts open-loop and circuit parameters except neutral inductance are presented in Table I. According to (13) and (14), the reasonable value of neutral inductance is between 0 and 4. 6 mH, and optimal value is 2. 3 mH. In Fig. 3, unbalanced load is $Z_a = Z_b = 7.5\Omega$ and Z_c is open circuit, Fig. 3(a) indicates that the optimal value of neutral inductance can immensely eliminate unbalanced phenomena, because the reference of output voltage can be smoothed by neutral inductance. However, neutral inductance cannot eliminate unbalanced voltage completely, eliminating unbalanced voltage drop in internal impedance needs an excellent control strategy. Neutral inductance values of Fig. 3(b) and (c) are 0 and 4.6 mH, respectively, which are boundary of reasonable value. Unbalanced phenomena is more serious than Fig. 3(a), and the unbalanced factors of Fig. 3(b) and (c) are almost identical. The most serious unbalanced phenomena is Fig. 3(d), because neutral inductance value of Fig. 3(d) is beyond reasonable value.

III. CONTROL STRATEGY OF RESONANT CONTROLLER

The main objective of the excellent control strategy is to decrease internal impedance, because neutral inductance does not constitute internal impedance, in order to build control model expediently, neutral inductance is neglected in the control model.

This paper adopts the traditional voltage and current double loop, as shown in Fig. 4. $G_v(s)$ and $G_i(s)$ are voltage controller and current controller, respectively; current loop adopts inductance current feedback, which has ability to limit inductance current. e^{-stp} is delay caused by the digital control system. If double-sampling mode is adopted, t_p can be reduced to $1.5t_s$ [27] (t_s is sampling time). The objective of voltage feed-forward scheme is to improve open-loop gain. In Fig. 4, u_{ref} is output voltage reference and i_{Lref} is inductance current reference.

Output voltage u_o can be derived as

$$u_o = G(s)u_{ref} - Z(s)i_o \tag{15}$$

where

$$G(s) = \frac{[G_v(s)G_i(s)+1]e^{-st_p}}{G_v(s)G_i(s)e^{-st_p} + sCG_v(s)e^{-st_p} + LCs^2 + rCs + 1}$$

$$Z(s) = \frac{G_i(s)e^{-st_p} + sL + r}{G_v(s)G_i(s)e^{-st_p} + sCG_i(s)e^{-st_p} + LCs^2 + rCs + 1}.$$

Equation (15) implies $G(s)$ and $Z(s)$ both can be controlled by $G_v(s)$ and $G_i(s)$, which means that it is possible to acquire excellent output characteristics by means of controlling $G_v(s)$ and $G_i(s)$; if (16) can be satisfied, excellent output characteristics will be achieved

$$\begin{cases} G(s) \approx 1 \\ Z(s) \approx 0. \end{cases} \tag{16}$$

Equation (16) guarantees excellent output voltage even in complex load condition, however, (16) cannot be realized easily, because lots of nonideal situation should be considered, such as control delay, discrete method, etc. These cases will seriously affect the output performance and stability.

A. Current Loop

Existing achievements have introduced the current loop design method [27], [28], however, most of them take no consideration of the control delay. This paper proposes a method to process control delay.

It is known that the current loop gain can be infinite in ideal system, but infinite gain is impossible in actual digital situation, because there is control delay in the digital control system. If current loop adopts a PID controller, the differential part of PID is likely to oscillate with delay, which makes the overall control system unstable. Therefore, the PID controller is not suitable for the current loop.

Extract current loop from Fig. 4 as

$$i_L = \frac{G_i(s)e^{-st_p}i_{Lref}}{G_i(s)e^{-st_p} + sL + r} + \frac{u_{ref}e^{-st_p} - u_o}{G_i(s)e^{-st_p} + sL + r}. \tag{17}$$

In (17), the control delay can be approximated by first-order PADE approach, as shown in (18), t_p is equal to $1.5t_s$ when control system acts in double-sampling mode [27]. PADE approach parameter a and circuit parameters are shown in Table I

$$e^{-st_p} = \frac{-s+a}{s+a}. \tag{18}$$

The existence of control delay makes it possible to oscillate in high-frequency area, it is necessary to choose appropriate controller to suppress the oscillation. For excellent voltage controller, $u_{ref}e^{-stp}$ is very close to u_o, (17) can be simplified into

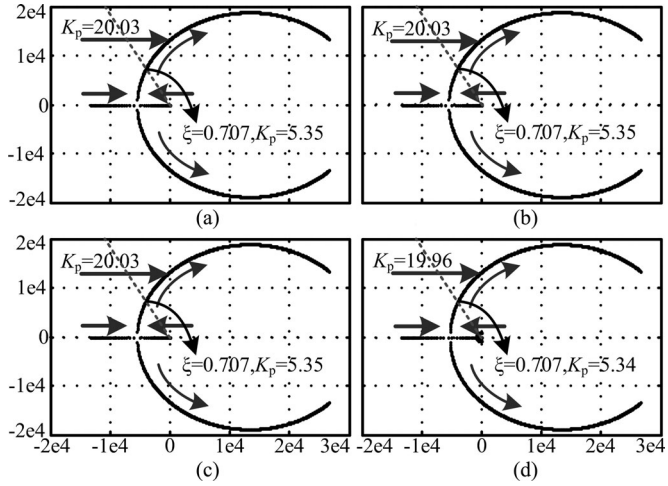

Fig. 5. Root locus diagrams with different integral parameters of $G_i(s)$. (a) K_p changes from 0 to 100 when K_i is equal to 0.001. (b) K_p changes from 0 to 100 when K_i is equal to 0.1. (c) K_p changes from 0 to 100 when K_i is equal to 10. (d) K_p changes from 0 to 100 when K_i is equal to 1000.

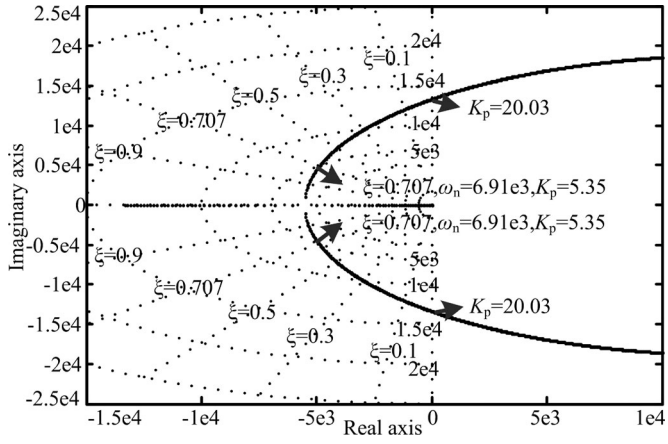

Fig. 6. Root locus with K_p changing from 0 to 100.

following equation:

$$i_L = \frac{G_i(s)(-s+a)i_{L\text{ref}}}{G_i(s)(-s+a) + Ls^2 + (aL+r)s + ar}. \tag{19}$$

If $G_i(s)$ adopts a PI controller, the root locus diagrams of (19) with different integral parameters are illustrated in Fig. 5. However, there are no obvious differences between four diagrams, the shape and stable region are almost identical and the optimal proportion parameters are almost identical (when ξ is equals to 0.707) too, which means integral parameter is useless. Therefore, a proportional controller is chosen finally.

Fig. 6 shows the root locus diagram with K_p changes from 0 to 100 when $G_i(s)$ is a proportional controller. It is obvious that $G_i(s)$ is critical stable when K_p is 20.03 and better performance can be achieved when K_p is 5.35.

The optimal value of K_p is obtained based on first-order PADE approximation, however, we cannot confirm the reasonableness of this approach. In Fig. 7, the comparison with different PADE approximation orders is given. Fig. 7(a) adopts first-order PADE

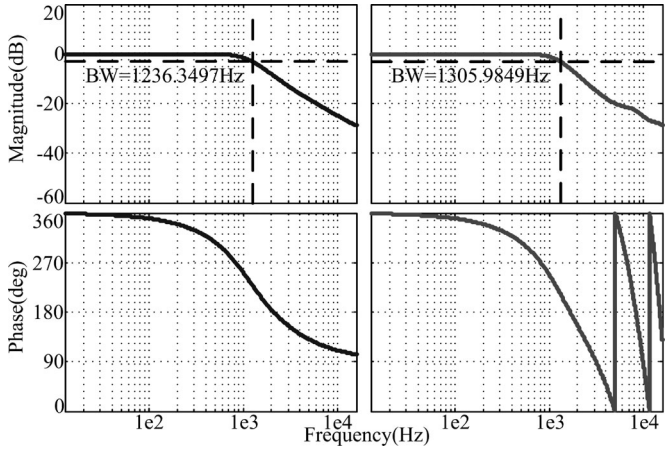

Fig. 7. Comparison of bode diagrams when PADE approximation order is different. (a) First-order PADE. (b) High-order PADE.

approximation and Fig. 7(b) adopts high-order PADE approximation, which is used to represent the control delay in actual system. Fig. 7 indicates that the obtained proportion parameter under first-order PADE approximation is still excellent in the actual system and the oscillation in high-frequency area is suppressed, the bandwidth is able to reach 1 kHz simultaneously, which is relatively good characteristics in 10-kHz sample frequency [29].

B. Voltage Loop

In voltage loop, a resonant controller [30], [31] is adopted, as shown in (20). For ac reference, the resonant controller can realize nonstatic error control; if ω_o is equal to fundamental frequency (50 Hz), the controller can offer excellent dynamic response and is provided with capacity of suppressing unbalanced voltage [32] and if ω_o is equal to harmonic frequency, the controller can offer excellent capacity of suppressing harmonic [32]

$$G_R(s) = \frac{K_{pr}s^2 + K_{ir}s}{s^2 + 2\omega_c s + \omega_o^2}. \tag{20}$$

The aforementioned equation has advantages of dc offset suppression and convenient parameters configuration. Fig. 8(a) indicates that low-frequency gain of the resonant controller is very low, which means dc offset in control strategy can be suppressed easily. Meanwhile low-frequency characteristic does not be affected by ω_c, ω_c can only affect the damping characteristic of the resonant point. Fig. 8(b) indicates that each parameter of the resonant controller can only affect part of full-band characteristic, K_{ir} can only affect low-frequency characteristic and K_{pr} can determine the gain of the full band, which means that parameters of the resonant controller can be configured conveniently.

Fig. 9 shows bode diagram of *G*(*s*) and *Z*(*s*) with fundamental and fifth, seventh, and eleventh resonant controller; control delay and current loop are both considered in Fig. 9. In Fig. 9(a), the gain below 1 kHz is approximately equal to 1. Fig. 9(b) implies that *Z*(*s*) is approximately equal to zero in 50, 250, 350, and 550 Hz. As fundamental impedance and harmonic impedance

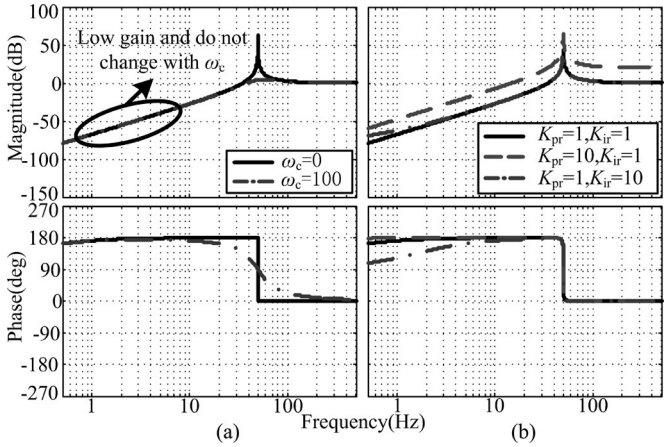

Fig. 8. Bode diagrams of the resonant controller. (a) Bode diagram of the resonant controller when $K_{\rm pr}=1$, $K_{\rm ir}=1$, $\omega_{\rm o}=100\pi$, and different $\omega_{\rm c}$. (b) Bode diagram of the resonant controller when $\omega_{\rm c}=1$, $\omega_{\rm o}=100\pi$, different $K_{\rm pr}$ and $K_{\rm ir}$.

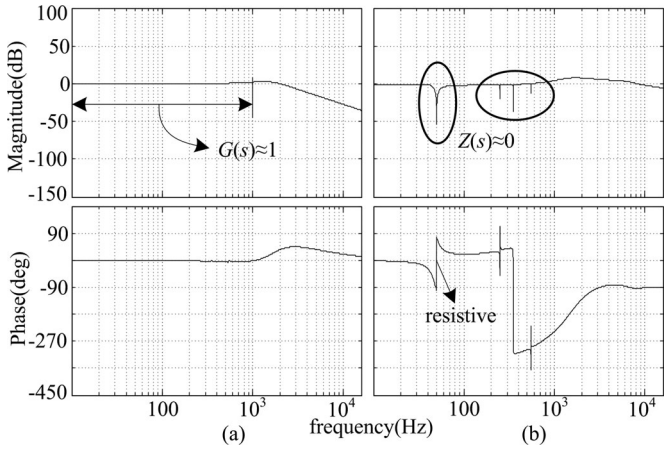

Fig. 9. Bode diagram of $G(s)$ and $Z(s)$ with first, fifth, seventh, and eleventh resonant controller. (a) Bode diagram of *G*(*s*). (b) Bode diagram of *Z*(*s*).

are approximately equal to zero, the effect of unbalanced load and nonlinear load can be suppressed. Fig. 9 indicates that (16) can be achieved approximately.

C. Parameters Configuration of the Resonant Controller

The papers [33] and [34] introduced the derivation of the resonant controller, but few of articles have ever introduced how to design the resonant controller. This paper proposes parameters configuration method and gives stability region of parameters in detail.

In Fig. 10, the bandwidth of the voltage loop mainly determined by $G_{R1}(s)$, $G_{R5}(s)$, and $G_{R7}(s)$ contribute to harmonic suppression, therefore, for calculating the bandwidth of voltage loop, $G_{R1}(s)$ is the only factor to be considered. From Fig. 10, it gives

$$u_o=\frac{(K_{\rm pr1}s^2+K_{\rm ir1}s)u_{\rm ref}-(s^2+2\omega_{c1}s+\omega_o^2)i_o}{Cs^3+(2\omega_{c1}C+K_{\rm pr1})s^2+(\omega_o^2C+K_{\rm ir1})s}. \quad (21)$$

Define $G_{\rm o}(s)=\dfrac{K_{\rm pr1}s+K_{\rm ir1}}{Cs^2+(2\omega_{\rm c1}C+K_{\rm pr1})s+\omega_{\rm o}^2C+K_{\rm ir1}}$.

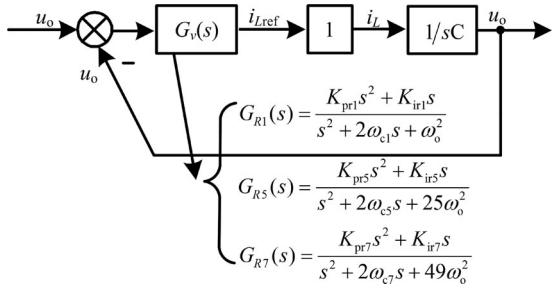

Fig. 10. Block diagram of system model below 1 kHz.

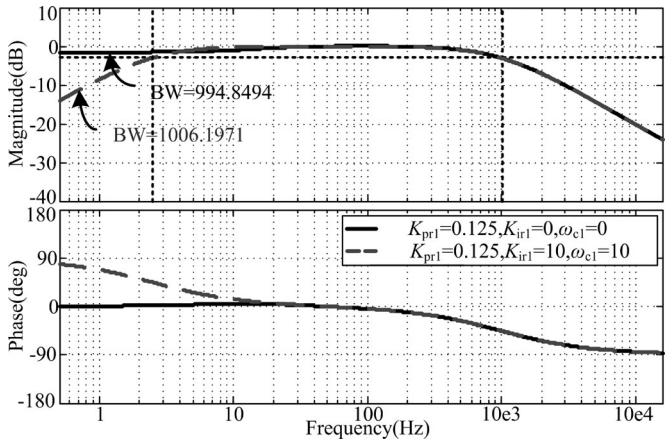

Fig. 11. Bode diagram of different parameters.

The bandwidth can be derived by simplifying $G_{\rm o}(s)$. It should be noted that $K_{\rm ir1}$ only appears in the constant term that mainly affects low-frequency characteristic and has little contribution to bandwidth, so $K_{\rm ir1}$ can be neglected. What is more, $\omega_{\rm c1}$ and C are both relatively small, so $2\omega_{\rm c1}C$ could be neglected too. Finally, $G_{\rm o}(s)$ can be simplified into

$$G_{\rm o}(s)=\frac{K_{\rm pr1}s}{Cs^2+K_{\rm pr1}s+\omega_{\rm o}^2C}. \quad (22)$$

According to the definition of bandwidth, substitute $s=j\omega$ into (22), it gives

$$\left|\frac{j\omega K_{\rm pr1}}{-C\omega^2+jK_{\rm pr1}\omega+\omega_o^2C}\right|=\frac{1}{\sqrt{2}}. \quad (23)$$

If the bandwidth is set to 1 kHz, $K_{\rm pr1}$ is equal to 0.125. Based on this, the bode diagram of different $K_{\rm ir1}$ and ω_{c1} could be plotted, as shown in Fig. 11, which further demonstrates the aforementioned exposition: when $K_{\rm pr1}$ is equal to 0.125, the bandwidth is substantially kept at 1 kHz in spite of different $K_{\rm ir1}$ and ω_{c1}.

Although $K_{\rm ir1}$ has little effect on bandwidth, it corrects the internal impedance to resistive, as shown in Fig. 9(b), which is beneficial to parallel operation of the inverter. $G_{R5}(s)$ and $G_{R7}(s)$ only contribute to harmonic suppression, parameters of which can be confirmed by experiment.

However, the bandwidth is not only determining factor, stability must be considered. The root locus of $K_{\rm pr1}$ is shown in

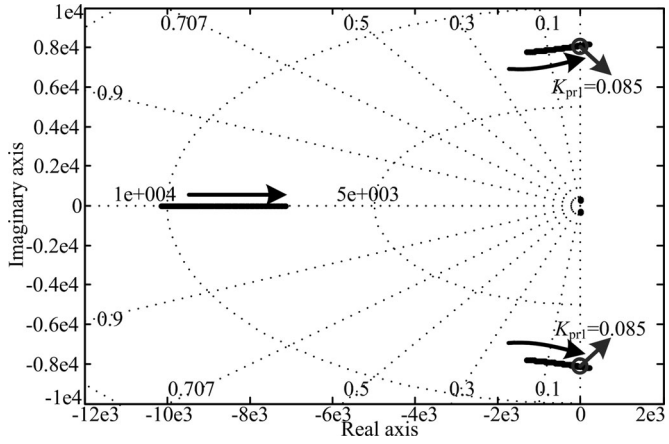

Fig. 12. Root locus about K_{pr1} and $K_{\mathrm{ir1}} = 0$ and $\omega_c = 0$.

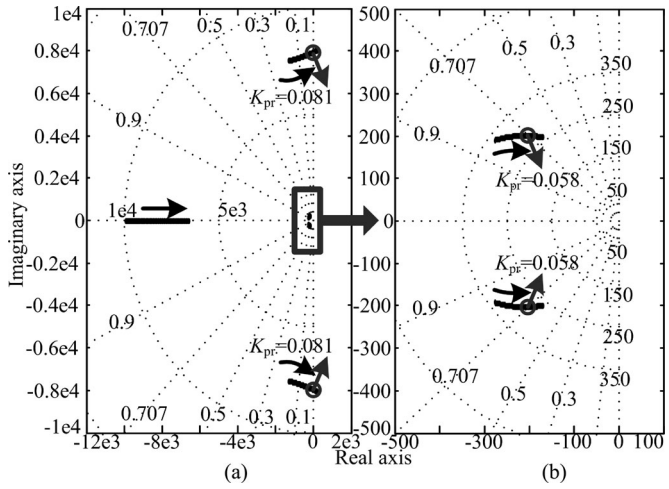

Fig. 13. Root locus about K_{pr1} and $K_{\mathrm{ir1}} = 90$ and $\omega_c = 0$.

Fig. 12, where $K_{\mathrm{ir1}} = 0$ and $\omega_c = 0$, it indicates that control system would become unstable if K_{pr1} exceeds critical stable value 0.085.

The root locus about K_{pr1} is shown in Fig. 13, where $K_{\mathrm{ir1}} = 90$ and $\omega_c = 0$. Comparing with Fig. 12, the left diagram of Fig. 13 indicates that the critical stable value of K_{pr1} decreases (from 0.085 to 0.081) when K_{ir1} increases (from 0 to 90). The right diagram indicates that the optimal value of K_{pr1} is 0.058 when K_{ir1} is equal to 90. However, the optimal value does not always exists, because the shape of root locus will change with variation of K_{ir1}, if the variation of K_{ir1} leads to the poles (damping coefficient ξ is 0.707) do not exist, the optimal value would disappear.

Fig. 14 shows the relationship between K_{ir1} and K_{pr1}. Curve1 is about the critical stable value of K_{pr1}, the critical stable value of K_{pr1} will decrease when K_{ir1} increases. Curve2 is about the optimal value of K_{pr1}, the optimal value of K_{pr1} will increase when K_{ir1} increases. Fig. 14 indicates that the optimal value of K_{pr1} will appear when K_{ir1} is greater than 78, and the optimal value will exceed the critical stable value when K_{ir1} is greater than 94, so K_{ir1} should be selected between 78 and 94. In order to make a compromise between stability and

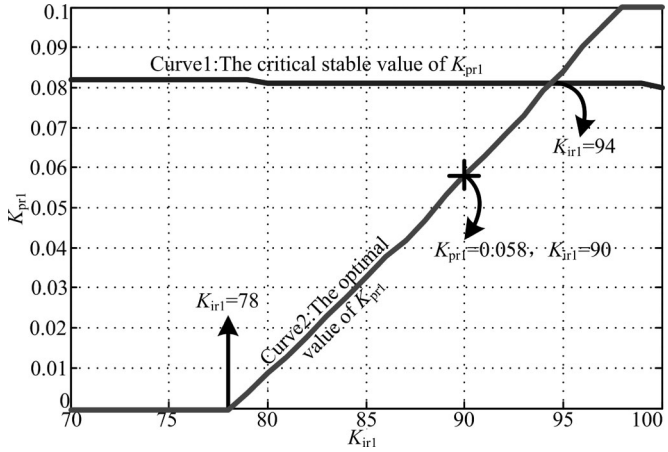

Fig. 14. Relationship between K_{pr1} and K_{ir1} when $\omega_c = 0$.

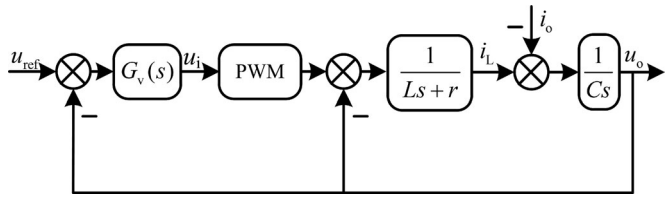

Fig. 15. Simplified control model.

dynamic characteristics, K_{ir1} cannot be so small that dynamic characteristics is limited and also cannot exceed 94. Based on the aforementioned discussion, $K_{\mathrm{pr1}} = 0.058$ and $K_{\mathrm{ir1}} = 90$ are selected finally.

IV. Elimination of Unshared Voltage in the Split Capacitors

In Section I, the topology in Fig. 1(e) implies extra devices and complex control scheme are necessary for balancing split capacitors voltage. The paper [35] introduced a novel method to balance capacitors voltage, however, the method also needs extra power switches. This paper adopts the proposed resonant controller, the shared voltage of the split capacitors could be realized automatically.

The cause of unshared voltage across the split capacitors is versatile, such as different capacitance, equivalent series resistance, and switching devices. Among all reasons, the existence of dc component in the sample system and unbalanced load are the most important.

For convenient explanation, a simplified control scheme is shown in Fig. 15; this paper assumes that there is only voltage loop, current loop and voltage feed-forward are ignored, it gives

$$u_{\mathrm{i}} = (u_{\mathrm{ref}} - u_{\mathrm{o}})G_{\mathrm{v}}(s). \tag{24}$$

where u_{i} is the input of the modulation strategy, u_{ref} is voltage reference, u_{o} is output voltage, and $G_{\mathrm{v}}(s)$ is the transfer function of the voltage controller.

Equation (24) implies that the duty ratio of switch comes from the comparison of u_{ref} and u_{o}, because u_{ref} is sinusoidal reference, dc bias does not exist in u_{ref} obviously. However, due

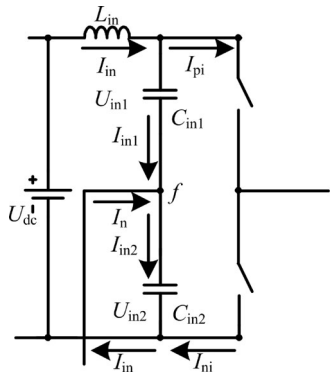

Fig. 16. Simplified inverter model.

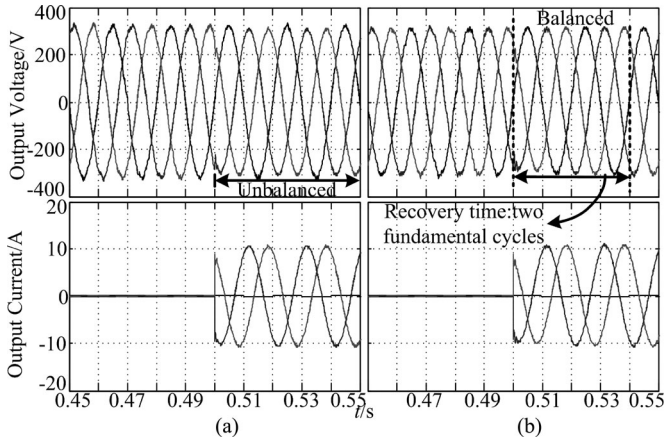

Fig. 17. Voltage and current waveforms with unbalanced load. (a) PID strategy. (b) Proposed control strategy.

to imperfect sampling system, dc bias is likely to be present in $u_{\rm o}$, it is possible that dc bias of $u_{\rm i}$ will be amplified and accumulated, especially when $G_{\rm v}(s)$ includes integrator, it implies that turn-on time of upper and lower switch will become different, which makes the voltage of split capacitors be unshared. In order to simplify the analysis, a simplified inverter model is shown in Fig. 16.

All current in Fig. 16 is RMS and switches are simplified to be ideal. It is assumed that T is fundamental period, $T_{\rm up}$ is turn-on time of upper switch and $T_{\rm down}$ is turn-on time of lower switch. The injected energy of $C_{\rm in1}$ in one fundamental period is

$$P_{C{\rm in}1} = \int_0^T I_{\rm in}^2 dt - \int_0^{T_{\rm up}} I_{\rm pi}^2 dt. \tag{25}$$

The injected energy of $C_{\rm in2}$ in one fundamental period is

$$P_{C{\rm in}2} = \int_0^T I_{\rm in}^2 dt - \int_0^{T_{\rm down}} I_{\rm ni}^2 dt. \tag{26}$$

1) If $T_{\rm up}$ is equal to $T_{\rm down}$, because $I_{pi} = I_{ni}$, $P_{Cin1} = P_{Cin2}$ can be derived, the voltage of split capacitors can be balanced.
2) If $T_{\rm up}$ is not equal to $T_{\rm down}$, the voltage of split capacitors will be unbalanced.

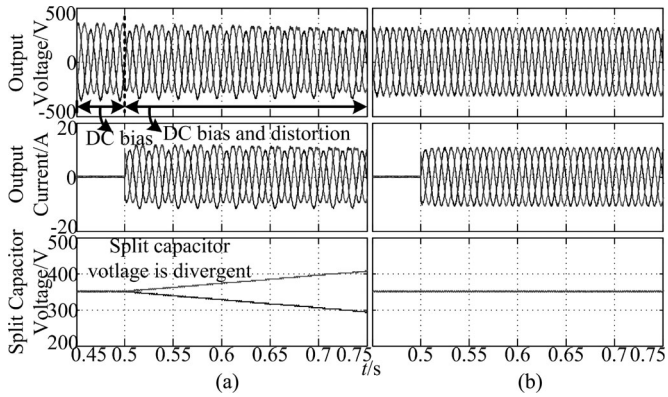

Fig. 18. Simulation waveform with instantaneous balanced load in inaccurate AD sampling. (a) PID strategy. (b) Proposed control strategy.

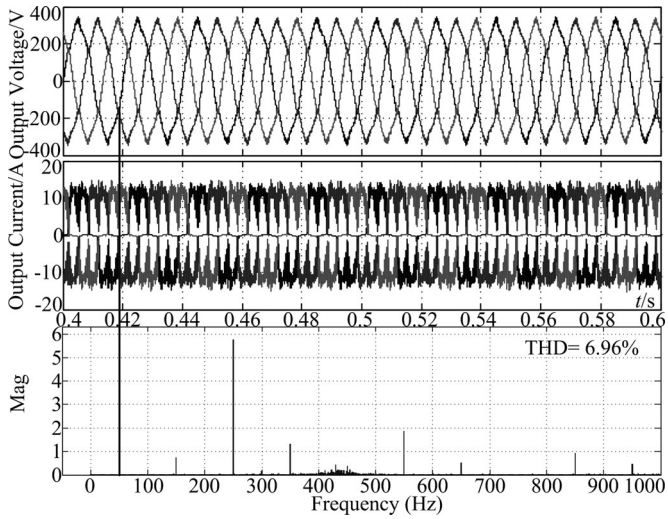

Fig. 19. Simulation waveform with nonlinear load in PID strategy.

Obviously, the longer turn-on time will prompt the lower voltage of corresponding switch, and vice versa.

The aforementioned problem can be resolved by the proposed strategy. Due to excellent capability of dc bias suppression, which has been illustrated in Fig. 8, if $G_{\rm v}(s)$ is the resonant controller, dc bias in $u_{\rm o}$ cannot affect $u_{\rm i}$, and turn-on time of upper and lower switch would be identical. Finally, the voltage of split capacitors can be balanced.

V. Simulation

The simulation model is built in Simulink and is carried out in 5-kVA power rate. The parameters used in the simulation are listed in Table I and the discretization of the resonant controller adopts PREWARD [36]. The paper compares the proposed control strategy with PID strategy [12], the parameters of the PID strategy are listed in Table I too.

Fig. 17(b) adopts the proposed strategy and gives the result of loading unbalanced load at 0.5 s, the output voltage drops temporarily but recovers quickly (about two fundamental cycles) and output voltage maintains balanced. Fig. 17(a) gives the simulation result in the same load condition with the PID control

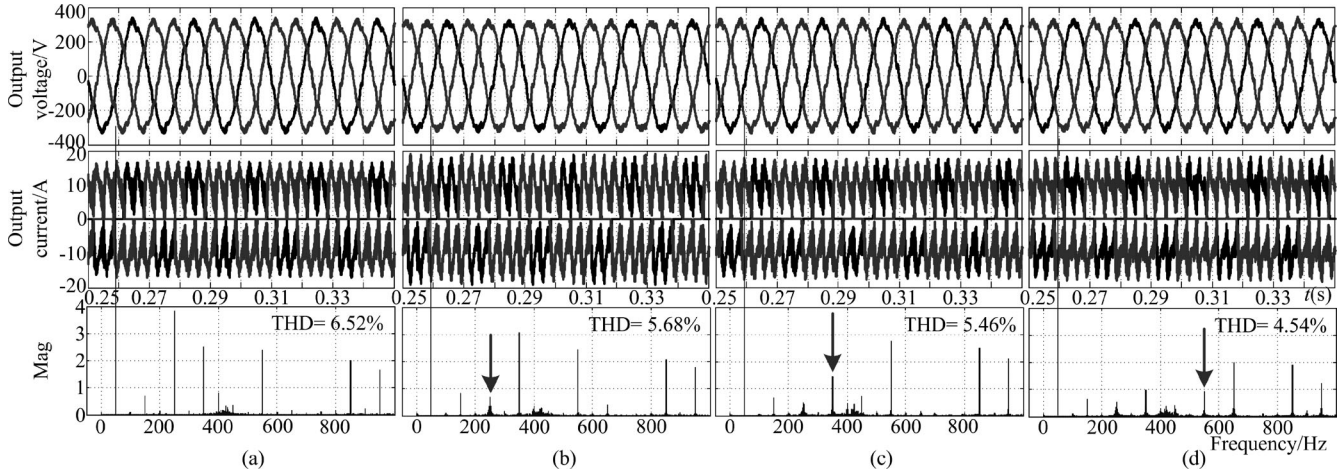

Fig. 20. Simulation results of proposed control strategy. (a) Only fundamental control. (b) With fifth harmonic control. (c) With seventh harmonic control. (d) With eleventh harmonic control.

strategy, when unbalanced load is loaded at 0.5 s, the balanced output voltage turns into unbalanced simultaneously. In order to carry out a more detailed comparison, this paper introduces unbalance factor (UF), which is defined as the ratio of zero-sequence component and positive-sequence component of the output voltage. The UF of Fig. 17(a) is 1.25% and of Fig. 17(b) is 0.107%, which indicates that the proposed strategy has better performance on suppressing the unbalanced output voltage.

Fig. 18 gives the simulation results with inaccurate AD sampling, +10% dc bias exists in sampling of phase A, and –10% dc bias exists in sampling of phase B and C. The PID strategy is used in Fig. 18(a) and the proposed control strategy is applied in Fig. 18(b). The dc bias exists in output voltage and distortion appears after loading in Fig. 18(a), because inaccurate AD sampling is accumulated by the PID controller so that divergence arises in split-capacitors voltage. However, due to low dc gain, the problem can be solved by the proposed control strategy. It is obvious that dc bias and distortion do not exist in Fig. 18(b).

The output voltage and fast Fourier transform (FFT) analysis result with nonlinear load are shown in Fig. 19. The PID strategy is powerless to suppress the effect of nonlinear load, which can be known from total harmonic distortion (THD) (6.96%) and low-order harmonic content. The reason is that harmonic impedance of the inverter is relatively high, and cannot be decreased by the PID strategy.

The output voltage and the FFT analysis results with nonlinear load are shown in Fig. 20. In Fig. 20(a), there is only fundamental control, THD is 6.52%. In Fig. 20(b), with fundamental control and fifth harmonic control scheme, the fifth harmonic is suppressed, THD is reduced to 5.68%. In Fig. 20(c), with fundamental, fifth and seventh harmonic control scheme, the seventh harmonic is suppressed, THD is reduced to 5.46%. In Fig. 20(d), with fundamental, fifth, seventh, and eleventh harmonic control scheme, the eleventh harmonic is suppressed, THD is further reduced to 4.54%. As shown in Fig. 20, low-order harmonics can be suppressed by the resonant controller and output voltage can be changed to be more sinusoidal. However, the resonant controller is not omnipotent in harmonic suppression, from Fig. 20

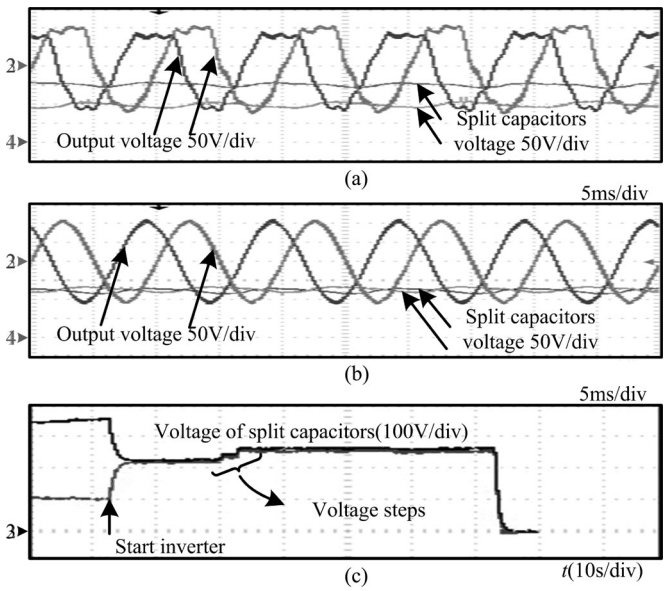

Fig. 21. Experimental results of suppressing neutral potential deviation. (a) With PID controller. (b) With resonant controller. (c) DC-link voltage step experiment with resonant controller.

we know that high-order harmonics will be enlarged when a resonant controller is used, and the order of the effective resonant controller cannot be more than eleventh, otherwise control system will be unstable.

VI. Experimental Results

In order to verify the rationality of the proposed control strategy, a prototype platform (5 kVA) is built. Experimental parameters are listed in Table I, and the discretization approach of the control system adopts PREWARD [36].

The comparative experiment of suppressing neutral potential deviation is shown in Fig. 21, the voltage loop of (a) adopts a PID controller, (b) adopts the proposed controller strategy. The results show that the PID controller cannot suppress neutral po-

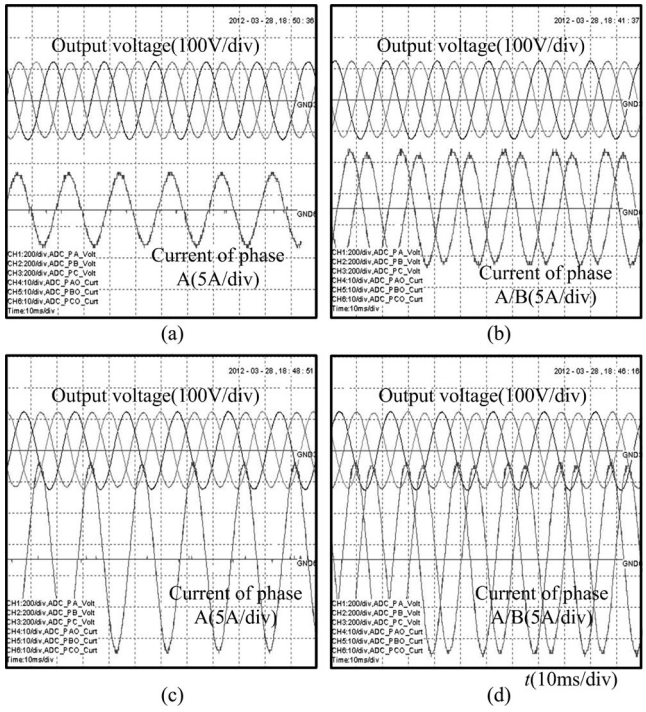

Fig. 22. Output waveforms with unbalanced load. (a) Single phase with half load. (b) Two phase with half load. (c) Single-phase with full load. (d) Two phase with full load.

tential deviation, and voltage of split capacitors is unbalanced, because voltage of one split capacitors is so low that half period of output voltage distorts. However, the proposed control strategy can suppress neutral potential deviation, so voltage of split capacitors is balanced. The dc-link voltage step experiment with a resonant controller is shown in Fig. 21(c), with seriously unequal initial voltages, it is obvious that balanced voltage is achieved quickly when inverter starts, and the balance is not affected by the change of dc-link voltage. The conclusion is that the resonant controller is provided with excellent capability in suppressing neutral potential deviation.

The output voltage of the inverter with unbalanced load is shown in Fig. 22. Waveforms are sampled by a virtual oscilloscope through Ethernet [37]. In Fig. 22(a) and (c), only phase A is loaded. In Fig. 22(b) and (d), phase A and B are both loaded simultaneously. From Fig. 22, it is obvious that balanced output voltage is achieved even with unbalanced load.

Figs. 23–25 are experimental waveforms with nonlinear load. In Fig. 23, only fundamental resonant controller is applied. Fig. 23(a) shows the waveform of phase voltage, Fig. 23(b) shows FFT result of phase voltage, and Fig. 23(c) is sampled by a virtual oscilloscope. In Fig. 23, the THD is highest, fifth harmonic and seventh harmonic are 3.6% and 2.5%, respectively. In Fig. 24, the fifth harmonic resonant controller is added, the fifth harmonic is suppressed greatly, THD is reduced from 5.2% to 4.6%, which shows output voltage is more sinusoidal than Fig. 23. In Fig. 25, seventh harmonic resonant controller is added, the seventh harmonic is suppressed greatly, THD is reduced to 3.8%, which shows output voltage is more sinusoidal than Fig. 24.

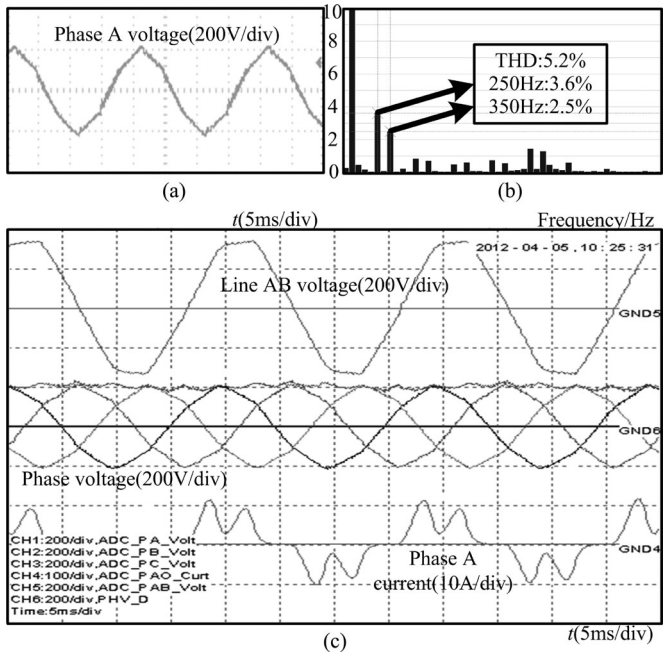

Fig. 23. Experimental results of nonlinear load under fundamental resonant controller. (a) Phase A voltage. (b) FFT analysis of (a). (c) Waveforms are displayed by a virtual oscilloscope through Ethernet.

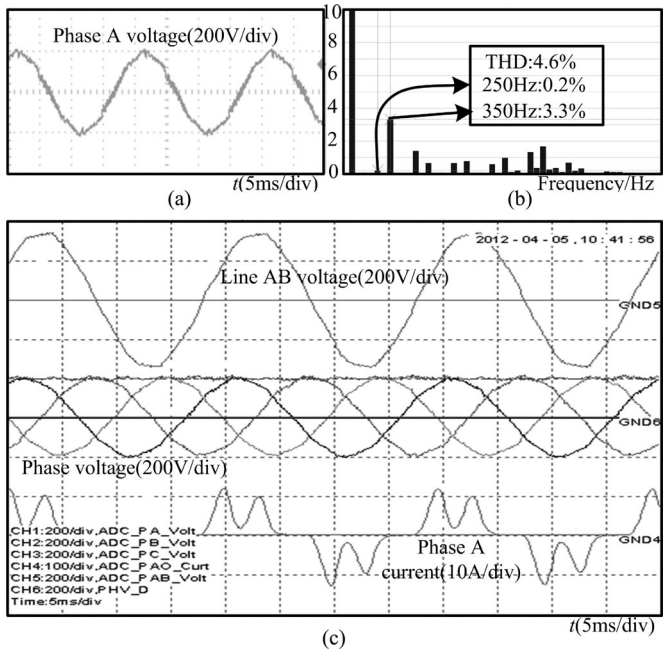

Fig. 24. Experimental results of nonlinear load under fifth resonant controller. (a) Phase A voltage. (b) FFT analysis of (a). (c) Waveforms are displayed by a virtual oscilloscope through Ethernet.

The aforementioned experimental results indicate that the proposed control strategy is very effective in suppressing effect of nonlinear load, however, the capacity is restricted to low-order resonant controller, the discrete coupling, truncation error, and control delay in the digital system make it unstable with more than seventh-order resonant controller.

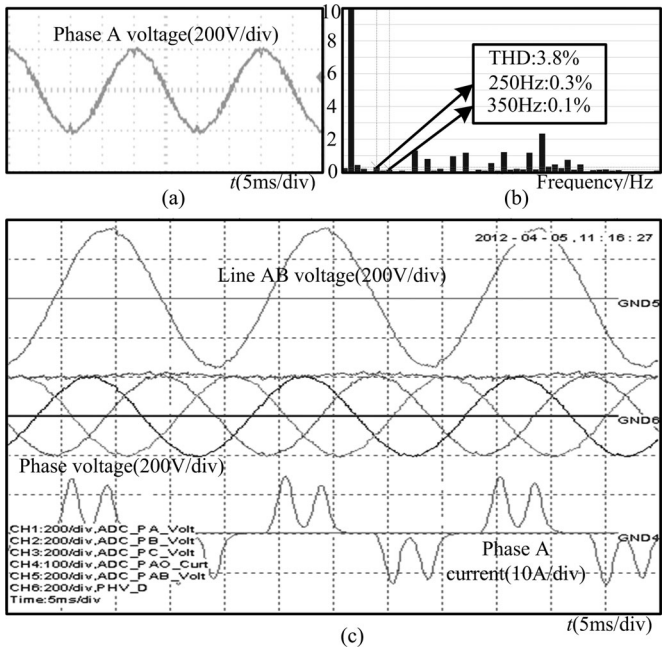

Fig. 25. Experimental results of nonlinear load under seventh resonant controller. (a) Phase A voltage. (b) FFT analysis of (a). (c) Waveforms are displayed by a virtual oscilloscope through Ethernet.

VII. Conclusion

In order to make the auxiliary inverter have excellent output characteristics in complicated load condition, this paper proposes a comprehensive control strategy, which includes a topology and double-loop control strategy. The topology combines neutral inductance with an SCI and utilizes neutral inductance to regulate the reference potential of the output voltage. The smoothed reference potential greatly decreases unbalanced voltage. The double-loop control strategy adopts voltage and current double closed loop. The current loop adopts simply proportion controller, this paper considers digital delay and presents a current loop design method. The voltage loop adopts a resonant controller; this paper synthesizes the demand of dynamic performance and stability, and presents a design method of the resonant controller. The proposed comprehensive control strategy greatly suppresses the effect of unbalanced load and nonlinear load, is provided with excellent dynamic performance and stability.

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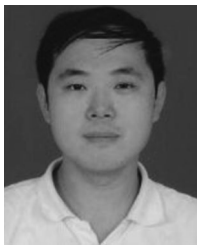

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