Burst Mode Elimination in High-Power LLC Resonant Battery Charger for Electric Vehicles

Navid Shafiei, *Student Member, IEEE*, Martin Ordonez, *Member, IEEE*, Marian Craciun, *Member, IEEE*, Chris Botting, *Member, IEEE*, and Murray Edington, *Member, IEEE*

***Abstract*—In order to recover and fully charge batteries in electric vehicles, smart battery chargers should not only work under different loading conditions and output voltage regulations (close to zero to 1.5 times the nominal output voltage), but also provide a ripple-free charging current for battery packs and a noise-free environment for the battery management system (BMS). In this paper, an advanced LLC design procedure is investigated to provide advantageous extreme regulation and eliminate detrimental burst mode operation. A modified, special LLC tank driven by both variable frequency and phase shift proves to be a successful solution to achieve all the regulation requirements for battery charging (from recovery, bulk, equalization, to finish). The proposed solution can eliminate the negative impact of burst mode noises on the BMS, provide a ripple-free charging current for batteries in different states of charge, reduce the switching frequency variation, and facilitate the EMI filter and magnetic components designs procedure. In order to fully consider the characteristics of the full bridge LLC resonant converter, especially the output voltage regulation range and soft transitions of the MOSFETs in the fixed frequency phase shift mode, a new set of analytical equations is obtained for the LLC resonant converter with consideration of separated primary and secondary leakage inductances of the high frequency transformer. Based on the proposed strategy and analytical equations, multivariate statistical design methodology is employed to design and optimize a 120 VDC, 3-kW battery charger. The experimental results exhibit the excellent performance of the resulting converter, which has a peak efficiency of 96.5% with extreme regulation capability.**

***Index Terms*—Battery charger applications, full bridge *LLC* resonant converter, full soft switching conditions, hybrid modulation strategy, recovering dead battery, wide output voltage regulation.**

NOMENCLATURE

C_j	Diode junction capacitance (F).
C_s	Series resonant capacitance (F).
$C_{w,s}$	Winding capacitance of the transformer secondary side (F).
f_0	Series resonant frequency (Hz).
$f_{r,oc}$	Open-circuit resonant frequency (Hz).
$f_{r,sc}$	Short-circuit resonant frequency (Hz).
f_s	Switching frequency (Hz).
$I_{L_{s_1}}$	Peak current of the first series resonant inductance (A).
$I_{L_{s_2}}$	Peak current of the second series resonant inductance (A).
I_{out}	Dc output current (A).
L_{ext}	External series inductance (H).
$L_{lk,p}$	Transformer primary leakage inductance (H).
$L_{lk,s}$	Transformer secondary leakage inductance (H).
L_m	Transformer magnetizing inductance (H).
L_n	Resonant inductance ratio $(L_n = L_{s1}/L_p)$.
L_p	Parallel resonant inductance (H).
L_s	Series resonant inductance ratio $(L_s = L_{s1}/L_{s2})$.
L_{s_1}	First series resonant inductance (H).
L_{s_2}	Second series resonant inductance (H).
M_{V_r}	Ac–ac voltage transfer function due to the first harmonic.
M_{V_R}	Ac–dc voltage transfer function of the current driven rectifier.
M_{V_s}	Dc–ac voltage transfer function of the full bridge inverter.
n	Transformer turns ratio $(n = N_p/N_s)$.
Q_L	Loaded quality factor.
R_L	Load resistance (Ω).
V_{AB_1}	First harmonic of the full bridge inverter.
$V_{R_{eq}}$	Output voltage amplitude of the LLC resonant inverter.
V_{in}	Dc input voltage (V).
V_{out}	Dc output voltage (V).
Z_0	Series characteristic impedance (Ω).

Manuscript received November 16, 2014; revised February 11, 2015; accepted March 22, 2015. Date of publication April 6, 2015; date of current version September 29, 2015. This work was supported by the Natural Sciences and Engineering Research Council, Canada. Recommended for publication by Associate Editor S. Williamson.

N. Shafiei and M. Ordonez are with the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC V6T 1Z4 Canada (e-mail: navid@ece.ubc.ca; mordonez@ieee.org).

M. Craciun, C. Botting, and M. Edington are with Delta-Q Technologies Corporation, Burnaby, BC V5G 3H3 Canada (e-mail: mcraciun@delta-q.com; cbotting@delta-q.com; murray.edington@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2420573

I. INTRODUCTION

RECENTLY, the technology of rechargeable battery packs (Li-ion, lead-acid, NiMH, etc.) has been improved for deeply discharged conditions in order to provide more energy for powering electric motors in electric vehicles (EVs). In most applications, batteries are subjected to a complex charging profile which is determined by the battery type [1]–[6]. According to Fig. 1, the battery charge profile includes three main phases: bulk (max charging current), absorption (constant voltage), and finish (a limited current to offset the internal soft discharge). During the bulk phase, the battery is less than fully charged and the maximum charging current is provided while monitoring the battery voltage. In the absorption mode, the charger increases the battery voltage to V_{abs}, which is typically specified by the battery manufacturer. At this point, the battery has been charged to between 70% and 90% of its capacity and the remainder is filled with the slower topping charge that occurs during absorption phase. Under certain circumstances, if the battery pack is

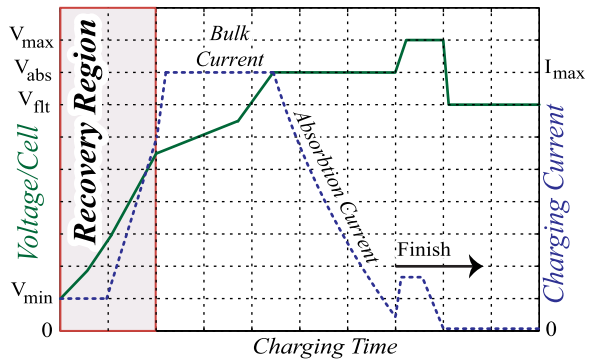


Fig. 1. Different steps of deep-cycle battery charging profile including recovery region.

judged to be out of balance, an overcharge mode is performed to equalize the voltage of the cells in a battery module [7]–[9]. According to Fig. 1, the most difficult charging cycle occurs when the battery pack has been discharged completely owing to either overdischarging or extended storage time. In this situation, the voltage of the battery pack drops into dead-zone, close to zero volts per cell (recovery region) [9]–[12]. Due to the battery's different operating modes, it is necessary to design and implement smart battery chargers that can respond to the battery charge profile. Recently, various studies have been dedicated to developing reliable and high-efficiency battery chargers for EVs [1]–[6], [9]–[18]. Among power converter topologies, phase shift full bridge (PSFB) power converter and resonant power converters have attracted the most attention. Depending on the technologies and packages available for power MOSFETs (e.g., drain-source resistance, power dissipation, cooling), it is appropriate to employ a full bridge inverter for several kilowatt dc–dc power applications. The conventional PSFB can regulate the output voltage widely by increasing the phase shift (PS) between two legs of the inverter, but PSFB loses the soft switching condition in light loads and/or wide output voltage regulation [13], [14]. This problem can be solved by increasing the series inductance. However, the drawback of the large series inductance is that it causes higher peak current, which leads to lower efficiency, and more voltage and current stresses on passive and active elements [14]. Several approaches for the PSFB, including symmetric passive auxiliary circuit, hybrid converters, fixed-variable duty cycle, and self-sustained oscillating control, have been studied in order to extend the output voltage regulation, while providing soft switching condition for semiconductor elements [14]–[17], [19]. However, extreme regulation, which is essential for the recovery region has not been studied yet for PSFB. Another problem with the conventional PSFB converter is that it causes voltage peak across the output rectifier diodes, which gives rise to a higher blocking voltage. Different techniques, such as *LC* circuits, RCD networks, and active rectifiers, have been presented for the PSFB in order to eliminate the voltage peak across the output rectifier diodes, but resolving the negative impact on efficiency and reducing the number of active and passive circuits still remain as research opportunities [15]–[17]. Softly switched resonant converters are also candidates for the design of battery chargers, due to their capability to produce variable voltage gains in different operating frequencies [9]–[12], [18], [20]–[30]. A fifth order $L3C2$ resonant converter for battery charging application has been studied that can regulate output voltage over a wide range [18]. This resonant converter can absorb parasitic inductances and capacitances of the elements and circuit effectively, employing them as resonant elements. However, wide switching frequency variation of the fifth order resonant converter creates difficulties in terms of optimum design.

The softly switched LLC resonant converter is another resonant topology that has recently been employed due to its ability to handle high power and produce variable voltage gains in different operating frequencies while providing soft switching for all semiconductor devices [21], [24]–[28]. Theoretically, this topology allows the output voltage of the LLC resonant converter to be decreased by increasing the switching frequency. However, the existence of parasitic capacitances (diode junction, transformer secondary side, and PCB layers) leads to undesired oscillation in the secondary side of the transformer and limits the maximum operating frequency [9]–[12], [18], [31]. Fig. 2(a) presents the full bridge inverter based on MOSFET switches and the LLC resonant circuit schematic along with parasitic elements. Fig. 2(b) shows the normalized voltage gains of the LLC resonant converter compared to frequency, with and without consideration of the parasitic capacitances effect of the transformer secondary side. According to this figure, because there are few parasitic capacitances (fewer than 300 pF in this study), their effect on the voltage gain curves is considerable only in light and no-load conditions. These parasitic capacitances lead to a second resonant frequency in the voltage gain curves, which is far from the short circuit resonant frequency ($f_{r,sc}$). After the maximum switching frequency, the voltage gain at no-load or light-load conditions (e.g., blue and purple curves) increases as the switching frequency increases, causing reverse polarity of the feedback signal and turning negative feedback into positive feedback. This problem is usually dealt with using a dummy load in the output of the converter. However, in battery charger applications, employing dummy loads in the output leads to the battery slow discharging, which is not acceptable. This feedback reversal necessitates the use of burst mode strategy in the LLC resonant converter designs. Based on the continuous conduction mode (CCM) and burst mode operation control technique (combined variable frequency (VF), 150-450 kHz, fixed on time and fixed frequency variable on time), Musavi *et al.* designed and implemented an LLC resonant converter as a lead-acid battery charger [9], [10], [32], [33]. Generally, burst mode strategy is employed in light and no-load conditions in order to provide wide output voltage regulation and have proven successful for LED applications [32], [33], rather than battery chargers. Fig. 2(c) illustrates the principle operation of burst mode along with resonant converter waveforms. According to this figure, in burst mode, the switching driver signals are turned-on and off periodically with an intermittent cycle much lower than the main switching frequency. Although employing burst mode leads to better regulation, the interaction between parasitics capacitances (including MOSFET drain-source and diodes junction) and the resonant circuit elements leads to high frequency oscillation

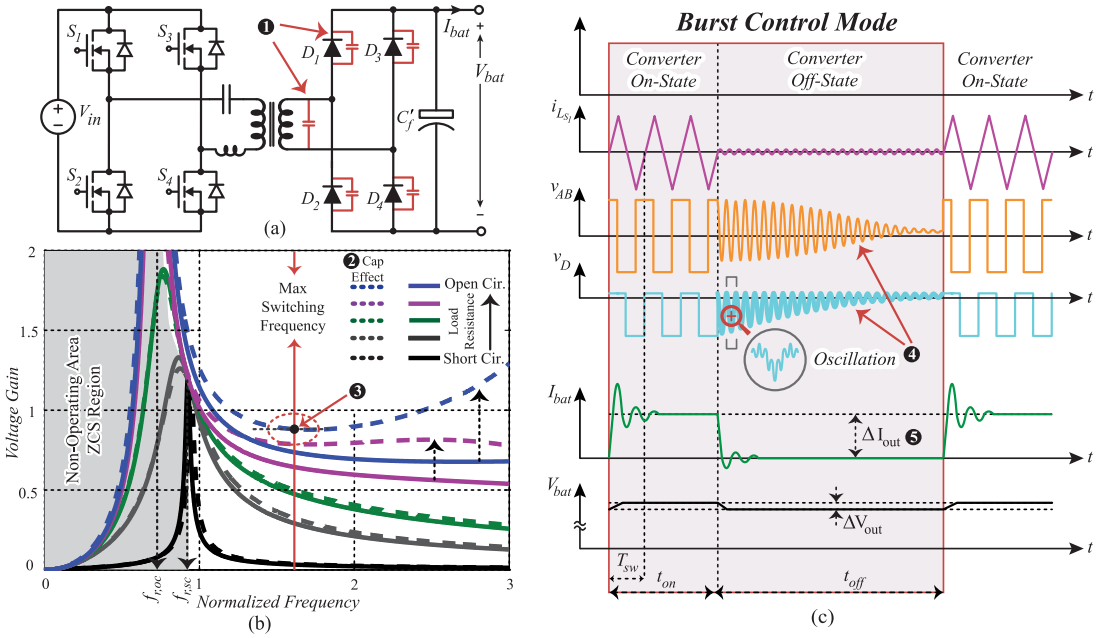


Fig. 2. (a) Full bridge LLC resonant converter schematic and the parasitic capacitances ①, (b) effect of the parasitics capacitors on the voltage gaine curves ②, LLC voltage gain issues ③, and (c) burst mode and its issues: high frequency oscillation due to the interaction between parasitic capacitances (MOSFET drain-source and diodes junction) and the resonant circuit ④, battery charging current ripple ⑤.

during converter off-state and produces high EMI noises, which have a negative effect on battery management system (e.g., unwanted tripping in recovery mode, interfering with the sensing and feedback circuit). Moreover, burst current ripple and ripple in general can affect the battery life cycle. In other words, the cleaner the charging current, the longer the battery's lifespan. Fig. 2(c) shows the ripple and ringing issues introduced by burst operating mode in battery chargers.

In this paper, an advanced LLC design procedure is investigated to provide advantageous extreme regulation and eliminate detrimental burst mode operation. A modified, special LLC tank driven by both VF and PS proves to be a successful solution to achieve all the regulation requirements for battery charging (from recovery, bulk, equalization, to finish). In particular, the performance in the recovery region allows the elimination of burst mode, resulting in a significant practical advancement for high efficiency battery chargers. The proposed LLC tank and modulation strategy is applied to a high power full-bridge topology, which is able to regulate the output voltage from close to zero to 1.5 times the nominal output voltage under different output load conditions. The ability of the full bridge LLC resonant converter to operate with soft-switching transitions (in all operating regions) without employing burst mode operation, provides a noise free environment for all auxiliary circuits, and effectively increases the performance of the battery charger. Moreover, the process provides almost ripple-free charging current in order to charge batteries in different states of charge, which can increase battery lifespan. Furthermore, the proposed modulation strategy leads to a limited switching frequency variation of the LLC resonant converter; as a result the selection of magnetic parts (including high frequency transformer, and resonant inductor), control circuit, and semiconductor devices are facilitated. In order to optimize the design procedure and deal with multiple parameters, multivariate statistical design is used to consider the steady-state equations behavior. The experimental results, extracted from a 3-kW power platform prove that the proposed proposed LLC tank and modulation strategy can effectively increase the range of output voltage regulation from no-load to full-load conditions without employing detrimental burst mode.

II. Secondary Leakage Inductance Effect on Wide Regulation

The principle and operation modes of the LLC resonant converter with nonideal transformer have been discussed in many papers. Typically, the literature replaces the high frequency transformer with a second order model, which incorporates effective leakage inductance along with magnetizing inductance, and employs an ac equivalent circuit for steady-state analysis [21], [25]–[28]. Due to the existence of leakage inductance not only in the primary side, but also in the secondary side, a virtual voltage gain should be introduced, which presents the effect of secondary leakage inductance on the LLC voltage gain [34], [35]. However, failing to consider the leakage inductance in the transformer's secondary side in the equivalent ac circuits, results in incorrect steady state equations for the input impedance phase and input resonant circuit current, which are essential for wide regulation, soft switching, and high efficiency power converter design procedure. In this paper, primary and secondary leakage inductances of the transformer are considered separately in order to examine the effect of secondary leakage inductance on the output voltage regulation and obtain a more accurate steady-state analysis. The complete schematic of the LLC resonant

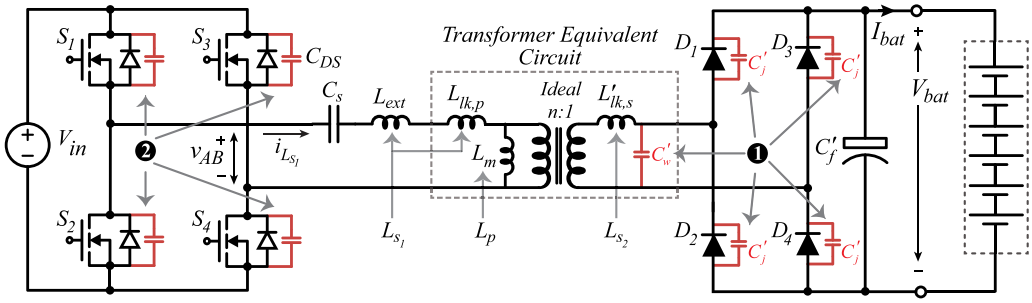


Fig. 3. Full bridge LLC resonant converter schematic along with parasitic elements (including MOSFET drain-source capacitances, transformer elements, and output rectifier diodes junction capacitances). ① indicates that the parasitic capacitances in the secondary side of the circuit causes unwanted oscillation and the regulation issue for the LLC resonant converter. ② indicates MOSFETs drain-source effective capacitances that should be discharged completely during dead time intervals.

converter with a nonideal transformer has been presented in Fig. 3. According to this figure, the nonideal transformer has been replaced by a third order model equivalent circuit [36], [37]. The secondary leakage inductance and the magnetizing inductance of the transformer are considered L_{s_2} and L_p, respectively. The primary leakage inductance is absorbed by the external resonant inductor and is a part of L_{s_1}. In this study, the equivalent capacitor in the secondary side of the transformer (including diode junction, transformer secondary side, and PCB layers) has been calculated and measured less than 300 pF after selecting the output rectifier diodes and fabricating the transformer. According to Fig. 2(b), this amount of equivalent parasitic capacitances can make difference just in light and no-load conditions. Due to the designing the LLC resonant converter in nominal operating point (nominal output voltage and maximum output current), the effect of this parasitic capacitances is negligible and considering this parasitic capacitances in the steady-state procedure just results in too complicated equations without any advantage. It is necessary to mention in order to draw the voltage gains of the LLC resonant converter with these parasitic capacitances, the voltage gain equation of the fifth order $L3C2$ resonant converter should be employed [20]. Also, the MOSFETs drain-source capacitances just can affect the inverter transient behaviour and do not participate in the resonant circuit steady-state analysis. Fig. 4(a) demonstrates three main parts of the LLC resonant converter, namely, the full bridge inverter, resonant circuit, and output rectifier. Fig. 4(b) shows the ac equivalent circuit of the LLC resonant converter with separated primary and secondary leakage inductances. Note that other parasitic inductances in both primary and secondary side of the transformer are integrated in L_{s_1} and L_{s_2} (e.g., PCB traces, transformer connection, diodes pins). In this figure, the variables and elements are transferred to the primary side of the transformer (without an apostrophe). The steady-state analysis of the resonant converter can be carried out by using this ac equivalent circuit and first harmonic approximation (FHA) analysis [5], [9], [18], [20], [21]. According to this figure, the input impedance of the resonant circuit is obtained as follows:

$$\mathbf{Z_{in}}(j\omega_s) = \frac{1}{j\omega_s C_s} + j\omega_s L_{s_1} + (j\omega_s L_p)||(j\omega_s L_{s_2} + R_{eq}). \tag{1}$$

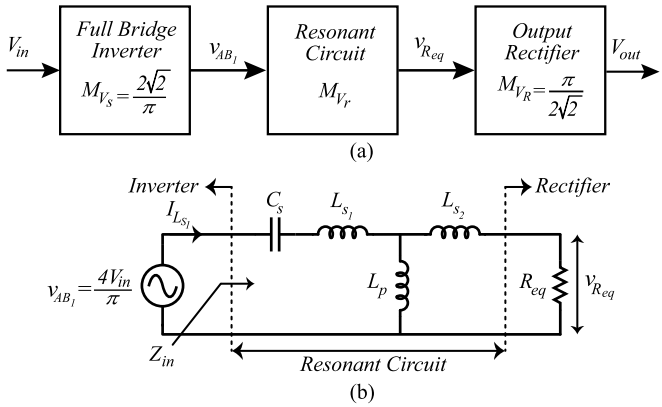


Fig. 4. (a) Block diagram of the LLC resonant converter with capacitive output filter, and (b) ac equivalent circuit of the LLC resonant converter.

The following normalized parameters are introduced for the resonant circuit:

$$Q_L = \frac{R_L}{Z_0},\ Z_0 = \sqrt{\frac{L_{s_1}}{C_s}},\ \omega_0 = \frac{1}{\sqrt{L_{s_1} C_s}}$$
$$\omega_n = \frac{\omega_s}{\omega_0},\ L_s = \frac{L_{s_1}}{L_{s_2}},\ L_n = \frac{L_{s_1}}{L_p}. \tag{2}$$

Considering (1) and (2), the normalized input impedance can be expressed as

$$\frac{\mathbf{Z_{in}}(j\omega_n)}{Z_0} = \left(j\omega_n + \frac{1}{j\omega_n}\right) + \frac{\frac{j\omega_n}{L_n}\left(\frac{j\omega_n}{L_s} + Q_L\right)}{\frac{j\omega_n}{L_n} + \frac{j\omega_n}{L_s} + Q_L}$$
$$= \left|\frac{\mathbf{Z_{in}}(j\omega_n)}{Z_0}\right| e^{j\varphi}. \tag{3}$$

In the above equation, φ indicates the phase of the input impedance and should be positive in all operating conditions to provide turn on zero voltage switching (ZVS) conditions for power MOSFETs. Operation in this mode is recommended for practical applications. In the LLC resonant converter with selected L_n and L_s, there is a resonance frequency f_r for each constant value of Q_L which is defined as the boundary condition between capacitive and inductive regions and occurs at the peak

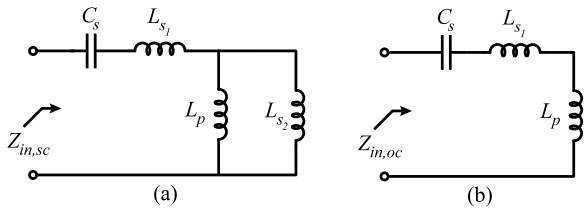


Fig. 5. (a) Ac equivalent circuit in short-circuit condition, (b) ac equivalent circuit in open-circuit condition.

of the voltage gain curves. The minimum and maximum range of f_r versus Q_L variation is located between open-circuit and short-circuit resonant frequency, respectively. Fig. 5(a) and (b) shows the ac equivalent circuit of the LLC resonant converter in output short-circuit and open-circuit conditions, respectively. The normalized input impedance and resonant frequency in the conditions described are calculated as follows:

$$\frac{Z_{\text{in},sc}(j\omega_n)}{Z_0} = \frac{1-\left(1+\frac{1}{L_n+L_s}\right)\omega_n^2}{j\left(\frac{1}{L_n}+\frac{1}{L_s}\right)\omega_n},$$
$$\omega_{n,sc} = \frac{1}{\sqrt{1+\frac{1}{L_n+L_s}}} \tag{4}$$

$$\frac{Z_{\text{in},oc}(j\omega_n)}{Z_0} = \frac{1}{j\omega_n}+j\omega_n\left(1+\frac{1}{L_n}\right),$$
$$\omega_{n,oc} = \frac{1}{\sqrt{1+\frac{1}{L_n}}}. \tag{5}$$

According to (4), short-circuit resonance frequency depends on L_s, and for a nonideal transformer the short circuit resonant frequency is always less than unity. By setting the input impedance phase equal to zero, the normalized resonant frequency can be obtained, which is presented in (6) shown at the bottom of the page. Fig. 6 shows $\frac{\omega_r}{\omega_0}$ versus loaded quality factor for $L_n = 1$ and different constant values of L_s. According to this figure, a low value of L_s (existence of the secondary leakage inductance) leads to a narrow range of resonant frequency variation versus loaded quality factor, and *vice versa*. In other words, low values of L_s in the LLC resonant converter put the open-circuit and short-circuit resonant frequency close to each others, which lead to steeper voltage gain curves and therefore these curves can approach almost zero voltage in high frequency, which means better output voltage regulation with less switching frequency variation. This finding is particularly important to achieve extreme regulation for the battery charger while keeping a limited frequency range.

In order to figure out the voltage transfer function, it is necessary to calculate the voltage gain of each part of the LLC resonant converter. According to Fig. 4(a), the voltage transfer

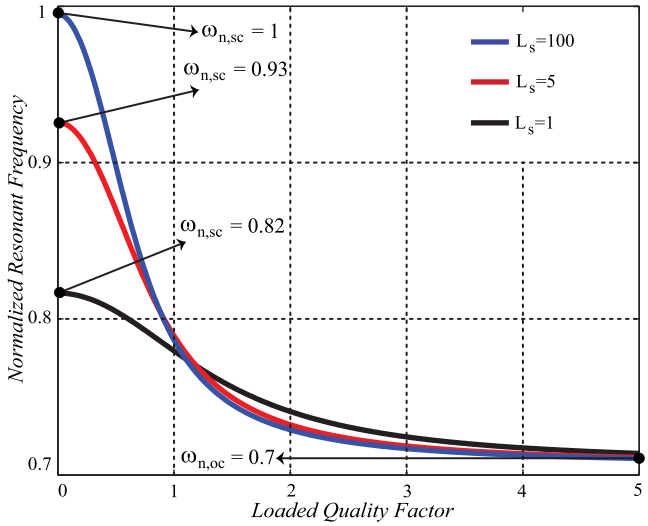


Fig. 6. Normalized resonant frequency as a function of loaded quality factor for different constant values of L_s and $L_n = 1$.

function of the LLC resonant converter is a product of three parts of the block diagram. In the VF method, the fundamental component of full bridge output voltage can be expressed as

$$v_{AB_1}(t) = \frac{4V_{\text{in}}}{\pi}\sin\omega_s t. \tag{7}$$

Also the voltage transfer function and ac equivalent resistance of the current-driven rectifier in CCM of the output rectifier is obtained as

$$M_{v_R} = \frac{\pi}{2\sqrt{2}} \text{ and } R_{eq} = \frac{8n^2}{\pi^2}R_L. \tag{8}$$

By using KVL and KCL rules and (2), the voltage transfer function of the resonant circuit is

$$M_{v_r} = \left|\frac{j\omega_n Q_L L_s}{Q_L L_n L_s + j\omega_n(L_n+L_s)}\right| \frac{1}{|\mathbf{Z_{in}}(j\omega_n)|} \tag{9}$$

and finally, the voltage transfer function of the full bridge LLC resonant converter is obtained as follows:

$$M_v = \frac{V_{\text{out}}}{V_{\text{in}}} = M_{v_s}.M_{v_r}.M_{v_R} = \frac{2\sqrt{2}}{\pi}.M_{v_r}.\frac{\pi}{2\sqrt{2}} = M_{v_r}. \tag{10}$$

The amplitude of the input resonant circuit current (switches current) in VF mode is obtained using (3) and (7) as follows:

$$|I_{L_{s_1}}| = \frac{4V_{\text{in}}}{\pi|Z_{\text{in}}(j\omega_n)|}. \tag{11}$$

(3), (7), (9), and (11) will be used in order to design a high power LLC resonant converter with wide output voltage regulation.

$$\frac{\omega_r}{\omega_0} = \sqrt{\frac{(L_n+L_s)^2+(1+L_n)L_nL_s^2Q_L^2+\sqrt{(-(L_n+L_s)^2+(1+L_n)L_nL_s^2Q_L^2)^2+4L_n^2L_s^2Q_L^2((L_n+L_s)^2+L_n+L_s)}}{2((L_n+L_s)^2+L_n+L_s)}} \tag{6}$$

III. Soft Transitions in Fixed Frequency Phase Shift (FFPS) Approach

In order to provide a noise-free environment for the control circuits, it is vital to achieve soft switching conditions for all MOSFETs in different output load conditions. In VF mode, the LLC resonant converter should be designed in the inductive region, while in FFPS approach, not only the zero crossings of the resonant current must be within the full-bridge output voltage pulse, but also the resonant current should charge and discharge the MOSFETs drain-source capacitances. This means the energy stored in the resonant circuit should be enough to charge and discharge the drain-source effective capacitances within the dead time interval (see Fig. 3). In this section, the minimum essential circulating current for achieving soft switching conditions in maximum PS will be obtained. In the FHA technique, the resonant circuit is considered a low-pass filter with nearly sinusoidal current waveforms in its input port. This means the power is transferred from the high frequency inverter to the load via fundamental harmonic of $v_{AB}(t)$, which is correct when the switching frequency is tuned to close to the circuit resonant frequency. But this assumption is not valid when the switching frequency is far from the resonant frequency. Moreover, the PS strategy, which happens in the maximum switching frequency for wide regulation, leads to amplitude variations of the square waveform harmonics. The Fourier series expansion of the square waveform with the amplitude of $\pm V_{\text{in}}$ and variable duty cycle D is expressed as

$$v_{AB}(t) = \frac{V_{\text{in}}}{\pi}\sum_{n=1}^{\infty}\frac{1-(-1)^n}{n}\left(\cos n\pi\left(\frac{1-D}{2}\right) - \cos n\pi\left(\frac{1+D}{2}\right)\right)\sin(n\omega t). \quad (12)$$

According to (12), the square waveform consists only of components of odd-integer harmonic frequencies, which can be considered as different excitations applied to the input port of the LLC resonant converter. Fig. 7 shows the amplitude of the square waveform harmonics versus duty cycle. Due to the negligible effect of higher harmonics on the steady-state behavior of the circuit, only harmonics up to fifth order are considered. Fig. 8 shows the key waveforms of the LLC resonant converter in FFPS mode. Due to the effect of higher harmonics on the resonant converter waveforms at maximum switching frequency, the resonant current is neither sinusoidal nor triangular. In this case, the amplitude of the resonant circuit input current can be determined by

$$i_{Ls_1}(t) = \sum_{k=1,3,5}\frac{v_{AB}(t)}{Z_{\text{in}}(jk\omega_n)} = I^1_{Ls_1}\sin(\omega t+\varphi_1) + I^3_{Ls_1}\sin(3\omega t+\varphi_3) + I^5_{Ls_1}\sin(5\omega t+\varphi_5). \quad (13)$$

To achieve minimum output current in short-circuit conditions, the maximum PS is required. In this case, the minimum circulating current exists in the resonant circuit, and the phase angle of all harmonics in (13) is equal to 90°. Therefore, the minimum resonant current amplitude is obtained as follows:

$$I_{L_{s_1}} = I^1_{Ls_1} - I^3_{Ls_1} + I^5_{Ls_1}. \quad (14)$$

Fig. 8 shows the resonant current waveforms along with its different harmonics (first, third, and fifth) in PS mode. In the full bridge inverter and during the dead time interval, the resonant

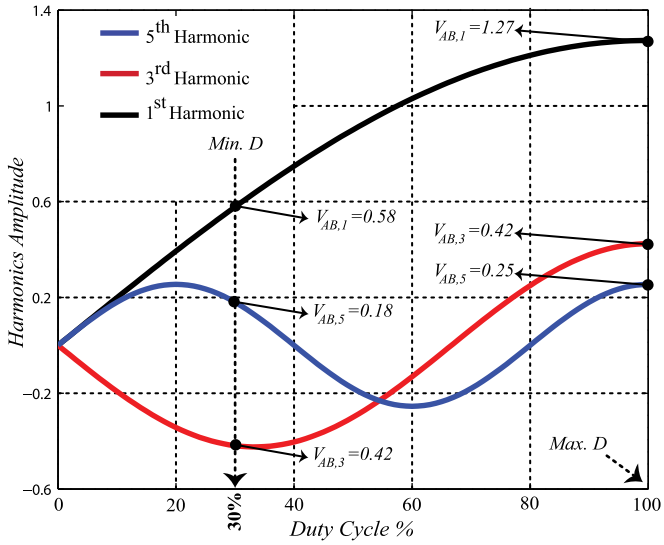


Fig. 7. Amplitude of square waveform harmonics as a function of duty cycle.

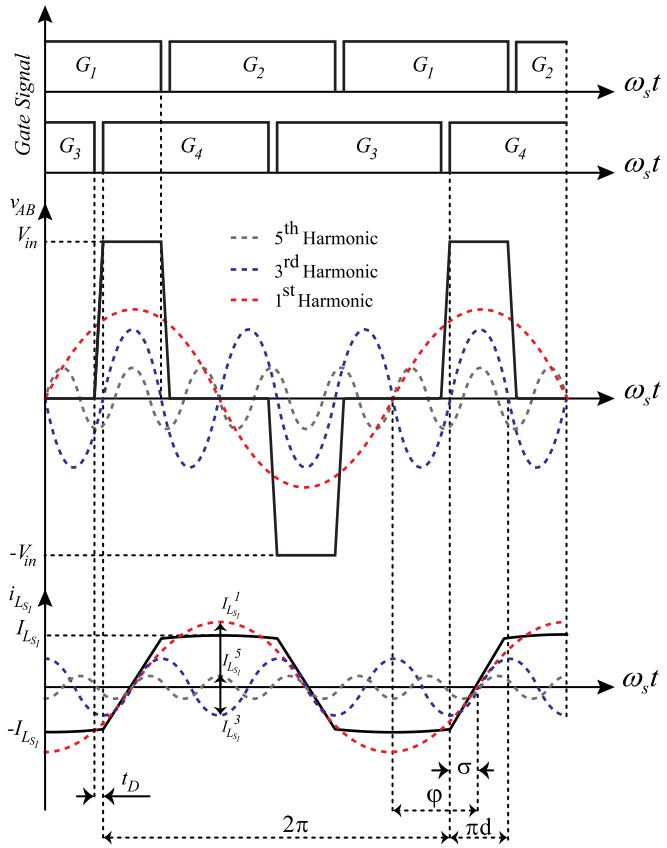


Fig. 8. Main waveforms of the LLC resonant converter in FFPS mode.

current should charge and discharge two drain-source capacitances. Therefore the minimum resonant circuit current is defined as follows:

$$| I_{Ls_1} | \geq 2C_{DS}\frac{V_{\text{in}}}{t_D}. \tag{15}$$

As demonstrated by the analysis and (14)–(15), the LLC resonant tank driven by FFPS should be designed to provide the minimum circulating current required to achieve soft switching transitions (to discharge the drain-source effective capacitance of the MOSFETs). The minimum circulating current depends on selected MOSFET specifications, the minimum dead time, and the input voltage level.

IV. Multivariate Statistical Design Methodology

Due to the battery charger application, the main objective of the design procedure is to obtain a special LLC resonant tank to provide maximum output voltage regulation, while minimizing circulating current in part load conditions and providing soft switching conditions (in both VF and FFPS mode). In this section, multivariate statistical design methodology is employed to consider the behavior of the LLC resonant converter when responding to variations in different normalized parameters. This methodology provides a systematic approach for applying statistics to experimentation in order to achieve efficient and accurate results. In other words, it is used to find cause-and-effect relationships. There are many advantages to using this modeling process, such as it is quick, practical, and easy to employ [38], [39]. In this paper, this methodology is employed to consider the behaviour of the LLC resonant converter when responding to variations in different normalized parameters of the LLC resonant converter, including L_n, L_s, and Q_L. The output response surfaces have been selected based on the most important attributes for a battery charger application, which are wide output voltage capability, high part load efficiency and soft switching in all conditions. In the following paragraphs, these attributes will be discussed in detail.

A. Maximum Output Voltage Regulation

In order to respond to the charge algorithm, the charger should regulate the output voltage from near zero up to 1.5 times the nominal voltage under different loading conditions. In the LLC resonant converter, the voltage gain curves can approach almost zero voltage in high frequency when the absolute value of the gain curves' slope at the short-circuit resonant frequency is set to be maximized. Also, in Section II, it was stated that in order to obtain maximum slope for voltage gain, the difference between $f_{r,oc}$ and $f_{r,sc}$ should be minimized. Therefore, output response surfaces is based on the optimization of the following criteria:

$$\begin{cases} \left| \frac{\partial M_v}{\partial f_n} \right|_{f_n = f_{r,sc}} & \rightarrow \text{Maximize or} \\ f_{r,sc} - f_{r,oc} & \rightarrow \text{Minimize.} \end{cases} \tag{16}$$

According to Section II, both terms presented in (16) have the same meaning, and in the following section, the first one will be used as the first output of the methodology.

B. High Part Load Efficiency

Through appropriate selection of resonant circuit elements, the amplitude of the resonant circuit current decreases with increasing load resistance, reducing conduction loss and providing high part-load efficiency. In other words, the less part load circulating current there is, the flatter the efficiency curve is in relation to load. (17) presents the second output of the methodology that should be maximized

$$\frac{I_{L_{s1},FL}}{I_{L_{s1},HL}} \rightarrow \text{Maximize.} \tag{17}$$

C. Soft Switching Condition

In order to provide safe and efficient performance for the drive circuits of the power MOSFETs as well as for the BMS, it is necessary to provide soft switching conditions for the LLC resonant converter in all operating areas. In the following, this criterion will be considered for both VF and FFPS approaches.

1) VF Mode: To guarantee the soft transient in the VF mode, the phase angle of the input impedance in all load conditions should be positive. ZVS is guaranteed for the VF mode, if the switching frequency is greater than the resonant frequency ($\varphi > 0$), which means the resonant current is lagging the output voltage of the full-bridge inverter. Ideally, in order to minimize the resonant circuit current, which is defined as the conduction losses in all active and passive elements, it is desirable to set φ equal to zero. But in practice, variations (including the resonant circuit elements variations versus temperature and the input voltage ripple of the power factor correction (PFC) stage) necessitate a minimum margin for φ during the design procedure. Moreover, in order to provide enough time to charge and discharge the MOSFETs drain-source capacitances in the same leg, a dead time should be defined between gate signals (e.g., 200 ns). On the other hand, if this angle is too steep, the input resonant current peak will increase, which leads to more conduction losses and more voltage stresses on semiconductor devices and other passive elements. (18) presents the minimum range of the input impedance phases in nominal load conditions that the output response should fall within

$$\begin{cases} \varphi > 10^\circ, & \text{for practical margin} \\ \varphi < 30^\circ, & \text{for high efficiency achievement.} \end{cases} \tag{18}$$

2) FFPS Mode: In terms of resonant converter power loss, the main concern is the circulating current in the primary side. However, for high input voltage applications (e.g., $V_{\text{in}} = 400$ VDC), the switching loss is more than the conduction loss and, therefore, the existence of circulating current leads to soft switching conditions. According to Fig. 8, the minimum circulating current occurs under short-circuit conditions and when using the FFPS method, and in this case it is vital to set this current in such a way as to almost completely charge and discharge MOSFETs' drain-source capacitances. According to (15) and Fig. 8, the minimum current depends on the effective capacitance displayed in parallel with the drain-sources of the power MOSFETs, the level of the input voltage, and the

TABLE I
NORMALIZED PARAMETERS RANGE AND SELECTED VALUE

Parameters	Range	Selected
L_n	[0.5−1.5]	1
L_s	[2−10]	5
Q_L	[0.2−1]	0.5

TABLE II
MODELING RESULTS OF THE NORMALIZED LLC RESONANT CONVERTER

L_n	L_s	Q_L	$\left\| \frac{\partial M_v}{\partial f_n} \right\|$	φ	$\frac{I_{Ls1,FL}}{I_{Ls1,HL}}$	$\frac{I_{Ls1,sc}Z_0}{V_{in}}$
0.5	4.75	0.44	1.51	12.4	4.3	0.396
1	4.75	0.44	3.67	21.4	2.66	0.405
0.5	8.25	0.44	1.31	12.2	4.27	0.44
1	8.25	0.44	2.85	22.3	2.56	0.444
0.5	4.75	0.81	1.7	21.9	2.61	0.396
1	4.75	0.81	3.64	36	1.68	0.405
0.5	8.25	0.81	1.3	22	2.59	0.44
1	8.25	0.81	3.17	37.3	1.63	0.444
0.33	6.5	0.625	0.86	11.9	4.39	0.42
1.17	6.5	0.625	3.89	33.5	1.79	0.43
0.75	5.56	0.625	3.65	23	2.46	0.376
0.75	9.44	0.625	2	22.4	2.36	0.45
0.75	6.5	0.31	2.2 3	11.9	4.31	0.425
0.75	6.5	0.94	2.22	33.9	1.77	0.425
0.75	6.5	0.625	2.56	24	2.38	0.425

maximum allowable dead time. (19) presents the last output of the methodology that should be optimized

$$| I_{Ls_1} | = I^1_{Ls_1} - I^3_{Ls_1} + I^5_{Ls_1} \rightarrow \text{Maximize.} \quad (19)$$

In the following paragraphs, the output response surfaces of the multivariate statistical design methodology will be considered. According to the steady-state analysis performed in Section II, the equations obtained for the LLC resonant converter are functions of three normalized variables, which are L_n, L_s, and Q_L. Table I presents the range for normalized parameters, which will be used as the input range of normalized parameters. In order to select the optimized LLC resonant converter parameters, based on the number of normalized parameters, the methodology dictates the minimum number of simulation (which is 15 simulations in this example) to cover the effects of all three normalized parameters in the ranges discussed. The left side of Table II presents the values of the normalized parameters that must be used in order to extract different responses, such as voltage gain slope, phase of the input impedance, etc. In fact, the normalized parameters are input into the steady-state equations of the LLC resonant converter and output results will be entered in the right side of Table II. Then the analysis of variance regression is employed to extract the mathematical equations, which are presented in (20)–(22), in order to model the system and draw the response surfaces. The response surfaces for LLC resonant converters have been presented in Fig. 9. It is necessary to mention that the surface responses presented in Fig. 9(a)–(d) have been drawn based on the two normalized parameters that have the most impact on the surface

$$\varphi^{1.41} = -4.76 - 28.83L_n - 1.72L_s + 13.2Q_L + 3.66L_nL_s + 211.28L_nQ_L \quad (20)$$

$$\frac{I_{Ls1,FL}}{I_{Ls1,HL}}^{-1.17} = 0.026 - 0.12L_n - 3.95L_s - 0.1Q_L + 8.83L_nL_s + 0.63L_nQ_L + 0.06Q_L^2 \quad (21)$$

$$\frac{I_{Ls1,sc}Z_0}{V_{in}} = 0.26 + 0.03L_n - 2.86L_nL_s - 1.38L_s^2. \quad (22)$$

Having identified the above requirements, it is now possible to select normalized parameters by considering the different response surfaces at the same time. According to Fig. 9(a), in order to satisfy (16), the L_n and L_s should be, respectively, at the highest and lowest possible levels. Two ranges can be defined for normalized parameters (gray band), and the points located in the common area (dark gray) are candidates for optimum L_n and L_s parameters. The same concept can be applied to other surfaces of Fig. 9 with respect to (17)–(19), and finally, the intersection between different common areas determines the values of normalized parameters. The final values of normalized parameters have been selected after conducting simulations and taking into account practical considerations (e.g., the maximum allowable dead time, obtainable amount of secondary leakage inductance, the effective drain-source capacitance of the selected MOSFET). The selected values for normalized parameters are presented in Table I. According to Fig. 9(a), the secondary leakage inductance has a positive effect on output voltage regulation. As mentioned in Section II, a high quantity of secondary leakage inductance (low value of L_s) can expand the output voltage regulation, which is a mandatory requirement to recover batteries.

V. RESONANT POWER CONVERTER DESIGN

Based on optimized selection of normalized parameters, the normalized steady-state equations of the LLC resonant converter will be used to design a high power LLC resonant converter. Fig. 10 presents the voltage transfer function M_v, the first series inductance current $I_{L_{s_1}}$, and the input impedance phase φ versus frequency for the selected values of normalized parameters ($L_n = 1$, $L_s = 5$) and the constant values for normalized load resistances Q_L. According to Fig. 10(a), the voltage gains are almost independent from the load when the switching frequency is around f_0, resulting in minimum switching frequency variation versus load at nominal output voltage. Moreover, Fig. 10(b) shows that at f_0 the input resonant circuit current decreases in higher Q_L, resulting in high efficiency in part load conditions. This point is selected for nominal output voltage operation. As shown in Fig. 10(a), the minimum switching frequency is determined by the maximum output voltage in nominal output power ($Q_L = 1.12$). Fig. 10(c) presents the phase of the resonant circuit input impedance versus frequency for different load conditions. In order to obtain high efficiency and provide a noise-free environment for BMS, soft switching should be provided for the power MOSFETs. Therefore, it

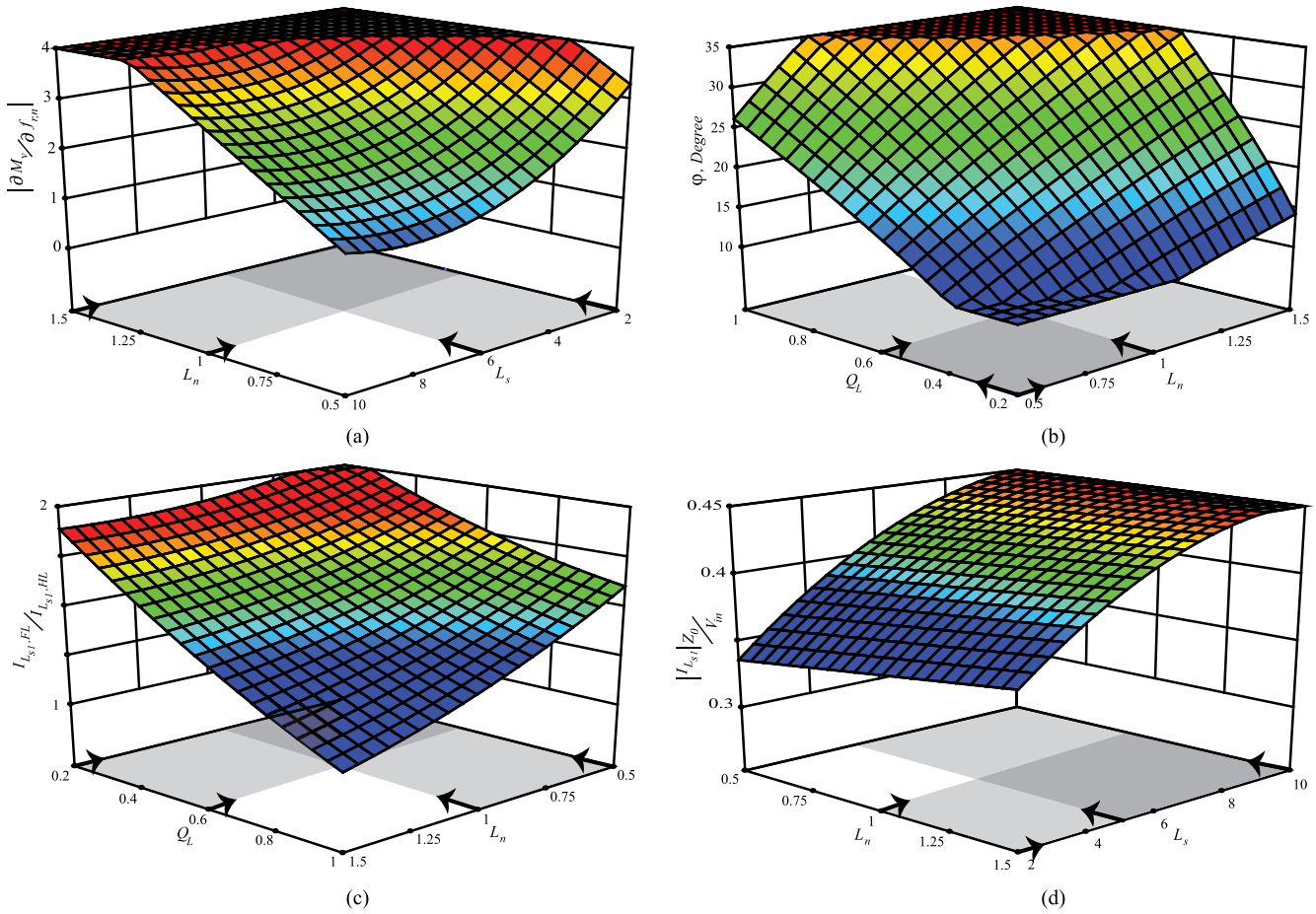


Fig. 9. Multivariate statistical design methodology response surfaces for LLC resonant converter: (a) voltage gain slope surface versus L_n and L_s, (b) input resonant circuit current ratio versus L_n and Q_L, (c) phase of the input impedance versus L_n and Q_L, (d) circulating current amplitude under short-circuit conditions.

is vital that the resonant circuit behave like an inductive load. According to Fig. 10(c), the resonant circuit works in inductive mode for the operating regions described, and ZVS is provided for the full-bridge inverter. In the following description, the LLC resonant circuit elements are calculated based on the voltage transfer function curves and the charger specifications including the input voltage, output voltage, output power and switching frequency variations. The main specifications of the battery charger are as follows:

$$\begin{aligned} V_{\text{in}} &= 400 \text{ VDC},\ V'_{\text{out}} = 120 \text{ VDC},\ P_{\text{out}} = 3 \text{ kW} \\ f_s &= 100{-}200 \text{ kHz}. \end{aligned} \tag{23}$$

According to Fig. 10(a), the minimum normalized switching frequency is equal to 0.82. Therefore, the series resonant frequency (f_0) is calculated using the following equation:

$$\begin{aligned} & f_{n,\min} = 0.82,\ f_{s,\min} = 100 \text{ kHz},\ f_n = \frac{f_s}{f_0} \\ & \Rightarrow f_0 = 122 \text{ kHz}. \end{aligned} \tag{24}$$

Note that due to the practical restriction at light or no-load condition (the oscillation between transformer secondary side capacitances and other parasitics elements) the maximum switching frequency has been selected 1.6 times f_0 to prevent the LLC resonant converter from entering in positive feedback signal. In nominal load conditions ($Q_L = 0.5$), the voltage gain is equal to 1.17 and, as a result, the transformer turn's ratio is obtained as follows:

$$n = \frac{N_p}{N_s} = \frac{V_{\text{out},n}}{V'_{\text{out},n}} = \frac{M_v.V_{\text{in}}}{V'_{\text{out}}} = 3.9. \tag{25}$$

In the LLC resonant converter with capacitive output filter, the equivalent resistance is obtained using (8)

$$R'_L = \frac{{V'_{\text{out}}}^2}{P\text{out}} = 4.8\ \Omega \Rightarrow R_{eq} = n^2 R'_{eq} = 59.2\ \Omega. \tag{26}$$

Finally, the circuit elements of the LLC resonant converter are calculated as follows:

$$\begin{aligned} Z_0 &= \frac{R_{eq}}{Q_L} = 118.4\ \Omega,\ \omega_0 = \frac{\omega_s}{\omega_n} = 244\pi e^3 \Rightarrow \\ L_{s_1} &= \frac{Z_0}{\omega_0} = 154\ \mu\text{H},\ C_s = \frac{1}{Z_0.\omega_0} = 11 \text{ nF} \\ L_{s_2} &= 31\ \mu\text{H},\ L_p = 154\ \mu\text{H}. \end{aligned} \tag{27}$$

The circuit parameters for the LLC resonant converter are provided in Table III.

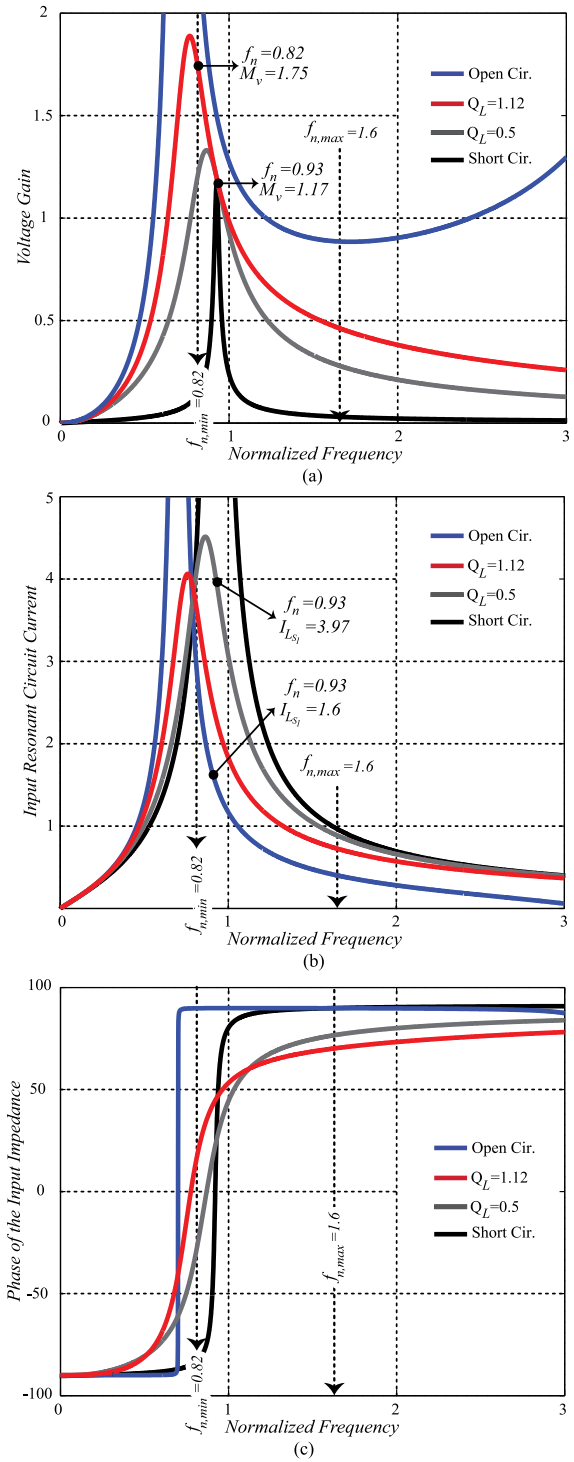


Fig. 10. FHA analysis of the LLC resonant converter for $L_n = 1$, and $L_s = 5$, with constant values for normalized load resistances (Q_L): (a) magnitude of voltage transfer function (M_v), (b) magnitude of input resonant circuit current ($I_{L_{s_1}}$), (c) phase of the input impedance (φ).

VI. Simulation and Experimental Results

In order to investigate the performance of the proposed modulation strategy, a prototype platform has been employed to extract the maximum obtainable output voltage regulation under different load conditions. The components, which are used in the prototypes, are shown in Table IV. The simulation and experimental results for the output voltage versus frequency are presented in Fig. 11 for different output load conditions in solid and dotted shapes, respectively. According to Fig. 11, in the LLC resonant converter, the simulation and experimental results are almost the same for $R'_L = 4.8\ \Omega$ and $R'_L = 10.8\ \Omega$. But for no-load conditions, there is a discrepancy between simulation and experimental results. In fact, the effect of the parasitic capacitances on the secondary side of the transformer leads to increased output voltage in the LLC at no-load condition. Moreover, around $f_{sw} = 200$ kHz, the output voltage curves start to flatten, meaning that there is no more regulation after maximum switching frequency. Fig. 12 presents the voltage and current waveforms for the the proposed battery charger in VF mode. According to these figures, the zero crossings of the resonant

TABLE III
LLC Prototype Platform Parameters

Parameters	Value
Input Voltage, V_{in}	400 VDC
Nominal Output Voltage, $V'_{\text{out},n}$	120 VDC
Maximum Output Voltage, $V'_{\text{out},m}$	180VDC
Maximum Output Power, P_{out}	3 kW
Switching Frequency Range, f_s	100-200 kHz
Resonant Frequency, f_0	122 kHz
Series Resonant Capacitance, C_s	11 nF
First Series Resonant Inductance, L_{s_1}	154μH
Second Series Resonant Inductance, L_{s_2}	31μH
Parallel Resonant Inductance, L_p	154μH
Transformer Turn's Ratio, $n = \frac{N_p}{N_s}$	3.9

TABLE IV
Components of Resonant Converters Platforms

Component	Part Number	Ratings
MOSFET's	$IXFX64N60$	600 VDC, 64 A
Resonant Cap.	Film Cap.	10 nF, 2000 VDC
Resonant Ind.	$3F3$	$***$
Transformer	$3F3$	$***$
Rectifier Diode	$MBR40250$	250 VDC, 40 A
Output Capacitor	Film Capacitor	18 μF, 250 VDC

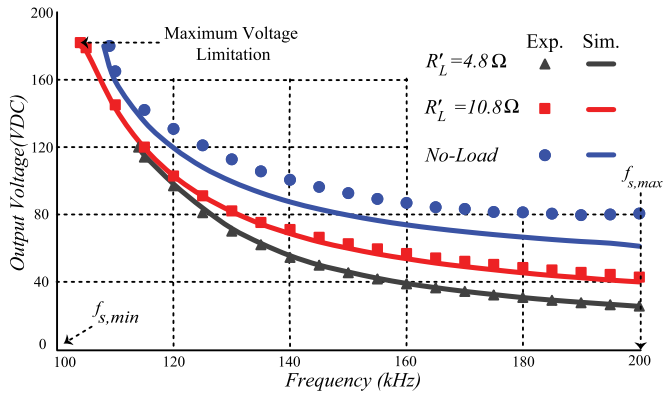
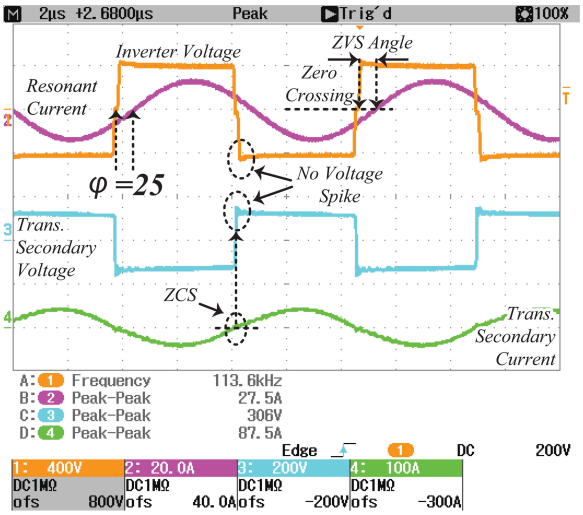
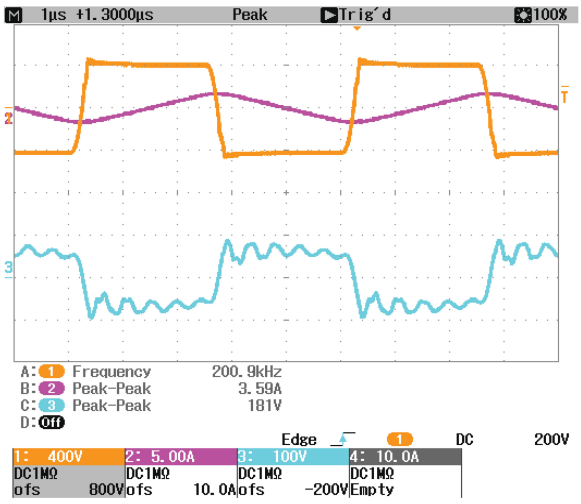


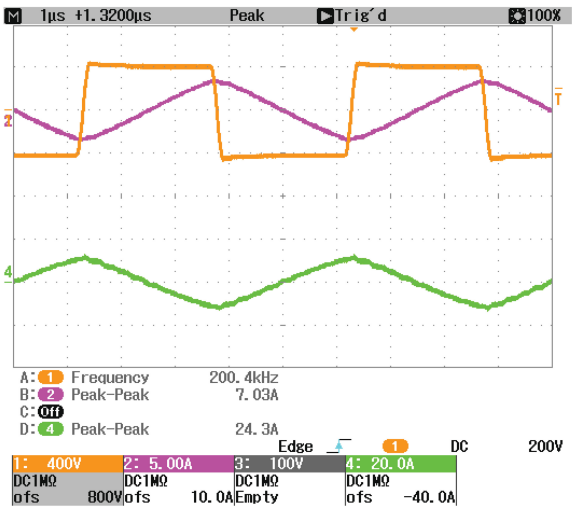
Fig. 11. Simulation and experimental results for dc voltage gain versus frequency.



(a)

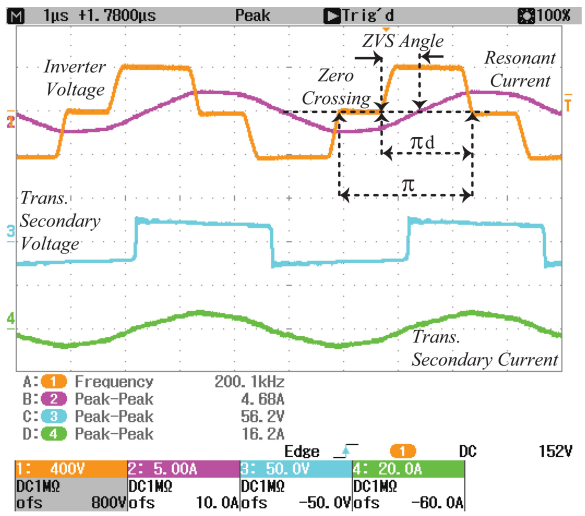


(b)

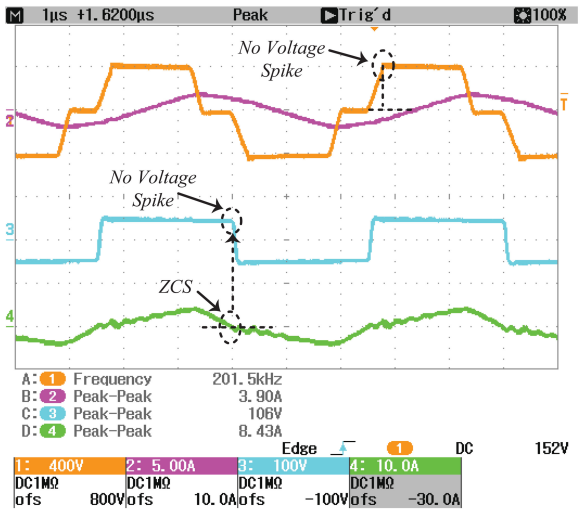


(c)

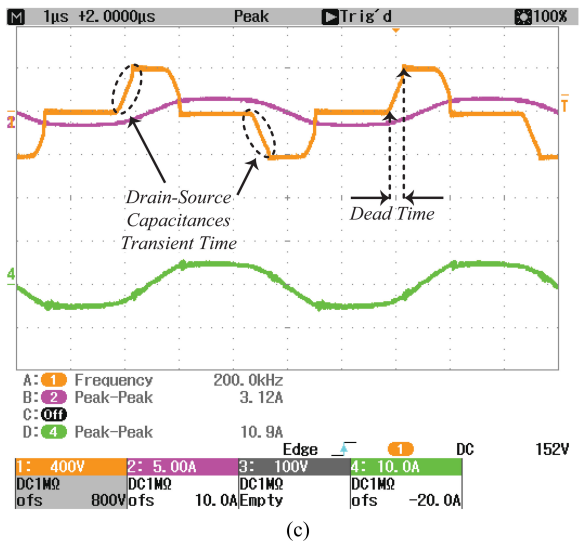
Fig. 12. Experimental results for the LLC resonant converter in VF mode, (a) $V_{\text{out}} = 120$ VDC and $P_{\text{out}} = 3$ kW, (b) $V_{\text{out}} = 90$ VDC and $P_{\text{out}} = 0$ W, and (e) $V_{\text{out}} = 0$ VDC and $I_{\text{out}} = 7A$.



(a)



(b)



(c)

Fig. 13. Experimental results for the LLC resonant converter in FFPS mode, (a) $V_{\text{out}} = 20$ VDC and $I_{\text{out}} = 4.5$ A, (b) $V_{\text{out}} = 45$ VDC and $I_{\text{out}} = 2$ A, and (c) $V_{\text{out}} = 0$ VDC and $I_{\text{out}} = 2$ A.

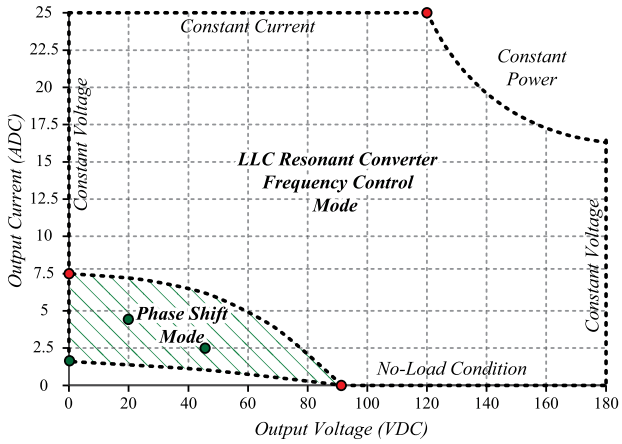


Fig. 14. *V–I* plane obtained from the LLC resonant converters by employing digital hybrid modulation technique (The green dashed area is obtained by FFPS.).

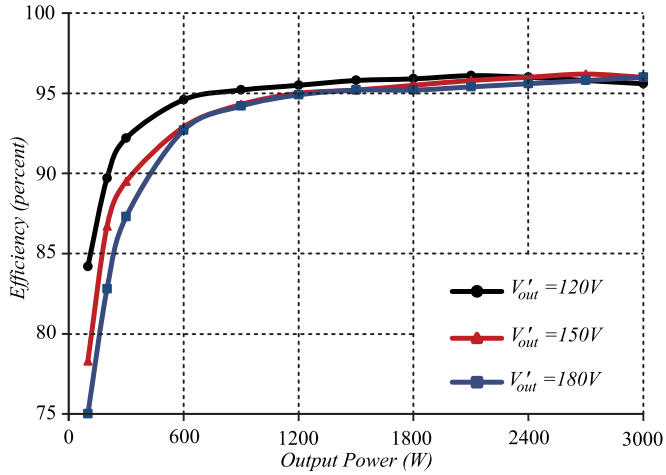


Fig. 15. Efficiency curves of the LLC resonant converter at different fixed output voltages.

circuit input current are within the inverter output voltage pulse and, as a result, in all of the conditions described, the full-bridge switches are fully turned on under zero voltage. Fig. 13 present the experimental results of LLC converter in the FFPS mode. The operating mode selection is made by a digital controller. In fact, there is a low and high limitation for switching frequency (f_s = 100-200 kHz), and after reaching to the maximum switching frequency, the controller changes the modulation strategy to PS in order to decrease the output voltage. By employing this modulation strategy at the maximum switching frequency, it is possible to improve the output voltage regulation, even under no-load conditions. According to these figures, the zero crossings of the resonant circuit input current are within the full bridge output voltage pulse and, as a result, the full-bridge switches are fully turned on under zero voltage. As predicted, the worse case scenario for ZVS occurs under short-circuit and maximum PS conditions (minimum effective duty cycle), which is shown in Fig. 13(c). According to (15) and the selected MOSFETs type for the full bridge inverter, the amount of circulating current in short circuit conditions is nearly enough to charge and discharge the the drain-source capacitances of the power MOSFETs during the specified dead time, which is equal to 250 ns. The *V–I* plane obtained from the experimental results is shown in Fig. 14. In the *V–I* plane, there are different limitations on the boundaries, including current, voltage, power, and no-load conditions, and each point in the plot indicates one experimental test (red and green points indicate VF and FFPS, respectively). According to Fig. 14, due to the effects of the junction capacitances of the output diodes on the voltage gains, the LLC resonant converter cannot cover all of the regions in the *V–I* plain in the VF mode (f_s = 100-200 kHz). The unobtainable area of the LLC resonant converter starts in the no-load boundary at $V_{\text{out}} = 90$ V DC and $f_s = 200$ kHz, and for short-circuit conditions, the output current is equal to 7 A. As mentioned in the introduction, the battery charger must be able to respond to different modes of the charge algorithms and cover almost all of the *V–I* plane region. The experimental results show that employing the FFPS strategy in the maximum switching frequency and allowable PS decreases the output voltage in different load conditions, which results in improved regulation. The green dashed region in Fig. 14 indicates the regulation improvement obtained by using FFPS. Fig. 15 presents the efficiency curves of the LLC resonant converters for three different output voltages. According to these curves, the resonant converters designed for this study present a maximum efficiency equal to 96.5%.

In the following section, the effect of the input voltage variation on the resonant power converter operation will be investigated. Generally, battery charger power architectures include two main stages, which are ac–dc PFC and dc–dc isolated power converter. Therefore, the input voltage of the dc–dc resonant converter is provided by a PFC stage, which could be a conventional or interleaved CCM boost topology [9], [14]. Generally, the output voltage of the PFC stage is not constant and can have $\pm 10\%$ voltage ripple, so the dc–dc power stage has to compensate this variation. In order to investigate the effect of the input voltage variation for the designed resonant converter, the prototype platform has been tested for the minimum and maximum input voltage ($V_{\text{in}} = 360 \sim 440$) and the maximum output power condition ($P_{\text{out}} = 3000$ W). According to the experimental results presented in Fig. 16, the designed LLC resonant converter can compensate the effect of the input voltage variation using frequency control modulation, while transferring the maximum power to the battery pack. Comparing Figs. 12(a) and 16(a) reveals the difference between the input impedance phase in two different input voltages and in fixed output voltage and output power condition. According to Fig. 16(a), the input impedance phase angle of the LLC resonant converter is 16°, which still guarantees soft switching conditions.

In order to examine the performance of the resonant converter with the proposed modulation technique, the prototype platform has been tested in the recovery region. One of the main advantages of the LLC resonant converter is the output filter type, which consists only of a capacitor. According to Table IV, the output filter consists of an 18-μF film capacitor and can perfectly provide a ripple free charging current for the battery pack in normal switching operation ($f_s = 100 \sim 200$ kHz). But

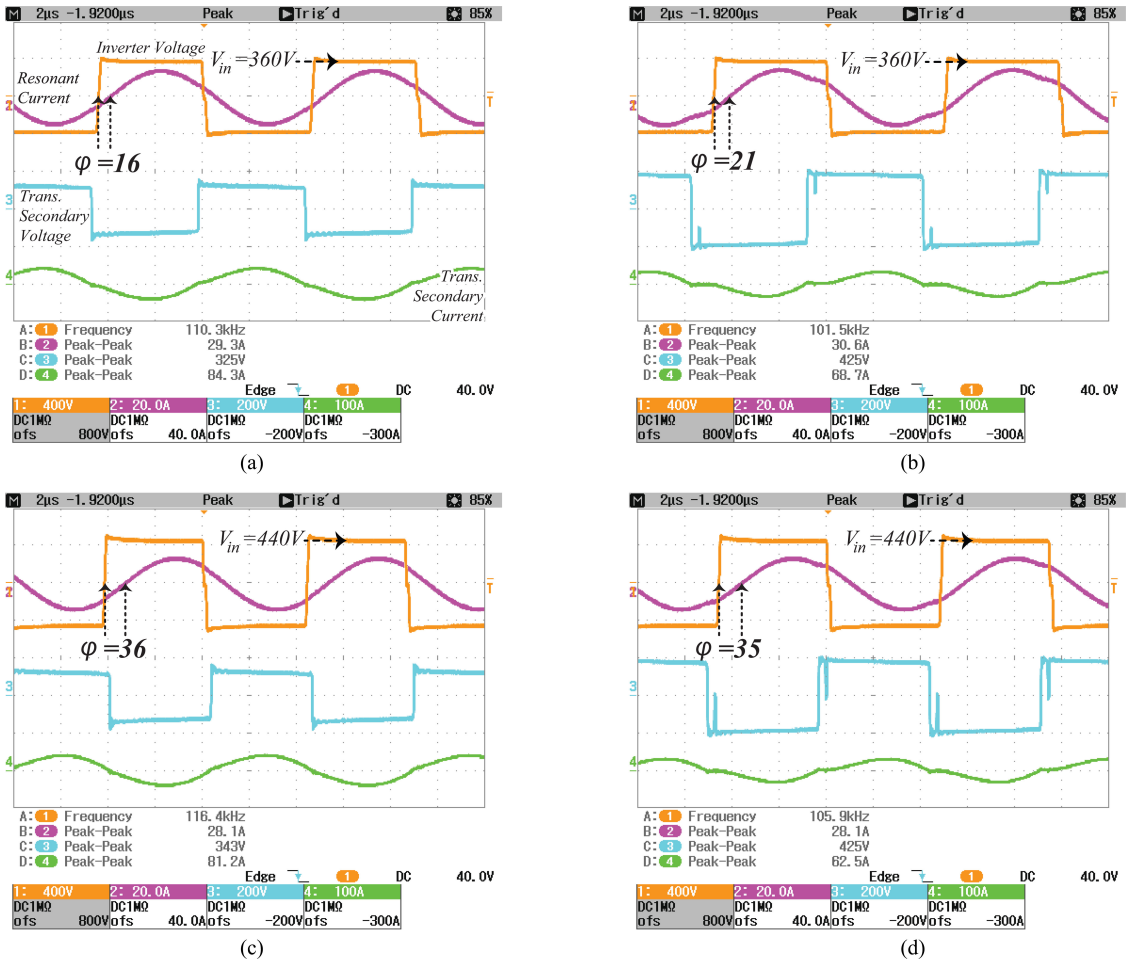


Fig. 16. Effect of input voltage variation on the resonant converter operation in the maximum output power condition ($P_{\text{out}} = 3$ kW), (a) $V_{\text{in}} = 360$ VDC, and $V_{\text{out}} = 120$ VDC, (b) $V_{\text{in}} = 360$ VDC, $V_{\text{out}} = 180$ VDC, (c) $V_{\text{in}} = 440$ VDC, $V_{\text{out}} = 120$ VDC, and (d) $V_{\text{in}} = 440$ VDC, $V_{\text{out}} = 180$VDC.

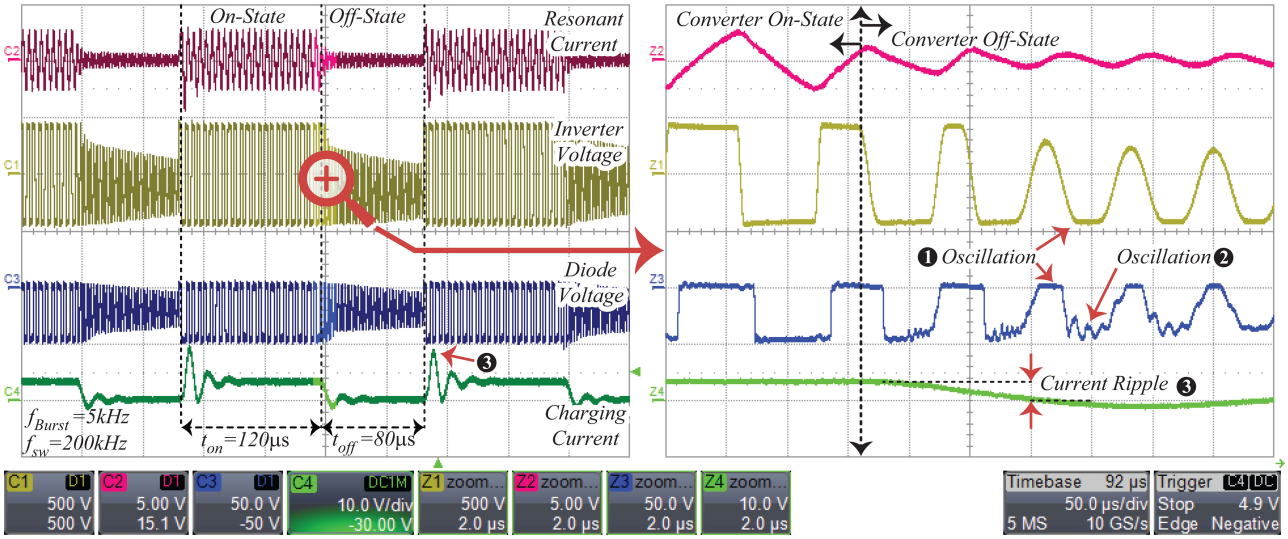


Fig. 17. Burst mode issues in the full bridge LLC resonant converter for the $V_{\text{out}} = 45$ VDC and $I_{\text{out}} = 2$ A recovery region. ① High frequency, high voltage oscillation across inverter output nodes and output rectifier diodes caused by the interaction between MOSFET drain-source capacitances and the resonant circuit, ② high frequency oscillation caused by the interaction between output rectifier diodes junction capacitances and the resonant circuit. ③ Output current variation and spikes, which lead to unwanted tripping in recovery mode and interfere with the BMS current sensing circuit.

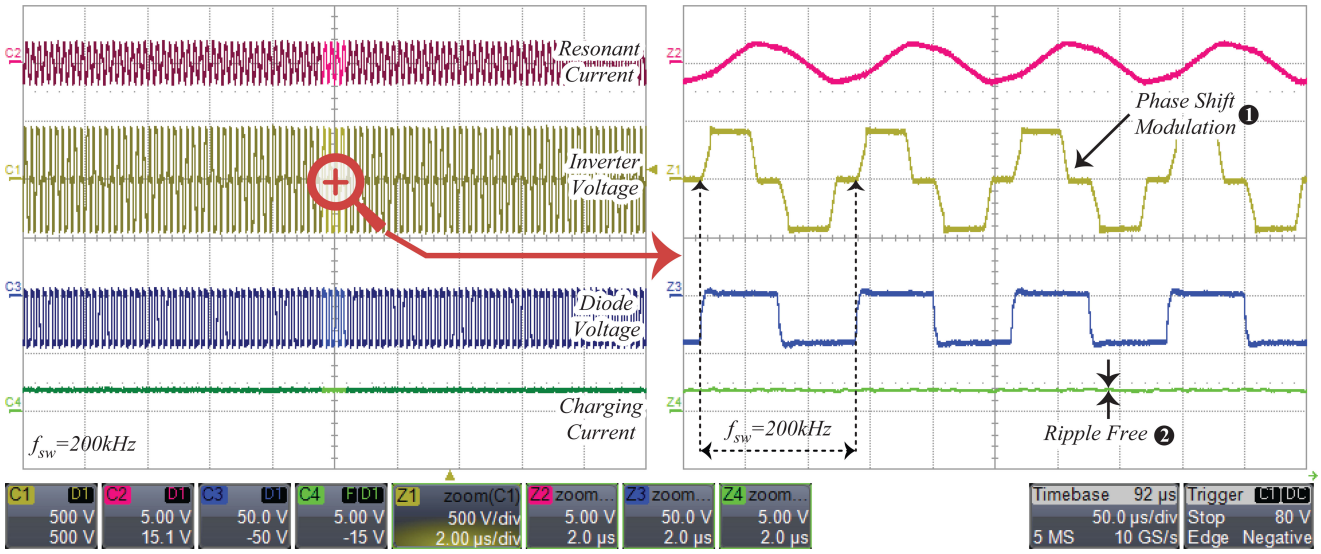


Fig. 18. The Experimental result of the proposed modulation technique for the $V_{\text{out}} = 45$ VDC and $I_{\text{out}} = 2$ A recovery region. ① indicates the PS strategy, which is applied in the reconvery region for wider regulation. ② shows the smooth charging current without any ripple.

in the burst mode modulation, the switching driver signals are turned on and off periodically with an intermittent cycle much lower than the minimum switching frequency ($f_{\text{Burst}} = 5$ kHz). When revitalizing a dead battery, the battery absorbs current and the output filter, which is designed for minimum switching frequency operation ($f_s = 100$ kHz), cannot absorb the current ripple of the burst mode cycle. As a result, the battery charger operation in this mode leads to a low quality charging current, and the battery pack is charged with a burst frequency current ripple that can reduce the battery's life span. In order to show the drawback of the burst mode modulation strategy, experimental results are presented to show the amount of charging current ripple in both burst and PS modulations. The experimental results in Fig. 17 show the detrimental effect of using the full bridge LLC resonant converter in burst mode and in the 0.6 duty cycle. In this figure, the output voltage and current are set to 45 VDC and 2 ADC. According to this figure, the output current variation alternates between 0 and 4.2 A. Also, there is a spike in the current up to 8 A during the transient time as a result of the interaction between output filter capacitor and the parasitic inductance of the charger cable. The pulsating current and spikes lead to unwanted tripping in recovery mode and interfere with the BMS current sensing circuit. In order to reduce the charging current ripple in the burst mode operation, it is essential to install additional LC filters in the output of the dc–dc stage, meaning higher cost and lower power density. Also, adding extra filters to the current sensing circuit is vital. As can be seen in Fig. 17, due to the interaction between parasitic capacitances (including MOSFET drain-source and diodes junction) and the resonant circuit elements, there is high frequency, high voltage oscillation in different points of the circuit, which results in a noisy environment for the BMS. Fig. 18 presents the experimental result for the LLC resonant converter when it operates in PS modulation mode with the same output voltage and current as assumed for Fig. 17. According to Fig. 18, there is no ripple in the battery charging current, which proves the capability of the proposed modulation strategy in terms of working in recovery region. All in all, the proposed PS modulation technique can provide ripple-free charging current without requiring any additional filters in the output of the converter, thereby providing a noise-free environment for the reliable operation of the BMS.

VII. Conclusion

This paper introduced a special LLC tank design method driven by both VF and PS to achieve all the regulation requirements for battery charging (from recovery, bulk, equalization, to finish). The design procedure was based on multivariate design methodology and resulted in advantageous extreme regulation in the converter and the elimination of detrimental burst mode operation. The complete analysis of the resonant converter (higher order including leakage inductance), along with mathematical equations, were presented in order to optimize and select the normalized parameters of the LLC resonant converter. The main advantage of the LLC resonant converter with the proposed modulation strategy is its ability to regulate the output voltage from close to zero up to 1.5 times the nominal voltage in CCM with low switching frequency variation, while providing soft switching conditions for semiconductor devices in all operating conditions. The low-ripple output voltage enhanced the quality of the charging current for battery charger applications in all conditions, especially the recovery region, thereby providing a noise-free environment for the reliable operation of a battery management system. The experimental results proved that the LLC resonant converter with this special modulation strategy covered almost all regions in the *V–I* plane, and had a peak efficiency of 96.5%, which can be employed as a high power, wide voltage regulator for battery charger applications.

References

[1] M. Yilmaz and P. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[2] S. Ryu, D. Kim, M. Kim, J. Kim, and B. Lee, "Adjustable frequencydutycycle hybrid control strategy for full-bridge series resonant converters in electric vehicle chargers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5354–5362, Oct. 2014.
[3] I. Lee and G. Moon, "Half-bridge integrated ZVS full-bridge converter with reduced conduction loss for electric vehicle battery chargers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3978–3988, Aug. 2014.
[4] A. Kuperman, U. Levy, J. Goren, A. Zafransky, and A. Savernin, "Battery charger for electric vehicle traction battery switch station," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5391–5399, Dec. 2013.
[5] J. Deng, S. Li, S. Hu, C. Mi, and R. Ma, "Design methodology of LLC resonant converters for electric vehicle battery chargers," *IEEE Trans. Veh. Technol.*, vol. 63, no. 4, pp. 1581–1592, May 2014.
[6] M. Bhatt, W. G. Hurley, and W. H. Wolfle, "A new approach to intermittent charging of valve-regulated Lead Acid batteries in standby applications," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1337–1342, Oct. 2005.
[7] Trojan Battery Company. Deep-cycle batteries user's guide. (2013). [Online]. Available: www.trojanbattery.com
[8] Fairchild Semiconductor Corporation, AN-9721 Li-Ion Battery Charging Basics, Featuring the FAN5400/FAN 5420 Family of PWM Battery Chargers, Fairchild Semiconductor Corporation, Rev. 1.0.0, 2010.
[9] F. Musavi, M. Craciun, D. Gautam, W. Eberle, and W. Dunford, "An LLC resonant DC-DC converter for wide output voltage range battery charging applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5437–5445, Dec. 2013.
[10] F. Musavi, M. Craciun, D. Gautam, and W. Eberle, "Control strategies for wide output voltage range LLC resonant DCDC converters in battery chargers," *IEEE Trans. Veh. Technol.*, vol. 63, no. 3, pp. 1117–1125, Mar. 2014.
[11] F. Musavi, M. Craciun, D. Gautam, M. Edington, W. Eberle, and W. Dunford, "Control strategies for a LLC multi-resonant DC-DC converter in battery charging applications," in *Proc. Appl. Power Electron. Conf. Expo.*, 2013, pp. 1803–1813.
[12] F. Musavi, M. Craciun, M. Edington, W. Eberle, and W. Dunford, "Practical design considerations for a LLC multi-resonant DC-DC converter in battery charging applications," in *Proc. Appl. Power Electron. Conf. Expo.*, 2012, pp. 2596–2602.
[13] D. Gautam, F. Musavi, W. Eberle, and W. Dunford, "A zero-voltage switching full-bridge DC-DC converter with capacitive output filter for plug-in hybrid electric vehicle battery charging," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5728–5735, Dec. 2013.
[14] M. Pahlevaninezhad, P. Das, J. Drobnik, P. Jain, and A. Bakhshai, "A novel ZVZCS full-bridge DC/DC converter used for electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 12752–2769, Jun. 2012.
[15] B. Gu, C. Lin, B. Chen, J. Dominic, and J. Lai, "Zero-voltage-switching PWM resonant full-bridge converter with minimized circulating losses and minimal voltage stresses of bridge rectifiers for electric vehicle battery chargers," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4657–4667, Oct. 2013.
[16] D. Gautam, F. Musavi, M. Edington, W. Eberle, and W. Dunford, "An automotive onboard 3.3-kW battery charger for PHEV application," *IEEE Trans. Veh. Technol.*, vol. 61, no. 8, pp. 3466–3474, Oct. 2012.
[17] T. Mishima, K. Akamatsu, and M. Nakaoka, "A high frequency-link secondary-side phase-shifted full-range soft-switching PWM DC-DC converter with ZCS active rectifier for EV battery chargers," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5758–5773, Dec. 2013.
[18] N. Shafiei and M. Ordonez, "Improving the regulation range of EV battery chargers with $L3C2$ resonant converters," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 85–100, Jun. 2015.
[19] M. Pahlevaninezhad, S. Eren, P. Jain, and A. Bakhshai, "Self-sustained oscillating control technique for current-driven full-bridge DC/DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5293–5310, Nov. 2013.
[20] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard, A Bakhshai, and P. Jain, "Analysis of a fifth-order resonant converter for high-voltage DC power supplies," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3166–3184, Jan. 2013.
[21] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*. New York, NY, USA: Wiley, 1995.
[22] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174–182, Apr. 1988.
[23] C. Chang, E. Chang, and H. Cheng, "A high-efficiency solar array simulator implemented by an LLC resonant DC-DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 3039–3046, Jun. 2013.
[24] J. Kim, G. Choe, H. Jung, and B. Lee, "Design and implementation of a high-efficiency on-board battery charger for electric vehicles with frequency control strategy," in *Proc. Vehicle Power Propulsion Conf.*, 2010, pp. 1–6.
[25] H. Hu, X. Fang, F. Chen, Z. Shen, and I. Batarseh, "A Modified high-efficiency LLC converter with two transformers for wide input-voltage range applications," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1946–1960, Apr. 2013.
[26] H. Kim, J. Baek, M. Ryu, J. Kim, and J. Jung, "The high-efficiency isolated ACDC converter using the three-phase interleaved LLC resonant converter employing the Y-Connected rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4017–4028, Aug. 2014.
[27] T. Jiang, J. Zhang, X. Wu, K. Sheng, and Y. Wang, "A bidirectional LLC resonant converter with automatic forward and backward mode transition," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 757–770, Aug. 2014.
[28] J. Kim and G. Moon, "A new LLC Series resonant converter with a narrow switching frequency variation and reduced conduction losses," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4278–4287, Aug. 2014.
[29] J. Hayes, J. Hal, M. Egan, and J. Murphy, "Full-bridge, series-resonant converter supplying the SAE 5-1773 electric vehicle inductive charging interface," in *Proc. Power Electron. Spec. Conf.*, 1996, pp. 1913–1918.
[30] J. Hayes, M. Egan, J. Murphy, S. Schulz, and J. Hall, "Wide-load-range resonant converter supplying the SAE J-1773 electric vehicle inductive charging interface," *IEEE Trans. Ind. Appl.*, vol. 35, no. 4, pp. 884–895, Jul. 1999.
[31] B. Lee, M. Kim, C. Kim, K. Park, and G. Moon, "Analysis of LLC resonant converter considering effects of parasitic components," in *Proc. Telecommun. Energy Conf.*, 2009, pp. 1–5.
[32] S. Zhao, J. Xu, and O. Trescases, "Burst-mode resonant LLC converter for an LED luminaire with integrated visible light communication for smart buildings," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4392–4402, Aug. 2014.
[33] W. Feng, F. Lee, and P. Mattavelli, "Optimal trajectory control of LLC resonant converters for LED PWM dimming," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 979–987, Feb. 2014.
[34] H. Choi and FPS Application Group, Half-Bridge LLC Resonant Converter Design Using FSFR-Series Fairchild Power Switch, Fairchild Semiconductor Corporation, Rev. 1.0.0, 2007.
[35] H. Choi, "Analysis and design of LLC resonant converter with integrated transformer," in *Proc. Appl. Power Electron. Conf. Expo.*, 2007, pp. 1630–1635.
[36] W. Flanagan, *Handbook of Transformer Design and Applications*. New York, NY, USA: McGraw-Hill, 1992.
[37] D. Bortis, J. Biela , G. Ortiz, and J. W. Kolar, "Design procedure for compact pulse transformers with rectangular pulse shape and fast rise times," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 18, no. 4, pp. 1171–1180, Aug. 2011.
[38] D. C. Montgomery, *Design and Analysis of Experiments*. New York, NY, USA: Wiley, 2001.
[39] S. R. Cove, M. Ordonez, F. Luchino, and J. E. Quaicoe, "Applying response surface methodology to small planar transformer winding design," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 483–493, Feb. 2013.

Navid Shafiei (S'11) received the B.S. degree in electrical engineering, in 2005, from Kashan University, Kashan, Iran, and the M.S. degree in electrical engineering, in 2011, from Islamic Azad University, Najafabad, Iran. He is currently working toward the Ph.D. degree at the University of British Columbia, Vancouver, BC, Canada.

He worked as a Technical Designer at the Information and Communication Technology Institute, Isfahan University of Technology, Isfahan, Iran, from 2005 to 2013, where he was involved in the design and implementation of resonant converters. His current research interests include resonant converters and their application in pure electric vehicles.

Martin Ordonez (S'02–M'09) was born in Neuquen, Argentina. He received the Ing. degree in electronics engineering from the National Technological University, Cordoba, Argentina, in 2003, and the M.Eng. and Ph.D. degrees in electrical engineering from the Memorial University of Newfoundland (MUN), St. Johns, NL, Canada, in 2006 and 2009, respectively.

He is currently an Assistant Professor at the Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada. He is also a Canada Research Chair in Power Converters for Renewable Energy Systems, as well as an Adjunct Professor with Simon Fraser University, Burnaby, BC, Canada, and MUN. His industrial experience in power conversion includes research and development at Xantrex Technology Inc./Elgar Electronics Corp. (now AMETEK Programmable Power, San Diego, CA, USA), Deep-Ing Electronica de Potencia (Rosario, Argentina), and TRV Dispositivos (Cordoba). With the support of industrial funds and the Natural Sciences and Engineering Research Council, he has contributed to more than 60 publications and R&D reports.

Dr. Ordonez is an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, serves on several IEEE committees, and reviews widely for IEEE/IET journals and international conferences. He was awarded the David Dunsiger Award for Excellence in the Faculty of Engineering and Applied Science (2009) and the Chancellors Graduate Award/Birks Graduate Medal (2006), and became a Fellow of the School of Graduate Studies, MUN.

Marian Craciun (M'00) received the B.Sc. degree in electronics engineering from the Polytechnic Institute of Bucharest, Bucharest, Romania, in 1989.

He has more than 20 years of experience in developing telecom and industrial power electronics products and sustaining engineering. His industrial experience includes positions at Energo repairs RENEL and Asea Brown Boveri Ltd., Bucharest; Argus Technologies Ltd. and Alpha Technologies Ltd., Burnaby, BC, Canada. He is currently a Power Electronics R&D Engineer at Delta-Q Technologies Corp., Vancouver, BC, Canada. His current research interests include high-power high-efficiency converter topologies, high-power-factor rectifiers, resonant converters, electric vehicles, and sustainable and renewable energy sources.

Chris Botting (M'04) received the B.Sc. degree in electrical engineering from Calvin College, Grand Rapids, MI, USA, in 2001.

From 2001 to 2012, he worked as Lead Systems Engineer at Azure Dynamics, Burnaby, BC, Canada, a manufacturer of electric and hybrid electric commercial vehicles, where he was responsible for energy storage, high voltage distribution and auxiliary systems, and power train architecture. He is currently the Manager of Research Engineering at Delta-Q Technologies, Burnaby, where he is responsible for research activities, funding, university collaboration, technology roadmap, intellectual property portfolio, and battery test lab functions. His research interests include high-efficiency converter topologies, electric drive systems, energy storage systems, and renewable energy sources.

Murray Edington (M'02) received the B.Sc. (honors) degree in mechanical engineering from Cambridge University and the University of Newcastle upon Tyne, in 1985.

He has 14 years of experience in developing automotive power electronics products (specifically electric and hybrid electric vehicle system components) and 15 years of experience in the development of industrial power electronics products. His industrial experience includes positions at Ricardo Consulting Engineers, Motorola Automotive Industrial Electronics Group, Farnell Advance Power, and Wavedriver Ltd. He was most recently the Director of Engineering at Delta-Q Technologies Corp., Burnaby, BC, Canada.