A Novel Three-Phase Current Source Rectifier With Delta-Type Input Connection to Reduce the Device Conduction Loss

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***Abstract*—The three-phase current source rectifier (CSR) features a step-down ac–dc voltage conversion function, smaller ac filter size compared with the traditional two-level voltage source rectifier, and inrush current limiting capability. However, large conduction loss of semiconductor devices has limited the wide application of traditional CSRs. In this paper, a new CSR topology, delta-type current source rectifier (DCSR), is proposed to reduce the conduction loss. The proposed rectifier has delta-type connections on its ac input side and its dc-link current can be shared by multiple devices at a given time. This paper introduces the DCSR's operation principle, modulation scheme, and design method. Based on the analysis, the conduction loss can be reduced by up to 20% with the proposed topology. An 8-kW prototype is then built to experimentally verify the performance of the DCSR.**

***Index Terms*—Buck rectifier, current source rectifier (CSR), delta type, high efficiency.**

I. Introduction

THE three-phase current source rectifier (CSR), or buck-type rectifier, features a step-down ac–dc voltage conversion function, smaller ac filter size compared with the traditional two-level voltage source rectifier, and inrush current limiting capability [1]–[7]. It has been applied as the active front-end in high-efficiency power supplies for telecommunication and data centers [1], [2], where 480 or 380 V ac voltage is stepped down to 400-V dc voltage in a single conversion stage. It can also be used as the off-board dc fast charger for electric vehicles to increase efficiency [3]. In high-power applications such as dc arc furnace and induction melting, CSRs can largely reduce the size, loss, and cost of the transformer and harmonic filter [4], [5]. For a variable speed motor drive application, CSRs have lighter input EMI filter compared with the traditional two-level voltage source rectifier [6], [7].

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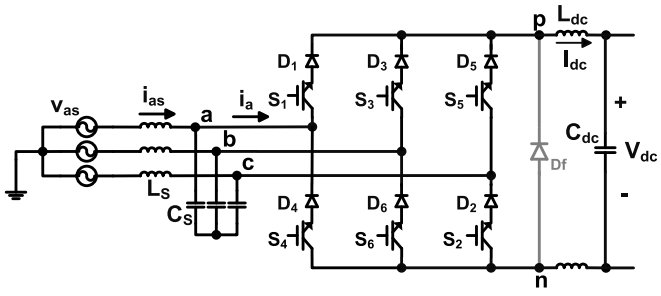

Fig. 1. Traditional three-phase CSR.

The switches in CSRs need to have a reverse-blocking capability to operate under ac voltage. The reverse blocking IGBT (RB-IGBT) has been developed in recent years to reduce the conduction loss for current source converters and matrix converters [8]–[11]. But the switching loss of RB-IGBT is still higher than standard IGBTs due to its longer "tail current", worse voltage overshoot, and larger reverse recovery current [11]. The symmetric GTO or GCT usually has a blocking voltage of several kilovolts but is only applied in limited high-power, high-voltage applications with less than 1-kHz switching frequency [12]. In most applications of PWM CSRs, the switches are usually formed by connecting an active device (IGBT, MOSFET, or JFET) with a diode in series [1], [2], [5], [7], [11], [13], [14]. Even with several devices in parallel in one switch, the high conduction loss still accounted for up to 50% of the total converter loss in traditional CSRs [1], [2]. In previous comparison with voltage source converters, the large conduction loss and corresponding heatsink size are the main drawbacks for current source converters [15], [16].

The traditional three-phase CSR is shown in Fig. 1. In this topology, the dc-link current flows through four devices in series, leading to high conduction loss. Although a freewheeling diode (Df) can be added to reduce the conduction loss during the freewheeling state, the efficiency does not improve much especially when the modulation index is high. The three-switch CSR was proposed in [17] to reduce the number of active switches. It has even more conduction loss than the traditional topology since the current will flow through as many as six devices in series [15]. The buck-type third harmonic current injection rectifier (Swiss Rectifier) was proposed in [3] to reduce the switching

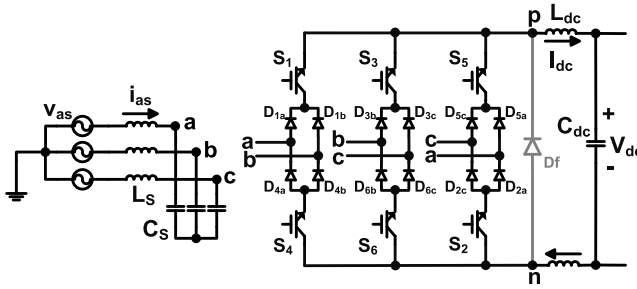

Fig. 2. Proposed DCSR.

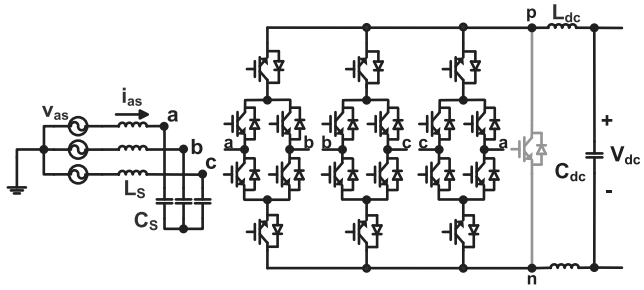

Fig. 3. Bidirectional DCSR.

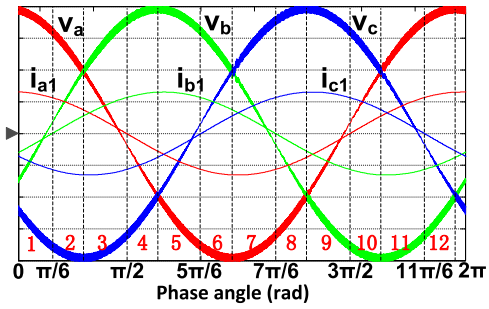

Fig. 4. Fundamental components of the input current and voltage.

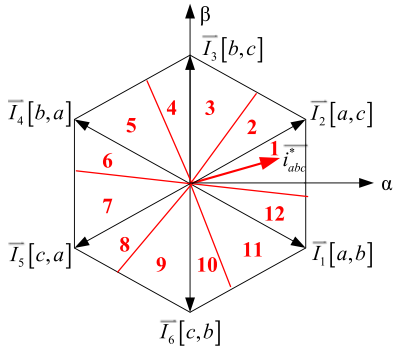

Fig. 5. Space vector plane.

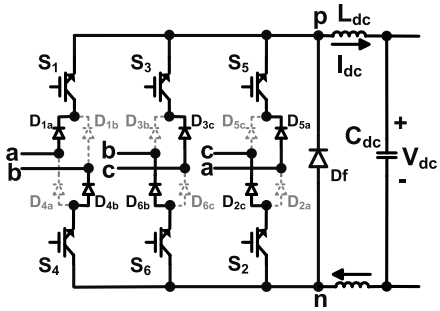

Fig. 6. Equivalent circuit of the DCSR in Sector 12.

loss of the converter. But due to more devices in the current path, it will also increase the conduction loss.

In this paper, a new three-phase CSR, referred as delta-type current source rectifier (DCSR), is proposed to reduce the device conduction loss. As shown in Fig. 2, the three legs in the rectifier are delta connected on the ac input side. Each leg includes two active switches and a diode bridge connected with two phases. In this way, the dc-link current can be shared by multiple legs during operation to reduce the device conduction loss. Although six more diodes are added in DCSR, the current rating of each diode is only half of that in the original topology in Fig. 1. The control algorithm, input and output filters of the traditional CSR can be applied to DCSR directly. Since the output dc voltage must be positive, the energy transfer can only be unidirectional from ac to dc with DCSR in Fig. 2. With the bidirectional DCSR in Fig. 3, the energy can be transferred in both directions.

The operation principle of the DCSR is demonstrated in Section II of this paper. For the design of the DCSR, the voltage and current stresses of the semiconductor devices and the passive components are derived in Section III. Then, the DCSR and the traditional CSR are compared on their current stress and conduction loss in Section IV. Finally, an 8-kW prototype is built to verify the performance of the proposed topology in Section V.

II. Operation Principle

For the analysis of the DCSR rectifier, its input voltages v_a, v_b, and v_c, and the fundamental components i_{a1}, i_{b1}, and i_{c1} of its input currents are defined in (1), where V_m and I_m are the peak values of the sinusoidal voltage and current, respectively, ω is the mains angular frequency, and φ is the phase angle between v_a and i_{a1}

$$\begin{cases} v_a = V_m \cos(\omega t + \varphi) \\ v_b = V_m \cos\left(\omega t - \dfrac{2\pi}{3} + \varphi\right) \\ v_c = V_m \cos\left(\omega t + \dfrac{2\pi}{3} + \varphi\right) \end{cases}$$

$$\begin{cases} i_{a1} = I_m \cos(\omega t) \\ i_{b1} = I_m \cos\left(\omega t - \dfrac{2\pi}{3}\right) \\ i_{c1} = I_m \cos\left(\omega t + \dfrac{2\pi}{3}\right). \end{cases} \quad (1)$$

TABLE I
CONDUCTION STATES OF THE TRADITIONAL CSR AND THE DCSR

Sector	Vector	Traditional CSR	DCSR	Sector	Vector	Traditional CSR	DCSR
Sector 1 $\left(-\varphi, \frac{\pi}{6}\right)$	$\overrightarrow{I_1}$	$[S_1, S_6]$	$[(S_1 S_5), S_4]$	Sector 7 $\left(\pi-\varphi, \frac{7\pi}{6}\right)$	$\overrightarrow{I_4}$	$[S_3, S_4]$	$[S_1, (S_4 S_2)]$
	$\overrightarrow{I_2}$	$[S_1, S_2]$	$[(S_1 S_5), (S_6 S_2)]$		$\overrightarrow{I_5}$	$[S_5, S_4]$	$[(S_3 S_5), (S_4 S_2)]$
	$\overrightarrow{I_0}$	$[S_3, S_6]$	$[S_3, S_4]$		$\overrightarrow{I_0}$	$[S_3, S_6]$	$[S_1, S_6]$
Sector 2 $\left(\frac{\pi}{6}, \frac{\pi}{3}-\varphi\right)$	$\overrightarrow{I_2}$	$[S_1, S_2]$	$[(S_1 S_5), (S_6 S_2)]$	Sector 8 $\left(\frac{7\pi}{6}, \frac{4\pi}{3}-\varphi\right)$	$\overrightarrow{I_5}$	$[S_5, S_4]$	$[(S_3 S_5), (S_4 S_2)]$
	$\overrightarrow{I_3}$	$[S_3, S_2]$	$[S_3, (S_6 S_2)]$		$\overrightarrow{I_6}$	$[S_5, S_6]$	$[(S_3 S_5), S_6]$
	$\overrightarrow{I_0}$	$[S_3, S_6]$	$[S_3, S_4]$		$\overrightarrow{I_0}$	$[S_3, S_6]$	$[S_1, S_6]$
Sector 3 $\left(\frac{\pi}{3}-\varphi, \frac{\pi}{2}\right)$	$\overrightarrow{I_2}$	$[S_1, S_2]$	$[S_5, (S_6 S_2)]$	Sector 9 $\left(\frac{4\pi}{3}-\varphi, \frac{3\pi}{2}\right)$	$\overrightarrow{I_5}$	$[S_5, S_4]$	$[(S_3 S_5), S_2]$
	$\overrightarrow{I_3}$	$[S_3, S_2]$	$[(S_1 S_3), (S_6 S_2)]$		$\overrightarrow{I_6}$	$[S_5, S_6]$	$[(S_3 S_5), (S_4 S_6)]$
	$\overrightarrow{I_0}$	$[S_1, S_4]$	$[S_5, S_4]$		$\overrightarrow{I_0}$	$[S_1, S_4]$	$[S_1, S_2]$
Sector 4 $\left(\frac{\pi}{2}, \frac{2\pi}{3}-\varphi\right)$	$\overrightarrow{I_3}$	$[S_3, S_2]$	$[(S_1 S_3), (S_6 S_2)]$	Sector 10 $\left(\frac{3\pi}{2}, \frac{5\pi}{3}-\varphi\right)$	$\overrightarrow{I_6}$	$[S_5, S_6]$	$[(S_3 S_5), (S_4 S_6)]$
	$\overrightarrow{I_4}$	$[S_3, S_4]$	$[(S_1 S_3), S_4]$		$\overrightarrow{I_1}$	$[S_1, S_6]$	$[S_1, (S_4 S_6)]$
	$\overrightarrow{I_0}$	$[S_1, S_4]$	$[S_5, S_4]$		$\overrightarrow{I_0}$	$[S_1, S_4]$	$[S_1, S_2]$
Sector 5 $\left(\frac{2\pi}{3}-\varphi, \frac{5\pi}{6}\right)$	$\overrightarrow{I_3}$	$[S_3, S_2]$	$[(S_1 S_3), S_6]$	Sector 11 $\left(\frac{5\pi}{3}-\varphi, \frac{11\pi}{6}\right)$	$\overrightarrow{I_6}$	$[S_5, S_6]$	$[S_3, (S_4 S_6)]$
	$\overrightarrow{I_4}$	$[S_3, S_4]$	$[(S_1 S_3), (S_4 S_2)]$		$\overrightarrow{I_1}$	$[S_1, S_6]$	$[(S_1 S_5), (S_4 S_6)]$
	$\overrightarrow{I_0}$	$[S_5, S_2]$	$[S_5, S_6]$		$\overrightarrow{I_0}$	$[S_5, S_2]$	$[S_3, S_2]$
Sector 6 $\left(\frac{5\pi}{6}, \pi-\varphi\right)$	$\overrightarrow{I_4}$	$[S_3, S_4]$	$[(S_1 S_3), (S_4 S_2)]$	Sector 12 $\left(\frac{11\pi}{6}, 2\pi-\varphi\right)$	$\overrightarrow{I_1}$	$[S_1, S_6]$	$[(S_1 S_5), (S_4 S_6)]$
	$\overrightarrow{I_5}$	$[S_5, S_4]$	$[S_5, (S_4 S_2)]$		$\overrightarrow{I_2}$	$[S_1, S_2]$	$[(S_1 S_5), S_2]$
	$\overrightarrow{I_0}$	$[S_5, S_2]$	$[S_5, S_6]$		$\overrightarrow{I_0}$	$[S_5, S_2]$	$[S_3, S_2]$

According to the input voltage and the input current, each line period is divided into 12 sectors for CSR as in Fig. 4. On the space vector plane in Fig. 5, the input current space vector $\overrightarrow{i^*_{\rm abc}} = \sqrt{\frac{2}{3}}\left(i_{a1} + i_{b1}e^{j\frac{2\pi}{3}} + i_{c1}e^{j\frac{-2\pi}{3}}\right) = \sqrt{\frac{3}{2}} I_m e^{j\omega t}$ can be synthesized by six active space vectors $\overrightarrow{I_1}, \overrightarrow{I_2}, \ldots, \overrightarrow{I_6}$ and a zero vector $\overrightarrow{I_0}$. The switches connected with phases x and y are conducting the dc-link current in a space vector, this is denoted by $[x, y], x, y = a, b, c, x \neq y$. Considering both the switching loss and the modulation index range, $\overrightarrow{i^*_{\rm abc}}$is usually realized by two consecutive active vectors and the zero vector in each sector [18]–[24]. In the following analysis, Sector 12 ($11\pi/6 \leq \omega t < 2\pi - \varphi, V_a > V_c \geq V_b$) will be selected as an example to demonstrate the operation principle of the DCSR.

A. Conduction States

In Fig. 6, the equivalent circuit of the DCSR in Sector 12 is drawn with a solid line when $V_a > V_c \geq V_b$. According to the relationship of the input ac voltages, the diode bridge in each leg will clamp the higher phase voltage to the common cathode of two upper diodes, while clamping the lower phase voltage to the common anode of two lower diodes. For example, the diode D_{1b} is blocked and D_{1a} is conducting, since $V_a > V_b$. Similarly, D_{4a} is OFF and D_{4b} is ON in this sector.

The conduction state in the DCSR for each space vector is different from that in the traditional CSR, as compared in Table I. For the traditional CSR, the on state of the switches S_x and S_y in the conduction state is indicated by $[S_x, S_y], x = 1, 3, 5, y = 2, 4, 6$. In the DCSR, the conduction states usually involve three or four switches. $[(S_x S_y), (S_u S_v)], x, y = 1, 3, 5, u, v = 2, 4, 6$ indicates the on state of the switches S_x, S_y, S_u, and S_v in the DCSR.

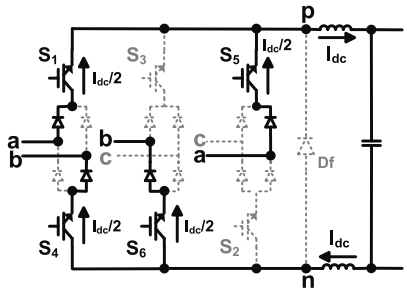

Fig. 7. Conduction state $[(S_1 S_5), (S_4 S_6)]$ in the DCSR.

In Sector 12, the reference current vector $\overrightarrow{i^*_{\rm abc}}$is synthesized with $\overrightarrow{I_1}, \overrightarrow{I_2}$ and $\overrightarrow{I_0}$, as shown in Table I. The current path is shown with solid lines in Fig. 7 for the conduction state $[(S_1 S_5), (S_4 S_6)]$ of the space vector $\overrightarrow{I_1}$. In this state, both S_1 and S_5 are turned ON to share the current in phase a, and both S_4 and S_6 are turned ON to share the current in phase b. In the traditional CSR, the conduction state $[S_1, S_6]$ of the space vector $\overrightarrow{I_1}$ has only S_1 and S_6 ON, as shown in Fig. 8.

In the DCSR, the conduction state for each space vector will change in different sectors depending on the input voltages. In Sector 1 ($-\varphi \leq \omega t < \pi/6, V_a > V_b \geq V_c$), the equivalent circuit is shown in Fig. 9, which is different from that in Sector 12. Accordingly, the conduction states of $\overrightarrow{I_1}, \overrightarrow{I_2}$, and $\overrightarrow{I_0}$ in Sector 1 are different from those in Sector 12, as shown in Table I.

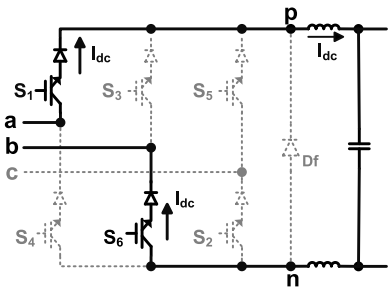

Fig. 8. Conduction state $[S_1,\ S_6]$ in the traditional CSR.

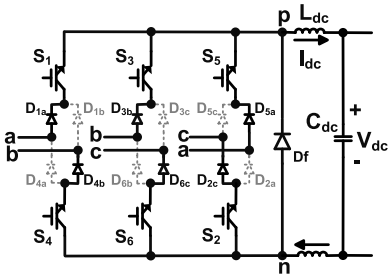

Fig. 9. Equivalent circuit of the DCSR in Sector 1.

B. Modulation Schemes

The "3-switch" and "4-switch" space vector modulation schemes, which contain three and four commutations in a switching period, respectively, are most widely used in traditional CSRs, because they achieve a good compromise between the switching loss and the harmonic current level [22]. "Modified full-wave symmetrical modulation (MFSM)" was introduced in [19]. The space vectors in MFSM are arranged to make the switching voltage the lowest, such that the switching loss is at the minimum [1], [2], [19]–[21]. The gate signals of six switches in the traditional CSR are shown in Fig. 10 for MFSM in Sector 12. The modulation scheme can be characterized through its output voltage $v_{\rm pn}$ and input currents i_a, i_b, and i_c in Fig. 10.

The modulation scheme in the traditional CSR can be simply transformed and applied in the DCSR by substituting the traditional conduction state of each space vector with the new one. The modulation scheme of the DCSR for minimum conduction loss is demonstrated in Fig. 11. To reduce the conduction loss of the converter, it is desirable to use as many devices as possible to share the dc-link current. So the conduction state $[(S_1 S_5)\,, (S_4 S_6)]$ is selected for the space vector $\overrightarrow{I_1}$ instead of $[S_1, S_6]$, and $[(S_1 S_5)\,, S_2]$ is chosen for $\overrightarrow{I_2}$ to replace $[S_1, S_2]$. The switching loss will remain unchanged if the switching energy is assumed to be proportional to the product of the operating voltage and current. At the moment t_1, S_1 and S_5 are turned OFF simultaneously. Since they each carry only half the dc-link current, the total switching energy in the DCSR is comparable to the one in the traditional CSR. In the following sections, the modulation scheme in Fig. 11 is employed in the analysis and experiment.

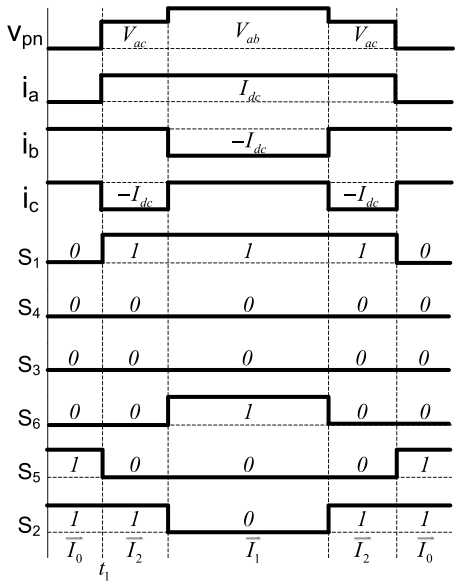

Fig. 10. Modulation scheme MFSM of the traditional CSR in Sector 12.

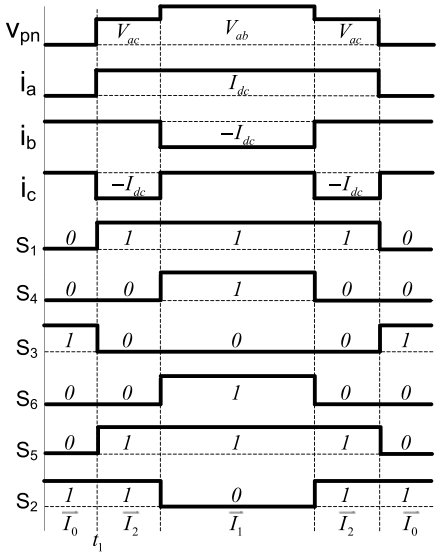

Fig. 11. Modulation scheme of the DCSR in Sector 12 for the minimum conduction loss.

III. Component Stress and Loss Analysis

In this section, the voltage and current stresses of semiconductor devices and passive components in the DCSR will be analyzed. Based on the analysis, the device loss can be calculated and the passive components can be designed. To simplify the analysis, several assumptions are specified as follows:

1) the input voltage on the input capacitor C_s is assumed to be purely sinusoidal, as defined in (1);
2) the fundamental-frequency component of the input current of the DCSR has a phase difference φ from the C_s voltage, as defined in (1);
3) the load current is constant dc current $I_{\rm dc}$ and the load voltage is constant dc voltage $V_{\rm dc}$;

4) the switching frequency f_s is assumed to be much higher than the ac line frequency f;
5) the switching energy has a linear relationship with respect to the product of the operating voltage v_s and current i_s. The turn-on energy is $E_{\rm on} = k_{\rm on}\,|v_s i_s|$, where $k_{\rm on}$ is the turn-on energy coefficient. The turn-off energy is $E_{\rm off} = k_{\rm off}\,|v_s i_s|$, where $k_{\rm off}$ is the turn-off energy coefficient.

A. Stress on Semiconductor Devices

1) Active Switches: Take S_1 as an example. The maximum voltage stress $V_{S_1,\max,\rm DCSR}$ on the switches in the DCSR is 1.5 times of the maximum line-to-neutral ac voltage V_m, which is given as

$$V_{S_1,\max,\rm DCSR} = \frac{3}{2}V_m. \tag{2}$$

The modulation index is defined as

$$M = \frac{I_m}{I_{\rm dc}} = \frac{2V_{\rm dc}}{3V_m\cos\varphi}. \tag{3}$$

The average and rms currents of the switch S_1 are given by

$$\begin{aligned} I_{S_1,\rm avg,DCSR} &= \frac{I_{\rm dc}M}{\pi} \\ I_{S_1,\rm rms,DCSR} &= I_{\rm dc}\sqrt{\frac{M\left(4-\sqrt{3}\cos\varphi\right)}{4\pi}}. \end{aligned} \tag{4}$$

Utilizing the derived rms and average currents, the conduction loss of S_1 can be calculated by (5), where $V_{S_1,\rm on}$ and $R_{S_1,\rm on}$ are the forward voltage bias and the on-resistance of S_1, respectively

$$\begin{aligned} P_{S_1,\rm conduction,DCSR} &= I_{S_1,\rm avg,DCSR}V_{S_1,\rm on} \\ &\quad + I^2_{S_1,\rm rms,DCSR}R_{S_1,\rm on}. \end{aligned} \tag{5}$$

The switching loss of S_1 in the DCSR is given by (6), which is the same as the one in the traditional CSR [21]

$$P_{S_1,\rm switching,DCSR} = \frac{\sqrt{3}V_m f_s I_{\rm dc}\left(k_{\rm on}+k_{\rm off}\right)}{2\pi}. \tag{6}$$

2) Branch Diodes: Take D_{1a} and D_{1b} as an example. The maximum voltage stress on the branch diodes is the peak line-to-line ac voltage $\sqrt{3}V_m$. The average and rms currents of the branch diodes D_{1a} and D_{1b} are given by

$$\begin{aligned} I_{D_{1a},\rm avg,DCSR} &= \frac{I_{\rm dc}M\left(2-\sin\varphi\right)}{4\pi} \\ I_{D_{1a},\rm rms,DCSR} &= I_{\rm dc}\sqrt{\frac{M\left(4-\sqrt{3}\cos\varphi-2\sin\varphi\right)}{8\pi}} \\ I_{D_{1b},\rm avg,DCSR} &= \frac{I_{\rm dc}M\left(2+\sin\varphi\right)}{4\pi} \\ I_{D_{1b},\rm rms,DCSR} &= I_{\rm dc}\sqrt{\frac{M\left(4-\sqrt{3}\cos\varphi+2\sin\varphi\right)}{8\pi}}. \end{aligned} \tag{7}$$

Utilizing the derived rms and average currents, the conduction loss of D_{1a} and D_{1b} are given by (8), where $V_{D,\rm on}$ and $R_{D,\rm on}$ are the forward voltage bias and the on-resistance of the branch diodes, respectively

$$\begin{aligned} P_{D_{1a},\rm conduction,DCSR} &= I_{D_{1a},\rm avg,DCSR}V_{D,\rm on} \\ &\quad + I^2_{D_{1a},\rm rms,DCSR}R_{D,\rm on} \\ P_{D_{1b},\rm conduction,DCSR} &= I_{D_{1b},\rm avg,DCSR}V_{D,\rm on} \\ &\quad + I^2_{D_{1b},\rm rms,DCSR}R_{D,\rm on}. \end{aligned} \tag{8}$$

As shown in (7), the current stresses are different on D_{1a} and D_{1b} and are closely related with the phase angle φ. To demonstrate the difference of the current stresses on D_{1a} and D_{1b}, two parameters $k_{D,\rm rms}$ and $k_{D,\rm avg}$ are defined in (9). The difference between the current stresses of D_{1a} and D_{1b} becomes larger as φ deviates from zero, as shown in Fig. 12

$$\begin{aligned} k_{D,\rm rms} &= \frac{I^2_{D_{1a},\rm rms,DCSR}}{I^2_{D_{1b},\rm rms,DCSR}} \\ k_{D,\rm avg} &= \frac{I_{D_{1a},\rm avg,DCSR}}{I_{D_{1b},\rm avg,DCSR}}. \end{aligned} \tag{9}$$

The range of the 12 sectors in the space vector plane will change with φ, impacting the conduction time of each branch diode. As shown in Fig. 13(a) when $\varphi > 0$, D_{1a} has smaller current stress than D_{1b} due to less conduction time. Otherwise, D_{1b} has smaller current stress, as shown in Fig. 13(b) when $\varphi < 0$.

3) Freewheeling Diode: The maximum voltage stress on the Df is the peak line-to-line ac voltage $\sqrt{3}V_m$. The average and

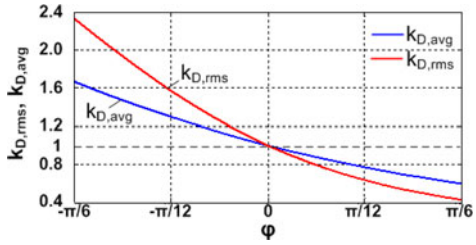

Fig. 12. $k_{D,\rm rms}$ and $k_{D,\rm svg}$ under different φ.

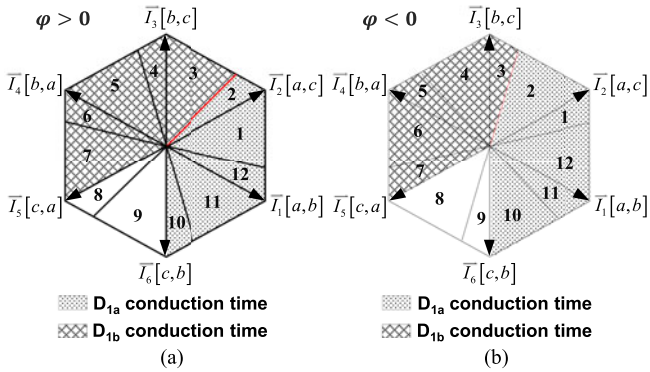

Fig. 13. Conduction time of the branch diodes D_{1a} and D_{1b}, when (a) $\varphi > 0$ and (b) $\varphi < 0$.

rms currents of Df are given by

$$I_{\mathrm{Df,avg,DCSR}} = I_{\mathrm{dc}} - \frac{3I_{\mathrm{dc}}M}{\pi}$$

$$I_{\mathrm{Df,rms,DCSR}} = I_{\mathrm{dc}}\sqrt{1-\frac{3M}{\pi}}. \quad (10)$$

Utilizing the derived rms and average currents, the conduction loss of Df is given by (11), where $V_{\mathrm{Df,on}}$ and $R_{\mathrm{Df,on}}$ are the forward voltage bias and the on-resistance of the Df, respectively

$$P_{\mathrm{Df,conduction,DCSR}} = I_{\mathrm{Df,avg,DCSR}}V_{\mathrm{Df,on}} + I^2_{\mathrm{Df,rms,DCSR}}R_{\mathrm{Df,on}}. \quad (11)$$

B. Stress on Passive Components

1) Dc-Link Inductor L_{dc}: The dc-link inductance is usually selected to limit the dc-link current ripple within 15% to 20% of the load current at full load [25]. When φ is close to 0, the peak value of the dc-link current ripple can be calculated by

$$\Delta i_{L_{\mathrm{dc}},\mathrm{peak,DCSR}} = \frac{V_{\mathrm{dc}}}{2L_{\mathrm{dc}}f_s}\left(1-\frac{\sqrt{3}V_{\mathrm{dc}}}{3V_m}\right) < 7.5\%\cdot I_{\mathrm{dc}}. \quad (12)$$

The rms current of the dc-link current can be derived by (13), shown at the bottom of the page.

2) Output Capacitor C_{dc}: The maximum voltage stress of C_{dc} is the dc output voltage. When φ is close to 0, the rms current of the output capacitor can be approximated by

$$i_{C_{\mathrm{dc}},\mathrm{rms,DCSR}} = \frac{1.11\times10^{-2}V_{\mathrm{dc}}}{L_{\mathrm{dc}}f_s} \times\sqrt{\left(180\pi+45\sqrt{3}\right)M^2-\left(352+600\sqrt{3}\right)M+240\pi}. \quad (14)$$

3) Input Capacitor C_S: The maximum voltage stress of C_S is the peak ac line-to-neutral voltage V_m. The rms current of C_S is given by

$$i_{C_s,\mathrm{rms,DCSR}} = \sqrt{\frac{4I^2_{\mathrm{dc}}V_{\mathrm{dc}}}{3\pi V_m\cos\varphi}-\frac{I^2_m}{2}}. \quad (15)$$

4) Input Inductor L_S: When φ is close to 0, the rms value of the ripple current in the input inductor L_S is given by (16), shown at the bottom of the page.

TABLE II
SPECIFICATION OF THE DCSR

Input voltage	480 V_{ac}, 60 Hz
Input inductor L_S	110 μH
Input capacitor C_S	6.8 μF
Output voltage V_{dc}	400 V_{dc}
Output capacitor C_{dc}	150 μF
Switching frequency f_S	28 kHz
DC-link inductor L_{dc}	1.9 mH

TABLE III
COMPONENT STRESS COMPARISON

Component stress	Analysis	Simulation	Deviation (%)
$I_{S_1,\mathrm{avg,DCSR}}$	4.09 A	4.13 A	0.97
$I_{S_1,\mathrm{rms,DCSR}}$	6.61 A	6.71 A	1.49
$I_{D_{1a},\mathrm{avg,DCSR}}$	1.97 A	1.98 A	0.51
$I_{D_{1a},\mathrm{rms,DCSR}}$	4.51 A	4.61 A	2.17
$I_{D_{1b},\mathrm{avg,DCSR}}$	2.13 A	2.15 A	0.93
$I_{D_{1b},\mathrm{rms,DCSR}}$	4.83 A	4.93 A	2.03
$I_{D_f,\mathrm{avg,DCSR}}$	6.47 A	6.38 A	1.41
$I_{D_f,\mathrm{rms,DCSR}}$	11.02 A	10.95 A	0.64
$\Delta i_{L_{\mathrm{dc}},\mathrm{peak,DCSR}}$	1.54 A	1.54 A	0.00
$i_{L_{\mathrm{dc}},\mathrm{rms,DCSR}}$	18.77 A	18.77 A	0.00
$i_{C_{\mathrm{dc}},\mathrm{rms,DCSR}}$	0.85 A	0.81 A	4.94
$i_{C_s,\mathrm{rms,DCSR}}$	8.45 A	8.68 A	2.65
$\Delta i_{L_s,\mathrm{rms,DCSR}}$	0.28A	0.28 A	0.00

For the input filter design, the total harmonic distortion (THD) is limited to less than 5%, which is given by

$$\Delta i_{L_s,\mathrm{rms,DCSR}} < 5\%\frac{I_m}{\sqrt{2}}. \quad (17)$$

With the converter parameters in Table II, the stresses of the semiconductor devices and passive components have been calculated based on the derived equations under 7.5-kW output power. The analytical results agree well with the simulation ones in Table III.

IV. COMPARISON WITH THE TRADITIONAL CSR

A. Comparison of the Current Stress

The analytical expressions of the current stress of the device have been derived in Section III for the DCSR. In the previous research works, the design procedure has been well demonstrated for the traditional CSR [1], [2]. The current stresses are listed in Table IV for the traditional CSR. Compared with the traditional CSR, the DCSR can reduce the rms current on

$$i_{L_{\mathrm{dc}},\mathrm{rms,DCSR}} = \sqrt{\left(\frac{1.11\times10^{-2}V_{\mathrm{dc}}}{L_{\mathrm{dc}}f_s}\right)^2\left(\left(180\pi+45\sqrt{3}\right)M^2-\left(352+600\sqrt{3}\right)M+240\pi\right)+I^2_{\mathrm{dc}}}. \quad (13)$$

$$\Delta i_{L_s,\mathrm{rms,DCSR}} = \frac{MI_{\mathrm{dc}}}{f_s^2L_sC_s}\sqrt{\frac{1}{36864}\left(25.6-\left(96+\frac{24\sqrt{3}}{\pi}\right)M^2+\frac{398.76}{\pi}M^3-\left(34+\frac{13.5\sqrt{3}}{\pi}\right)M^4\right)} \quad (16)$$

TABLE IV
CURRENT STRESS IN THE TRADITIONAL CSR

Component	Current stress
Switch S_1	$I_{S_1,\mathrm{avg,CSR}} = \frac{I_{\mathrm{dc}}M}{\pi}, I_{S_1,\mathrm{rms,CSR}} = I_{\mathrm{dc}}\sqrt{\frac{M}{\pi}}$
Branch diode D_1	$I_{D_1,\mathrm{avg,CSR}} = \frac{I_{\mathrm{dc}}M}{\pi}, I_{D_1,\mathrm{rms,CSR}} = I_{\mathrm{dc}}\sqrt{\frac{M}{\pi}}$
Freewheeling diode Df	$I_{\mathrm{Df,avg,CSR}} = I_{\mathrm{dc}} - \frac{3I_{\mathrm{dc}}M}{\pi}$ $I_{\mathrm{Df,rms,CSR}} = I_{\mathrm{dc}}\sqrt{1-\frac{3M}{\pi}}$

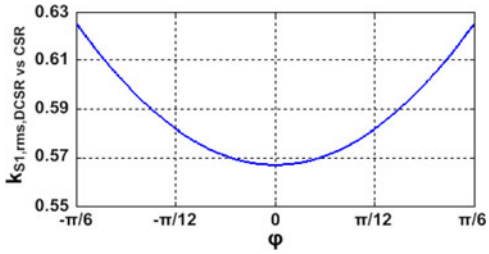

Fig. 14. $k_{S1,\mathrm{rms,DCR\,versus\,CSR}}$ under different φ.

the switches significantly. To compare the rms currents of S_1 in two topologies, the parameter $k_{S_1,\mathrm{rms,DCSR versus CSR}}$ is defined in (18), where $I_{S_1,\mathrm{rms,DCSR}}$ and $I_{S_1,\mathrm{rms,CSR}}$ are the rms currents of S_1 in the DCSR and the traditional CSR, respectively

$$k_{S_1,\mathrm{rms,DCSR\,versus\,CSR}} = \frac{I_{S_1,\mathrm{rms,DCSR}^2}}{I_{S_1,\mathrm{rms,CSR}^2}}. \tag{18}$$

The parameter $k_{S_1,\mathrm{rms,DCSR versus CSR}}$ is related with the phase angle φ, as shown in Fig. 14. It has minimum value when $\varphi = 0$. The rms current of the switch can be reduced by 25% in the DCSR when $\varphi = 0$.

To compare the rms currents of the branch diode in two topologies, the parameter $k_{D,\mathrm{rms,DCSR versus CSR}}$ is defined in (19), where $I_{D_{1a},\mathrm{rms,DCSR}}$ and $I_{D_{1b},\mathrm{rms,DCSR}}$ are the rms currents of D_{1a} and D_{1b}, respectively, in the DCSR, and $I_{D_1,\mathrm{rms,CSR}}$ is the rms current of D_1 in the traditional CSR. The factor 0.5 in (19) indicates that the branch diode D_1 in the traditional CSR has half on-resistance of the branch diode D_{1a} in the DCSR, assuming the total chip area of the branch diodes is the same in both topologies and the on-resistance of the diode is inversely proportional to its chip area

$$k_{D,\mathrm{rms,DCSR versus CSR}} = \frac{I^2_{D_{1a},\mathrm{rms,DCSR}} + I^2_{D_{1b},\mathrm{rms,DCSR}}}{I^2_{D_1,\mathrm{rms,CSR}} \times 0.5}. \tag{19}$$

The parameter $k_{D,\mathrm{rms,DCSR versus CSR}}$ is also related with the phase angle φ, as shown in Fig. 15. $k_{D,\mathrm{rms,DCSR versus CSR}} > 1$, indicating that the rms current of the branch diode will increase in the DCSR. The rms current is increased by 6% on the branch diodes in the DCSR when $\varphi = 0$, which is much lower compared with the current stress reduction on S_1.

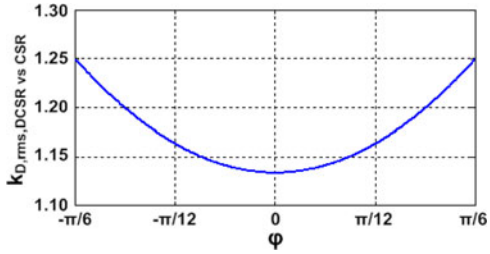

Fig. 15. $k_{D,\mathrm{rms,DCSR\,versus\,CSR}}$ under different φ.

TABLE V
CONDITIONS FOR CONDUCTION LOSS COMPARISON

Topology	DCSR	Traditional CSR
Output power	0–100 kW	
Input voltage	480 Vac, 60 Hz	
Modulation index	0.5–1	
Phase angle φ	$-\pi/6 - \pi/6$	

B. Comparison of the Conduction Loss

Based on the above analysis, the conduction loss of the semiconductor devices can be calculated under different operating conditions in Table V. The 1200-V SiC Schottky diode from CREE is selected as the branch diode or the Df [26]. The switches are realized with either 1200-V SiC MOSFET from CREE or 1200-V Si Trench and Fieldstop IGBT from Infineon [26], [27]. The two topologies are compared assuming the same semiconductor chip area.

To generalize the comparison to different power levels, the chip area is assumed to be proportional to the current rating of the device [28]. Based on the datasheets provided by the semiconductor manufacturers, this relationship is fitted by (20), where $A_{\mathrm{SiIGBT,1200\,V}}$ is the chip area of Si IGBT, $A_{\mathrm{SiCMOSFET,1200\,V}}$ is the chip area of SiC MOSFET, $A_{\mathrm{SiCdiode,1200\,V}}$ is the chip area of SiC Schottky diode, and I_N is the device current rating

$$\begin{aligned} A_{\mathrm{SiIGBT,1200\,V}} &= (0.95I_N + 3.2)\,\mathrm{mm}^2 \\ A_{\mathrm{SiCMOSFET,1200\,V}} &= (0.52I_N)\,\mathrm{mm}^2 \\ A_{\mathrm{SiCdiode,1200\,V}} &= (0.45I_N + 0.59)\,\mathrm{mm}^2. \end{aligned} \tag{20}$$

In the calculation, the forward voltage bias of the Si IGBT and SiC Schottky diode is assumed to be constant under different current ratings. The on-resistance of the device is inversely proportional to its chip area. The forward voltage drop V_{on} of the device can be given by (21), where V_o is the forward voltage bias, i is the device current, R_o is the on-resistance when the chip area is A, and $R_{o,N}$ is the on-resistance when the chip area is A_N

$$\begin{aligned} V_{\mathrm{on}} &= V_o + i \cdot R_o \\ R_o &= \frac{R_{o,N} \cdot A_N}{A}. \end{aligned} \tag{21}$$

Given the output power level, the current rating, the die area, and the on-resistance of the device can be determined subsequently. Then, the conduction loss can be calculated under

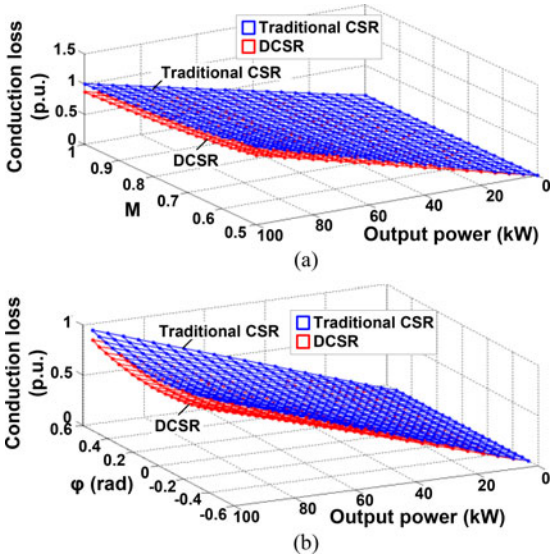

Fig. 16. Comparison of the conduction loss in two topologies using Si IGBT, when (a) $\varphi = 0$ or (b) $M = 1$.

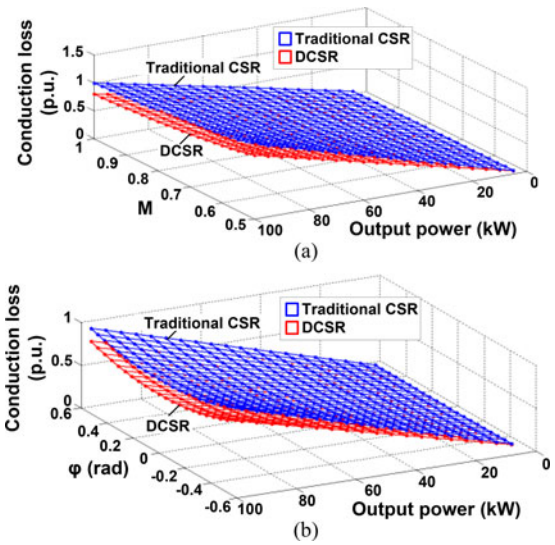

Fig. 17. Comparison of the conduction loss in two topologies using SiC MOSFET, when (a) $\varphi = 0$ or (b) $M = 1$.

different output power levels, modulation indices, and phase angles φ. As shown in Fig. 16, the DCSR has 10% to 15% less conduction loss than the traditional CSR when Si IGBT is applied as the switch. If SiC MOSFET is applied as the switch, the savings on the conduction loss in the DCSR can reach 15% to 20% in Fig. 17.

V. Experimental Verification

As shown in Fig. 18, an 8-kW prototype of the DCSR has been built with the specification in Table II. The size of the prototype is 9.1 in (L) × 6.9 in (W) × 5.0 in (H). The semiconductor devices and passive components used in the prototype are listed in Table VI. In the prototype, the 1200-V, 20-A SiC MOSFETs and 1200-V, 18-A SiC Schottky diodes are applied as

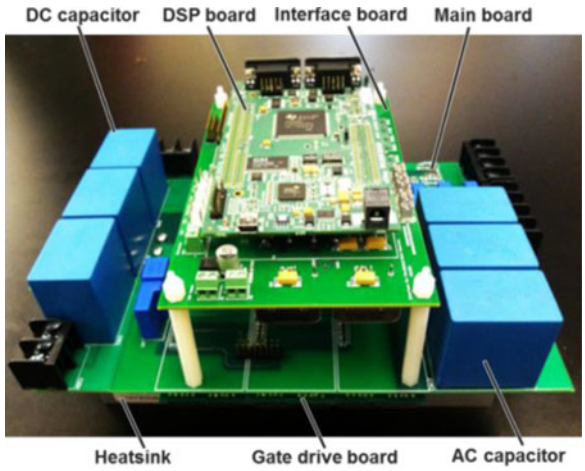

Fig. 18. 8-kW prototype of the DCSR.

TABLE VI
Device and Passive Components in Prototype

Component	Description
Switches	SiC MOSFET, 1200 V/20 A, C2M0080120D, CREE
Branch and Dfs	SiC Schottky diode, 1200 V/18 A, C4D10120D, CREE
Input inductor	110 μH, Ferrite R, EE core, 0R45724EC, Magnetics 13 turns of AWG#12 wire
Input capacitor	6.8 μF/330 V_{ac}, film, B32916A3685, EPCOS
Dc-link inductor	1.9 mH, Nanocrystalline, C core, MK Magnetics 42 turns of copper foil (cross section area = 12.9 mm^2)
Output capacitor	3 × 50 μF/450 V_{dc}, film, B32776G4506, EPCOS

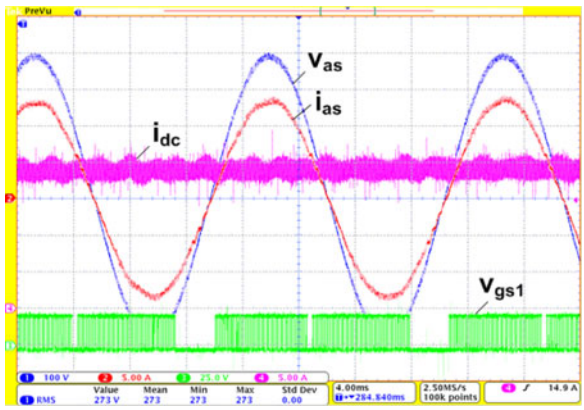

Fig. 19. Experimental waveforms of the DCSR under 8-kW output power (v_{as} 100 V/div, i_{as} 5 A/div, i_{dc} 5 A/div, v_{gs1} 25 V/div, time 4 ms/div).

the switches and diodes, respectively [26]. Moreover, the prototype can be easily configured as a traditional CSR by paralleling the two branch diodes in the DCSR. In this way, the performance of both topologies can be measured and compared.

A. Experimental Results Under Different Operating Conditions

The experimental waveforms of the DCSR under 8-kW output power are shown in Fig. 19. The input current i_{as} has almost

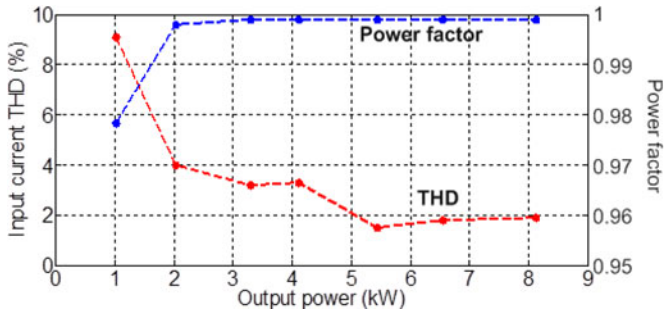

Fig. 20. Input current THD and power factor of the DCSR.

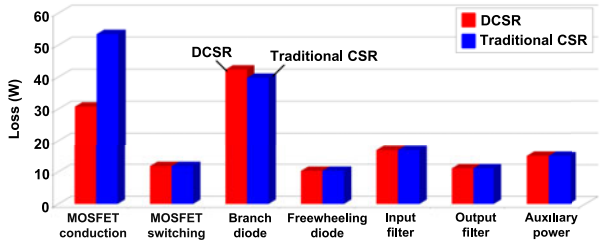

Fig. 21. Calculated loss breakdown of the DCSR and the traditional CSR.

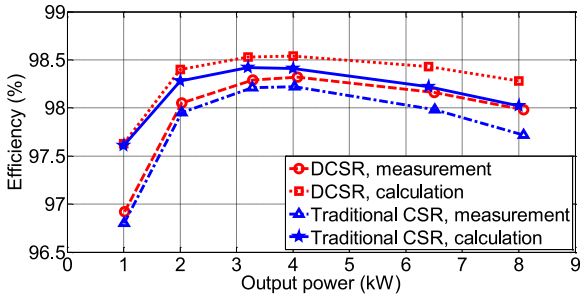

Fig. 22. Calculated and measured efficiency of the two topologies.

sinusoidal waveform and is in phase with the input voltage $v_{\rm as}$. The dc-link current $i_{\rm dc}$ is controlled to be almost constant. The gate signal of the switch S_1 is shown as $v_{\rm gs1}$ in Fig. 19 as well.

The input current THD and the power factor are shown in Fig. 20 under different output power levels. The DCSR can achieve unity power factor and low input harmonics in most of the power range.

The semiconductor device loss of the DCSR and the traditional CSR can be calculated based on the analysis in the previous sections. The loss of passive components can be calculated according to the design method in [2]. The loss breakdown of the two topologies is shown in Fig. 21 under 8-kW output power. The DCSR can save significant conduction loss on SiC MOSFETs while keeping other parts of loss comparable to the traditional CSR.

The efficiencies of both topologies are measured with YOKOGAWA power analyzer PZ4000 and compared under different output power levels in Fig. 22. The DCSR has higher efficiency over the traditional CSR, which is more obvious under large output power. The total loss is reduced by 13% under 8 kW with the DCSR. The peak efficiency of the DCSR is 98.3% under 4 kW. The error between the calculated efficiency and the measured one may come from the linear model of the switching energy and the inaccurate estimation of the junction temperature.

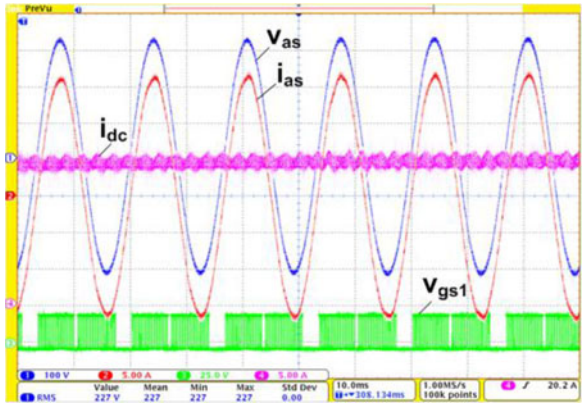

Fig. 23. Experimental waveforms under 400 $V_{\rm ac}$ ($v_{\rm as}$ 100 V/div, $i_{\rm as}$ 5 A/div, $i_{\rm dc}$ 5 A/div, v_{gs1} 25 V/div, time 10 ms/div).

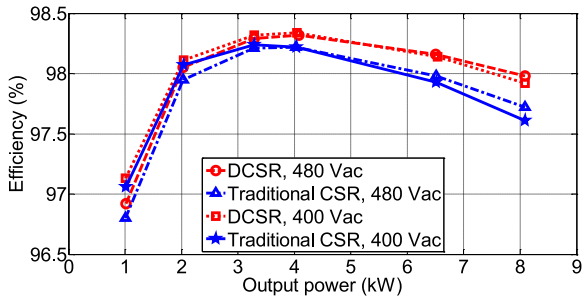

Fig. 24. Efficiency comparison under different input voltages.

The prototype is also tested under 400 $V_{\rm ac}$ input voltage, as shown in Fig. 23. When the input voltage is 400 $V_{\rm ac}$, the conduction loss will increase, but the switching loss will decrease. The measured efficiency curves are compared in Fig. 24, where the DCSR has higher efficiency than the traditional CSR under either 400 or 480 $V_{\rm ac}$. To compensate the reactive power in the input filter, the input current and input voltage of the rectifier have a phase angle difference φ, which varies with the output power and input voltage, as shown in Fig. 25.

Furthermore, the prototype is tested under 46-kHz switching frequency, as shown in Fig. 26. The efficiency curves of the two topologies are measured and compared in Fig. 27, where the DCSR has a higher efficiency than the traditional CSR under either 28- or 46-kHz switching frequency.

B. Device Current Sharing

To maximize the benefit of the DCSR, the dc-link current should be shared equally between two legs. The current sharing depends on the characteristics of the semiconductor devices, as well as on the layout of the commutation circuit [29]–[34].

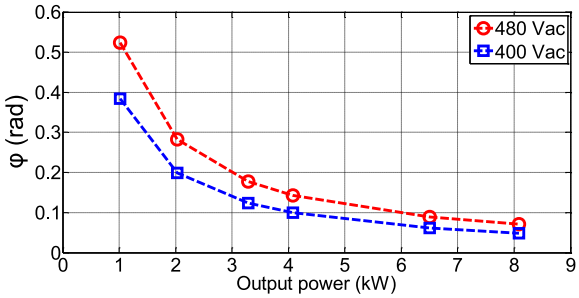

Fig. 25. Input phase angle φ as function of output power.

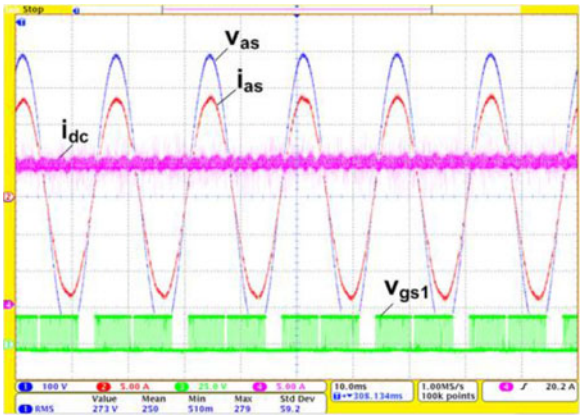

Fig. 26. Experimental waveforms with 46-kHz switching frequency ($v_{\rm as}$ 100 V/div, $i_{\rm as}$ 5 A/div, $i_{\rm dc}$ 5 A/div, v_{gs1} 25 V/div, time 10 ms/div).

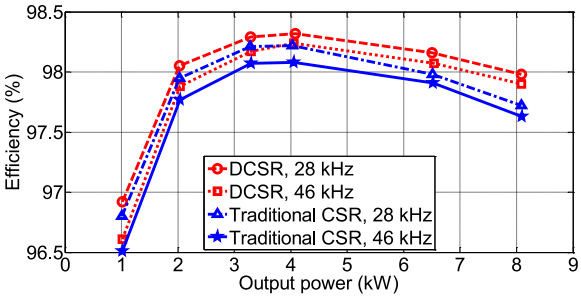

Fig. 27. Efficiency comparison for different switching frequencies.

In previous research works, some work has been done to balance the current in paralleled devices (IGBTs and MOSFETs) in a single switch [32]–[34]. The problem is not totally the same in the DCSR, where two legs are in parallel to share the current. Moreover, the location of the paralleled legs depends on the input voltages and the modulation scheme.

For the DCSR design, first the device characteristics were measured with 371B curve tracer [35]. Then, the devices with similar characteristics were selected and applied in the prototype. Three legs in the DCSR were placed close to each other in the PCB layout to reduce the parasitic inductance in the commutation loop. The decoupling capacitors were then distributed on three ac buses. The advanced power module package can be implemented to further reduce the parasitic inductance in the DCSR [36]. Some active control methods invented previously can also be applied in the DCSR to control the gate drive signals of the switches to balance the transient and static currents [32]–[34].

VI. Conclusion

In this paper, a new three-phase CSR topology, DCSR, has been proposed. It has a delta connection on its input side, and the dc-link current can be shared by more switches to reduce up to 20% conduction loss. The conduction states and modulation schemes have been discussed, and the analytical equations of the current stress have been derived for the design of the DCSR. Compared with the traditional CSR, the DCSR has lower device current stress on the active devices. To validate the performance of the proposed topology, an 8-kW prototype has been built and tested. It has been shown experimentally that DCSR has higher efficiency over the traditional CSR under various operating conditions.

Acknowledgment

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