A Single-Phase Four-Switch Rectifier With Significantly Reduced Capacitance

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***Abstract*—A single-phase four-switch rectifier with considerably reduced capacitance is investigated in this paper. The rectifier consists of one conventional rectification leg and one neutral leg linked with two capacitors that split the dc bus. The ripple energy in the rectifier is diverted into the lower split capacitor so that the voltage across the upper split capacitor, designed to be the dc output voltage, has very small ripples. The voltage across the lower capacitor is designed to have large ripples on purpose so that the total capacitance needed is significantly reduced and highly reliable film capacitors, instead of electrolytic capacitors, can be used. At the same time, the rectification leg is controlled independently from the neutral leg to regulate the input current to achieve unity power factor and also to maintain the dc-bus voltage. Experimental results are presented to validate the performance of the proposed strategy.**

***Index Terms*—Electrolytic capacitors, neutral leg, reliability, ripple eliminator, single-phase rectifiers, voltage ripples.**

I. Introduction

MORE and more microgrids are now connected to the public grid and various loads through power converters [1]. For both ac and dc microgrids, single-phase rectifiers are often needed when supplying dc loads. Such rectifiers are expected to have high power density, high efficiency, high reliability and low costs. There are numerous topologies in the literature, aiming to have improved performance from these three aspects. Moreover, with the integration of renewable energy sources into the power grid, there is a trend to have bidirectional single-phase power converter as an interface between power grid and energy sources [1]–[3]. As a result, the study of single-phase rectifiers has attracted more and more attention.

Conventionally, bulky electrolytic capacitors are required for single-phase rectifiers to produce smooth dc-bus voltage, due to the pulsating input power. However, the volume and weight of bulky electrolytic capacitors could be a serious problem for volume-critical and/or weight-critical applications, such as electrical vehicles [4] and aircraft power systems [5]. What is worse is that electrolytic capacitors, known to have limited lifetime, are one of the most vulnerable components in power electronic systems [6]–[8]. As a result, in order to enhance the reliability of power electronic systems, it is highly desirable to minimise the usage of electrolytic capacitors and use highly-reliable small capacitors like film capacitors if possible, while maintaining low voltage ripples.

In general, the reduction of electrolytic capacitors can be achieved in four approaches. One approach is to inject harmonic currents to suppress fluctuations of input energy by changing control strategies for existing power switches in rectifiers. In [9], it was proposed to reduce the dc-bus capacitor by injecting third harmonic component to the grid current. This approach benefits from fewer switches and easier implementation, which lead to lower system costs compared to other solutions. The second approach is to add an active energy storage compensator in parallel with dc-bus capacitors to bypass ripple energy that originally flows into dc-bus capacitors [5], [10]–[16]. This has been extensively studied in the last few years. Normally, the added compensator is operated as buck/boost converters to inject/absorb ripple currents from dc bus. The third approach is based on connecting an active compensator in series with the dc bus [17]. The compensator basically behaves as a voltage source to offset voltage ripples. Due to the series connection, the compensator has lower voltage stress compared to parallel compensators. The last approach is to introduce a ripple port terminated with a capacitor, as reported in [8], [18], to store the ripple power. Different from other solutions, an ac capacitor instead of a dc capacitor is used to handle ripple energy, which also reduces the voltage stress on the switches.

Following the preliminary conference version of this paper [19], a four-switch rectifier is proposed to significantly reduce the dc-bus capacitance in the widely-adopted asymmetrical single-phase systems, where the midpoint of the ac side is not available. The rectifier only uses four switches, which is similar to a conventional bridge PWM rectifier, but the switches are formed as a rectification leg and a neutral leg and operated differently from a conventional full-bridge rectifier. The rectification leg is operated as a half-bridge rectifier to regulate the dc-bus voltage via controlling the grid current to make it clean and in phase with the grid voltage to achieve unity power factor. The neutral leg, consisting of two active switches, two split capacitors and one inductor, maintains a stable dc output voltage. The control of the two legs are independent from each other, which makes control design very flexible, and the corresponding control strategies can be designed according to their own objectives. Importantly, the neutral leg is able to divert the ripple energy from the upper split (output) capacitor to the lower split capacitor. As a result, the output voltage does not contain

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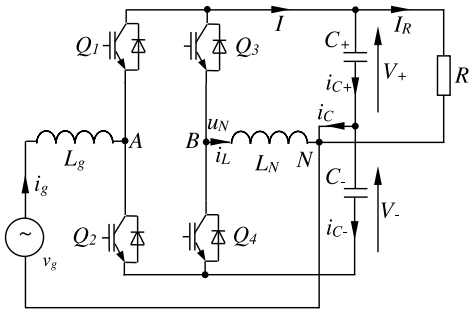

Fig. 1. Single-phase rectifier under investigation.

any low frequency ripples and hence, the upper split capacitor can be significantly reduced. Note that the voltage across the lower split capacitor is designed to have relatively large ripples on purpose because it is not supplied to any loads. Accordingly, the total usage of dc-bus capacitors could be reduced significantly so that it is now possible to use highly reliable film capacitors, instead of bulky electrolytic capacitors. This makes the rectifier very suitable for high-reliability applications. The selection criteria of the split capacitors are discussed with the aim to minimise their usage. This is mainly for systems without hold-up time requirement. For systems with hold-up requirement, the required capacitance needs to be large enough if no other means is applied to provide the energy required [17].

The rest of the paper is organised as follows. Section II introduces the rectifier under investigation. In Section III, how to significantly reduce dc-bus capacitors is discussed and, in Section IV, the associated control strategies are developed. In order to achieve the minimal capacitance, the selection criteria of the split capacitors are then discussed in Section V and the impact of the different voltages across the split capacitors are analyzed in Section VI. Experimental results are provided in Section VII and the conclusions are made in Section IX.

II. Single-Phase Rectifier Under Investigation

The rectifier proposed in the preliminary version of this paper [19] is investigated further in this paper. It consists of one rectification leg and one neutral leg, as shown in Fig. 1. The rectifier can be formed by adding two active switches into a conventional half-bridge PWM rectifier by putting a neutral leg consisting of two switches across the dc bus with their midpoint connected to the midpoint of the split capacitors through an inductor. The neutral leg is actually a typical dc/dc converter, which has been widely adopted in industry. In particular, the neutral leg has been applied to three-phase four-wire power inverters as reported in [1], [20]–[22]. According to the analysis made in [1], the neutral leg is a stable system although the inductor is coupled with the split capacitors.

It is well known that bulky electrolytic capacitors are often needed for single-phase rectifiers to smooth the second-order voltage ripples on the dc bus. However, the reliability, volume and weight of electrolytic capacitors could be a serious problem for high-reliability, volume-critical and weight-critical applications [6]–[8]. As a result, in order to enhance the reliability and power density of rectifiers, it is highly desirable to reduce the usage of capacitors so that highly-reliable capacitors like film capacitors could be used to replace electrolytic capacitors. However, for conventional single-phase rectifiers, there exists a tradeoff between reducing required capacitors and reducing the output voltage ripples because single-phase full-bridge rectifiers have only one dc voltage, which is used as both the dc output and the only ripple energy buffer on the dc bus. In light of this, a lot of auxiliary circuits are proposed to construct another dc or ac voltage to store the voltage ripples, which can be connected in parallel or in series at the ac or dc sides [5], [8], [13], [23], [24].

For the topology shown in Fig. 1, there are two dc voltages because of the split capacitors. This provides a possible way to operate the rectifiers to make one of the voltages as the output voltage to supply loads and to make the other voltage as the ripple energy buffer. The total capacitance could be significantly reduced because the ripple energy is diverted from the output capacitor to the other capacitor, which could have high voltage ripples. By diverting all the ripple power to the lower capacitor C_-, the output voltage V_+ can become ripple free, which means the output capacitance C_+ can be reduced a lot because it does not need to process any low frequency ripple energy. Importantly, the capacitor C_- can also be significantly reduced because its voltage is not supplied to any loads so it can be designed to have large ripples on purpose. Accordingly, both capacitors can be significantly reduced and replaced with highly-reliable film capacitors. This improves the system power density and reliability and reduces system weight and volume. Although costly film capacitors are used to replace electrolytic capacitors, the cost arising from capacitors could still be reduced because the total capacitance required is considerably reduced.

III. Reduction of the Bulky DC-Bus Capacitors

In order to clearly show how to significantly reduce the dc-bus capacitors, there is a need to analyze the relationship between the ripple energy and the required capacitors for the investigated rectifier. For this purpose, an average circuit model is built up at first.

A. Circuit Analysis

It is assumed that the dc-bus voltage of the rectifier is

$$V_{DC} = V_+ + V_- \tag{1}$$

where V_+ and V_- are the voltages across the split capacitors C_+ and C_- with respect to the neutral point N and the negative point of the dc bus, respectively. Suppose that the grid current is

$$i_g = I_g \sin \omega t \tag{2}$$

and the grid voltage is

$$v_g = V_g \sin \omega t \tag{3}$$

in which V_g and I_g are the peak values of the grid voltage and current, respectively, and ω is the angular line frequency. Note that the grid voltage and current are supposed to be in phase in

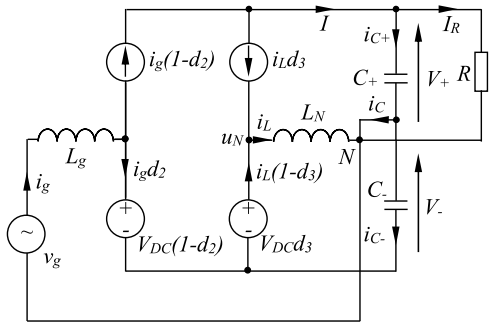

Fig. 2. Average circuit model of the rectifier shown in Fig. 1.

order to achieve unity power factor, and i_g is a pure ac current without a dc component.

Because the switches are operated at a frequency much higher than the fundamental frequency, the averaged variables, e.g., average currents and average voltages, can be adopted to well represent the original variables according to the averaging theory [25] so that the circuit can be analysed by using the average circuit model [26], [27]. The average circuit model of the rectification leg can be built following the procedures developed in [26]. The switches Q_1 and Q_2 are replaced with a current source $i_g(1-d_2)$ and a voltage source $V_{DC}(1-d_2)$, where d_2 is the duty cycle of Q_2, as shown in Fig. 2. Similarly, the average circuit model of the neutral leg can be obtained as shown in Fig. 2, where d_3 is the duty cycle of Switch Q_3. Note that, in this paper, the split capacitors are not necessarily the same, unlike the case in [26], [28], [29], so the model in this paper is more generic. Also note that in order to facilitate the exposition in the sequel, the duty cycle of the lower switch of the rectification leg (Q_2) and the duty cycle of the upper switch of the neutral leg (Q_3) are adopted in the model.

According to the average circuit model of the rectifier shown in Fig. 2, the capacitor currents can be found as

$$i_{C+} = i_g(1-d_2) - I_R - i_L d_3 \tag{4}$$

$$i_{C-} = -i_g d_2 + i_L(1-d_3) \tag{5}$$

and the neutral current i_L can be found as

$$i_L = i_{C-} - i_{C+} + i_g - I_R. \tag{6}$$

In order to obtain the unity power factor, the two switches Q_1 and Q_2 can be operated complementarily to track the reference of the grid current, which is in phase with the grid voltage. Since the switching frequency is much higher than the line frequency, the duty cycle of switch Q_2 can be calculated in the average sense as

$$d_2 = \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}}\sin\omega t \tag{7}$$

to maintain the dc-bus voltage V_{DC}, according to [26], [29]. Normally, switches Q_3 and Q_4 are operated complementarily to split the dc-bus voltage V_{DC} into V_+ and V_- [1], [21], [30], [31]. The duty cycle of switch Q_3 can be calculated as

$$d_3 = \frac{V_-}{V_{DC}} \tag{8}$$

because the neutral leg is operated as a dc/dc buck converter. Because of the power balance between the ac and dc sides (ignoring the power losses), there is

$$\frac{V_g I_g}{2} = \frac{V_+^2}{R} \tag{9}$$

and the load current is

$$I_R = \frac{V_g I_g}{2V_+}$$

which is also the dc component of current I. (4) can then be rewritten as

$$\begin{aligned} i_{C+} &= I_g \sin\omega t\left(\frac{V_-}{V_{DC}} + \frac{V_g}{V_{DC}}\sin\omega t\right) - \frac{V_g I_g}{2V_+} - \frac{V_-}{V_{DC}} i_L \\ &= \frac{V_-}{V_{DC}} i_g - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t \\ &\quad - \frac{V_g I_g V_-}{2V_+ V_{DC}} - \frac{V_-}{V_{DC}} i_L. \end{aligned} \tag{10}$$

Similarly, (5) can be rewritten as

$$\begin{aligned} i_{C-} &= -I_g \sin\omega t\left(\frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}}\sin\omega t\right) + i_L\left(1 - \frac{V_-}{V_{DC}}\right) \\ &= -\frac{V_+}{V_{DC}} i_g - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t \\ &\quad + \frac{V_g I_g}{2V_{DC}} + \frac{V_+}{V_{DC}} i_L. \end{aligned} \tag{11}$$

As is well known, no dc currents could pass through capacitors. As a result, i_L should have a dc component so that i_{C+} and i_{C-} do not have any dc component. It can be found out from (10) and (11) that the dc component of i_L is $-I_R = -\frac{V_g I_g}{2V_+}$, i.e., the same value as the load current.

If the neutral current i_L is controlled to provide the dc component only, that is

$$i_L = -I_R$$

then the capacitor currents are

$$i_{C+} = \frac{V_-}{V_{DC}} i_g - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t$$

and

$$i_{C-} = -\frac{V_+}{V_{DC}} i_g - \frac{V_g I_g}{2V_{DC}}\cos 2\omega t.$$

In addition to the same second-order ripple current $-\frac{V_g I_g}{2V_{DC}}\cos 2\omega t$ flowing through the split capacitors, the grid current i_g is split between i_{C+} and i_{C-} because in this case

$$i_{C+} + (-i_{C-}) = i_g$$

which could lead to high voltage ripples and hence bulky electrolytic capacitors are needed. In order to reduce the voltage ripples, the current flowing through the capacitors should be regulated differently. For this reason, a different control strategy is proposed in the next section.

B. Reduction of DC-Bus Capacitance

The idea is to push the current components of i_{C+} in (10) through the neutral leg instead of through the upper split capacitor so that i_{C+} does not contain any fundamental or second order ripple currents. That is to make $i_{C+}=0$, ignoring the switching ripples. Hence, according to (10), the current i_L should be controlled to satisfy

$$i_L = i_g - \frac{V_g I_g}{2V_-}\cos 2\omega t - \frac{V_g I_g}{2V_+}. \tag{12}$$

On the other hand, i_L should also satisfy (6). Hence, in this case, the current flowing through the lower split capacitor should be

$$i_{C-} = -\frac{V_g I_g}{2V_-}\cos 2\omega t. \tag{13}$$

In other words, it only contains the second-order harmonic component or the second-order component only flows through the lower split capacitor. As a result, all the voltage ripples are then diverted to the lower capacitor C_-, which would increase the voltage ripples on C_-. However, this does not matter because there is no load connected to V_- and the voltage V_- can tolerate a much higher ripple voltage. Hence, only a small C_- is needed. Since the upper capacitor C_+ does not contain any fundamental and second-order ripple voltage components any more, it can be reduced a lot while maintaining low voltage ripples. As a result, both capacitors C_+ and C_- can be very small, which makes it possible to replace the required bulky electrolytic capacitors with film capacitors.

IV. Control Design

A. Control of the Neutral Leg

The neutral leg should be controlled to maintain the output voltage V_+, to remove the ripple components in i_{C+} and also to remove the fundamental component in i_{C-}.

1) Regulation of the Output Voltage V_+: Maintaining a stable output voltage V_+ with very small ripples at the desired output reference voltage V_+^* is a major target. The regulation of the sum of the voltages V_+ and V_-, i.e., the dc-bus voltage V_{DC}, is the task of the rectification leg and will be discussed in the next section. The neutral leg is responsible for splitting the dc-bus voltage into V_+ and V_-, which are independent from each other. Since the voltage V_+ is used as the output voltage, it can be directly controlled by forming a voltage loop and then the voltage V_- can be indirectly controlled by regulating the dc-bus voltage.

In order to regulate the output voltage V_+, it is measured and put through the hold filter

$$H(s) = \frac{1-e^{-Ts}}{Ts} \tag{14}$$

where T is the fundamental period of the grid voltage, to extract its dc component, as shown in Fig. 3. A simple proportional-integral (PI) controller is then applied to regulate the voltage. The output of the PI controller can be converted to PWM signals to drive the switches. The parameters for the PI controller can be selected according to classical design methods for a second-order system, with the characteristic equation given by

$$s^2 + \frac{K_p}{C_+}s + \frac{K_i}{C_+} = 0$$

where K_p and K_i are the gains of the PI controller. These parameters can be chosen to obtain the damping coefficient of

$$\frac{K_p}{2}\sqrt{\frac{1}{C_+K_i}} = \frac{1}{\sqrt{2}}.$$

As a result

$$K_p^2 = 2C_+K_i. \tag{15}$$

The relationship between K_p and K_i is mostly related to the capacitor C_+. In practice, K_p or K_i can be initially set to small values, which approximately satisfy (15), and then gradually be increased to achieve the desired performance. In this way, both parameters can be well tuned.

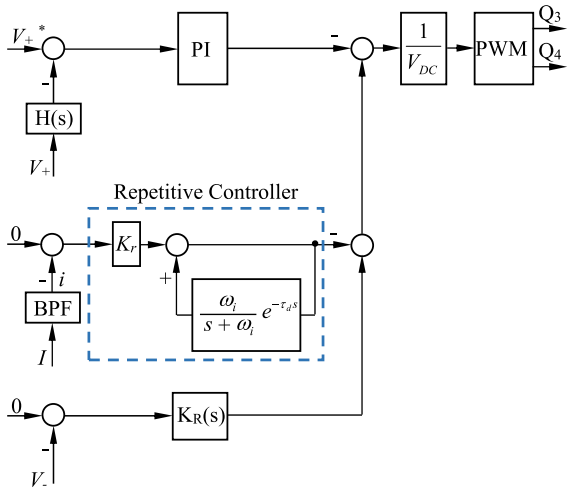

Fig. 3. Controller for the neutral leg.

2) Removal of the Ripple Components in i_{C+}: As discussed before, the capacitor current i_{C+} should be maintained around zero in order to smooth the ripples of the output voltage V_+. Note that C_+ is now very small so the ripple current may flow through the dc load and it is more effective to minimize the ripple component i in the dc-bus current I. As a result, instead of controlling i_{C+}, the strategy to minimize the dc-bus ripple current i is adopted in this paper. In order to extract this second-order ripple component, a bandpass filter (BPF) is adopted, via adding a resistor–capacitor circuit on the path of the measured I to filter out the switching ripples at first and then using a digital high pass filter $\frac{s}{s+10}$ to remove the dc component. The used resistor and capacitor are 10 kΩ and 0.01 μF. As a result, the transfer function of the BPF is $\frac{10000s}{(s+10)(s+10000)}$. The cutoff frequencies of the BPF are 1.59 Hz on the lower side and 1591 Hz on the higher side so the bandwidth of the BPF is 1589 Hz.

Several possible controllers, e.g., hysteresis controllers with a variable switching frequency and repetitive controllers with a fixed switching frequency, can be applied to minimize the ripple current i. In order to reduce the stress on the switches,

a repetitive controller is applied in this paper as shown in the dashed box of Fig. 3. Another benefit of the repetitive controller is its high performance to handle harmonics [1], [32]. The repetitive controller consists of a proportional controller K_r and an internal model given by

$$C(s) = \frac{K_r}{1 - \frac{\omega_i}{s+\omega_i} e^{-\tau_d s}}$$

where τ_d is designed based on the analysis in [1], [32] as

$$\tau_d = \tau - \frac{1}{\omega_i} = 0.0196\,\text{s}$$

with $\omega_i = 2550,\ \tau = 0.02$ s.

Note that the regulation of V_+ deals with the dc component but the removal of the ripple components of i_{C+} deals with non-dc components. Hence, the output of the repetitive controller can be added to the output of the PI controller for V_+ to generate the PWM signals for the switches Q_3 and Q_4, as shown in Fig. 3. Note that the "$-$" sign at the output of the controllers is because the duty cycle controlled is d_3 instead of d_4, which is $1 - d_3$.

In general, the adoption of the BPF does not lead to any resonance of the controllers with the rectifier. This is mainly due to the fact that the BPF behaves as a low-pass filter at high frequencies and is cascaded with the repetitive controller, which again is a low-pass filter.

3) Removal of Fundamental Component in i_{C-}: The control of the dc-bus ripple current i to 0 leads to the fact that the ripples are now diverted to the lower capacitor C_-. In this case, the current of the capacitor C_- is expected to only have a second-order component. However, according to (6), when $i = 0$, there is

$$i_g = i_L - i_{C-} + I_R$$

which means that the grid current i_g could flow through the inductor L_N and the capacitor C_- if not controlled properly. Hence, there is a need to make sure that no fundamental component flows through the capacitor C_- otherwise it would lead to increased voltage ripples without providing any benefits.

This can be achieved by forcing the fundamental component of V_- to be zero, as shown in Fig. 3. The following resonant controller

$$K_R(s) = \frac{K_h 2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2} \tag{16}$$

with $\xi = 0.01$, $h = 1$, and $\omega = 2\pi f$, can be adopted. The output of the resonant controller is then added onto the outputs of the other two controllers before sending to the PWM conversion block, as shown in Fig. 3. The gain K_h of the resonant controller can be selected by fine tuning through trial-and-error in practice; it is chosen as $K_h = 10$ for the experimental system to be tested. In general, a large gain should improve the performance of the control but may lead to a large charging current when starting up the system that might trigger the current protection and also may introduce noticeable disturbance into the current controller. These should be avoided. Note that the output of this controller is "+" because the voltage under control relates to V_-.

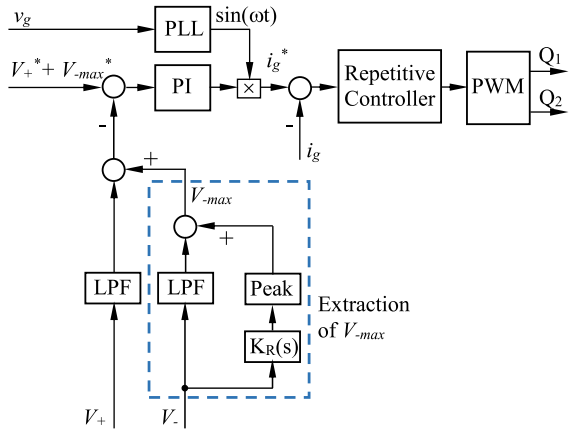

Fig. 4. Controller for the rectification leg.

B. Control of the Rectification Leg

The control of the rectification leg is very similar to that of conventional half-bridge rectifiers, which is mainly used to regulate the grid current and to control the whole dc-bus voltage. To be more precise, the grid current is expected to be in phase with the grid voltage and also to be clean with low harmonics. For this purpose, the grid current i_g should be measured as a feedback to form a current tracking controller. Here, the repetitive controller shown in the dashed box of Fig. 3 is adopted again. In order to generate the grid current reference i_g^*, an outer-loop voltage controller can be constructed.

There can be different ways to construct this voltage controller; see, e.g., [33]. In this paper, the voltage controller is designed to maintain the maximum voltage $V_{-\max}$ of V_- constant. Hence, the total dc-bus voltage is maintained at $V_+^* + V_{-\max}^*$, with a PI controller. The output of the controller can be used as the peak value of the grid current reference i_g^*, as shown in Fig. 4. This is multiplied with the phase signal of the grid voltage, which can be obtained from a phase-locked-loop, to form the grid current reference i_g^*. As a result, the grid current is in phase with the grid voltage to achieve the unity power factor. Here, the phase-locked-loop proposed in [34] is adopted.

The aforementioned control strategy of the half-bridge rectification leg is now somewhat standard [26], [28], [29], [35]. What is different here is that the maximum dc-bus voltage, instead of the average dc-bus voltage, is selected as the controlled output. As a result, the objective here is set to control the maximum dc-bus voltage. For this purpose, the maximum dc-bus voltage should be extracted at first. Since the voltage V_+ is controlled to be more or less pure dc without second-order components, it is only required to extract the maximum value of the voltage V_-, which can be obtained by adding the dc component with the peak voltage of the ripple component, as shown in Fig. 4. The hold filter (14) is again used to obtain the dc component. In order to extract the second-order component, the resonant filter (16) is again adopted with $\xi = 0.01$, $h = 2$, and $\omega = 2\pi f$. A peak block in Fig. 4 is used to calculate the peak value of the ripple component. The sum of the average voltage and the peak voltage of the ripple component then forms the maximum voltage of the voltage V_-, which is denoted as $V_{-\max}$ in Fig. 4

and is added with V_+ to obtain the maximum dc-bus voltage for feedback.

C. Stability of the System

Because of the decoupled nature of the controllers for the two legs, the stability of the system can be easily guaranteed. The controller for the rectification leg has a very typical structure, which is very mature and widely used in industry. The controller for the neutral leg has a very special structure with one current loop and two voltage loops. What is special is that these three loops are in parallel rather than cascaded so the stability of each loop can be treated individually. The current loop is designed to regulate the ac components of i_{C_+} (or i) to be around zero, i.e., to remove any non-dc components in i. At the same time, the voltage loop related to V_+ is to maintain the dc component of the voltage V_+ while the voltage loop related to V_- is designed to reduce the fundamental component of voltage V_-. Hence, the functions of the three loops are decoupled in the frequency domain for current or voltage. The three loops consist of simple PI, repetitive and resonant controllers, which have been widely analyzed in the literature. See, for example, [1]. Hence, detailed analysis of the stability of the loops is not repeated in this paper.

V. Selection of Components

A. Selection of Capacitor C_-

As demonstrated in [9], [24], the total ripple energy stored in the split capacitors over a charging period for single-phase rectifiers with the unity power factor is

$$E_r = \frac{V_g I_g}{2\omega}.$$

With the proposed strategy, all the ripple energy is now stored on the lower capacitor C_- instead of both capacitors C_+ and C_-. Hence

$$C_- = \frac{2E_r}{V_{-\max}^2 - V_{-\min}^2} \tag{17}$$

where $V_{-\max}$ and $V_{-\min}$ are the maximum and minimum voltages of V_-, respectively. A small capacitor means that high $V_{-\max}$ and/or low $V_{-\min}$ is needed. However, in order to ensure the proper boost operation of the rectifier

$$V_- \geqslant V_g|\sin\omega t| \tag{18}$$

should be satisfied. In other words

$$V_{-\min} \geqslant V_g. \tag{19}$$

At the same time, $V_{-\max}$ has an upper bound as well because of the limit on the devices and/or the applications. Hence, the capacitor is mainly limited by the allowed maximum voltage $V_{-\mathrm{amax}}$ and the required minimum capacitance $C_{-\min}$ is

$$C_- = \frac{V_g I_g}{\omega(V_{-\mathrm{amax}}^2 - V_{-\min}^2)} \tag{20}$$

which can be small if $V_{-\mathrm{amax}}$ is high enough.

In addition, another important factor for selecting capacitors is the maximum allowable ripple currents [4], [7], [36]. This is very important for the reliability of capacitors. In general, large current ripples lead to short lifetime. The current ripples are closely related to the voltage ripples and the equivalent impedance of capacitors. In order to evaluate the level of voltage ripples, (20) can be rewritten as

$$\begin{aligned} C_- &= \frac{V_g I_g}{\omega \triangle V_-(V_{-\max} + V_{-\min})} \\ &= \frac{V_g I_g}{2\omega \triangle V_- V_{-\mathrm{ave}}} \end{aligned} \tag{21}$$

where $\triangle V_- = V_{-\max} - V_{-\min}$ and $V_{-\mathrm{ave}} = \frac{V_{-\max}+V_{-\min}}{2}$ are the peak-peak ripple voltage and the average voltage of V_-, respectively. Since the capacitor impedance at the second-order frequency is $\frac{1}{2\omega C_-}$, the peak-peak value $\triangle i_{C-}$ of the second-order ripple current flowing through C_- is

$$\triangle i_{C-} = \frac{\triangle V_-}{\frac{1}{2\omega C_-}} = 2\omega C_- \triangle V_-. \tag{22}$$

Substitute (21) into (22), then there is

$$\triangle i_{C-} = \frac{V_g I_g}{V_{-\mathrm{ave}}}. \tag{23}$$

This is consistent with (13). The average voltage should be increased in order to reduce the ripple current. For the proposed strategy, the voltage V_- can be different or the same as V_+. As a result, the voltage $V_{-\mathrm{ave}}$ can be maintained at a higher value in order to reduce the ripple current. This can be naturally achieved when the maximum voltage $V_{-\max}$ is controlled at the allowable value because the higher the maximum voltage is, the higher the average voltage $V_{-\mathrm{ave}}$ is.

Of course, some other factors such as hold-up time requirement [17], current stress and limited voltage rating of the capacitors and switches, should be taken into account when selecting capacitors. If the maximum voltage of the capacitor is determined, then increased capacitance means increased hold-up time and reduced current stress, which is preferred in practical applications. As a result, there are several tradeoffs when selecting capacitors for a certain application.

B. Selection of Inductor L_N

The fast switching of the neutral leg leads to switching ripples over the current flowing through the inductor L_N. Since the two switches Q_3 and Q_4 are operated complementarily, the on time of Q_3 is $\frac{d_3}{f_s}$ and the on time of Q_4 is $\frac{1-d_3}{f_s}$ in one PWM period. Since the switching frequency is much higher than the line frequency, it can be assumed that the current increased $\frac{V_+ d_3}{L_N f_s}$ (to withstand the positive voltage V_+) and the current decreased $\frac{V_-(1-d_3)}{L_N f_s}$ (to withstand the negative voltage V_-) in these two modes are the same. According to (8), the maximum peak-peak current ripple $\triangle i_{Lm}$ on the inductor L_N is reached when the duty cycle d_3 reaches the maximum, which is when the voltage V_- reaches the maximum. That is

$$\triangle i_{Lm} = \frac{V_+ d_{3\max}}{L_N f_s} = \frac{V_+ V_{-\max}}{L_N f_s(V_+ + V_{-\max})}. \tag{24}$$

TABLE I
PARAMETERS OF THE SYSTEM

Parameters	Values
Grid voltage (RMS)	110 V
Line frequency f	50 Hz
Switching frequency f_s	19 kHz
V_+^*	200 V
V_{-max}	750 V
R	220 Ω
C_+	5 μF
C_-	5 μF
L_N	2.2 mH
L_g	2.2 mH

For the given maximum allowed ripple current $\triangle i_{Lm}$, the minimum inductance is

$$L_{N\min} = \frac{V_+ V_{-\max}}{\triangle i_{Lm} f_s (V_+ + V_{-\max})}. \quad (25)$$

The inductance can be reduced if the switching frequency f_s is increased. When choosing the magnetic core for the inductor, the dc current component in i_L should be taken into consideration to avoid saturation.

Note that increasing $V_{-\max}$ helps reduce the capacitor C_- but it leads to increased inductance L_N so there is a tradeoff between these two. One possible option to break this tradeoff is to reduce C_- by increasing $V_{-\max}$ but decrease L_N by increasing f_s.

C. Selection of Capacitor C_+

When Q_3 is turned on, C_+ is discharged through L_N and the maximum ripple current is given in (24). If the switching frequency of the rectifier is high and the inductance in series with the dc load is considered [37], it is reasonable to assume that the switching ripple current mainly flows through the capacitor C_+. According to [38], the peak-peak switching ripple voltage across the capacitor C_+ is

$$\begin{aligned} \triangle V_{+s} &= \frac{\triangle i_{Lm}}{8 C_+ f_s} + \triangle i_{Lm} R_{C+} \\ &= \left(\frac{1}{8 C_+ f_s} + R_{C+} \right) \frac{V_+ V_{-\max}}{L_N f_s (V_+ + V_{-\max})} \end{aligned} \quad (26)$$

where R_{C+} is the equivalent series resistance (ESR) of the capacitor C_+. The second part, i.e., $\triangle i_{Lm} R_{C+}$, is caused by the ESR of the capacitor. Since R_{C+} is often negligible for film capacitors, (26) becomes

$$C_{+\min} \approx \frac{\triangle i_{Lm}}{8 f_s \triangle V_{+sm}} \quad (27)$$

for the given maximum switching ripple voltage $\triangle V_{+sm}$ and the maximum ripple current $\triangle i_{Lm}$. Note that increasing the switching frequency reduces C_+.

D. Design Example

Here, an example is given for demonstration. The selected components, as summarized in Table I, are also used when building up the test rig.

For the inductor L_N with $\triangle i_{Lm} = 4$ A, the required minimum inductance is $L_N \approx 2.1$ mH, according to (25). In this study, 2.2 mH is used. Note that the inductor can be reduced a lot if the switching frequency f_s is significantly increased, again according to (25).

Based on (20), the required minimum capacitance is $C_{-\min} = \frac{V_g I_g}{\omega (V_{-\max}^2 - V_{-\min}^2)} \approx 2.76$ μF. Here, $I_g = 3$ A is used in the calculation, considering the losses of the rectifier. In order to leave some margin, the capacitor C_- is selected as 5 μF. According to (23), the maximum second-order ripple current is $\triangle i_{C-\max} = \frac{V_g I_g}{V_{-\text{ave}}} = \frac{V_g I_g}{(V_{-\max} + V_g)/2} \approx 1$ A. The capacitor C_- can then be selected based on $C_{-\min}$ and $\triangle i_{C-\max}$.

For the selection of the capacitor C_+, according to (27), if the maximum switching ripple voltage $\triangle V_{+sm}$ is expected to be around 5 V, then $C_{+\min} \approx 5$ μF.

If a conventional single-phase full-bridge rectifier is adopted, then the dc-bus capacitor should be larger than $\frac{V_g I_g}{2\omega \triangle V_- V_{-ave}} \approx 740$ μF in order for the output ripple voltage to be maintained lower than 5 V. For capacitors at this level, electrolytic capacitors are often needed. The experimental results presented later show that the rectifier under investigation can achieve 5 V output ripple voltage only with two 5 μF film capacitors. This means the dc-bus capacitors can be reduced by over 70 times while maintaining the same level of output voltage ripples.

VI. IMPACT OF DIFFERENT VOLTAGES V_+ AND V_-

The voltages across the two split capacitors are normally maintained to be the same in similar topologies. However, as mentioned above, the voltages are controlled to be different on purpose for the proposed strategy, which contributes to suppressing the voltage ripples and reducing the required capacitors. One question that arises naturally is whether the voltage difference would cause any problem to the control of the rectification leg and the neutral leg. This is analyzed in this section.

A. Impact on the Rectification Leg

The main objective of the rectification leg is to maintain the grid current to be clean and to be in phase with the grid voltage. As stated previously, the control of the rectification leg and the neutral leg are independent from each other. As a result, the regulation of the input current only depends on the rectification leg instead of both legs. According to (7), the maximum and minimum values of the duty cycle of the two switches in the rectification leg are

$$\begin{aligned} d_{2\max} &= \frac{1}{V_{DC}} (V_+ + V_g) \\ d_{2\min} &= \frac{1}{V_{DC}} (V_+ - V_g). \end{aligned}$$

Since V_+, $V_- > V_g$, then $d_{2\min} > 0$ and $d_{2\max} < 1$ can be achieved for any combinations of V_+ and V_-. According to the average model, the duty cycle of the switch Q_2 is

$$\begin{aligned} d_2 &= \frac{V_+}{V_{DC}} - \frac{V_g}{V_{DC}} \sin \omega t \\ &= \frac{1}{V_+ + V_-} (V_+ - V_g \sin \omega t). \end{aligned} \quad (28)$$

If all the ripple power is provided by the lower capacitor, then (28) becomes

$$d_2 = \frac{1}{V_+ + \sqrt{V_{-\min}^2 + \frac{P_o}{C_-}(1-\sin 2\omega t)}}(V_+ - V_g \sin \omega t)$$

where the derivation of V_- can be found in [24] for a given load power P_o. It is clear that the obtained duty cycle contains a second-order ripple component coming from V_-. The existence of a second-order ripple component is common for all rectifiers based on the half-bridge structure and does not constitute any problem because the switching frequency is much higher than the second-order frequency. The only difference here is that the ripples are stored in the lower capacitor only.

Because the rectification leg is independently controlled, the input power factor and the THD of the input current can be regulated as usual and are not affected by the difference between V_+ and V_-. As a result, the regulation of the input current is not affected by the voltage difference between V_+ and V_-.

B. Impact on the Neutral Leg

The neutral leg is used for two purposes, i.e., splitting the dc-bus voltage to V_+ and V_- and diverting the ripple power to the lower capacitor C_-. According to the average model, the duty cycle of the switch Q_3 can be given as

$$\begin{aligned} d_3 &= 1 - \frac{V_+}{V_{DC}} \\ &= 1 - \frac{V_+}{V_+ + \sqrt{V_{-\min}^2 + \frac{P_o}{\omega C_-}(1-\sin 2\omega t)}} \end{aligned}$$

which is also affected by a second-order ripple component. As long as $V_- < V_{DC}$, which is always true because $V_{DC} = V_+ + V_- > V_+, V_-$, the duty cycle d_3 can be always achieved by controlling the two switches Q_3 and Q_4 in an complementary way. Hence, the voltage difference does not cause any problem to the control of the neutral leg either.

C. Impact on the Current Stress of the Switches

The voltage difference may lead to different current stresses to the switches. The average currents are very important when selecting a switch or a diode [26]. As a result, they are calculated here in order for selecting suitable switches and diodes for both legs.

1) Switches and Diodes of the Rectification Leg: For the rectification leg, there are two switches and two diodes in total. The current flowing through the rectification leg mainly depends on the grid current i_g. The positive cycle of the grid current i_g flows through the switch Q_2 and the corresponding free-wheeling diode is D_1. On the other hand, the negative cycle of the grid current i_g flows through the switch Q_1 and the the corresponding free-wheeling diode is D_2. As demonstrated in [26], the average currents flowing through active switches Q_1 and Q_2 and diodes D_1 and D_2 are

$$\begin{aligned} I_{Q_1} &= \frac{1}{2\pi}\int_{\pi}^{2\pi} i_g(1-d_2)dt = I_R\left(\frac{2V_-}{V_g\pi} - 0.5\right) \\ I_{Q_2} &= \frac{1}{2\pi}\int_{0}^{\pi} i_g d_2 dt = I_R\left(\frac{2V_+}{V_g\pi} - 0.5\right) \\ I_{D_1} &= \frac{1}{2\pi}\int_{0}^{\pi} i_g(1-d_2)dt = I_R\left(\frac{2V_-}{V_g\pi} + 0.5\right) \\ I_{D_2} &= \frac{1}{2\pi}\int_{\pi}^{2\pi} i_g d_2 dt = I_R\left(\frac{2V_+}{V_g\pi} + 0.5\right). \end{aligned} \tag{29}$$

It can be seen that most of the currents flow through the diodes rather than the active switches. More importantly, the currents of the active switches are different if $V_+ \neq V_-$. The same is true for the diode currents. For example, if $V_- > V_+$, which is preferred in order to reduce C_-, then $I_{Q_1} > I_{Q_2}$ and $I_{D_1} > I_{D_2}$. As a result, the power loss of the upper switch Q_1 is higher than that of the lower switch Q_2 if $V_- > V_+$. (29) can be used as a principle to select the active switches and diodes. Of course, the two voltages can be controlled to be the same. In this case, the average currents of the switches become the same and also, the average currents of the switches become the same too.

2) Switches and Diodes of the Neutral Leg: For the neutral leg, there are also two switches and two diodes in total. The current flowing through the neutral leg mainly depends on the inductor current i_L. In order to analyze the average currents, similar analysis can be done. The only difference here is the conduction periods of Q_3, Q_4 and D_3, D_4. For example, the conduction period of switch Q_1 in the rectification leg is from π to 2π, which is not affected by other factors like the input or output power. This is because the periods of the positive and negative cycles of the current i_g are the same, which is π. However, it is obvious that those periods of the current i_L are not the same according to (12), which leads to the fact that the conduction periods of Q_3, Q_4 and D_3, D_4 are not the same. In order to calculate their average currents, there is a need to first know these periods. Let $i_L = 0$, then

$$I_g \sin \omega t - \frac{V_g I_g}{2V_-}\cos 2\omega t - \frac{V_g I_g}{2V_+} = 0$$

or

$$\sin^2 \omega t + \frac{V_-}{V_g}\sin \omega t - \frac{1}{2} - \frac{V_-}{2V_+} = 0.$$

Hence

$$\sin \omega t = -\frac{V_-}{2V_g} \pm \frac{1}{2}\sqrt{\frac{V_-^2}{V_g^2} + 2 + \frac{2V_-}{V_+}}.$$

Because of (19), the "$-$" sign is not valid. There are two solutions within $[0, \frac{\pi}{\omega}]$, which are

$$\begin{aligned} t_1 &= \frac{1}{\omega}\arcsin\left(\frac{1}{2}\sqrt{\frac{V_-^2}{V_g^2} + 2 + \frac{2V_-}{V_+}} - \frac{V_-}{2V_g}\right) \\ t_2 &= \frac{\pi}{\omega} - \frac{1}{\omega}\arcsin\left(\frac{1}{2}\sqrt{\frac{V_-^2}{V_g^2} + 2 + \frac{2V_-}{V_+}} - \frac{V_-}{2V_g}\right). \end{aligned}$$

As a result, the average currents flowing through active switches Q_3 and Q_4 and diodes D_3 and D_4 can be calculated from

$$\begin{aligned} I_{Q_3} &= \frac{1}{2\pi}\int_{t_1}^{t_2} i_L d_3 dt \\ I_{Q_4} &= \frac{1}{2\pi}\int_{t_2}^{t_1+2\pi} i_L (1-d_3) dt \\ I_{D_3} &= \frac{1}{2\pi}\int_{t_2}^{t_1+2\pi} i_L d_3 dt \\ I_{D_4} &= \frac{1}{2\pi}\int_{t_1}^{t_2} i_L (1-d_3) dt. \end{aligned} \tag{30}$$

The analytical solutions are complicated but, in principle, the currents I_{D_3} and I_{D_4} are again higher than the currents I_{Q_3} and I_{Q_4}. Moreover, because V_- is set higher than V_+, I_{Q_3} and I_{D_3} are higher than I_{Q_4} and I_{D_4}, respectively.

For certain applications with known system parameters, the average currents flowing through the switches and diodes of both legs can be easily obtained based on the above analysis. Together with the voltage stress, i.e., the dc-bus voltage V_{DC}, suitable switches and diodes can be selected.

D. Impact on the Voltage Stress of the Switches

In order to choose suitable switches for both legs, the voltage stress of the switches is another factor to be considered.

Compared to the current stress of the switches, it is more straightforward to analyze the voltage stress of the switches. Regardless of other system parameters, the voltage stress of the switches is always the sum of the voltages V_+ and V_-. It is well known that low voltage stress generally leads to low costs and high efficiency. As a result, it is always hoped to maintain the voltage stress within a reasonable level. Either decreasing V_+ or V_- can help to reduce the voltage stress. The level of the voltage V_+ is determined by the requirement of the dc load and cannot be changed. However, the voltage V_- does have some freedom to be decreased. According to the discussion before, the proposed rectifier can still perform well to control the grid current and the dc output voltage as long as the minimum voltage of V_- is higher than the peak of the grid voltage. Hence, there is $V_{-\min} = V_g$. Note that the ripple level of the output voltage V_+ is still very low even if $V_{-\min} = V_g$. The only compromise here is the dc-bus capacitance. In order to meet a given maximum voltage stress $V_{\max}$, the maximum voltage of V_- is then fixed, which is $V_{-\max} = V_{\max} - V_+$. It is clear that low voltage stress means low $V_{-\max}$. Since both maximum and minimum values of the voltage V_- are fixed now, the minimum required capacitance can be obtained according to (20). The higher the voltage stress can be, the smaller the capacitance C_- can be. It is worth mentioning that high voltage stress leads to high switching loss, which decreases the efficiency. When large electrolytic capacitors are used, the voltage stress could be lower because $V_{-\max}$ could be reduced. In this case, the switching loss of the rectifier is lower. However, the loss caused by the ESR of the capacitors becomes higher because the required capacitance can be very large and electrolytic capacitors have to be used. The additional loss caused by the high voltage stress may have been well compensated by the reduction of the loss in capacitors.

E. Impact on Switching Ripples of the Grid Current

Since the switching frequency is much higher than the fundamental frequency, the average grid current over each switching period can be controlled to track its reference, which is a sinusoidal signal. Apart from controlling the average grid current, it is also desirable to maintain the switching ripple of the grid current under a certain level, in order not to introduce power pollution to the grid. According to [26], the peak-peak switching ripple of the grid current can be given as

$$\begin{aligned} \triangle i_g &= \frac{\frac{V_-}{V_{DC}} V_{DC} + V_g \sin\omega t}{L_g f_s} d_2 \\ &= \frac{1}{L_g f_s V_{DC}} (V_+ V_- - V_g^2 \sin^2 \omega t) \\ &\quad + \frac{(V_+ - V_-) V_g}{L_g f_s V_{DC}} \sin\omega t. \end{aligned} \tag{31}$$

Apparently, increasing the inductor and/or increasing the switching frequency could reduce the switching current ripple. According to (31), the switching ripple current is related to almost all system parameters. Compared to most of the analysis in the literature, the only difference here is that the voltages V_+ and V_- are designed to be different on purpose. The first part of the switching ripple, i.e., $\frac{1}{L_g f_s}(\frac{V_+ V_-}{V_{DC}} - \frac{V_g^2}{V_{DC}} \sin^2 \omega t)$, is always positive in the positive and negative half cycles of the grid current. However, the second part, i.e., $\frac{(V_+ - V_-) V_g}{L_g f_s V_{DC}} \sin\omega t$, changes its sign during the positive and negative cycles of the grid current. For example, if $V_+ < V_-$, it is negative in the positive half cycle of the grid current but is positive in the negative half cycle of the grid current. The resulted effect is that the switching ripples of the grid current in the negative half cycle are larger than those in the positive half cycle. If $V_+ > V_-$, then the switching ripples of the grid current in the negative half cycle are smaller than those in the positive half cycle. However, the slightly different switching ripples does not constitute any noticeable problems to the grid. If needed, an *LCL* filter, instead of an inductor L_g, can be adopted so that the switching ripple currents can flow through the filter capacitor instead of the grid.

VII. Experimental Validation

In order to validate the design and operation of the rectifier, experiments were conducted on a test rig in the lab. The test system consists of the investigated rectifier and its control circuit, which was constructed based on TMS320F28335 DSP. The main parameters of the test system are the same as the ones in the design example of Section V as summarized in Table I. The system parameters like the inductor L_g and the switching frequency are selected according to the test rig and the available components in the lab and hence are not optimized for performance. Note that the two split capacitors are very small (5 μF), which demonstrates the capability of significantly reducing capacitors while maintaining low ripples on the dc output voltage.

The required usage of capacitors is reduced by over 70 times from 740 to 10 μF. Here, two 5 μF metallized polypropylene film capacitors (MKP1848C55012JK2) are used as the two split capacitors in experiments. The system responses both in the steady state and during transient period are presented.

A. Steady-State Performance

1) Grid Current i_g and the DC Voltages V_+ and V_-: The system steady-state performance with $V_+^* = 200$ V is given in Fig. 5(a)–(d) for $V_{-\max}^* = 600$, $V_{-\max}^* = 650$, $V_{-\max}^* = 700$ and $V_{-\max}^* = 750$, respectively. It is clear that the dc output voltage V_+ is always maintained around its reference 200 V while the ripple voltage of V_- varies from 337 to 431 V depending on the maximum voltages of V_-. Importantly, the voltage ripples of the voltage V_+ are only about 5 V when $V_{-\max}^* = 700$ V and 750 V. As a result, nearly all the ripple power is now stored on the lower capacitor C_- instead of both C_+ and C_- over a wide range of V_-. It is worth again pointing out that only two 5 μF are used in the system. The reduction of capacitors and ripples on the output V_+ have been achieved at the same time.

In order to clearly illustrate the relationship between the voltage ripples and the average voltage on the capacitor C_-, the steady-state performance to reduce the ripple voltage under different average voltage of V_- is shown in Fig. 6. It can be clearly seen that the ripples of V_+ were kept around 5 V over a wide range of V_- while the ripples of V_- are much larger, ranging from 337 to 431 V. Furthermore, the ripples of V_- decreased along with the increase of its average voltage. The obtained experimental results nicely match the condition (21) with $\triangle V_- = \frac{185000}{V_{-\text{ave}}}$ (represented by the dashed line in Fig. 6) over a wide range of $V_{-\text{ave}}$ as long as the boost operation of the rectifier is successful. Here, the number 185000 was found via curve fitting.

Moreover, the grid current i_g is always regulated to be clean and in phase with the grid voltage and, thus, the unity power factor is achieved. According to the recorded experimental data, the THD of the grid current is around 4% and the input power factor is above 0.99 for all cases. This verifies that the regulation of the grid current is not affected by large ripples of V_- and the voltage difference between V_+ and V_-. Note that the experimental test rig is not optimized for high power quality because it is not the main focus of this paper. In light of this, the obtained results are very good.

In order to further demonstrate the operation of the system, another two results are shown in Figs. 7 and 8, respectively, for the cases when the dc voltages V_+ and V_- were lower than the peak grid voltage and when the controller that removes the fundamental component from i_{C-} was disabled. As shown in Fig. 7, the output voltage ripple becomes around 80 V, much larger than 5 V, when $V_{-\max}^*$ is set at 500 V. The relatively low voltages of V_+ and V_- also lead to distorted grid current as highlighted by the dashed circles in Fig. 7 when both voltages are lower than the peak grid voltage. When the controller that removes the fundamental component from i_{C-} was disabled, the results are shown in Fig. 8. The voltage V_- now consists of a noticeable fundamental component. The experimental data of Figs. 5(c) and 8 were processed in MATLAB/SIMULINK

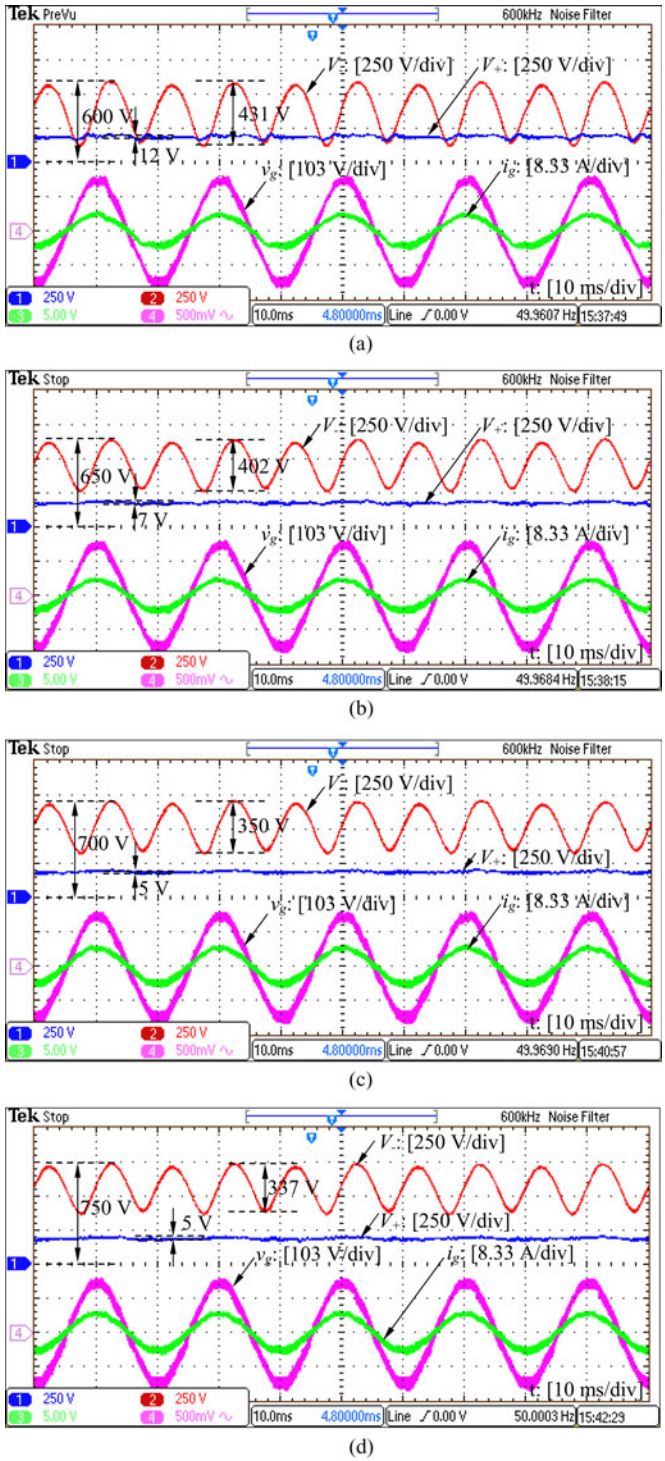

Fig. 5. Grid voltage v_g, grid current i_g and dc voltages V_+ and V_- with $V_+^* = 200$ V: (a) when $V_{-\max}^* = 600$ V, (b) when $V_{-\max}^* = 650$ V, (c) when $V_{-\max}^* = 700$ V and (d) when $V_{-\max}^* = 750$ V.

to extract the fundamental component and indeed the fundamental component increased from 2 to 15 V when the resonant controller was disabled.

2) DC-Bus Current and the Capacitor Currents: As mentioned above, the reduction of the voltage ripples is achieved by controlling the ac component i of the dc-bus current I. In

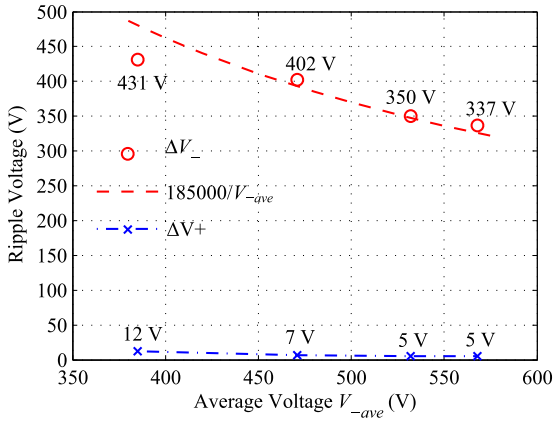

Fig. 6. Voltage ripples of V_+ and V_- over a wide range of $V_{-\mathrm{ave}}$.

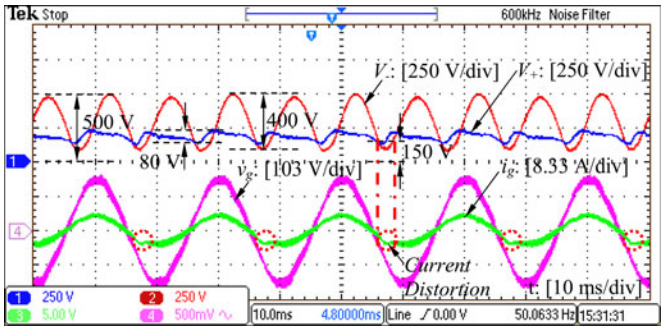

Fig. 7. Deteriorated system performance with $V_+^* = 200$ V when $V_{-\mathrm{max}}^* = 500$ V.

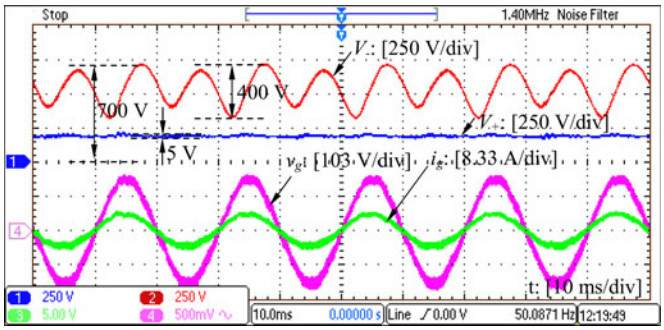

Fig. 8. Deteriorated system performance when the controller that removes the fundamental component from i_{C-} was disabled ($V_{-\mathrm{max}}^* = 700$ V).

order to show the system performance of the current control, the waveforms of the dc-bus current and the capacitors currents i_{C+} and i_{C-} over a wide range of V_- are shown in Fig. 9(a)–(d). Note that a low-pass filter with a cutoff frequency of 6 kHz is applied to remove the high frequency component in the currents. It can be seen that the ac component of the dc-bus current and the current i_{C+} are always maintained around zero for different voltages of V_-. On the other hand, the ripples of the capacitor current i_{C-} are relatively large because all the ripple power is now stored on the capacitor C_-. In general, it can be seen that the higher the capacitor voltage V_-, the lower the capacitor current i_{C-}. The relationship between the capacitor voltage and the

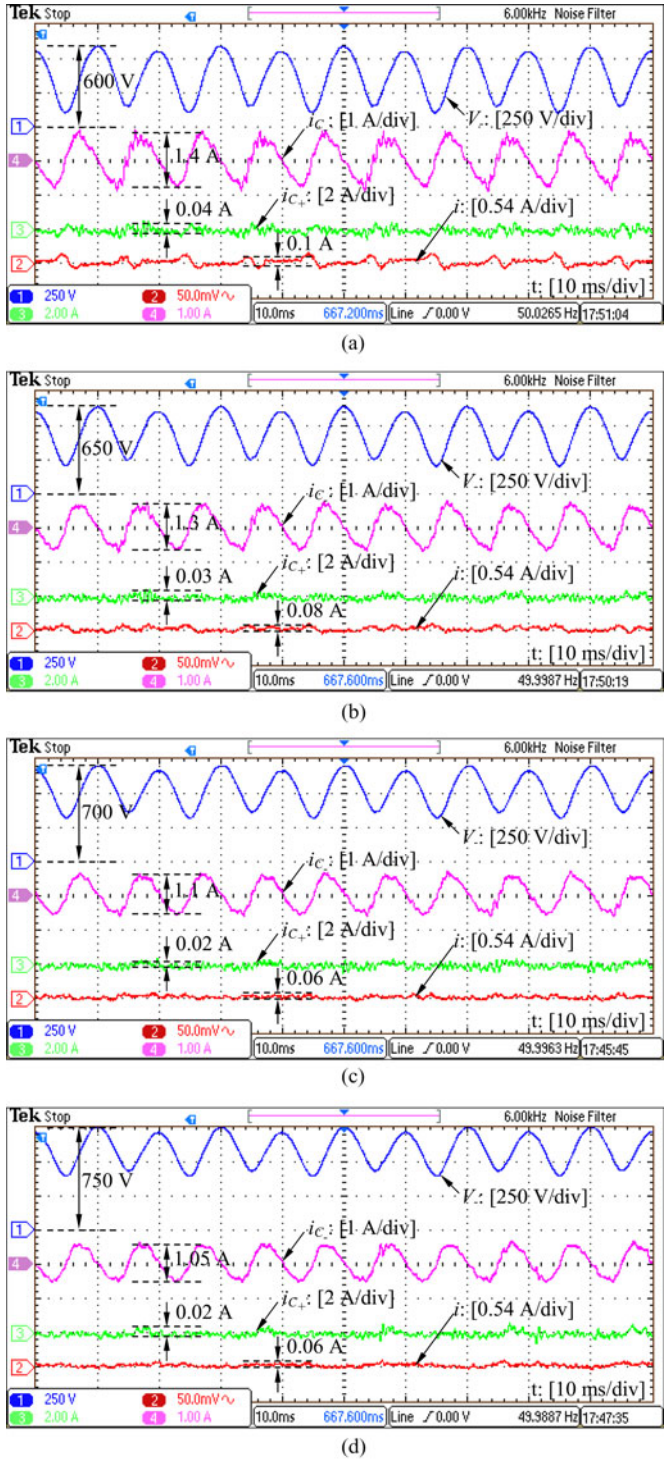

Fig. 9. Voltage V_-, dc-bus ripple current i and capacitor currents i_{C+} and i_{C-} with $V_+^* = 200$ V: (a) when $V_{-\mathrm{max}}^* = 600$ V, (b) when $V_{-\mathrm{max}}^* = 650$ V, (c) when $V_{-\mathrm{max}}^* = 700$ V and (d) when $V_{-\mathrm{max}}^* = 750$ V.

capacitor current is shown in Fig. 10, which nicely matches the condition $\triangle i_{C-} = \frac{600}{V_{-ave}}$, where the number 600 was found via curve fitting.

Moreover, the spectra of the dc-bus current I are shown in Fig. 11(a) and (b) to demonstrate the performance of reducing the second-order ripples in the current I for the cases without

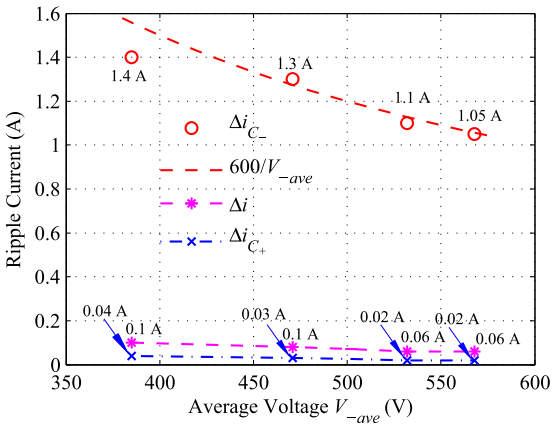

Fig. 10. Dc-bus current i and capacitor currents i_{C+} and i_{C-} over a wide range of $V_{-\mathrm{ave}}$.

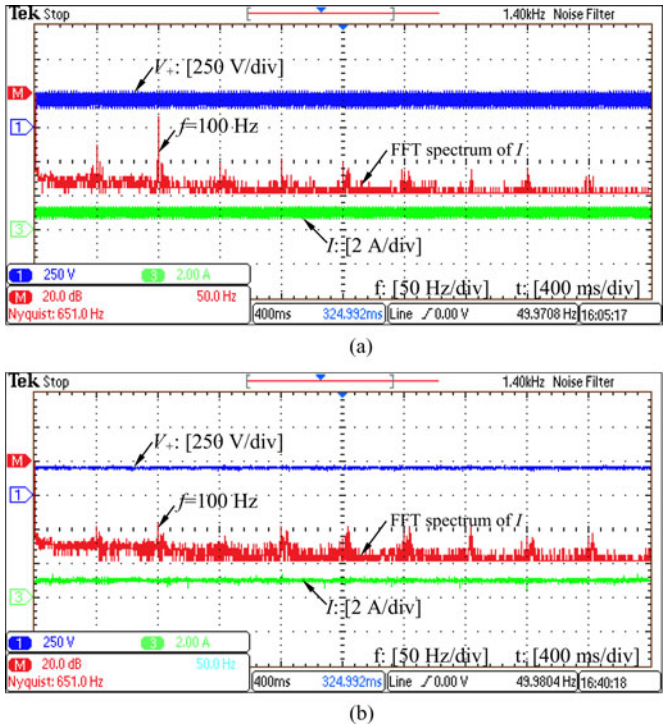

Fig. 11. Comparison of (a) without and (b) with the repetitive current controller for the neutral leg.

and with the repetitive controller, respectively. It is obvious that the second-order harmonic component, i.e., 100 Hz, in the current I is significantly reduced when the repetitive controller is enabled. Most of the 100 Hz component is diverted to the neutral leg from the output capacitor. Due to the diverted 100 Hz current, both the ripples of the output voltage V_+ and dc-bus current I are considerably reduced as shown in Fig. 11(b).

B. Transient Performance

1) System Start-Up: In order to demonstrate the transient response of the proposed system, the results during the system start-up are shown in Fig. 12. The grid current first increased to

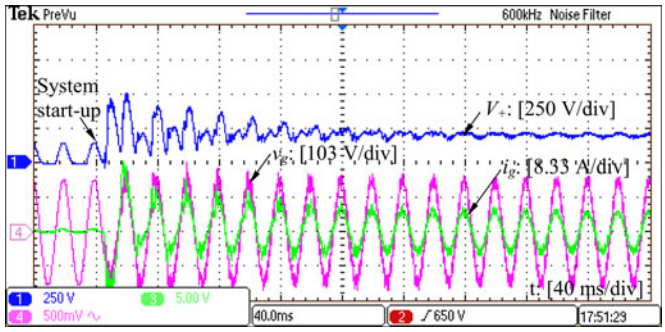

Fig. 12. System start-up ($V_+^* = 200$ V and $V_-^* = 700$ V).

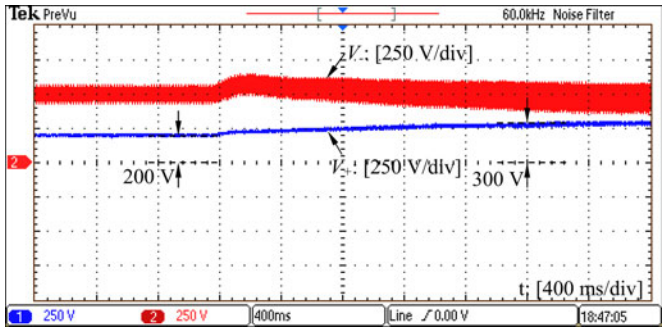

Fig. 13. Transient response when the reference of the voltage V_+ was changed from 200 to 300 V.

charge the capacitors and then the current was maintained well back to its steady-state value after the dc output voltage was settled. The system start-up took about 200 ms, which is only about ten cycles.

2) Change of the Voltage Reference: When the reference of the voltage V_+ was changed from 200 to 300 V, the results are shown in Fig. 13. The voltage V_+ was smoothly increased from 200 to 300 V without any spikes. It is worth highlighting that the ripple level of the output voltage V_+ is always small during the transient period. However, the ripples of the voltage V_- became larger in order to tackle the increased ripple power caused by the increased voltage reference (and the power). This transient response took about 2 s, which is limited by the allowable maximum neutral current of the experimental system, and could be made much faster if the allowable maximum neutral current is increased. For the test rig, the neutral current is limited by the neutral inductor, which would be saturated if the neutral current exceeds about 5 A.

3) Hold-Up Time: Although the dc-bus capacitors are designed for systems without hold-time requirement, it is still interesting to see how the proposed rectifier responds to a sudden ac power outage. Here, two experiments were conducted in order to show the system performance regarding to the hold-up time under different capacitors. In order for a fair comparison, only the capacitor C_+ was changed while the other system parameters were kept unchanged. With $C_+ = 5$ μF, the time for the voltage V_+ decreased from 200 to 0 V is about 14 ms as shown in Fig. 14(a). Of course, this time is too short for systems with hold-up requirement. A simple way to increase this time is

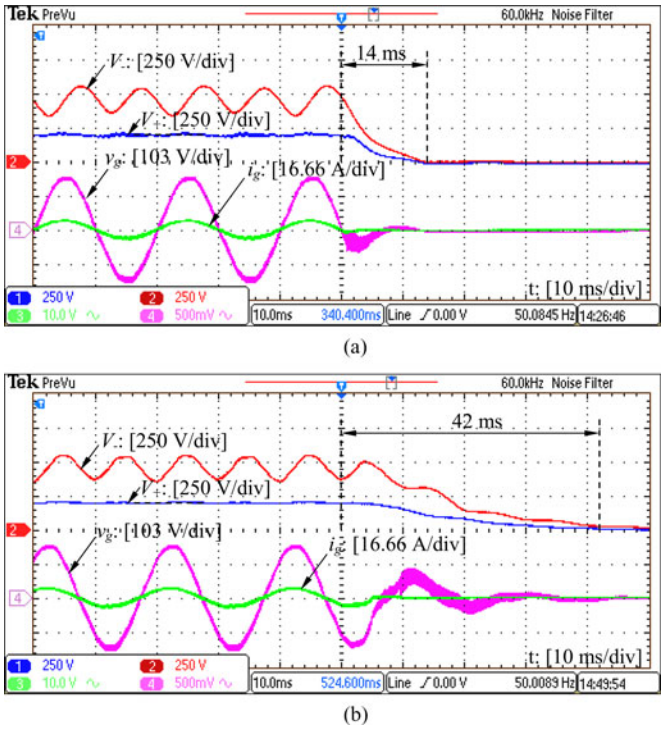

Fig. 14. Transient response after a sudden ac power outage with (a) $C_+ = 5\ \mu$F, $C_- = 10\ \mu$F and (b) $C_+ = 100\ \mu$F, $C_- = 10\ \mu$F.

to use a larger capacitor. The experimental result with a larger capacitor ($C_+ = 100\ \mu$F) is shown in Fig. 14(b). Indeed, the voltage V_+ was decreased at a much slower pace, which took about 42 ms for the voltage V_+ to decrease from 200 to 0 V. Since the main focus of this paper is not about the hold-up time, no further mathematical analysis is made. Interested readers are referred to [17] to see how to design capacitors for single-phase rectifiers with hold-up time requirement.

C. System Performance with a Switching Load

Apart from resistive loads, rectifiers often have switching devices connected as loads. Such switching devices can include dc/dc converters and dc/ac converters. In order to validate this, a buck dc/dc converter shown in Fig. 15(a) was built as the switching load and its output voltage V_b is regulated to be around 48 V while its input voltage V_+ is 200 V and the load R_b is 20 Ω. Note that a 470 Ω resistor is also connected across the voltage V_+, which means the equivalent load of the rectifier is a combination of resistive and switching loads. As shown in Fig. 15(b), the voltage V_+ (200 V) is levelled down to the voltage V_b (48 V) and the ripples of the voltage V_+ are again kept to be very low. As a result, the proposed rectifier can indeed work well with both resistive and switching loads.

VIII. Comparison with a Typical System

In this section, the proposed rectifier is compared to a system to evaluate the efficiency performance. In order to be fair, the system used for comparison should be able to work with the widely-spread single-phase unbalanced power grid and also should have the following features: 1) a common ac and dc ground; 2) capability of working with any power factor; 3) bidirectional power flow; 4) capability of reducing the usage of dc capacitors. Because of so many integrated features, it is not easy to find a suitable solution. For example, most rectifiers would fail if their ac and dc grounds are directly connected together. Indeed, there are a few topologies with common ac and dc ground in the literature, such as the Zigzag converter proposed in [39] and the Karschny converter proposed in [40]. However, they are not good candidates for the comparison because the Karschny converter cannot work with nonunity power factor [40] while the Zigzag converter requires relatively large and increased number of capacitors [39]. It is worth mentioning that the Zigzag converter benefits with multilevel outputs, which helps improve the power quality of the grid current and also to reduce the size of ac filters.

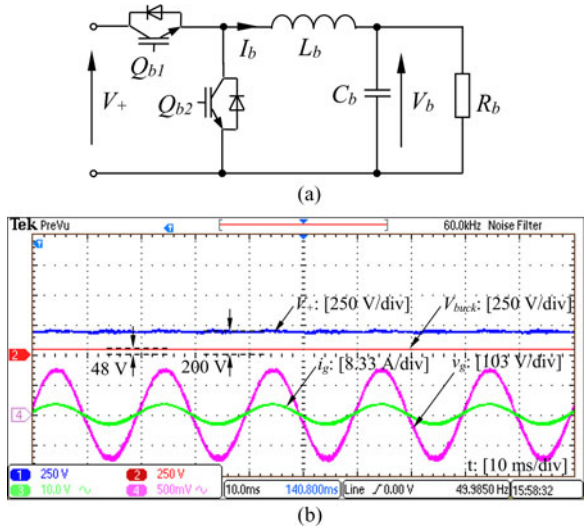

Fig. 15. System performance with a buck dc/dc converter and a resistor as the load of the rectifier.

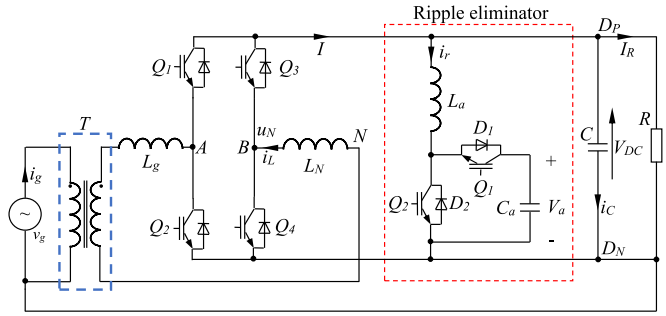

Fig. 16. Full-bridge system used for the comparison.

After careful comparison among different systems, the full-bridge system shown in Fig. 16 is used for the comparison. The isolating transformer T facilitates the direct connection between ac and dc grounds. Moreover, the conventional single-phase full-bridge rectifier is used as the interface between the ac and dc sides to achieve any power factor. At the same time, a ripple eliminator [8], [11]–[14] is hooked onto the dc bus to absorb the ripple energy. Hence, the total usage of capacitors can be significantly reduced while having low dc-bus voltage ripples.

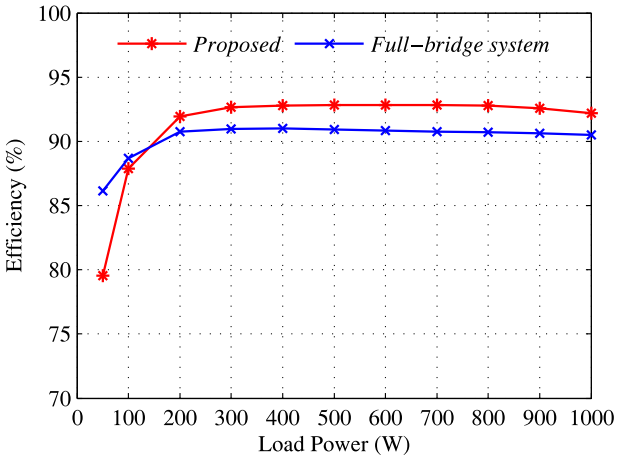

Fig. 17. Efficiency comparison.

Based on the above discussion, it is clear that the full-bridge system shown in Fig. 16 is a good candidate for the comparison because it has all the four main features of the proposed rectifier. The full-bridge system and the proposed rectifier have their own merits. For example, the proposed rectifier does not need the isolating transformer and the number of used switches are only four, which means two switches are saved compared to the full-bridge system. Moreover, it is easier to commercially implement the proposed rectifier by using a power module with four switches. On the other hand, the full-bridge system benefits with lower voltage stress of switches because of the adopted full-bridge topology. As a result, the switching loss of the full-bridge system is expected to be lower than the proposed rectifier. However, because of the reduced number of switches and the removed isolating transformer, the efficiency of the proposed system could be comparable with that of the full-bridge system even if the switching loss of the proposed rectifier is higher.

In order to compare the efficiency between the full-bridge system and the proposed rectifier, PLECS simulations of both systems were constructed. The same dc capacitors and switches are used for both systems for a fair comparison. A 1-kW system was built based on PLECS and MATLAB/Simulink and the system power ranging from 50 to 1000 W was tested by changing the dc load while keeping the dc output voltage constant. The obtained result is shown in Fig. 17. It is obvious that the proposed rectifier are almost always more efficient than that of the full-bridge system except when the power is low ($<$150 W).

As to power density, the proposed converter is absolutely higher than the full-bridge system shown in Fig. 16. This also means reduced system cost even if the increased cost of the switches due to the increased voltage stress.

To sum up, the proposed rectifier is always better than the full-bridge system shown in Fig. 16 in terms of power density, efficiency and cost, and is a very competitive solution for high power density rectifiers.

IX. Conclusion

This paper has addressed a big issue for single-phase rectifiers, which is to reduce dc-bus capacitors. It has been demonstrated that the required usage of dc-bus capacitors can be significantly reduced while maintaining low output voltage ripples by advanced control strategies. As a result, highly-reliable film capacitors can be used to replace bulky electrolytic capacitors. The elimination of dc-bus electrolytic capacitors is achieved by the neutral leg of the rectifier without adding any other power components. To be more precise, all the ripple energy is diverted from the upper (output) capacitor to the lower capacitor through the neutral leg so that the upper capacitor can be reduced a lot. At the same time, the voltage across the lower capacitor is designed to have large ripples as it is not supplied to any loads. In this case, both capacitors can be reduced to a level that film capacitors are cost effective to be used.

The rectification leg of the rectifier is used to maintain the grid current and the dc-bus voltage. Importantly, the impact of different voltages across the capacitors are analyzed in detail. It has been found that the different voltages and large voltage ripples do not affect the aforementioned functions of the two legs but do affect the selection of the switches because the upper switches and lower switches of both legs may have different voltage and current stresses. Experimental results have been presented to show that the required usage of capacitors can be reduced by over 70 times while maintaining the same level of output voltage ripples for the test rig. The rectifier can indeed work well without using dc-bus electrolytic capacitors.

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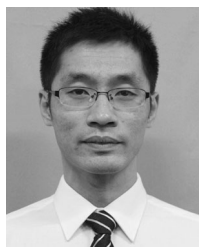

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