A Series–Parallel Current-Driven Full-Bridge DC/DC Converter

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***Abstract*—This paper presents a novel series–parallel current-driven (SPCD) full-bridge dc/dc converter, which is able to process and deliver power efficiently over a wide range of load variations. In order to guarantee reliable operation of high-frequency dc/dc converters, the converter should be able to sustain soft switching for a wide range of operating conditions. The SPCD full-bridge converter, proposed in this paper, is able to offer soft switching for the input power semiconductors and smooth commutations for the output diodes. Also, the particular structure of the proposed converter eliminates the need for extra auxiliary circuits to provide reactive current for soft switching at light loads. The proposed topology can fully eliminate voltage spikes across the output diodes by providing smooth and lossless commutations for the output diodes. Thus, the proposed converter can be an efficient and reliable solution for variety of applications with a high switching frequency and a high output voltage. The SPCD full-bridge converter has the ability to integrate all magnetic components into an integrated transformer in order to achieve a high power density. The integrated transformer is thoroughly analyzed using ANSYS high-frequency structure simulator. Simulation and experimental results confirm the superior performance of the proposed SPCD full-bridge dc/dc converter.**

***Index Terms*—Current-driven converter, dc/dc converter, full-bridge converter, lagging leg, leading leg, shoot through, snubber capacitor, zero-current switching (ZCS), zero-voltage switching (ZVS), zero-voltage zero-current switching (ZVZCS).**

I. Introduction

ISOLATED dc/dc converters have widely been used in several applications such as renewable energy power conditioning systems, electric vehicles (EVs), Telecom, etc. [1]–[8]. The well-known full-bridge inverter (including two legs with high-side and low-side power semiconductors) have extensively been utilized for dc/dc converters in industrial applications. Since the switch ratings are optimized for the full-bridge topology, the industry has adopted the full-bridge topology as an integral part of different power converters [9]–[14]. For applications in the range of a few kilowatts, MOSFETs are mostly used to implement the full-bridge inverter. In order to have robust and reliable operation, MOSFETs should be switched under zero voltage. Operation with zero-voltage switching (ZVS) has numerous advantages including elimination of switching losses, a noise free environment for the control circuit, superior EMI performance, and reliable operation of the power converter. ZVS is achieved by discharging the output capacitor of the MOSFET prior to the rising edge of the gate signal [5]. In isolated full-bridge converters the energy stored in the leakage inductance of the transformer is used to realize ZVS. However, in most cases, this energy is adequate only for heavy loads and the converter loses ZVS for light-load conditions. For high-frequency power converters, loss of ZVS implies that there will be extremely high switching losses and very high EMI due to the high di/dt of the snubber discharge current. Loss of ZVS can also cause a noisy control circuit, which leads to shoot through and loss of power semiconductor switches. The ZVS range can be extended by increasing the series inductance. However, having a large series inductance limits the power transfer capability of the converter and reduces the effective duty ratio of the converter.

Another fundamental problem related to the conventional full-bridge phase-shift dc/dc converter is the voltage spikes across the output diodes. The voltage spikes are caused by the interaction between the leakage inductance of the transformer and the output inductor. The power losses caused by the voltage spikes are intensified by increasing the switching frequency and the load of the converter. Thus, the diodes are usually designed to be overrated so that they are able to withstand the voltage spikes (in many design exercises, the diodes are designed to be able to withstand twice the nominal output voltage). In addition, the voltage spikes significantly contribute to the EMI noise produced by the converter. The aforementioned difficulties greatly confine the application of the full-bridge topology for high-frequency, high-voltage applications with a wide range of load variations. Resonant converters are widely used to mitigate the aforementioned difficulties of the full-bridge converters [15],[16]. The performance of the current-driven resonant converters (e.g., series resonant converters and *LLC* resonant converters) has proven to be superior compared to the voltage-driven resonant converters (e.g., *LCC* resonant converters). Resonant converters require extra passive components, which usually carry a significant amount of high-frequency current. Therefore, achieving high power density and high efficiency is very challenging with resonant topologies. Also, the resonant topologies may lose soft switching for light loads depending on the resonant circuit design and control system [17]–[23]. In [5] and [24], asymmetric auxiliary circuits are used to significantly extend the soft-switching range of the full-bridge converter. The auxiliary circuits provide inductive current to realize ZVS. Even

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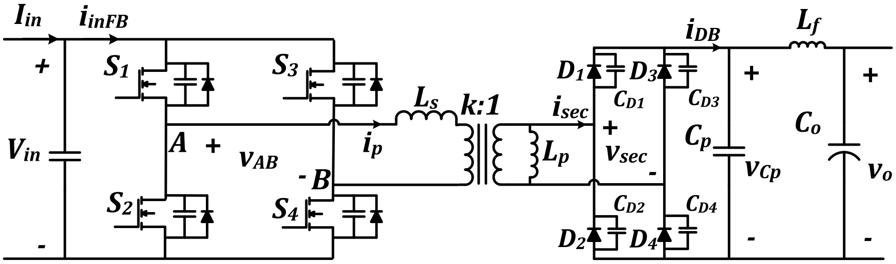

Fig. 1. Circuit diagram of proposed series–parallel current-driven full-bridge dc/dc converter.

though this topology is able to provide load-independent ZVS, it is not able to eliminate voltage spikes across the output diodes. Also, the auxiliary circuits increase the current burden of the power semiconductors. In some references, the voltage spikes are reduced by decreasing the leakage inductance as much as possible though the transformer winding structure. However, reducing the leakage inductance decreases the ZVS operating range of the full-bridge converter, which results in a narrow range of ZVS operation. Snubber circuits are commonly used to mitigate the voltage spikes across the diodes. The main problem with the snubber circuits is the amount of losses in the snubber resistor, which considerably degrades the efficiency of the converter especially at higher power and it can only reduce the peak value of the voltage spikes. In [25], an active clamp circuit has been added to the converter to clamp the voltage across the output diodes. This method can effectively clamp the voltage spikes of the output diodes. However, the active clamp circuit increases the complexity of the converter as well as small losses in the clamp circuit. Several energy recovery clamp circuits (ERCCs) have been proposed in [26]–[29]. Although the ERCC techniques are able to reduce the voltage stress across the output diodes, the amount of the voltage stress depends on the duty ratio and input voltage of the converter in most of the ERCC techniques. In addition, using extra semiconductors is inevitable in all of these aforementioned methods. The problem of voltage spikes is essentially related to the voltage-driven output rectifiers. In [30], a current-driven full-bridge dc/dc converter has been proposed, which is able to completely eliminate the voltage spikes across the output diodes. The current-driven structure of this topology guarantees the smooth performance of the output diodes. Therefore, the reverse-recovery losses of the output diodes are eliminated and there is no need for expensive Silicon-Carbide (SC) diodes. The topology proposed in [30] is a good candidate for high-frequency high-voltage dc/dc converters. The issue related to this topology is the need for an extra auxiliary circuit to guarantee ZVS for very light-load conditions. The auxiliary circuit increases the current ratings of the power semiconductor and also decreases the power density of the dc/dc converter.

In this paper, a series–parallel current-driven (SPCD) full-bridge converter is proposed, which is able to provide soft switching from light loads to full-load conditions without using any auxiliary circuit. Also, it is able to eliminate the voltage spikes across the output diodes and provide smooth commutations for the output diodes. This topology is intended for high-frequency high-voltage applications with high power density.

This paper is organized as follows. In Section II, the proposed topology is introduced and different operating modes are described. A qualitative analysis of the proposed SPCD full-bridge dc/dc converter is presented in Section III. In Section IV, the integrated magnetics used in the proposed topology is described in detail. The design procedure of the proposed SPCD full-bridge dc/dc converter is described in Section V. Section VI presents the simulation results and Section VII presents the experimental results obtained from the converter prototype. Section VIII presents a comparative study of the proposed topology. Finally, Section IX is the conclusion.

II. SPCD FULL-BRIDGE CONVERTER

The arrangement in Fig. 1 shows the proposed SPCD full-bridge dc/dc converter. The SPCD full-bridge topology consists of a series branch including L_s and a parallel branch including L_p and C_p. According to Fig. 1, the series inductor, L_s, is used to convert voltage pulses to current pulses and the parallel branch, L_p and C_p, is used to produce the reactive current for ZVS and realize the current-driven structure of the converter.

The series inductance, L_s, and the parallel inductance, L_p, can easily be embedded in the high-frequency transformer. Also, the parallel inductance eliminates the need for the auxiliary circuit used to achieve ZVS. Thus, the SPCD full-bridge topology can result in an efficient converter with a high power density. This is due to the fact that this topology is able to absorb the parasitic components of the transformer and use them to transfer power efficiently.

According to Fig. 1, when the parallel inductance current reaches the series inductance current, the output diodes turn OFF. Therefore, the energy stored in the series inductance as well as the energy stored in the parallel inductance at that instant is used to discharge the effective output capacitance of the power semiconductors of the leading leg (the effective output capacitance is the equivalent capacitor at the output of the power MOSFETs, including their parasitic capacitance and external snubber capacitors inserted to eliminate the turn-off losses of the MOSFETs). Since the energy of the two inductances are used to discharge the output capacitor of the power semiconductor, a small current is required to guarantee ZVS. Whereas, in the conventional full-bridge converter, only the energy of the leakage inductance is used to provide ZVS. This is the reason that the conventional full-bridge converter loses ZVS at light loads. Next, the different operating modes of the proposed SPCD topology will be explained in detail.

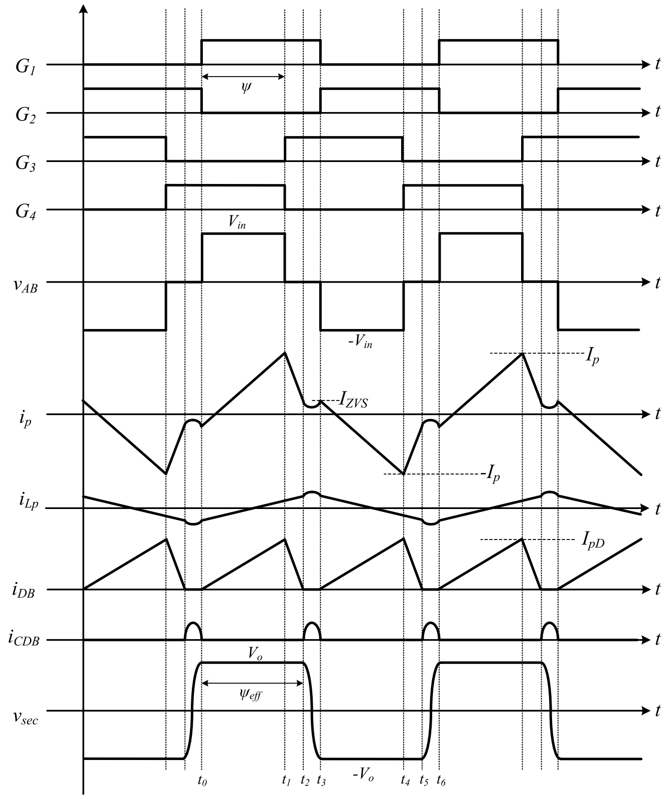

Fig. 2. Key waveforms of the SPCD dc/dc converter.

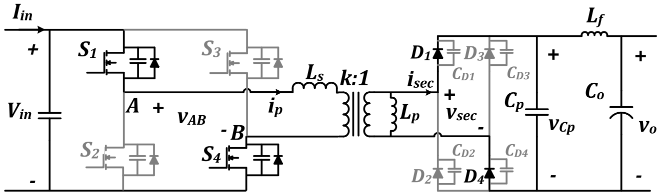

Fig. 3. Equivalent circuit diagram during Mode I.

Fig. 2 shows the key waveforms of the proposed topology. According to this figure, the operation of the converter is divided into six different operating modes. Due to the symmetry, only three modes are presented as follows.

1) Mode I ($t_0 \leq t < t_1$): During this mode, the difference between the input voltage and the reflected parallel capacitor voltage is applied to the series inductor, L_s. At the beginning of this mode, the negative current discharges the output capacitor of S_1, and hence, the MOSFET is turned ON under zero voltage. Fig. 3 shows the equivalent circuit diagram of the proposed SPCD full-bridge topology during Mode I. During this mode, the system dynamics is given by

$$\frac{di_{Ls}}{dt} = \frac{1}{L_s}V_{\text{in}} - \frac{1}{L_s}kv_{Cp} \tag{1}$$

$$\frac{di_{Lp}}{dt} = \frac{1}{L_p}v_{Cp} \tag{2}$$

$$\frac{dv_{Cp}}{dt} = \frac{1}{C_p}ki_{Ls} - \frac{1}{C_p}i_{Lp} - \frac{1}{C_p}i_{Lf} \tag{3}$$

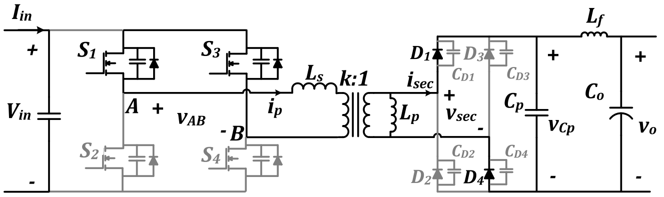

Fig. 4. Equivalent circuit diagram during Mode II.

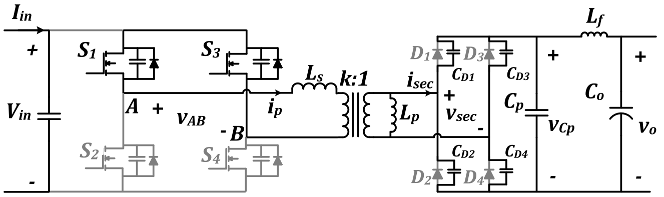

Fig. 5. Equivalent circuit diagram during Mode III.

$$\frac{di_{Lf}}{dt} = \frac{1}{L_f}v_{Cp} - \frac{1}{L_f}v_o. \tag{4}$$

2) Mode II ($t_1 \leq t < t_2$): Mode II starts when the gate signal is applied to S_3 based on the phase shift, ψ. During this mode, the reflected parallel capacitor voltage is applied to the series inductor, L_s. This mode continues until the series inductor current reaches the reflected parallel inductor current. At this point, the output diodes turn OFF naturally. Thus, the commutation is smooth, which is attributed to the current-driven nature of the proposed topology. Fig. 4 shows the equivalent circuit diagram of the proposed SPCD full-bridge topology during Mode II. The converter dynamics are given as follows during this mode:

$$\frac{di_{Ls}}{dt} = -\frac{1}{L_s}kv_{Cp} \tag{5}$$

$$\frac{di_{Lp}}{dt} = \frac{1}{L_p}v_{Cp} \tag{6}$$

$$\frac{dv_{Cp}}{dt} = \frac{1}{C_p}ki_{Ls} - \frac{1}{C_p}i_{Lp} - \frac{1}{C_p}i_{Lf} \tag{7}$$

$$\frac{di_{Lf}}{dt} = \frac{1}{L_f}v_{Cp} - \frac{1}{L_f}v_o. \tag{8}$$

3) Mode III ($t_2 \leq t < t_3$): When the series inductor current reaches the reflected parallel inductor current, the diodes D_1 and D_4 turn OFF. The series inductor, the parallel inductor, the parallel capacitor, and the output capacitances of the output diodes form a resonant circuit. The resonant circuit is effectively determined by the series inductor, L_s, and the output capacitance of the output diodes, C_D, since the parallel inductor is placed in parallel with the series inductor and the parallel capacitor is placed in series with the output capacitances of the diodes in the resonant circuit. Due to the fact that the parallel inductor is usually much larger than the series inductor and the parallel capacitor is much larger than the output capacitances of the diodes, the effective resonant frequency is determined by the series inductor and the output capacitance of the diodes. Fig. 5 shows the equivalent circuit diagram of the proposed SPCD full-bridge topology during Mode III. The voltages across C_{D2}

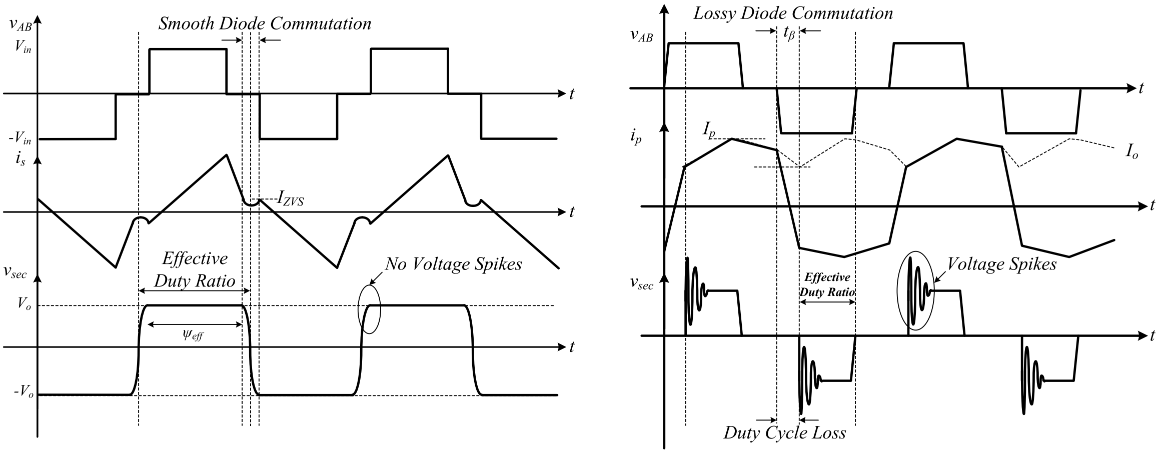

Fig. 6. Comparison between the proposed SPCD converter and conventional full-bridge converter.

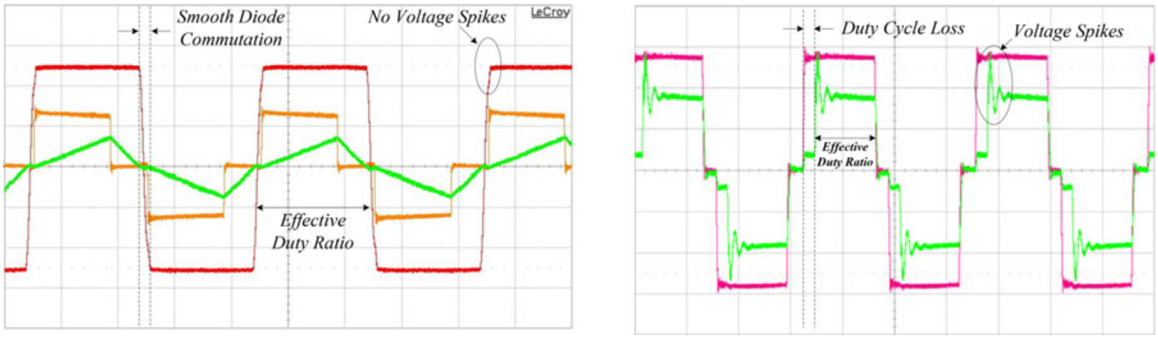

Fig. 7. Comparison between the proposed SPCD converter and conventional full-bridge converter (Experimental).

and C_{D4} are given by

$$v_{C_{D2}} = \frac{v_o}{2} + \frac{v_o}{2}\text{Cos}(\omega_{rd}t) \tag{9}$$

$$v_{C_{D4}} = \frac{v_o}{2} - \frac{v_o}{2}\text{Cos}(\omega_{rd}t) \tag{10}$$

where $\omega_{rd} = \frac{1}{\sqrt{L_{\text{eq}}C_{\text{eq}}}}$, $L_{\text{eq}} = \frac{L_s L_p}{L_s + L_p}$, and $C_{\text{eq}} = \frac{C_p C_{CD}}{C_p + C_{CD}}$.

Therefore, in Mode III, the voltage across the transformer secondary side is derived as

$$v_{\text{sec}} = v_o \text{Cos}(\omega_{rd}t). \tag{11}$$

The secondary voltage is applied across the primary series inductance, L_s, and the parallel inductance, L_p. Thus, the currents through the series inductance, L_s, and the parallel inductance, L_p, are given by

$$i_{Ls} = \frac{kV_o\psi_{\text{eff}}}{4\pi L_p f_{\text{sw}}} - \frac{kV_o}{L_s\omega_{rd}}\text{Sin}(\omega_{rd}t) \tag{12}$$

$$i_{Lp} = \frac{V_o\psi_{\text{eff}}}{4\pi L_p f_{\text{sw}}} + \frac{V_o}{L_p\omega_{rd}}\text{Sin}(\omega_{rd}t). \tag{13}$$

This resonance can be advantageous, since it can smoothly charge and discharge the respective output diodes as shown in Fig. 2. Also, this resonance can provide extra current for the ZVS of the input side MOSFETs. Thus, the advantages of the resonance are twofold: it can guarantee the smooth transition of the output diodes and also provide extra current for the soft switching of the input MOSFETs.

III. QUALITATIVE ANALYSIS OF SPCD DC/DC CONVERTER

In this section, the performance of the proposed SPCD converter is analyzed qualitatively. Figs. 6 and 7 depict the difference between the conventional dc/dc full-bridge converter and the proposed SPCD dc/dc converter. According to this figure, the SPCD topology offers several advantages over the conventional phase-shift full-bridge converter. The current-driven nature of the output rectifier provides smooth commutation of the output diodes and eliminates voltage spikes across the output diodes. Also, the SPCD topology significantly extends the effective duty ratio of the transformer secondary voltage. Whereas, the diode commutations cause duty-ratio loss in the conventional full-bridge converter, particularly for heavy loads.

From Figs. 6 and 7, it is evident that the proposed SPCD topology has far superior performance in terms of soft transitions during the switching intervals of the power semiconductors. However, comparing the current waveform for the SPCD full-bridge converter and the one for the conventional full-bridge converter, one can roughly conclude a higher current stress in the proposed SPCD full-bridge converter. In order to put the switching performance as well as the conduction performance of the proposed SPCD topology into perspective, the following sections analyze the switching losses and the conduction losses in detail.

A. Switching Losses

In this section, the switching performance of the converter is described in detail. In high switching frequency and high output voltage applications, the output rectifier is typically overdesigned due to high-voltage spikes. Therefore, the aforementioned advantages of the SPCD topology are very important. The SPCD topology is able to take advantage of the energy stored in the parallel inductor to provide ZVS conditions for the full-bridge MOSFETs. Also, the SPCD topology utilizes the resonance in mode III to perform smooth commutations of the output diodes simultaneously. The resonance in mode III must discharge the output capacitors of D_2 and D_4 and charge the output capacitors of D_1 and D_3 during the commutation intervals.

In order to ensure the ZVS of the power MOSFETs, the following condition must be satisfied:

$$I_{\text{ZVS}} = \frac{kV_o \psi_{\text{eff}}}{4\pi L_p f_{\text{sw}}} \geq 2C_{So}\frac{V_{\text{in}}}{t_d} \tag{14}$$

where C_{So} represents the output capacitance of the input MOSFETs as well as any snubber capacitors inserted across the power MOSFETs.

The proposed topology takes advantage of the parallel inductor, L_p, to significantly extend the ZVS range of the converter. The conventional phase-shift full-bridge converter usually loses ZVS for light-load conditions, where the energy of the leakage inductance is not enough to charge and discharge the output capacitances of the power MOSFETs. In the case of the SPCD topology, due to the large value of the parallel inductor (the transformer magnetizing inductance is usually utilized as the parallel inductor, L_p), a small amount of current can provide enough energy to guarantee ZVS. In the experimental section, a quantitative comparison of the ZVS range is given to compare the range of ZVS for the proposed SPCD topology with the one for a conventional phase-shift full-bridge topology with the same specifications.

During resonant mode III, the output diodes have soft transitions. Fig. 8 shows the resonant circuit during mode III. This resonance must continue for half a cycle of the resonance in order to guarantee the smooth operation of the output diodes (the output capacitor of D_2, C_{D2}, must be fully discharged and the output capacitor of D_1, C_{D1}, must be fully charged). Fig. 9 shows the smooth transition of the output diodes in the proposed SPCD full-bridge converter compared to the hard and lossy commutations of the output diodes in the case of the conventional phase-shift full-bridge converter. This figure highlights the advantage of the resonant mode. Unlike active clamp topologies, the proposed SPCD topology uses the parasitic components of the converter to form a resonant circuit and the resonant circuit is used to provide smooth transitions.

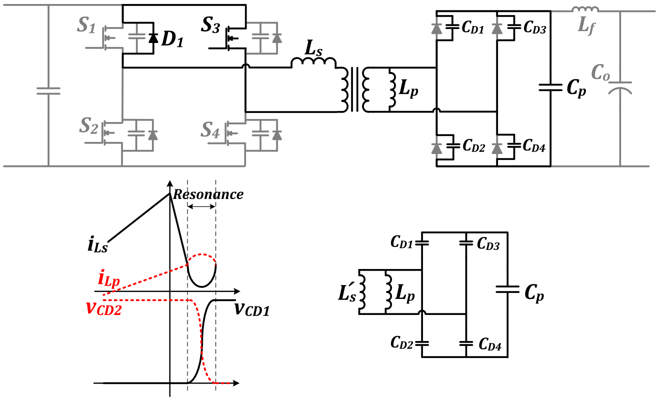

Fig. 8. Resonant circuit during Mode III.

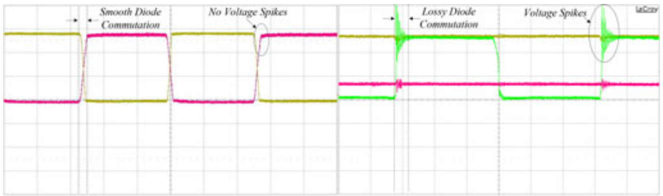

Fig. 9. Comparison between the performance of output diodes in the SPCD topology and the conventional full-bridge topology.

B. Conduction Losses

Generally speaking, the proposed topology has higher RMS current compared to the conventional phase-shift full-bridge converter due to the transformer primary current waveform (as illustrated in Fig. 2). In the conventional phase-shift full-bridge

$$i_{Ls}(t) = \begin{cases} \dfrac{v_{\text{in}} - kv_o}{L_s}t - I_{ZVS} & 0 \leq t < \dfrac{\psi_{\text{eff}}}{\pi}\dfrac{T_s}{2} \\ \dfrac{-kv_o}{L_s}\left(t - \dfrac{\psi_{\text{eff}}}{\pi}\dfrac{T_s}{2}\right) + \dfrac{2\pi P_o}{V_o\psi_{\text{eff}}} & \dfrac{\psi_{\text{eff}}}{\pi}\dfrac{T_s}{2} \leq t < \dfrac{T_s}{2} - \dfrac{\pi}{\omega_{rd}} \\ \dfrac{kV_o\psi_{\text{eff}}}{4\pi L_p f_{\text{sw}}} - \dfrac{kV_o}{L_s\omega_{rd}}\text{Sin}(\omega_{rd}\left(t - \dfrac{T_s}{2} + \dfrac{\pi}{\omega_{rd}}\right)) & \dfrac{T_s}{2} - \dfrac{\pi}{\omega_{rd}} \leq t < \dfrac{T_s}{2} \end{cases} \tag{15}$$

$$i_p(t) = \begin{cases} \left(\dfrac{2P_o}{V_o t_\beta} - \dfrac{(v_{\text{in}} - kv_o)v_o}{2L_f v_{\text{in}} f_s t_\beta}\right)t - \left(\dfrac{P_o}{V_o} - \dfrac{(v_{\text{in}} - kv_o)v_o}{4L_f v_{\text{in}} f_s}\right) & 0 \leq t < t_\beta \\ \left(\dfrac{(v_{\text{in}} - kv_o)}{L_f}\right)(t - t_\beta) + \left(\dfrac{P_o}{V_o} - \dfrac{(v_{\text{in}} - kv_o)v_o}{4L_f v_{\text{in}} f_s}\right) & t_\beta \leq t < \dfrac{\psi_{\text{eff}}}{\pi}\dfrac{T_s}{2} \\ \dfrac{-kV_o}{L_f}\left(t - \dfrac{\psi_{\text{eff}}}{\pi}\dfrac{T_s}{2}\right) + \left(\dfrac{P_o}{V_o} + \dfrac{(v_{\text{in}} - kv_o)v_o}{4L_f v_{\text{in}} f_s}\right) & \dfrac{\psi_{\text{eff}}}{\pi}\dfrac{T_s}{2} \leq t < \dfrac{T_s}{2} \end{cases}. \tag{16}$$

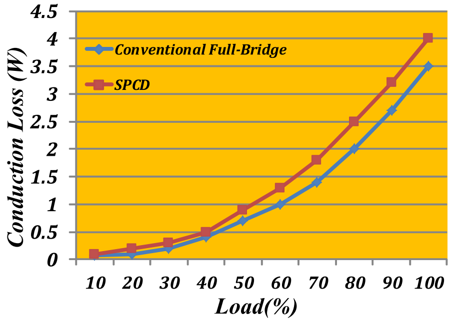

Fig. 10. Comparison between the conduction losses for the proposed SPCD topology and for the conventional full-bridge converter.

converter, the current waveform is closer to a square wave, whereas in the proposed SPCD full-bridge converter, the current waveform has a triangular shape. This shape provides soft transitions for the power semiconductors and other aforementioned advantages in the switching performance of the converter. However, this is at the price of higher RMS current. This drawback is not usually a limiting factor, since the chosen power MOSFETs usually have much higher current ratings than required by the converter in order to have a much lower $R_{\mathrm{DS}}(\mathrm{ON})$. Also, nowadays, MOSFETs with very low $R_{\mathrm{DS}}(\mathrm{ON})$ are available, which can handle very high currents. Therefore, this issue is not a restricting factor in many applications. However, in some applications where the primary-side current is very high, the performance of the converter may considerably deteriorate. Thus, for very high current applications, the proposed topology might not be a very appropriate candidate. In order to give some quantitative sense to this issue, the RMS current of the proposed SPCD full-bridge topology and the one for the conventional full-bridge converter are compared in this section.

According to Fig. 2, the transformer primary-side current waveform is given by (15), shown at the bottom of the previous page, and in the case of the conventional full-bridge converter the primary-side current is given by (16), shown at the bottom of the previous page, [5]. By using (15) and (16), the RMS current can be estimated for the proposed SPCD topology and the conventional full-bridge topology, respectively. It should be noted that the effective phase shift in the proposed SPCD is bigger than the duty ratio applied to the primary side (as shown in Figs. 6 and 7). Whereas, the effective duty ratio is smaller than the duty ratio applied to the primary side in the case of the conventional full-bridge converter. This is the reason that the proposed SPCD topology can provide higher gain compared to the conventional full-bridge converter.

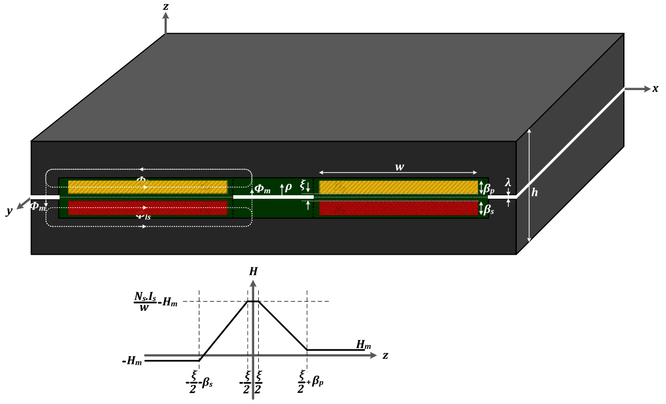

Fig. 11. Top–bottom winding arrangement.

Fig. 10 shows the comparison between the conduction losses of the proposed SPCD topology and those of the conventional full-bridge converter for this specific application (specifications are given in Section VII). This figure shows that the conduction losses are higher. However, due to the higher gain of the converter, the difference between the conduction losses is not as pronounced.

IV. INTEGRATED MAGNETIC DESIGN

This section describes how to integrate the series inductor, L_s, and parallel inductor, L_p, into an integrated transformer. The integration of the series and parallel inductors into the main transformer is commonly used in resonant topologies, particularly in *LLC* resonant converters [31], [32]. The series inductor is achieved through winding the primary and secondary windings beside each other instead of interleaving them, and the parallel inductor is realized by embedding a small air gap in the transformer core. The distance between the primary winding and the secondary winding has a significant impact on the series inductance value. Therefore, with a regular wire-wound transformer, it is very hard to get consistent results for mass production. However, a reliable transformer can be achieved by using planar transformers with windings laid out on a multilayer printed circuit board (PCB). In the following, the design of an

$$H(z) = \begin{cases} -H_m & -\dfrac{h}{2} \leqslant z < -\dfrac{\xi}{2} - \beta_s \\ \dfrac{N_s I_s}{\beta_s w}\left(z + \dfrac{\xi}{2} + \beta_s\right) - H_m & -\dfrac{\xi}{2} - \beta_s \leqslant z < -\dfrac{\xi}{2} \\ \dfrac{N_s I_s}{w} - H_m & -\dfrac{\xi}{2} \leqslant z < \dfrac{\xi}{2} \\ \dfrac{2H_m - N_s I_s}{\beta_s w}\left(z - \dfrac{\xi}{2}\right) + \dfrac{N_s I_s}{w} - H_m & \dfrac{\xi}{2} \leqslant z < \dfrac{\xi}{2} + \beta_p \\ H_m & \dfrac{\xi}{2} + \beta_p \leqslant z < \dfrac{h}{2} \end{cases} \tag{17}$$

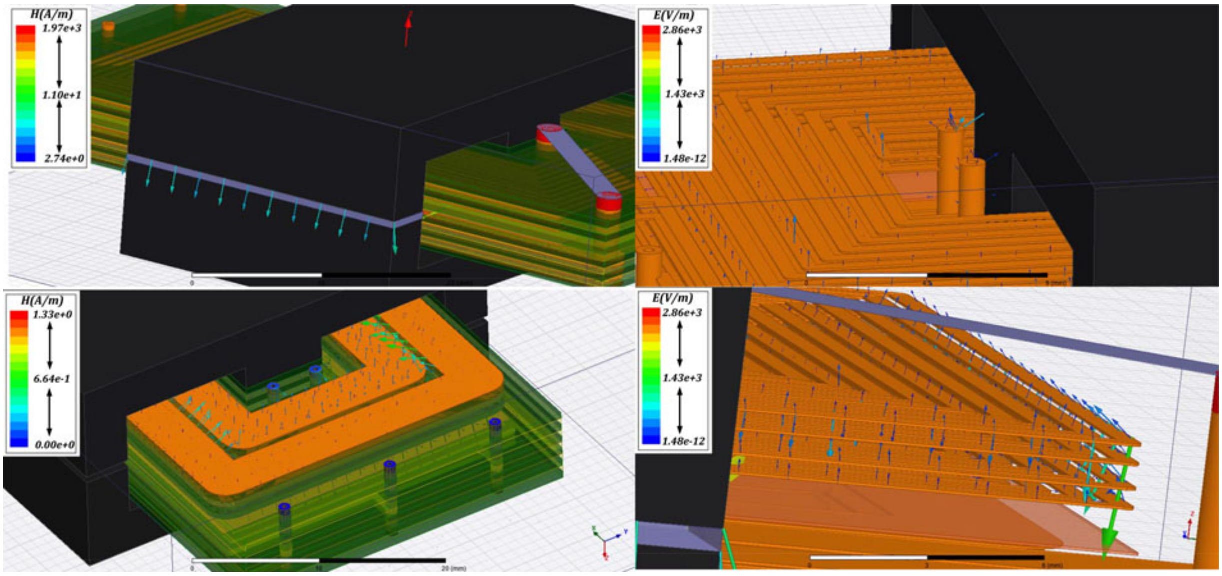

Fig. 12. Different field solutions in HFSS.

TABLE I
INTEGRATED TRANSFORMER PARAMETERS RESULTING FROM HFSS

Symbol	Parameter	Value
Core	Ferrite Core	$E38/8/25$
N_p	Primary Turns	2
N_s	Secondary Turns	40
L_{lk}	Leakage Inductance (primary side)	869 nH
L_m	Magnetizing Inductance (secondary side)	1.79 mH
λ	Air Gap	0.72 mm
ξ	Distance between Primary and Secondary	1.82 mm

integrated planar transformer for the proposed SPCD converter will be explained.

A. Design of an Integrated Planar Transformer

Low-profile planar magnetics are very preferable for applications where repeatability for mass production is of great importance. Since the windings are laid on a PCB, the mass production of the planar magnetics is much easier than with the conventional wire-wound magnetics. In this section, the design of an integrated planar transformer used in the proposed SPCD converter is described. The series inductor, L_s, the parallel inductor L_p, and the high-frequency transformer are integrated in the planar transformer (an EE-core with an air gap is used to realize the planar transformer. Therefore, the following analysis are based on an EE-core with an air gap).

In order to incorporate the series inductance, the primary and secondary windings should be laid out in a top–bottom arrangement instead of a side-by-side or interleaved arrangement [33]. Usually, the side-by-side arrangement cannot produce enough series inductance value for this application. Also, an air gap should be embedded in order to implement the parallel inductor. Fig. 11 shows the top–bottom winding arrangement with an air gap incorporated into the core. In addition, this figure shows how the magnetic flux is distributed in the transformer. The objective in this section is to determine the leakage inductance (series inductor) and the magnetizing inductance (parallel inductor) of the integrated planar transformer. In order to determine the inductances, the magnetic energy stored in the transformer must be determined using the magnetic field intensity, H. In the cross section of the transformer, shown in Fig. 11, the magnetic field intensity is given by (17), shown at the bottom of the previous page.

The leakage inductances are determined by shorting the secondary side of the transformer and calculating the magnetic energy stored in each winding [33]. Therefore, the leakage inductance, L_{lk1}, is given by

$$L_{\text{lk1}} = \frac{\mu_0}{I_p^2} \iiint_{V_p} H^2(\rho) dv \tag{18}$$

where I_p is the primary current and the integral in (18) is over the volume covered by the primary windings, N_p, (V_p). Similarly, reflected secondary leakage inductance, L_{lk2}, is derived as

$$L_{\text{lk2}} = \frac{\mu_0}{I_p^2} \iiint_{V_s} H^2(\rho) dv \tag{19}$$

where the integral in (19) is over the volume covered by the secondary windings, N_s, (V_s). Due to the fact that the permeability of the ferrite core is much bigger than that of air, H_m is negligible. Therefore, the leakage inductances are derived as

$$L_{\text{lk1}} = \frac{\mu_0}{w} N_p^2 \left(\frac{\xi}{2} + \frac{\beta_p}{3}\right) \eta \tag{20}$$

$$L_{\text{lk2}} = \frac{\mu_0}{w} N_p^2 \left(\frac{\xi}{2} + \frac{\beta_s}{3}\right) \eta \tag{21}$$

where η is mean length per turn of the windings.

Since the magnetizing inductance, L_m is much larger than L_{lk1} and L_{lk2}, the total leakage inductance, L_{lk} is estimated as

$$L_{\text{lk}} = L_s = L_{\text{lk1}} + L_{\text{lk2}} = \frac{\mu_0}{w} N_p^2 \left(\xi + \frac{\beta_s + \beta_p}{3}\right) \eta \tag{22}$$

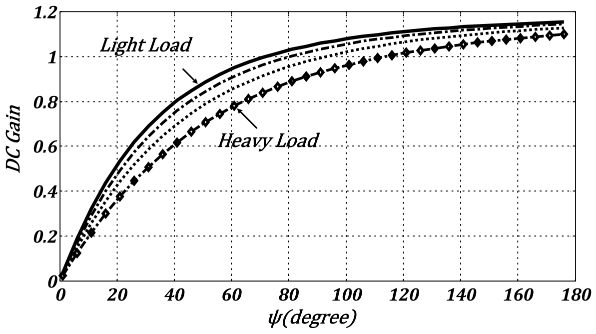

Fig. 13. SPCD converter dc-gain versus phase shift.

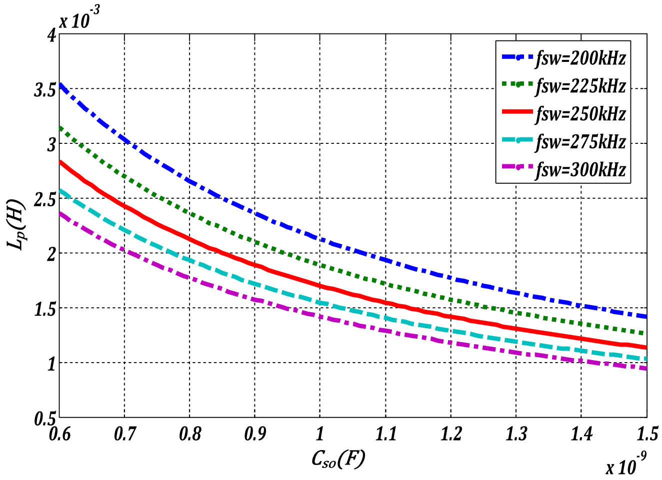

Fig. 14. Parallel inductance design curves.

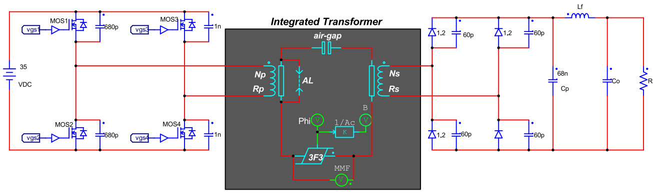

Fig. 15. Schematic of the SPCD full-bridge converter power circuit with integrated magnetics.

According to (22), the only parameter that can be adjusted to control the value of the leakage inductance (series inductor) is the distance between the primary windings and the secondary windings, ξ. By adjusting ξ the value of the series inductor can be determined. The magnetizing inductance is used as the parallel inductor, L_p, in the SPCD converter. The magnetizing inductance can be adjusted by the air gap embedded in the magnetic core. Therefore, the amount of air gap is the parameter used to adjust the value of the parallel inductor. The magnetizing inductance is given by [33]

$$L_m = L_p = \mu_0 N_s^2 \frac{A_e}{\lambda} \tag{23}$$

where A_e is the effective core cross section area and λ is the amount of air gap.

In summary, the series inductor, L_s, and the parallel inductor, L_p, can be adjusted by designing ξ and λ according to (22)–(23), respectively. Even though (22)–(23) provide a good approximation of the respective inductances, they cannot precisely determine the actual values due to different approximations used to derive the equations. However, they provide a very good starting point in the design of the integrated transformer. In the following section, the integrated transformer is modeled using ANSYS software in order to perform a finite-element analysis. The finite-element analysis can precisely produce different parameters of the integrated transformer. The calculated air gap and ξ are used as a starting point to establish the physical model for the finite-element analysis.

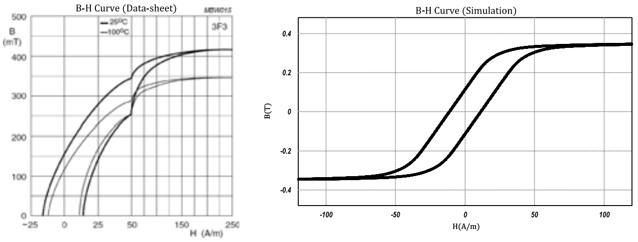

Fig. 16. B–H curve for $3F3$ core from the data sheet and from the simulation.

TABLE II
SIMULATION PARAMETERS

Symbol	Parameter	Value
P_o	Output Power	300 W
V_o	Output Voltage	400–450 V(DC)
$v_{\rm in}$	Input Voltage	32–55V(DC)
$f_{\rm sw}$	Switching Frequency	220 kHz
L_s	Series Inductance	870 nH
L_p	Parallel Inductance	1.80 mH
C_p	Parallel Capacitance	1.0 μF
L_f	Filter Inductor	2.2 μH
C_o	Output Capacitor	47 μF
$C_{\rm in}$	Input Capacitor	22 μF

B. Finite-Element Analysis of Integrated Transformer

In this section, the integrated transformer is analyzed using the finite-element method (FEM) in order to predict the transformer parameters. It should be noted that the details of the analysis are given in the appendix and only the key results are presented in this section. Included in the appendix is the procedure used to prepare a typical structure for the high-frequency structure simulator (HFSS) simulation. This simulation solves the structure for the electric field and magnetic field as well as their attributes. Fig. 12 shows different field solutions resulting from the HFSS analysis. In this figure, the magnetic field intensity within the air gap and the electric and magnetic fields are shown. Based on the HFSS analysis, the precise amount of air gap and the distance between the primary windings and the secondary winding are obtained in order to achieve the desired series and parallel inductances. The obtained values are listed in Table I. The values given in Table I should be very close to the final values of λ and ξ. According to Table I, the chosen core is $E38/8/25$ (the details of the converter are given in the experimental section). Since the output voltage is high (400 V),

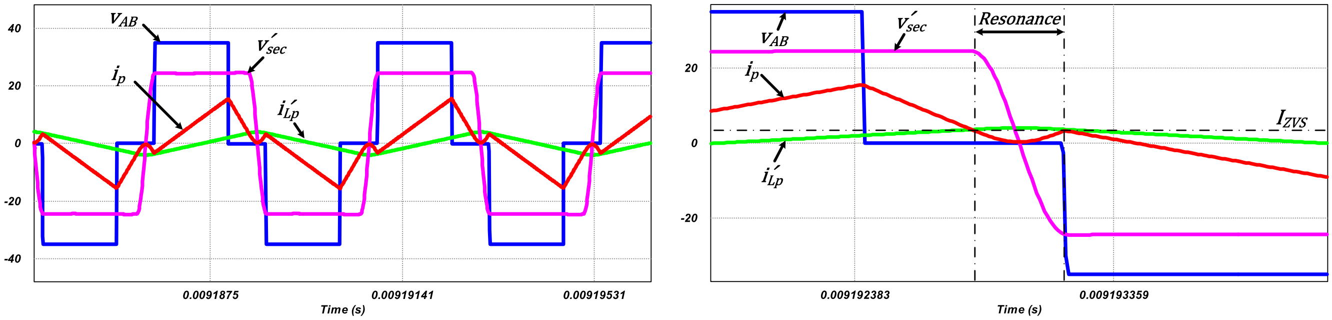

Fig. 17. Simulation waveforms of the SPCD full-bridge dc/dc converter in the transformer primary side.

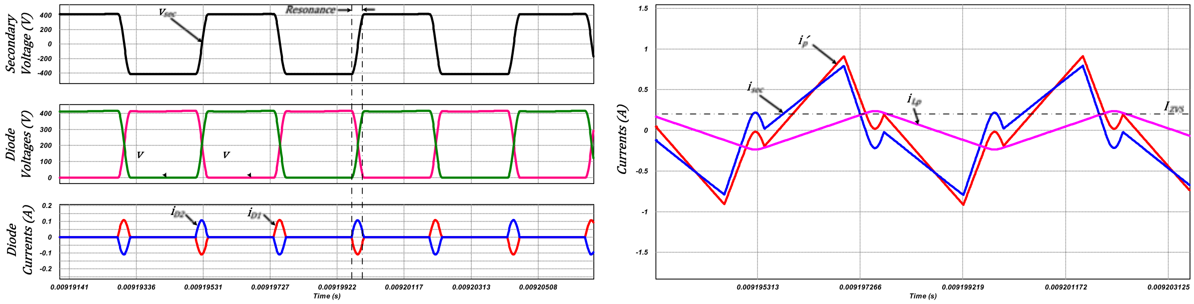

Fig. 18. Simulation waveforms of the SPCD full-bridge dc/dc converter in the transformer secondary side.

this core is selected to be able to accommodate the insulation requirements of the secondary side.

V. DESIGN OF SPCD FULL-BRIDGE DC/DC CONVERTER

In this section, different design parameters of the proposed SPCD full-bridge dc/dc converter are described in order to provide necessary information for a power engineer to design the converter. For instance, the gain of the converter, the design of different components, and the components' ratings are among the main information required to design a practical dc/dc converter. In the following subsections, the main design parameters of the SPCD converter will be explained in detail.

A. *SPCD Full-Bridge Converter DC Gain*

The dc-gain is one of the most important design parameters in a typical dc/dc converter. One of the main advantages of the proposed SPCD dc/dc converter is its ability to boost the voltage due to its "boost-like" structure. This advantage is very preferable in applications with high output voltage and low input voltage in order to reduce the turns ratio of the power transformer, and in turn reduce the copper losses of the transformer. The converter dc-gain is calculated by equating the input power and the output power of the converter (this is a common practice used to derive the dc-gain of dc/dc converters). According to Figs. 1 and 2, the output power is given by

$$P_o = V_o . \langle i_{\mathrm{DB}} \rangle_{T_{\mathrm{sw}}/2} \tag{24}$$

where $\langle i_{\mathrm{DB}} \rangle_{T_{\mathrm{sw}}/2}$ is the average value of the diode bridge output current over a half switching cycle.

TABLE III
EXPERIMENTAL PROTOTYPE PARAMETERS

Symbol	Parameter	Value/Part Number
P_o	Output Power	300 W
V_o	Output Voltage	400–450 V(DC)
v_{in}	Input Voltage	32–55 V (DC)
f_{sw}	Switching Frequency	220 kHz
L_s	Series Inductance	875 nH
L_p	Parallel Inductance	1.85 mH
C_p	Parallel Capacitance	$CKG57NX7T2J105M500JH$
L_f	Filter Inductor	$CLF10040T-2R2N$
C_o	Output Capacitor	$B32796G2506K$
C_{in}	Input Capacitor	$C3225X7S2A475M200AB$
S_i	Power MOSFETs	$BSC160N10NS3G$
D_i	Output Diodes	$MURS160$

Using the steady-state equations of the converter, the output power is calculated as

$$P_o = \frac{V_o}{4k} \left[\left(\frac{V_{\mathrm{in}} - kV_o}{L_s} \right) \left(\frac{\psi}{\pi} \right) (T_{\mathrm{sw}} - T_{rd}) \right] \tag{25}$$

where $T_{rd} = \frac{2\pi}{\omega_{rd}}$.

According to Figs. 1 and 2, the input power is given by

$$P_{\mathrm{in}} = V_{\mathrm{in}} . \langle i_{\mathrm{in}FB} \rangle_{T_{\mathrm{sw}}/2} \tag{26}$$

Similarly, the input power is calculated using the steady-state equations of the converter as follows:

$$P_{\mathrm{in}} = V_{\mathrm{in}} \left[\left(\frac{V_{\mathrm{in}} - kV_o}{L_s} \right) \left(\frac{\psi}{\pi} \right) - \frac{2I_{\mathrm{ZVS}}}{T_{\mathrm{sw}}} \right] \left(\frac{\psi T_{\mathrm{sw}}}{2\pi} - t_d \right) \tag{27}$$

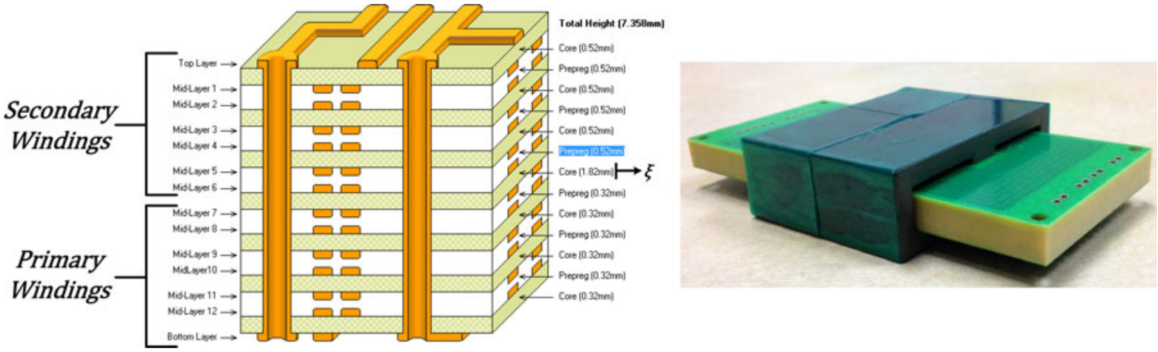

Fig. 19. Integrated planar transformer prototype.

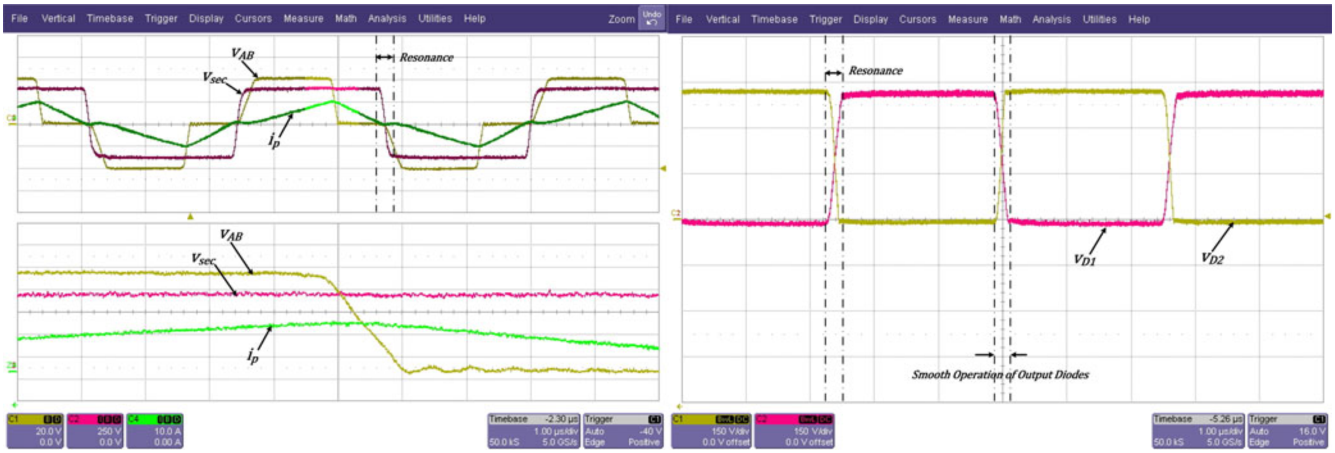

Fig. 20. Experimental waveforms for the proposed SPCD full-bridge dc/dc converter.

where t_d is the dead time. If the dead time is ignored, the converter dc-gain is calculated by equating the input power and the output power as follows:

$$G_{\mathrm{DC}} = \frac{V_o}{V_{\mathrm{in}}} = \frac{-\eta_2 + \sqrt{\eta_2^2 - 4\eta_1\eta_3}}{2\eta_1} \tag{28}$$

where

$$\eta_1 = \left(\frac{1}{L_s} + \frac{1}{L_p}\right)(T_{\mathrm{sw}} - T_{rd}/2)$$

$$\eta_2 = -\left[\frac{kV_{\mathrm{in}}}{L_s}\frac{\psi T_{\mathrm{sw}}}{2\pi} + \frac{V_{\mathrm{in}}}{kL_s}(T_{\mathrm{sw}} - T_{rd}/2)\right]$$

$$\eta_3 = \left[\frac{V_{\mathrm{in}}^2}{L_s}\frac{\psi T_{\mathrm{sw}}}{2\pi} - V_{\mathrm{in}} I_{ZVS}\right].$$

Equation (28) determines the dc-gain of the proposed SPCD full-bridge dc/dc converter. Fig. 13 shows the dc-gain of the converter with respect to the phase-shift angle for a typical design. According to this figure, the converter is able to boost the voltage, due to the increase in effective duty cycle.

B. Design of SPCD Converter Components

In the section, the design procedure of the different components used in the SPCD converter is explained in detail. The first component is the series inductor, L_s. The series inductor determines the power transfer capability of the converter. Lower values of the series inductor result in higher power transfer capability and vice versa. However, the very low value of the series inductor leads to high peak current in the primary side of the transformer. Therefore, the series inductor, L_s, is designed based on the power ratings of the converter and allowable peak current at the transformer primary side. The design equation for the series inductor, L_s, is given by

$$L_s = \frac{(V_{\mathrm{in}}^2 - kV_o V_{\mathrm{in}})\psi_{\max}^2}{4\pi^2 P_o f_{\mathrm{sw}}} \tag{29}$$

The RMS current of the series inductor is approximately derived as

$$I_{L_s}^{\mathrm{rms}} = \frac{(V_{\mathrm{in}} - kV_o)\psi_{\max}}{\sqrt{3}L_s\omega_{\mathrm{sw}}} \tag{30}$$

The parallel inductor, L_p is designed such that there is enough current to guarantee ZVS. This inductor should be designed to result in just enough current to charge and discharge the MOSFETs' output capacitors. Thus, according to (14), the value of the parallel inductor, L_p, is given by

$$L_p = \frac{kV_o V_{\mathrm{in}}\psi_{\mathrm{eff}} t_d}{4C_{So}V_{\mathrm{in}}\omega_{\mathrm{sw}}}. \tag{31}$$

Fig. 14 shows the design curve for the parallel inductance versus C_{So} (equivalent output capacitance of the power MOSFETs) for different switching frequencies. According to this figure, if

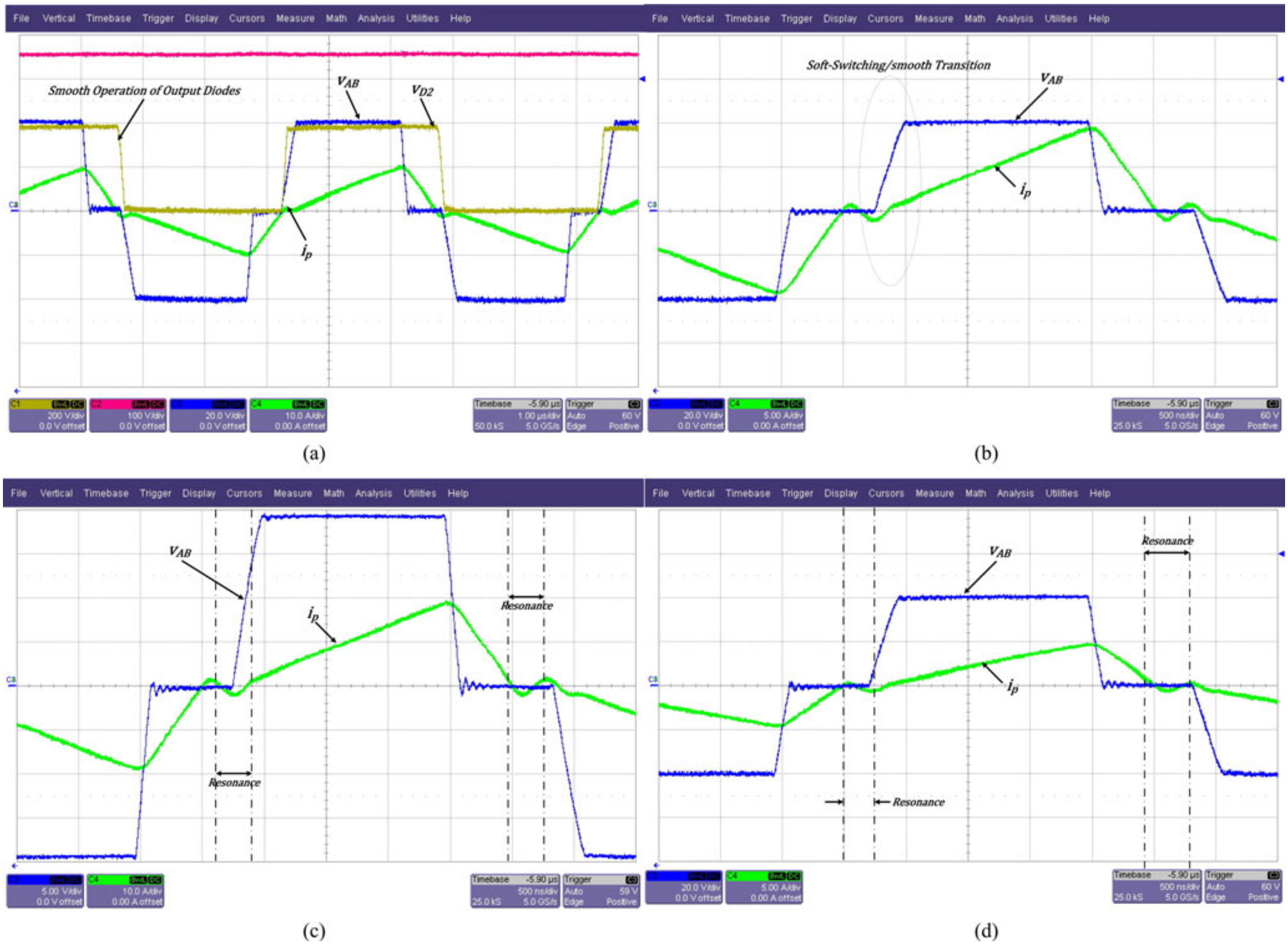

Fig. 21. Experimental waveforms for different loads/voltages, (a) full-bridge voltage, the transformer primary-side current, and the output diode voltage for $v_{\rm in} = 40$ V, $v_o = 400$ V, and 50% load, (b) full-bridge voltage, the transformer primary-side current for $v_{\rm in} = 40$ V, $v_o = 400$ V, and 50% load, (c) full-bridge voltage, the transformer primary-side current for $v_{\rm in} = 38$ V, $v_o = 420$ V, and 100% load, (d) full-bridge voltage, the transformer primary-side current for $v_{\rm in} = 40$ V, $v_o = 400$ V, and 20% load.

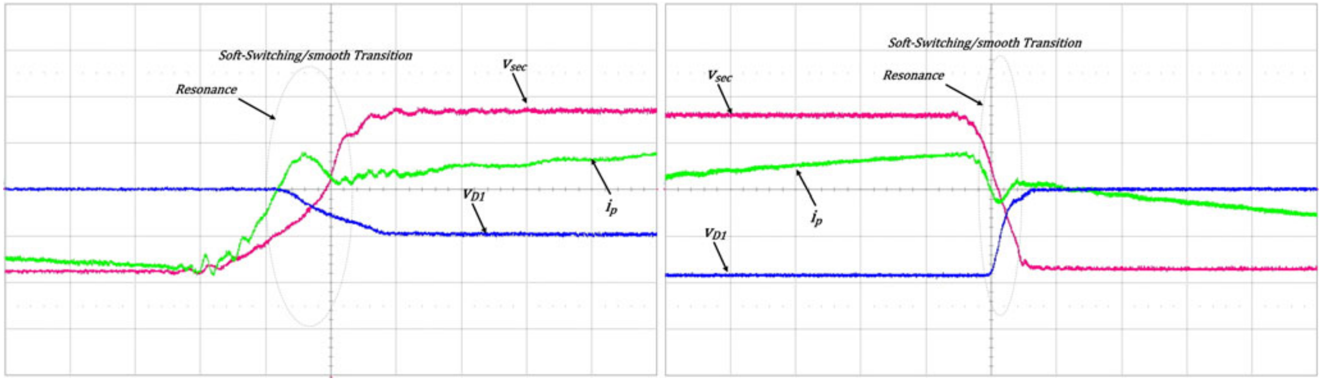

Fig. 22. Resonance mode of operation in the proposed SPCD full-bridge dc/dc converter.

the parallel inductance is designed such that it is underneath the corresponding curve, ZVS conditions are guaranteed.

The other component to be designed is the parallel capacitor, C_p. According to the converter operating principles, the voltage across the parallel capacitor, v_{Cp}, is very close to the output voltage, V_o. Therefore, the voltage rating of the parallel capacitor, C_p, is the output voltage of the converter. The current rating of this capacitor is the ripple component of $i_{\rm DB}$ (this current includes a dc component and a ripple component as shown in Fig. 2). Herein lies one advantage of the SPCD topology compared to the series resonant topology or *LCC* resonant topology. In the SPCD converter, the current ripple of the parallel capacitor is much less than the current flowing through the resonant capacitor in *LCC*/series resonant topologies. Therefore, the

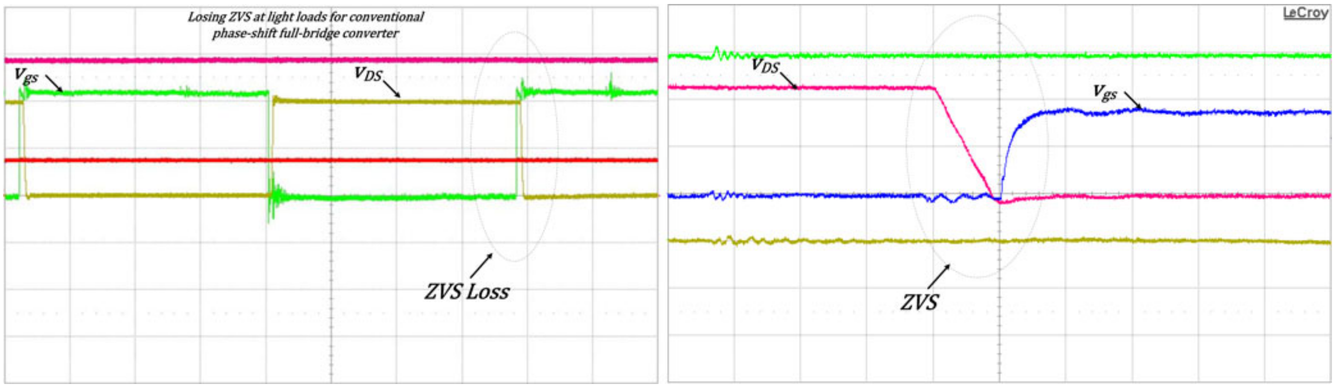

Fig. 23. ZVS comparison of the proposed SPCD topology and the conventional full-bridge topology at 20% load.

TABLE IV
ZVS RANGE COMPARISON

Topology	ZVS Load Range
SPCD Full-Bridge Toplogy	12%–100%
Conventional Full-Bridge Toplogy	37%–100%

losses of this capacitor are much less compared to the losses of the series capacitor in resonant topologies. Also, the breakdown voltage of the capacitor significantly reduces with switching frequency. Therefore, a resonant capacitor with high-frequency voltage ripple should be drastically overdesigned for reliable operation. This difficulty is rectified in the proposed SPCD topology due to the fact that the voltage across the parallel capacitor is mainly a dc voltage with a negligible high-frequency ripple. The current flowing through the parallel capacitor is given by

$$i_{Cp} = i_{\mathrm{DB}} - \langle i_{\mathrm{DB}} \rangle_{T_{\mathrm{sw}}/2}. \tag{32}$$

Therefore, the parallel capacitor RMS current is derived as

$$I_{Cp}^{\mathrm{rms}} = \frac{1}{k\sqrt{3}} \left(\frac{V_{\mathrm{in}} - kV_o}{L_s} - \frac{kV_o}{L_p} \right) \left(\frac{\psi}{\omega_{\mathrm{sw}}} \right) - \frac{1}{2k\sqrt{3}} \left(\frac{V_{\mathrm{in}} - kV_o}{L_s} - \frac{kV_o}{L_p} \right) \left(\frac{\psi}{\pi} \right) \left(\frac{T_{\mathrm{sw}} - T_{rd}}{2} \right). \tag{33}$$

The value of the parallel capacitor is designed such that there is a small high-frequency voltage ripple across the parallel capacitor. A 10% high-frequency ripple is reasonable for the design. Therefore, the value of the parallel capacitor, C_p, is given by

$$C_p \geq \frac{(i_{\mathrm{DB}} - \langle i_{\mathrm{DB}} \rangle_{T_{\mathrm{sw}}/2}) T_{\mathrm{sw}}}{0.2 V_o} \tag{34}$$

$$C_p \geq \frac{10\pi}{kV_o} \left(\frac{V_{\mathrm{in}} - kV_o}{\omega_{\mathrm{sw}} L_s} - \frac{kV_o}{\omega_{\mathrm{sw}} L_p} \right) \left\{ \left(\frac{\psi}{\omega_{\mathrm{sw}}} \right) - \left(\frac{\psi}{\pi} \right) \left(\frac{T_{\mathrm{sw}} - T_{rd}}{2} \right) \right\}. \tag{35}$$

VI. PERFORMANCE ANALYSIS THROUGH SIMULATION

In this section, the simulation results for the proposed SPCD full-bridge topology are presented. PowerSim V9.2.1 (PSIM) software has been used to obtain the simulation results. PSIM includes “Magnetic Elements,” which can be used to precisely model the magnetics. In order to accurately analyze the performance of the SPCD full-bridge topology, the integrated transformer can be modeled using “magnetic elements.”

Fig. 15 shows the schematic of the SPCD full-bridge converter power circuit with the integrated magnetics. The parameters of the integrated magnetic have been inserted into this simulation using the results obtained from the HFSS analysis (see Table I). According to Fig. 15, the air gap, the core properties, and the leakage inductance have been modeled through “magnetic elements.” There is an iterative process to make the *B–H* curve of the core in the simulation fit the one in the data sheet. Fig. 16 shows the *B–H* curve of the $3F3$ core from the data sheet and from the simulation.

Table II presents the parameters used to conduct the simulations for the SPCD full-bridge dc/dc converter. Fig. 17 shows the simulation waveforms of the SPCD full-bridge dc/dc converter. In this figure, the waveforms of the transformer secondary side are reflected to the primary side. The resonance mode is clearly seen in this figure. This resonance provide a smooth transition for the output diodes as well as ZVS for the leading-leg MOSFETs. The smooth operation of the output diodes are shown in Fig. 18. According to this figure, there are no voltage spikes across the output diodes and also the lossless commutations of the output diodes are evident. This figure also shows the reflected primary current, the parallel inductor current and the transformer secondary current.

VII. EXPERIMENTAL RESULTS

In order to evaluate the performance of the proposed SPCD full-bridge dc/dc converter, an experimental prototype has been prepared. Table III shows the parameters of the experimental prototype. The integrated planar transformer is implemented using a PCB. Fig. 19 shows the implemented integrated transformer. This figure shows how the primary windings and the secondary windings are laid out on the different layers of the PCB. Also, the distance between the primary windings and the secondary windings, ξ, is embedded in the PCB as shown in Fig. 19. The distance between the secondary windings are larger

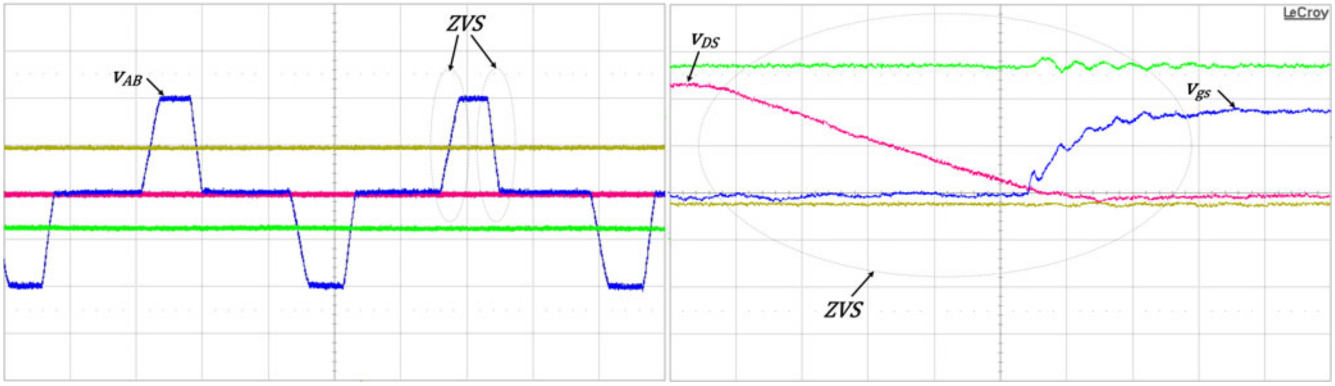

Fig. 24. ZVS performance of the SPCD converter at 12% load.

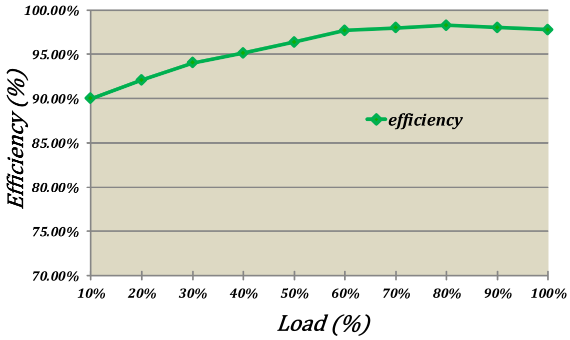

Fig. 25. Efficiency curve of the proposed SPCD full-bridge dc/dc converter.

than the one for the primary windings due to the different insulation requirements. The parameters of the implemented planar transformer are very close to the ones obtained from the HFSS simulations (see Table I).

The control system of the proposed SPCD full-bridge dc/dc converter is based on the peak current mode (PCM) control scheme [37], [38]. The PCM controller prevents transformer saturation and provides a fast cycle-by-cycle transient response. The control system is implemented using a Field-Programmable Gate Array (FPGA). The FPGA is able to provide a very fast and reliable solution to digitally implement the control system. In particular, Cyclone IV $EP4CE22F17C6N$ from Altera is used as the core FPGA to implement the control system. This FPGA provides a very fast and cost-effective solution for the control of power converters [39]–[43].

Fig. 20 shows the experimental waveforms of the proposed SPCD full-bridge dc/dc converter. This figure shows the primary current, i_p, full-bridge output voltage, v_{AB}, and the integrated transformer secondary voltage, $v_{\rm sec}$. According to this figure, the full-bridge output voltage demonstrates a smooth transition due to the soft switching. The secondary voltage also has smooth transitions due to the resonant mode (Mode III) in this particular topology. In addition, this figure shows the voltage across the output diodes. It is evident that there are no voltage spikes across the output diodes and the commutation is smooth and lossless.

Fig. 21 shows the experimental waveforms of the converter for different loads and different voltages. This figure demonstrates smooth voltage transitions and superior performance of the proposed SPCD full-bridge converter. Fig. 22 shows the resonance mode of operation (Mode III), which provides the required ZVS current and causes the smooth commutation of the output diodes. In addition, the SPCD topology extends the ZVS range significantly compared to the conventional phase-shift full-bridge topology. In the conventional full-bridge topology, ZVS is achieved through the energy of the leakage inductance, which is usually not enough to charge and discharge the MOSFETs' output capacitors at light loads. In the proposed SPCD topology, the energy of the parallel inductor is used to extend the ZVS range significantly.

Fig. 23 shows the ZVS performance of the proposed SPCD topology compared to the conventional full-bridge topology at 20% load. This figure shows that the proposed topology can successfully maintain ZVS for light loads owing to the energy stored in the parallel inductance. Table IV shows the ZVS range of the proposed SPCD converter and the one for the conventional full-bridge converter designed for the specifications given in Table III. Fig. 24 shows the ZVS performance of the SPCD converter at 12% load. It should be mentioned that the dead time for light loads should be larger than the one for heavier loads. Therefore, an adaptive algorithm is implemented to change the dead time accordingly. For very light loads (less than 12% load), the control system reduces the switching frequency drastically in order to reduce the driver losses of the converter. Therefore, the circuit loses ZVS for very light loads and there might be several periods of resonance between the series inductor and the capacitances of the output diodes.

The proposed SPCD topology is able to result in a high efficiency due to the soft switching in the primary and secondary side of the transformer. Fig. 25 shows the efficiency curve of the proposed SPCD full-bridge dc/dc converter. This figure confirms the highly efficient operation of the converter (peak efficiency of 98.26%).

VIII. COMPARATIVE STUDY

In this section, the performance of the proposed SPCD full-bridge topology is compared with the state-of-the-art topologies, which are the current-driven full-bridge converter and the current-driven resonant topologies (i.e., series resonant converter and *LLC* resonant converter) [23], [30], [44], [45]. Thus,

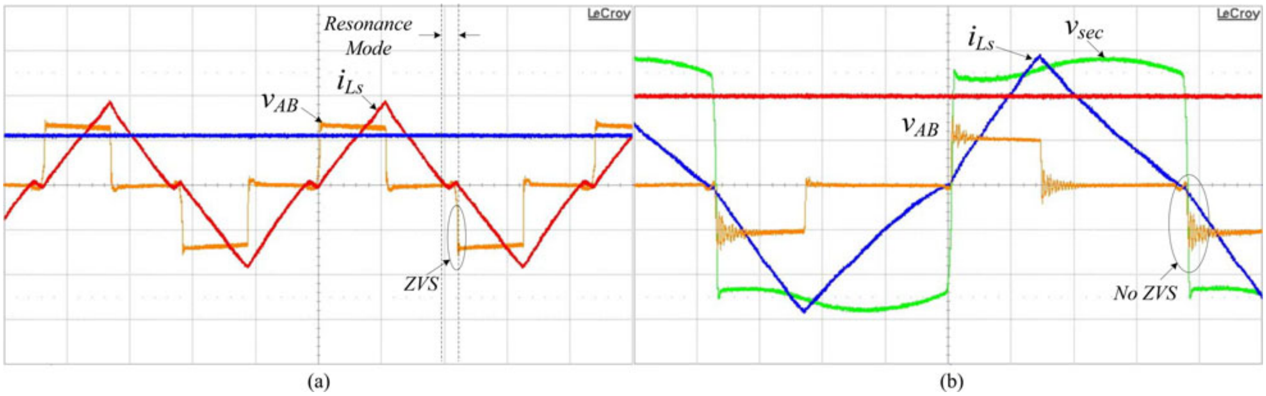

Fig. 26. Performance comparison between (a) proposed SPCD full-bridge converter and (b) current-driven full-bridge converter.

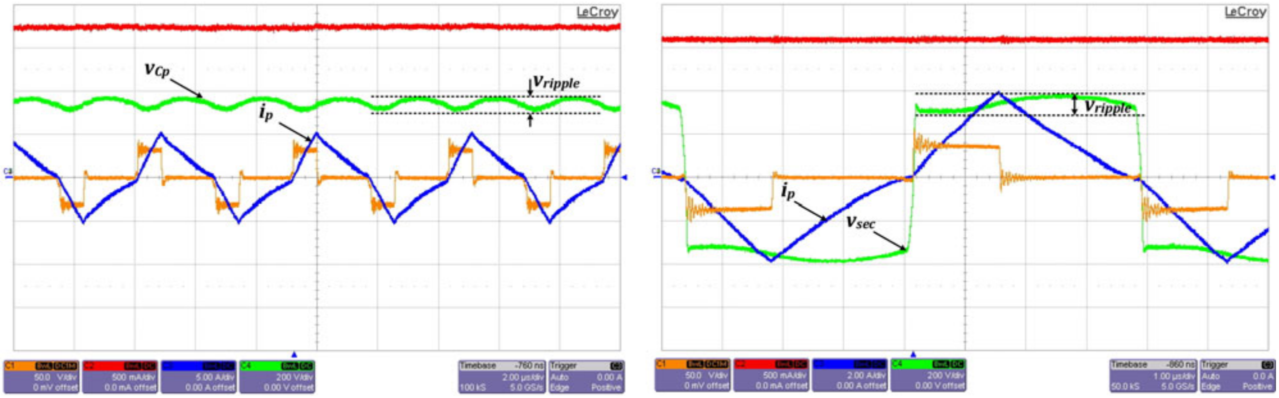

Fig. 27. Experimental waveforms of the current-driven full-bridge converter with reduced parallel capacitor.

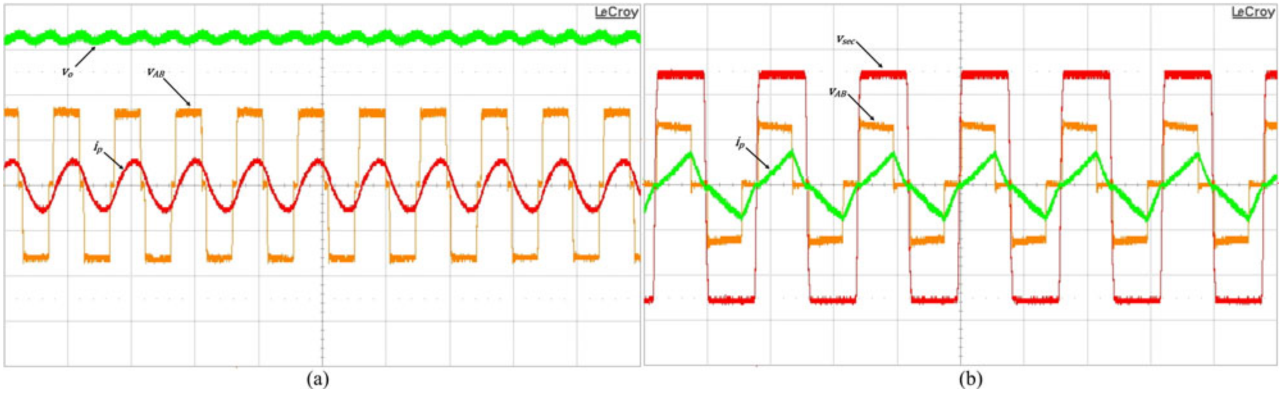

Fig. 28. Experimental waveforms of (a) resonant converter and (b) SPCD converter.

the aforementioned topologies are designed and implemented with the same specifications. The intended application in this paper is the first-stage dc/dc converter for a two-stage PV microinverter [46]. Fig. 26 illustrates the performance comparison between the proposed SPCD full-bridge converter and the current-driven full-bridge converter. This figure shows that the resonance mode in the proposed SPCD topology provides reactive current to realize ZVS, whereas in the case of current-driven topology, this reactive current should be provided by an extra auxiliary circuit, otherwise the MOSFETs of the leading leg do not turn ON with ZVS. Also, comparing this figure with Fig. 22, it is concluded that the output diodes have much smoother transitions in the case of the SPCD topology versus the current-driven topology. Although the current-driven topology can eliminate the voltage spikes across the output diodes, the commutations of the output diodes are not lossless. Whereas, in the proposed SPCD full-bridge topology, the commutations are lossless due to the resonant mode provided by the series inductance, parallel inductance, diodes' output capacitances, and the parallel capacitance. In the case of the SPCD topology, the voltage transitions of the output diodes are sinusoidal, whereas in the case of current-driven full-bridge or current-driven resonant topology, the voltage across the output diodes are square wave.

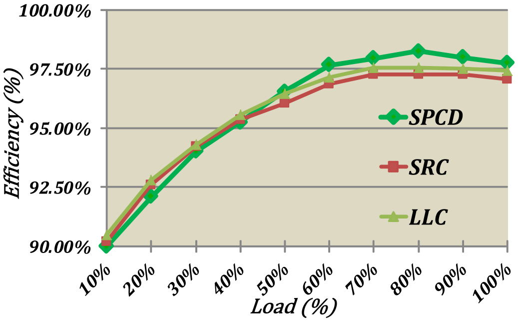

Fig. 29. Efficiency comparison of the SPCD, SRC, and *LLC* converters.

TABLE V
POWER DENSITY COMPARISON

Topology	Power Density
SPCD Toplogy	0.98 kW/L
SRC Toplogy	0.87 kW/L
LLC Toplogy	0.87 kW/L

TABLE VI
SPECIFICATIONS OF INTEGRATED TRANSFORMER

Symbol	Parameter	Value
Core	Ferrite Core	$E38/8/25$
P_{rated}	Rated Power	300 W
N_p	Primary Turns	2
N_s	Secondary Turns	40
L_{1k}	Leakage Inductance (primary side)	0.85 μH
L_m	Magnetizing Inductance (secondary side)	1.88 mH
λ	Air Gap	0.65 mm
ξ	Distance between Primary and Secondary	1.74 mm

It should be noted that the voltage across the parallel capacitor has a significant dc-component as well as a high-frequency ripple. Since the dc-component is much larger than the high-frequency ripple, the ripple is not clear in the experimental results. In order to demonstrate the presence of this high-frequency ripple, it can be amplified by reducing the parallel capacitor. Fig. 27 shows the voltage across the parallel capacitor when the value of the parallel capacitor is reduced significantly.

Current-driven type resonant converters (i.e., series resonant converters and *LLC* resonant converters) have widely been used for high-frequency applications with high output voltages [41], [42]. Since current-driven resonant topologies are able to eliminate the voltage spikes across the output diodes and provide soft switching for the power MOSFETs, they are good candidates for high-frequency/high-voltage applications. In order to compare the performance of the current-driven type resonant converters with the proposed SPCD full-bridge topology, a series resonant converter (SRC), and an *LLC* resonant converter have been designed and implemented with the same specifications for this particular application. Fig. 28 shows the experimental waveforms for the SPCD topology and the resonant topology, and Fig. 29 shows the efficiency comparison between the three converters. Also, the power densities of the three different topologies are summarized in Table V. According to Fig. 29 and Table V, the proposed SPCD topology can achieve slightly higher peak efficiency and higher power density.

The reason that the SPCD topology achieves higher efficiency and higher power density lies in the resonant circuit in the series and *LLC* resonant converters. In the SRC, the high-frequency voltage across the series capacitance is roughly QV (Q is the quality factor of the resonant circuit, and V is the voltage applied to the resonant circuit). This high-frequency voltage has two detrimental impacts on the performance of the converter. The first detrimental impact of the high-frequency voltage is that it creates a fairly large high-frequency voltage across the series inductor. Thus, there is a substantial amount of core losses in the series inductor. Due to the large high-frequency voltage, it is very hard to integrate the series inductor into the transformer and achieve reasonable core losses. In this particular application, an external inductor is used in order to achieve a high efficiency. The second detrimental impact of the high-frequency voltage across the series capacitor is on the design of the series capacitor. The challenge in the design is the breakdown voltage of the series capacitor. The breakdown voltage drastically degrades as the operating frequency (switching frequency) increases. Therefore, usually a high-voltage capacitor is used to be able to withstand the high-frequency voltage ripple (e.g., capacitors with 400-V breakdown voltage are selected to be able to withstand 50-V high-frequency voltage). Also, due to the high ripple current passing through the series resonant capacitor (in this particular application, the ripple current can be as high as 15 A), several high-voltage capacitors with high equivalent series resistance (ESR) should be used in parallel to reduce the conduction losses of the series resonant capacitor and achieve a reasonably high efficiency. Therefore, the series resonant inductor and capacitor greatly contribute to the volume and the cost of the SRC and LLC converters. This is not the case for the proposed SPCD topology whose parallel capacitor, C_p, is mainly subjected to a dc voltage (output voltage) and can easily be placed on the high voltage side after the diode rectifier with very small current ripple. This is the main reason for the lower power density and lower efficiency of the resonant topologies compared to the proposed SPCD converter. In addition, in the case of the SPCD topology, the voltage across the series inductor is much lower than the one in the SRC and *LLC*. Therefore, the series inductor can easily be integrated into the transformer. The power density achieved by this topology is close to 1.0 kW/L, which is higher than the SRC and *LLC* resonant converters used in the previous designs (power density around 0.87 kW/L). This topology is a good candidate for applications with a high switching frequency and a high output voltage, such as traction battery chargers for plug-in electric vehicles and also residential wind energy conversion systems [47]–[49].

The main disadvantage of the SPCD topology is the higher RMS current compared to the one in resonant topologies. In the resonant topologies, the current waveform is close to a sinusoidal waveform, whereas in the SPCD full-bridge converter the current waveform has a triangular shape. This is the reason the efficiency of the SPCD topology is not much higher than the resonant topologies, despite the high amount of losses

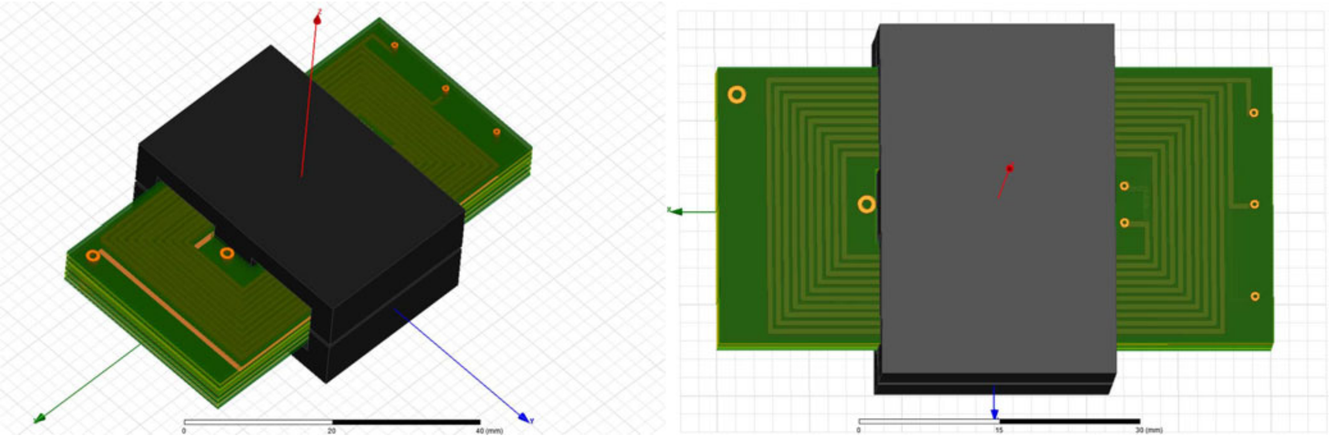

Fig. 30. Structure of the integrated transformer.

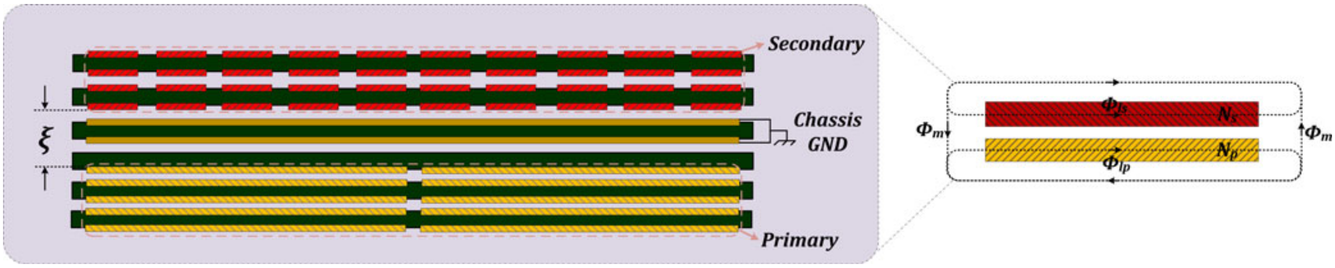

Fig. 31. Top-bottom arrangement of the primary and secondary windings.

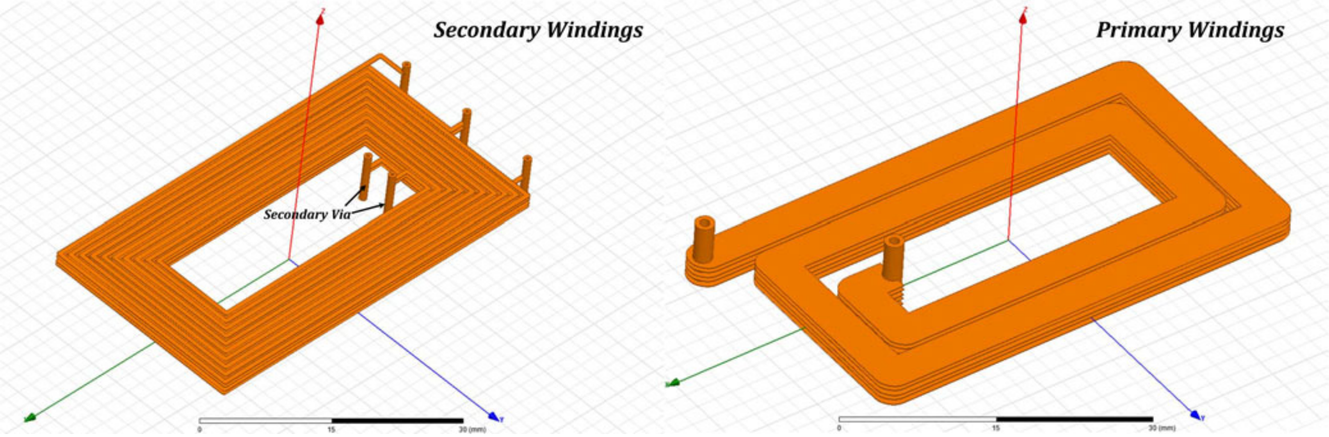

Fig. 32. Primary and secondary windings in HFSS.

in the resonant circuit. This drawback can be mitigated by using extremely low $R_{\mathrm{DS}}(\mathrm{ON})$ power MOSFETs. Nowadays, MOSFETs with very low $R_{\mathrm{DS}}(\mathrm{ON})$ are available, which can handle very high currents. In some applications, where the primary-side current is extremely high, the high RMS current in the SPCD topology may significantly deteriorate the performance of the converter. Thus, for high-current applications, the proposed topology might not be an appropriate candidate.

IX. CONCLUSION

A SPCD full-bridge dc/dc converter topology has been presented in this paper. The proposed converter is able to provide soft-switching for the primary-side MOSFETs as well as lossless and smooth commutations for the output diodes. The required passive components used in this topology are mostly integrated into the main transformer. The integrated planar transformer includes the series inductance and the parallel inductance used in this topology. A thorough HFSS analysis has been performed on the integrated planar transformer used in this topology. The results of the HFSS analysis can precisely predict the values of the passive components and provides the design parameters of the integrated planar transformer. The particular structure of the converter makes it a good candidate for applications with a high switching frequency and a high output voltage. Also, this topology is able to offer high power density due to the use of

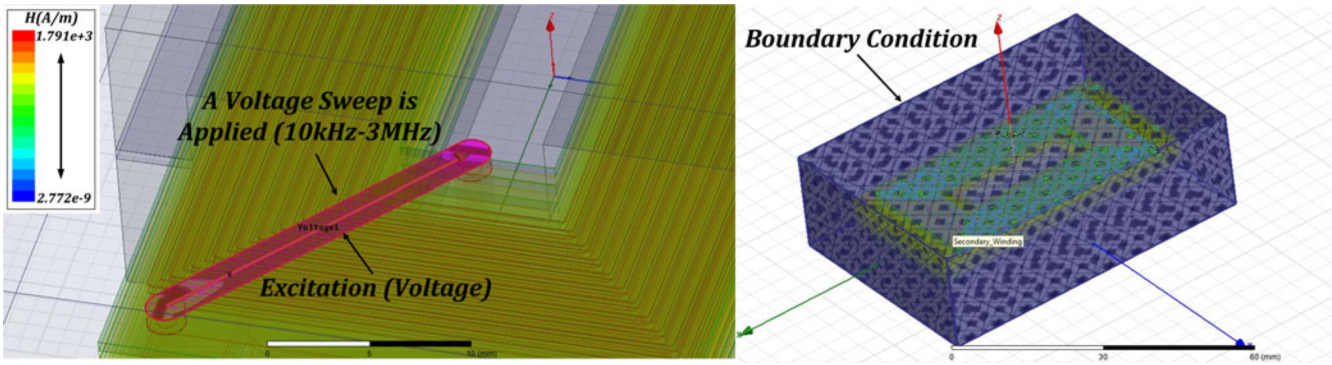

Fig. 33. Boundary condition and the field excitation in HFSS.

an integrated transformer in the converter and due to minimal extra components in the converter. Simulation and experimental results demonstrate the superior performance of the proposed SPCD full-bridge dc/dc converter.

APPENDIX
INTEGRATED MAGNETICS

An industry standard software used for finite-element analysis is ANSOFT high-frequency structure simulator (HFSS) from ANSYS Incorporation. The HFSS module uses an FEM solver to find the solution to the electric field and magnetic field equations given by

$$\nabla \times p\left(\frac{1}{\mu_r}\nabla \times \mathbf{E}\right) - k_0^2 \varepsilon_r \mathbf{E} = 0 \tag{36}$$

$$H = \frac{1}{\omega\mu}\nabla \times \mathbf{E} \tag{37}$$

where $\mu_r = \frac{\mu}{\mu_0}$, $\varepsilon_r = \frac{\varepsilon}{\varepsilon_0}$, $k_0^2 = \omega^2\varepsilon_0\mu_0 = \frac{\omega^2}{c^2}$.

The analysis in an HFSS starts with a precise 3-D structure of the integrated transformer. The structure is then subdivided into several smaller subsections called “finite elements.” This procedure is called “meshing” the structure. Then Maxwell’s equations are solved in each element such that the interelement boundary conditions are satisfied. Once the solution for the electric and magnetic fields are found, the S-matrix solution is generated for a very high frequency range as well as the lumped impedances for the lower frequency range [34], [35]. The HFSS provides precise information about the integrated transformer parameters. Also, HFSS offers adaptive analysis, which guarantees that the final results to a given FEM problem is very precise by refining the mesh iteratively.

The specifications of the integrated transformer used in this paper are shown in Table VI. It should be noted that the values of λ (air gap) and ξ (the distance between the primary and secondary windings) are derived from (22)–(23). These values are a good starting point for designing the structure for FEM analysis. After the solution is found, it is easy to make adjustments and find the precise values for λ and ξ based on the HFSS analysis. Fig. 30 shows the structure of the integrated transformer in HFSS and Fig. 31 shows how the primary and secondary windings are laid out in the top–bottom arrangement. Fig. 32 shows the primary and secondary windings implemented in the HFSS environment. The accurate modeling of vias and output terminals are illustrated in this figure.

There are three types of solutions, which produce different kinds of results in the HFSS. The following are the three types [36].

Driven Modal: The S-matrix is solved in terms of the incident and reflected powers of wave-guide modes.

Driven Terminal: The S-matrix is solved in terms of the terminal voltages and currents.

Eigenmode: The resonances of the simulated structure are determined.

In the present application, the “driven terminal” and “Eigenmode” solutions are of interest [36]. Before running the HFSS analysis, the boundary condition must be determined as well as the excitations. Fig. 33 shows the boundary condition as well as the field excitation for this simulation. The boundary condition is a perfect magnetic surface (e.g., $\vec{H} = 0$) surrounding the integrated planar transformer. The excitation is basically a type of boundary condition, which allows energy to go into and out of the structure. Excitations can be through “Wave Ports” or “Lumped Ports.” Lumped ports are useful for modeling the internal ports within the structure. Therefore, the ports are defined as a lumped port in the specified structure.

REFERENCES

[1] S. Fan, W. Ma, T. C. Lim, and B. W. Williams, “Design and control of a wind energy conversion system based on a resonant DC/DC converter,” *IET Renewable Power Generation* , vol. 7, no. 3, pp. 265–274, May 2013.

[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, “Power electronics as efficient interface in dispersed power generation systems,” *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[3] K. Sun, L. Zhang, Y. Xing, and J. M. Guerrero, “A distributed control strategy based on DC bus signaling for modular photovoltaic generation systems with battery energy storage,” *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 3032–3045, Oct. 2011.

[4] S. Dusmez and A. Khaligh, “Generalized technique of compensating low-frequency component of load current with parallel bidirectional DC/DC converter,” *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5892–5904, Nov. 2014.

[5] M. Pahlevaninezhad, J. Drobnik, P. K. Jain, and A. Bakhshai, “A load adaptive control approach for a zero-voltage-switching DC/DC converter used for electric vehicles,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 920–933, Feb. 2012.

[6] F. Liu, Z. Wang, Y. Mao, and X. Ruan, “Asymmetrical half-bridge double-input DC/DC converters adopting pulsating voltage source cells for low power applications,” *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4741–4751, Sep. 2014.

[7] M. Pahlevaninezhad, D. Hamza, and P. K. Jain, “An improved layout strategy for common-mode EMI suppression applicable to high-frequency planar transformers in high-power DC/DC converters used for electric vehicles,” *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1211–1228, Mar. 2014.

[8] M. Pahlevaninezhad, S. Eren, P. K. Jain, and A. Bakhshai, “Self-sustained oscillating control technique for current-driven full-bridge DC/DC converter,” *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5293–5310, Nov. 2013.

[9] Y. Ren, M. Xu, J. Sun, and F. C. Lee, “A family of high power density unregulated bus converters,” *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1045–1054, Sep. 2005.

[10] H. F. Xiao, X. P. Liu, and K. Lan, “Zero-voltage-transition full-bridge topologies for transformerless photovoltaic grid-connected inverter,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5393–5401, Oct. 2014.

[11] H. S. Ribeiro and B. Vieira Borges, “High-performance voltage-fed ACDC full-bridge single-stage power factor correctors with a reduced DC bus capacitor,” *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2680–2692, Jun. 2014.

[12] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, and K. Shiozaki, “A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[13] L. Roggia, L. Schuch, J. E. Baggio, C. Rech, and J. R. Pinheiro, “Integrated full-bridge-forward DC–DC converter for a residential microgrid application,” *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1728–1740, Apr. 2013.

[14] Z. Zhang, O. C. Thomsen, and M. A. E. Andersen, “Soft-switched dual-input DC–DC converter combining a boost-half-bridge cell and a voltage-fed full-bridge cell,” *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4897–4902, Nov. 2013.

[15] C. Tsang, M. Foster, D. Stone, and D. Gladwin, “Analysis and design of LLC resonant converters with capacitor-diode clamp current-limiting,” *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1345–1355, Mar. 2015.

[16] G. Yang, P. Dubus, and D. Sadarnac, “Double phase high efficiency, wide load range high voltage/low voltage LLC DC/DC converter for electric/hybrid vehicles,” *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1876–1886, Apr. 2015.

[17] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard, and S. R. Motahari, “Analysis and implementation of a fixed-frequency LCLC resonant converter with capacitive output filter,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4773–4782, Oct. 2011

[18] H. Chen, E. K. K. Sng, and K.-J. Tseng, “Generalized optimal trajectory control for closed loop control of series–parallel resonant converter,” *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1347–1355, Sep. 2006.

[19] J.-W. Kim, and G.-W. Moon, “A new LLC series resonant converter with a narrow switching frequency variation and reduced conduction losses,” *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4278–4287, Aug. 2014.

[20] M. Momeni, H. Meshgin-kelk, and H. Talebi, “Rotating switching surface control of series resonant converter based on piecewise affine model,” *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1762–1772, Mar. 2015.

[21] N. Shafiei, M. Pahlevaninezhad, H. Farzanehfard, A. Bakhshai, and P. Jain, “Analysis of a fifth-order resonant converter for high-voltage DC power supplies,” *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 85–100, Jan. 2013.

[22] N. Harischandrappa and A. K. S. Bhat, “A fixed-frequency LCL-type series resonant converter with capacitive output filter using a modified gating scheme,” *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 4056–4064, Nov./ Dec. 2014.

[23] I.-O. Lee and G.-W. Moon, “The *k*-Q analysis for an LLC series resonant converter,” *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 13–16, Jan. 2014.

[24] Jain, P. K., W. Kang, Soin, H., and Youhao Xi, “Analysis and design considerations of a load and line independent zero voltage switching full bridge DC/DC converter topology,” *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 649–657, Sep. 2002.

[25] J. A., Sabate, V. Vlatkovic, R. B. Ridley, and F. C. Lee, “High-voltage, high-power, ZVS, full-bridge PWM converter employing an active snubber,” in *Proc. 6th Annu. Appl. Power Electron. Conf. Expo.*, 10–15 Mar. 1991, pp. 158–163.

[26] E.-S. Kim, K.-Y. Joe, M.-H. Kye, Y.-H. Kim, and B.-D. Yoon, “An improved soft-switching PWM FB DC/DC converter for reducing conduction losses,” *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 258–264, Mar. 1999.

[27] E.-S. Kim and Y.-H. Kim, “A ZVZCS PWM FB DC/DC converter using a modified energy-recovery snubber,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1120–1127, Oct. 2002.

[28] A. Bendre, S. Norris, D. Divan, I. Wallace, and R. W. Gascoigne, “New high power DC-DC converter with loss limited switching and lossless secondary clamp,” *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 1020–1027, Jul. 2003.

[29] H. Cha, L. Chen, R. Ding, Q. Tang, and F. Z. Peng, “An alternative energy recovery clamp circuit for full-bridge PWM converters with wide ranges of input voltage,” *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2828–2837, Nov. 2008.

[30] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, “A novel ZVZCS full-bridge DC/DC converter used for electric vehicles,” *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2752–2769, Jun. 2012.

[31] Fairchild Semiconductor Corporation, “Half-bridge LLC resonant converter design using FSFR-series fairchild power switch”, Application Note AN-4151, 2007.

[32] H. Ding, “Design of Resonant Half-Bridge converter using IRS2795(1,2) Control IC,” Application Note AN-1160, 2012.

[33] A. A. Dauhajre, “Modeling and estimation of leakage phenomena in magnetic circuits,” Ph.D Thesis Dissertation, California Institute of Technology, Pasadena, CA, USA, 1986.

[34] J. DeLap, “3-D Design Flow Automation for HFSS” ANSYS, Inc., Canonsburg, PA, USA, Mar. 2014.

[35] L. Salman, “HFSS Solution Frequency Setup for Dual Band Antenna Design” ANSYS, Inc., Canonsburg, PA, USA, Dec. 2011.

[36] ANSYS, Inc., “Introduction to ANSYS HFSS”, Release 14.0, Feb. 2012.

[37] M. Hallworth and S. A. Shirsavar, “Microcontroller-based peak current mode control using digital slope compensation,” *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3340–3351, Jul. 2012.

[38] F. Tian, S. Kasemsan, and I. Batarseh, “An adaptive slope compensation for the single-stage inverter with peak current-mode control,” *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2857–2862, Oct. 2011.

[39] CYCLONE IV Device Handbook, Altera Corporation, San Jose, CA, USA, CYIV-53001-1.5, Vol. 3, Nov. 2011.

[40] P. Das, M. Pahlevaninezhad, J. Drobnik, G. Moschopoulos, and P. K. Jain, “A nonlinear controller based on a discrete energy function for an AC/DC boost PFC converter,” *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5458–5476, Dec. 2013.

[41] S. Eren, M. Pahlevani, A. Bakhshai, and P. Jain, “An adaptive droop DC-bus voltage controller for a grid-connected voltage source inverter with LCL filter,” *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 547–560, Feb. 2015.

[42] M. Mascioli, M. Pahlevaninezhad, and P. Jain, “FPGA-based implementation of an adaptive notch filter used for grid synchronization of grid-connected converters,” in *Proc. 39th Annual Conf. IEEE Ind. Electron. Soc.*, Nov. 10–13, 2013, pp. 7617–7622.

[43] M. Pahlevani, S. Pan, Eren, S., A. Bakhshai, and P. Jain, “An adaptive nonlinear current observer for boost PFC AC/DC converters,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6720–6729, Dec. 2014.

[44] C. Zhao, X. Wu, P. Meng, and Z. Qian, “Optimum design consideration and implementation of a novel synchronous rectified soft-switched phase-shift full-bridge converter for low-output-voltage high-output-current applications,” *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 388–397, Feb. 2009.

[45] C. W. Tsang, M. P. Foster, D. A. Stone, and D. T. Gladwin, “Analysis and design of LLC resonant converters with capacitordiode clamp current limiting,” *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1345–1355, Mar. 2015.

[46] N. Sukesh, M. Pahlevaninezhad, and P. K. Jain, “Analysis and implementation of a single-stage flyback PV microinverter with soft switching,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1819–1833, Apr. 2014.

[47] M. Pahlevaninezhad, D. Hamza, and P. K. Jain, “An improved layout strategy for common-mode EMI suppression applicable to high-frequency planar transformers in high-power DC/DC converters used for electric vehicles,” *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1211–1228, Mar. 2014.

[48] M. Pahlevaninezhad, A. Safaee, S. Eren, A. Bakhshai, and P. Jain, “Adaptive nonlinear maximum power point tracker for a WECS based on permanent magnet synchronous generator fed by a matrix converter,” *Energy Convers. Congr. Expo.*, Sep. 20–24, 2009, pp. 2578–2583.

[49] D. Moon, J. Park, and S. Choi, “New interleaved current-fed resonant converter with significantly reduced high current side output filter for EV and HEV applications,” *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4264–4271, Aug. 2015.

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