A New Multiinput Three-Level DC/DC Converter

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***Abstract*—Power electronics solutions based on multiple converter configurations offer cost-effective solutions by integrating a number of components at input or output power stages. This paper proposes a new multiinput isolated three-level converter for renewable and sustainable energy systems adopting high dc link voltage. Multiple dc sources are integrated to the three-level dc/dc converter before the isolation stage, resulting in reduced part-count, determining dc link voltage level and allowing flexibility in transformer design. The proposed architecture eliminates two boost switches which are present in the two-stage counterpart. The input inductors are operated in discontinuous conduction mode; thus, power can be shared between input sources through proper selection of input inductors. A low voltage prototype has been designed to serve as a proof of concept.**

***Index Terms*—DC/DC converter, multiinput converter, pulsating current cell, renewable energies, three-level converter.**

I. Introduction

MULTIINPUT converters offer a cost effective solution in applications which requires multiple input sources such as fuel cell vehicles and renewable energy systems [1]–[12]. The basic idea is to integrate a number of converters in either input dc/dc conversion stage or in isolation stage, in addition to commonly shared output stage. There are various multiinput topologies proposed in the literature based on nonisolated [13]–[18] and isolated structures [19]–[22]. In [13], a nonisolated multiinput buck/boost converter sharing the same switch has been proposed. A similar concept has been applied to four-switch bidirectional buck boost converter, where input sources are connected in parallel [14]. Each input source is interfaced with an individual buck switch, and the remaining three switches are shared by the input sources. In [15], two boost converters are connected in series and an auxiliary circuit is used to achieve soft-switching. A general derivation for nonisolated parallel-integrated multiinput converters including SEPIC and Cuk has been reported in [16]. In [17], a different approach based on switched capacitor converter has been reported.

For multiinput converters providing galvanic isolation, majority of the work has been devoted to phase-shifted full-bridge converters. In [19], two identical current fed full-bridge converters are connected in parallel to interface a common output rectifying diode-bridge. Similar concept has been applied using individual output rectification stages but sharing an integrated transformer in [20]. In [21], two current fed bridges are controlled in a phase-shifted manner. In [22], the parallel connection of multiinput cells are first identified as pulsating voltage-source cell and pulsating current-source cell, and various topological combinations have been presented. However, majority of the isolated multiinput converters presented in the literature are proposed as individual converters or shares only the output stage on the secondary side of the transformer. In [23], the concept of paralleling multiple input sources at the primary side of the transformer has been proposed.

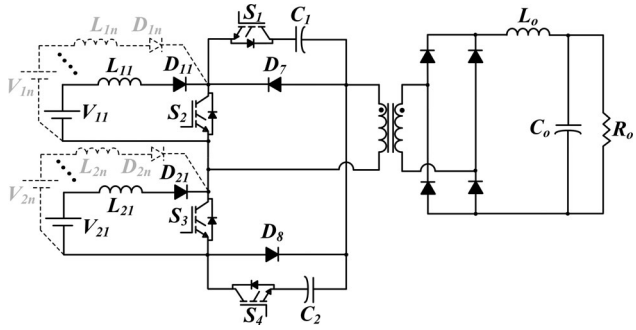

Fig. 1. Proposed multiinput isolated three-level dc/dc converter.

In this study, a new multiinput converter based on three-level structure for renewable energy systems is proposed, as shown in Fig. 1. Following the concept proposed in [23], pulsating current-source (PCC) cells are integrated to the same bridge before the isolation stage, while the adopted bridge offers utilizing low voltage rated upper and lower switches due to the three-level structure. The control of PCCs is integrated to the operation of the three-level bridge converter. Thus, the control complexity of the proposed converter is similar to that of a three-level dc/dc converter [24]. On the other hand, the proposed converter provides reduced part-count and lower voltage stress across the upper and lower switches. The input inductors are operated in discontinuous conducting mode (DCM), which allows autonomous power sharing between input sources with proper selection of input inductors.

This manuscript is organized as follows: Section II introduces the new multiinput three-level integrated dc/dc converter and explains the operation modes in detail. In Section III, the dynamics of converter is extracted, design procedure is explained and a design example for variable input sources is given. The simulation and experimental results for a low-voltage prototype are presented in Section IV. Finally, the study is summarized and conclusion is derived in Section V.

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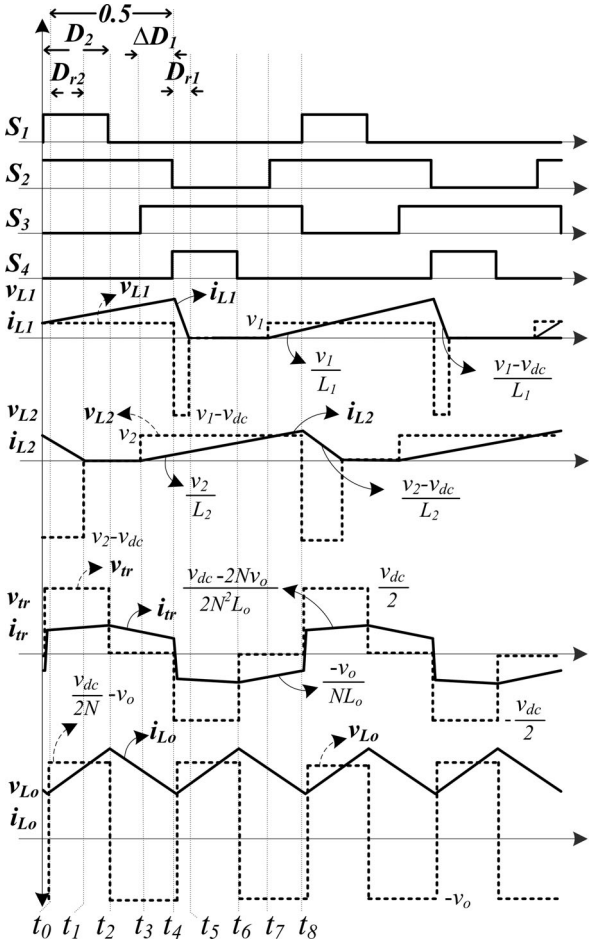

Fig. 2. Gating scheme and key waveforms.

II. Proposed Multiinput Isolated Three-Level DC/DC Converter

A. Topology Description

The proposed multiinput converter is essentially based on the operation of the three-level isolated dc/dc converter. The secondary side rectifier can be either a half-bridge rectifier accompanied by a tapped winding for low output voltage application, or a full-bridge rectifier for high output voltage applications as shown in Fig. 1. Since the PWM scheme here is similar to that in three-level converters, the control complexity is not intensive. The boost inductors, connected to the input sources of different voltages, are charged when S_2 and S_3 are turned on, respectively. When the related switch (S_2 or S_3) is turned off, the energy stored in the inductor is transferred to the load. The excess or insufficient energy is either absorbed or compensated by the dc link capacitors. At the same time, S_1 to S_4 are switched to apply $V_{\rm dc}/2, -V_{\rm dc}/2$, and zero voltage across the primary side of the transformer. In comparison with the two-stage counterpart, two active switches and boost diodes are eliminated, while two blocking diodes are added to block the reverse current from the dc link capacitors.

The switching scheme of the converter is given in Fig. 2. The switches S_2–S_3 and S_1–S_4 have 180° phase shift with respect to each other. The duty cycle of the middle switches should be greater than 50% such that they allow a freewheeling path for the transformer primary side current. The switching scheme is as follows: S_1 is turned on right after S_3 is turned off, and similarly, S_4 is turned on when S_2 is turned off. A dead-time should be inserted in between the turning on instant of S_1 and turning off instant of S_3, and likewise between switching of S_2 and S_4 to avoid short circuit.

B. Operation Principle

The operation modes of the circuits, which are given in Fig. 3, are explained in this section. It should be noted that these operation modes are valid when $i_{L2} > i_{L1.}$ For this case, $i_{L2,pk}$ is higher than primary side of the transformer at steady state. Under this condition, $i_{L1,pk}$ is smaller than primary side of the transformer at steady state. If $i_{L1} > i_{L2}$, the equivalent circuits would be different from the one presented here. Basically, the charging/discharging current of C_1 and C_2 would be exhanged.

Interval 1 [$t < t_0$]: Before t_0, S_3 is off and S_1 is on. The energy stored in L_2 is released to the load through the primary winding of the transformer. The excess energy is transferred to C_1 through conducting the body diode of S_1. Thus, S_1 can be turned on under zero voltage with proper time delay. The current of L_1 increases linearly under V_1. Total current of L_2 charges C_2. Meanwhile, $-V_{\rm dc}/2$ is applied to the primary side of the transformer

$$\mathrm{d}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_{Lo}(t) \\ v_{Co}(t) \end{bmatrix}/\mathrm{d}t = \begin{bmatrix} V_1/L_1 \\ (V_2 - v_{C1}(t) - v_{C2}(t))/L_2 \\ i_{L_2}(t)/C_1 - N i_{Lo}(t)/C_1 \\ i_{L_2}(t)/C_2 \\ v_{C1}(t)/NL_o - v_{Co}(t)/L_o \\ i_{Lo}(t)/C_o - v_{Co}(t)/C_o R_o \end{bmatrix}. \quad (1)$$

Interval 2 [$t_0 < t < t_1$]: At $t = t_0$, the current of L_1 becomes equal to that of primary side of the transformer. From this moment on, C_1 discharges over the primary side of the transformer to the load. The current of C_2 is equal to that of L_2. The state equations are same as in (1).

Interval 3 [$t_1 < t < t_2$]: At $t = t_1$, the currents of L_2 and C_2 reach to zero. The load current is solely supplied by C_1. The current of L_1 continues to store energy under the influence of V_1

$$\mathrm{d}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_{Lo}(t) \\ v_{Co}(t) \end{bmatrix}/\mathrm{d}t = \begin{bmatrix} V_1/L_1 \\ 0 \\ -N i_{Lo}(t)/C_1 \\ 0 \\ v_{C1}(t)/NL_o - v_{Co}(t)/L_o \\ i_{Lo}(t)/C_o - v_{Co}(t)/C_o R_o \end{bmatrix}. \quad (2)$$

Interval 4 [$t_2 < t < t_3$]: In the beginning of this interval, S_1 is turned off. The current in the leakage inductance conducts D_7 and the primary side current freewheels, hence, zero voltage is

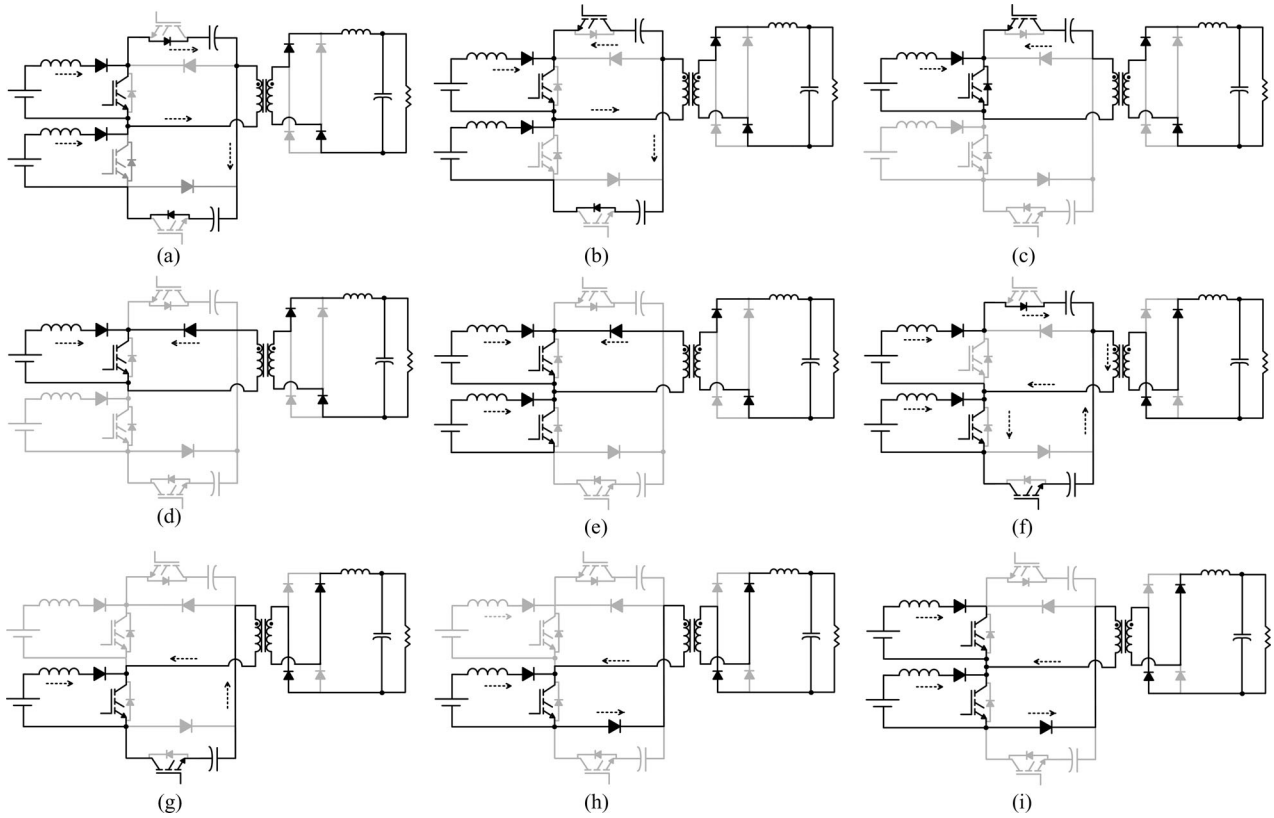

Fig. 3. Operation intervals of the converter. (a) Interval 1: $t < t_0$. (b) Interval 2: $t_0 < t < t_1$. (c) Interval 3: $t_1 < t < t_2$. (d) Interval 4: $t_2 < t < t_3$. (e) Interval 5: $t_3 < t < t_4$. (f) Interval 6: $t_4 < t < t_5$. (g) Interval 7: $t_5 < t < t_6$. (h) Interval 8: $t_6 < t < t_7$. (i) Interval 9: $t_7 < t < t_8$.

applied across the primary side of the transformer. The output inductor voltage is equal to $-V_o$ and the output inductor current decreases linearly

$$\mathrm{d}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_{Lo}(t) \\ v_{Co}(t) \end{bmatrix} /\mathrm{d}t = \begin{bmatrix} V_1/L_1 \\ 0 \\ 0 \\ 0 \\ -v_{Co}(t)/L_o \\ i_{Lo}(t)/C_o - v_{Co}(t)/C_oR_o \end{bmatrix}. \quad (3)$$

Interval 5 [$t_3 < t < t_4$]: At $t = t_3$, S_3 is turned on, while S_2 is kept on. The primary side current continues to freewheel and zero voltage is applied across the primary side; hence, the output inductor current continuous to decrease under output voltage. Meantime, V_2 is applied across L_2, and current increases linearly storing energy in L_2

$$\mathrm{d}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_{Lo}(t) \\ v_{Co}(t) \end{bmatrix} /\mathrm{d}t = \begin{bmatrix} V_1/L_1 \\ V_2/L_2 \\ 0 \\ 0 \\ -v_{Co}(t)/L_o \\ i_{Lo}(t)/C_o - v_{Co}(t)/C_oR_o \end{bmatrix}. \quad (4)$$

Interval 6 [$t_4 < t < t_5$]: At $t = t_4, S_2$ is turned off. The stored energy in L_1 is released to the load as well as to C_1. As stated before, peak current of L_1 is smaller than the load current for this case. Thus, C_2 discharges over to the load and $V_{\mathrm{dc}}/2$ is applied across the primary side of the transformer. The current of L_2 continues to store energy under the influence of V_2

$$\mathrm{d}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_{Lo}(t) \\ v_{Co}(t) \end{bmatrix} /\mathrm{d}t = \begin{bmatrix} (V_1 - v_{C1}(t) - v_{C2}(t))/L_1 \\ V_2/L_2 \\ i_{L_1}(t)/C_1 \\ i_{L_1}(t)/C_2 - Ni_{Lo}(t)/C_2 \\ v_{C2}(t)/NL_o - v_{Co}(t)/L_o \\ i_{Lo}(t)/C_o - v_{Co}(t)/C_oR_o \end{bmatrix}. \quad (5)$$

Interval 7 [$t_5 < t < t_6$]: At $t = t_5$, the energy stored in L_1 is completely transferred out. Its current reaches to zero at DCM. The load current is solely supplied by C_2

$$\mathrm{d}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_{Lo}(t) \\ v_{Co}(t) \end{bmatrix} /\mathrm{d}t = \begin{bmatrix} 0 \\ V_2/L_2 \\ 0 \\ -Ni_{Lo}(t)/C_2 \\ v_{C2}(t)/NL_o - v_{Co}(t)/L_o \\ i_{Lo}(t)/C_o - v_{Co}(t)/C_oR_o \end{bmatrix}. \quad (6)$$

Interval 8 [$t_6 < t < t_7$]: In this interval, S_4 is turned off. The current in the leakage inductance conducts D_8 and the primary side current freewheels, hence, zero voltage is applied across the primary side of the transformer. The current of L_2 continues to increase

$$\mathrm{d}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_{Lo}(t) \\ v_{Co}(t) \end{bmatrix}/\mathrm{d}t = \begin{bmatrix} 0 \\ V_2/L_2 \\ 0 \\ 0 \\ -v_{Co}(t)/L_o \\ i_{Lo}(t)/C_o - v_{Co}(t)/C_oR_o \end{bmatrix}. \quad (7)$$

Interval 9 [$t_7 < t < t_8$]: At $t = t_7, S_2$ is turned on while S_3 remains at on-state. The primary side current continues to circulate through D_8. The current of both inductors L_1 and L_2 increase linearly under the applied input voltages

$$\mathrm{d}\begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}\ (t) \\ i_{Lo}(t) \\ v_{Co}(t) \end{bmatrix}/\mathrm{d}t = \begin{bmatrix} V_1/L_1 \\ V_2/L_2 \\ 0 \\ 0 \\ -v_{Co}(t)/L_o \\ i_{Lo}(t)/C_o - v_{Co}(t)/C_oR_o \end{bmatrix}. \quad (8)$$

III. Analysis of the Proposed Converter

A. Averaged State-Variables

In order to obtain the averaged values for state variables, the expressions for state variables given in (1) to (8) are averaged over the given time intervals. The input inductor current can be averaged over the switching period as

$$\mathrm{d}\bar{i}_{L1}/\mathrm{d}t = \frac{V_1}{L_1}d_1 + \frac{V_1 - \bar{v}_{C1} - \bar{v}_{C2}}{L_1}d_{r1} \quad (9)$$

where d_{r1} denotes the duty ratio of the time interval in which inductor current decreases from its peak value to zero, when the boost switch is turned off. d_{r1} is a function of state variables; however it is yet neither a state nor a control variable. To substitute d_{r1} with state variables, one can use voltage-balance law of inductor. When the boost switch is turned on, the peak inductor current becomes

$$i_{L1,pk} = \frac{V_1}{L_1}d_1T_s. \quad (10)$$

When the boost switch is turned off, it becomes

$$i_{L1,pk} = \frac{V_1 - \bar{v}_{C1} - \bar{v}_{C2}}{L_1}d_{r1}T_s. \quad (11)$$

Equalizing (10) and (11), and solving it for d_{r1} yields

$$d_{r1} = \frac{V_1}{V_1 - \bar{v}_{C1} - \bar{v}_{C2}}d_1. \quad (12)$$

This conversion expresses d_{r1} in terms of control variable, d_1 and state variables v_{C1} and v_{C2}. Substituting (12) into (9) results in $d_{iL1}/dt = 0$; thus losing the dynamic inductor current information, which can be referred as reduced order modeling. In order to obtain a full order model, the average inductor current expression can be used for finding out d_{r1}

$$\bar{i}_{L1} = \frac{i_{L1,pk}}{2}(d_1 + d_{r1}). \quad (13)$$

By substituting (11) into (13), an expression which relates d_{r1} with d_1 and i_{L1} can be derived

$$d_{r1} = \frac{2\bar{i}_{L1}L_1}{V_1d_1T_s} - d_1. \quad (14)$$

The averaged inductor currents over the switching period can be found by inserting (14) into (9) as

$$\mathrm{d}\bar{i}_{L1}/\mathrm{d}t = \frac{\bar{v}_{C1} + \bar{v}_{C2}}{L_1}d_1 + \frac{2\bar{i}_{L1}}{d_1T_s}\frac{V_1 - \bar{v}_{C1} - \bar{v}_{C2}}{V_1} \quad (15)$$

$$\mathrm{d}\bar{i}_{L2}/\mathrm{d}t = \frac{\bar{v}_{C1} + \bar{v}_{C2}}{L_2}d_1 + \frac{2\bar{i}_{L2}}{d_1T_s}\frac{V_2 - \bar{v}_{C1} - \bar{v}_{C2}}{V_2}. \quad (16)$$

By using the same conversion and principle, the averaged expressions for the state variables of dc link capacitor voltages, output inductor and voltage can be found analogously. These state-equations are of paramount significance in analyzing the dynamic behavior of the converter as well as in designing the controller

$$\mathrm{d}\bar{v}_{C1}/\mathrm{d}t = \frac{\bar{i}_{L1} + \bar{i}_{L2}}{C_1} - \frac{d_1^2T_s}{2C_1}\left(\frac{V_2}{L_2} + \frac{V_1}{L_1}\right) - d_2\frac{N\bar{i}_{Lo}}{C_1} \quad (17)$$

$$\mathrm{d}\bar{v}_{C2}/\mathrm{d}t = \frac{\bar{i}_{L1} + \bar{i}_{L2}}{C_2} - \frac{d_1^2T_s}{2C_2}\left(\frac{V_2}{L_2} + \frac{V_1}{L_1}\right) - d_2\frac{N\bar{i}_{Lo}}{C_2} \quad (18)$$

$$\mathrm{d}\bar{i}_{Lo}/\mathrm{d}t = \frac{\bar{v}_{C1} + \bar{v}_{C2}}{NL_o}d_2 - \frac{\bar{v}_{Co}}{L_o} \quad (19)$$

$$\mathrm{d}\bar{v}_{Co}/\mathrm{d}t = \frac{\bar{i}_{Lo}}{C_o} - \frac{\bar{v}_{Co}}{C_oR_o}. \quad (20)$$

B. Design Considerations

As denoted in Section II, the minimum duty ratio of the middle two switches, D_1, should be at least 50%, in order to apply zero voltage to the primary side of the transformer. The remaining 50% is shared between the duty ratios of S_1 and S_4, denoted by D_2, and control signal of S_2 and S_3, denoted by ΔD_1. This leaves a margin for the control of duty ratios of S_2 and S_3

$$D_1 = 0.5 + \Delta D_1 \quad (21)$$

where

$$\Delta D_1 = 0.5 - D_{2,\max}. \quad (22)$$

1) Determination of $L_o, D_2, \Delta D_1$: The load side of the converter can be designed to operate in either CCM or DCM mode. The output inductor current can be continuous or discontinuous depending on the design criteria, or else it might be designed such that the operation of the converter can transit to DCM at light load condition to reduce the size of the output inductor. The required output inductance value can be determined by (23)

$$L_o \geq \frac{V_o^2(0.5 - D_{\min})}{2P_xf_s} \quad (23)$$

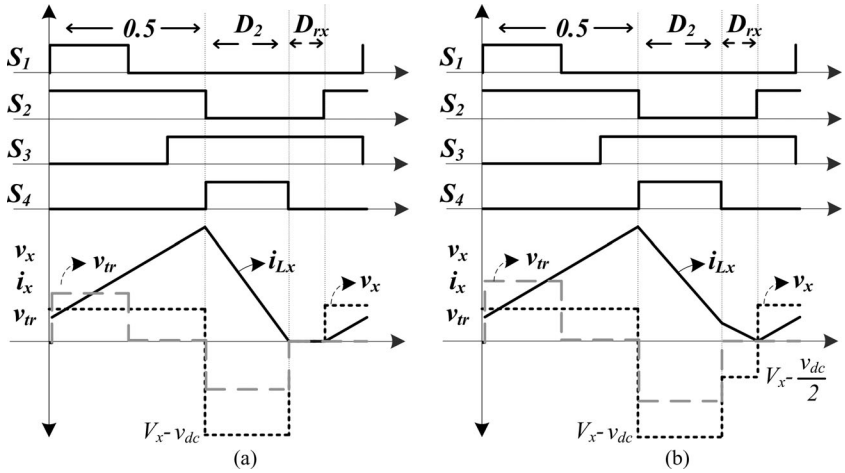

Fig. 4. DCM/CCM boundary cases. (a) Input inductor current reaches to zero within D_2T_s. (b) Input inductor current reaches to zero within $(D_2 + D_{rx})T_s$.

where P_x represents the minimum output power at which the converter is desired to be operated in CCM. When output inductor operates in CCM mode, D_2 can be expressed as in (24) at steady state

$$D_{2,\max} = \frac{NV_o}{V_{\mathrm{dc,min}}} \tag{24}$$

where *N* represents the turns ratio of the transformer windings. The equivalent duty ratio for DCM mode can be written as

$$D_2 = \sqrt{\frac{2L_o}{\mathrm{RT}_s\left(\left(\frac{V_{\mathrm{dc}}}{NV_o}-1\right)^2-1\right)}}. \tag{25}$$

Depending on the operation mode, *N* can be found from either (24) or (25). Once $D_{2,\max}$ and $V_{\mathrm{dc,min}}$ are determined, D_1 and the limits for ΔD_1 can be found using (21) and (22).

2) Determination of DCM Boundary and DC Link Voltage: In this paper, the operation principle is based on operating input inductors in DCM. This is due to the fact that input sources are controlled by D_1 and their voltages can be different, only one of the cells would be able to operate in CCM, while the other one would continue operating in DCM. Once one of the input sources transits to CCM, the continuous current forces to apply $-V_{\mathrm{dc}}$ to the other input, which keeps the voltage of latter at the same level; hence, latter continues to provide same amount of power in DCM mode. The rest of the necessary power is supplied from the input source operating in CCM. This operation could be considered for applications where output power of one of the input sources is maximized to definite value, while the secondary input source provides rest of the load power demand.

The operation modes shown in Fig. 3 has been given considering that the input inductors are well chosen for DCM operation under any load, and input inductor currents reach to zero within D_2T_s. In case this interval lasts longer depending on the chosen parameters and output power, there could be one more operation mode, which was not shown in Fig. 3. It is yet necessary to analyze this operation mode in order to define the CCM/DCM boundary. In such a circumstance, after the operation interval 7, the upper inductor would still continue to provide energy to the upper capacitor even after S_4 is turned off under the influence of $V_{\mathrm{dc}}/2$. The voltage of the primary side of the transformer remains at zero since D_8 conducts. Relevant waveforms are illustrated in Fig. 4.

To find the boundary operation point, one should consider that the inductor current reaches to zero at the end of the switching period. The critical dc link voltage can be found through the expression of the voltage balance equality of the inductor, as

$$V_xD_1 = (V_{\mathrm{dc,crt}} - V_x)\,D_2 + \left(\frac{V_{\mathrm{dc,crt}}}{2} - V_x\right)(1 - D_1 - D_2) \tag{26}$$

where V_x denote the voltage of the input source that provides higher output power. The lowest dc link voltage that should be adopted for DCM operation can be expressed as

$$V_{\mathrm{dc,crt}} = \frac{2V_x}{D_2 - D_1 + 1}. \tag{27}$$

For DCM operation, the following condition should be satisfied: $V_{\mathrm{dc,min}} > V_{\mathrm{dc,crt}}$.

3) Determination of L_1 and L_2: In this paper, the operation principle is based on operating input inductors in DCM. For the proposed converter, the duty ratios of S_2 and S_3 are the same, and equal to D_1. Hence, the output power of each cell is proportional to the square of its input voltage, and inversely proportional to the inductance. The total power fed by the input sources can be expressed as

$$P_o = \eta\frac{V_{\mathrm{dc}}D_1^2T_s}{2}\sum_1^n\frac{V_n^2}{L_n\left(V_{\mathrm{dc}} - V_n\right)}. \tag{28}$$

Thus, with proper design of these parameters with respect to behaviors of input source, an autonomous power sharing is possible. Based on (28), there are various possibilities to determine *L*. The bottom boundaries for L_n based on $V_{\mathrm{n,min}}$ and output power are defined as

$$P_{\max} \le \eta\frac{V_{\mathrm{dc}}D_{1,\max}^2T_s}{2}\sum_1^n\frac{V_{n,\min}^2}{L_n\left(V_{\mathrm{dc}} - V_{n,\min}\right)}. \tag{29}$$

The values of the inductances can be determined for rated power, which would fall into the boundary defined above. The

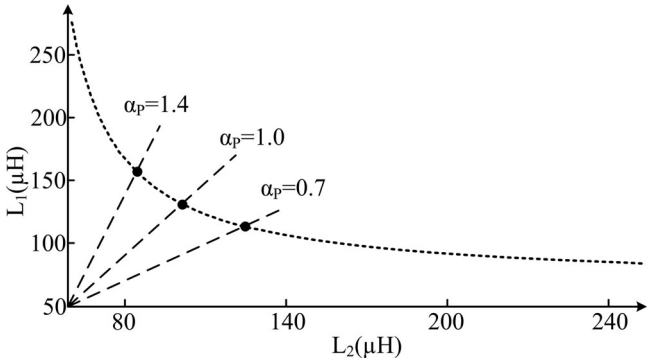

Fig. 5. Inductance determination based on power sharing when $V_1 = V_{1,\min}, V_2 = V_{2,\min}$.

determination of inductances depends on the application needs. For instance, for PV generation systems, the inductances can be calculated according to the desired load sharing at the maximum power operation point.

C. Design Example

The design procedure for constant power loads with constant input voltage sources is straightforward. Thus, this section illustrates a design procedure for an application with dynamic variables having the parameters of $V_{1,\min} = 110$ V, $V_{1,\max} = 130$ V, $V_{2,\min} = 100$ V, $V_{2,\max} = 150$ V, $V_o = 200$ V, $P_{\text{tot,max}} = 1.2$ kW, $f_s = 50$ kHz. In typical bridge-type isolated converters, the duty ratio of the second stage, D_2, is between 0.48 and 0.25. Since there is a limitation on the duty cycles in the proposed converter, as stated in (21) and (22), $D_{1,\max}$ can be set to 0.7, where ΔD_1 becomes 0.2. In this case, $D_{2,\max}$ is equal to 0.3. Using (27), the critical dc link voltage, $V_{\text{dc,crt}}$, is calculated as 500 V; thus, $V_{\text{dc,min}}$ is determined as 500 V. From (24), transformer turns ratio is calculated as 0.75.

Based on the condition given in (29), all possible L_1 and L_2 combinations can be found. Another criterion in determining the inductances is the power ratio among the input sources at desired input voltages. For this design, the power ratio of the second input source to the first input source at maximum output power and minimum input voltages, denoted as α_P, is evaluated. Based on the chosen α_P, the values of the inductances can be determined as shown in Fig. 5. In this study, α_P is determined as 0.7, which means that the second source provides 500 W and the first source provides 700 W under maximum load when $V_1 = V_{1,\min}$, and $V_2 = V_{2,\min}$. The corresponding L_1 and L_2 values, are selected from Fig. 5; $L_1 = 108$ μH, $L_2 = 122$ μH.

The output power capability of the first and second input sources according to D_1 and their respected voltages are plotted in Figs. 6 and 7, respectively. As it can be seen from the figures, the first input source provides 700 W, while the second one provides 500 W to fulfill the load demand at their respected minimum input voltages. On the other hand, the power ratio becomes 1.23 when the voltages of the input sources reach to highest values. The selection of the power ratio is completely dependent on the application needs, and it can be modified analogously. The total power supplied from the input sources as a function of duty ratio and dc link voltages for $V_1 = V_{1,\min}$, and $V_2 = V_{2,\min}$ is plotted in Fig. 8. As expected, higher dc link voltage results in lower output power for the same output voltage. This figure is of significant importance to evaluate the converter's output power capability at different dc link voltages. As it can be seen, the total power drawn from the

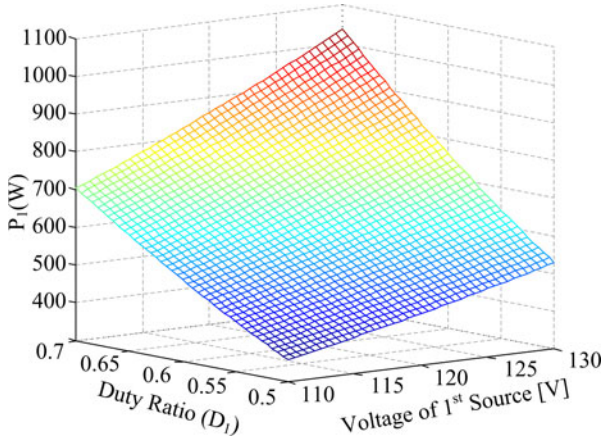

Fig. 6. Power can be drawn from the first input source at $V_{\text{dc}} = 500$ V under DCM mode.

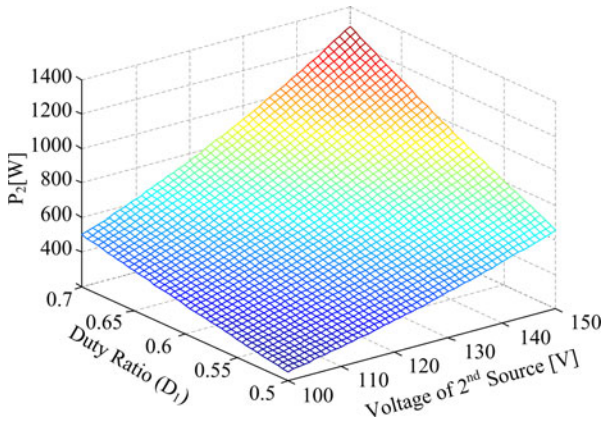

Fig. 7. Power can be drawn from the second input source at $V_{\text{dc}} = 500$ V under DCM mode.

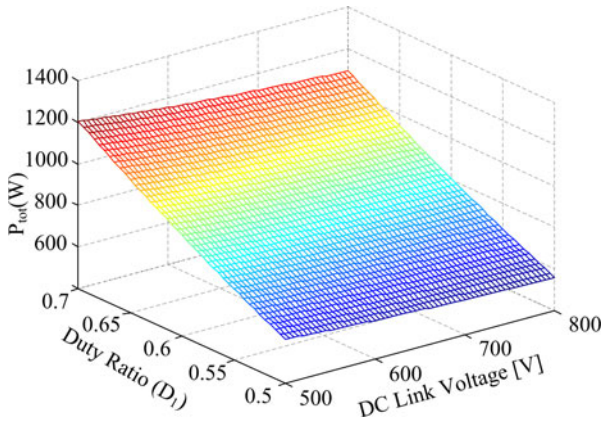

Fig. 8. Power can be drawn from both input sources at various dc link voltages when $V_1 = V_{1,\min}, V_2 = V_{2,\min}$.

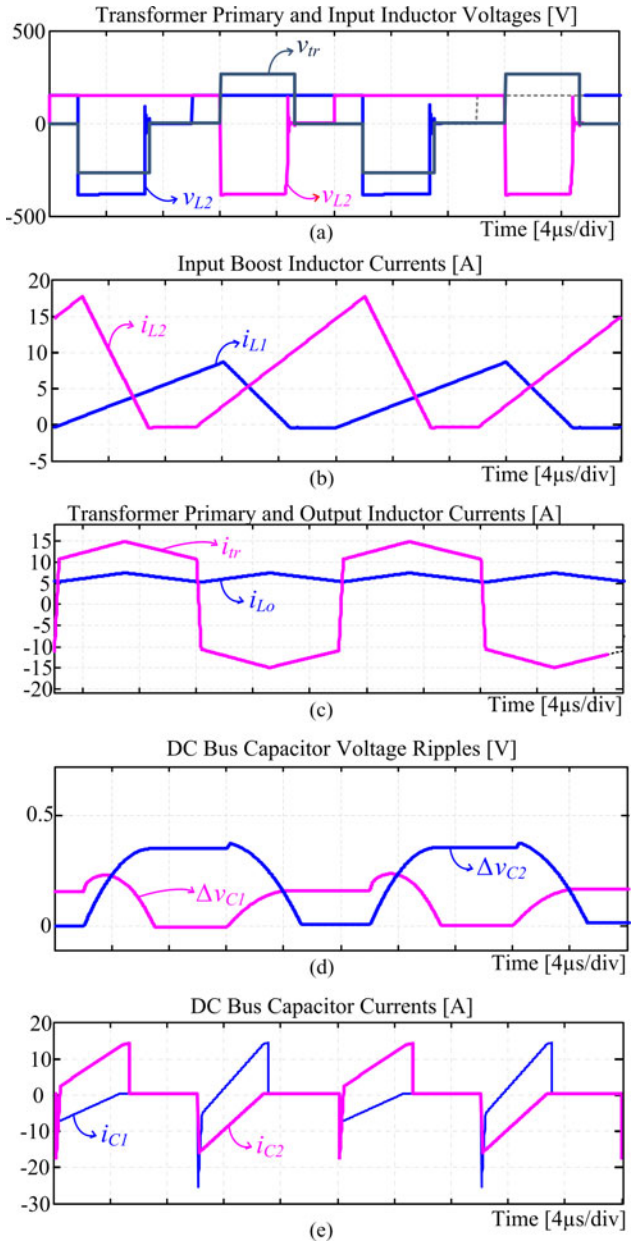

Fig. 9. Simulation waveforms when $V_1 = V_2 = 150$ V, $L_1 = 200$ μH, $L_2 = 100$ μH. (a) Transformer's primary winding voltage, and input inductor voltages. (b) Input boost inductor currents. (c) Transformer's primary winding current and output inductor current. (d) Dc bus capacitor voltage ripples. (e) Dc bus capacitor currents.

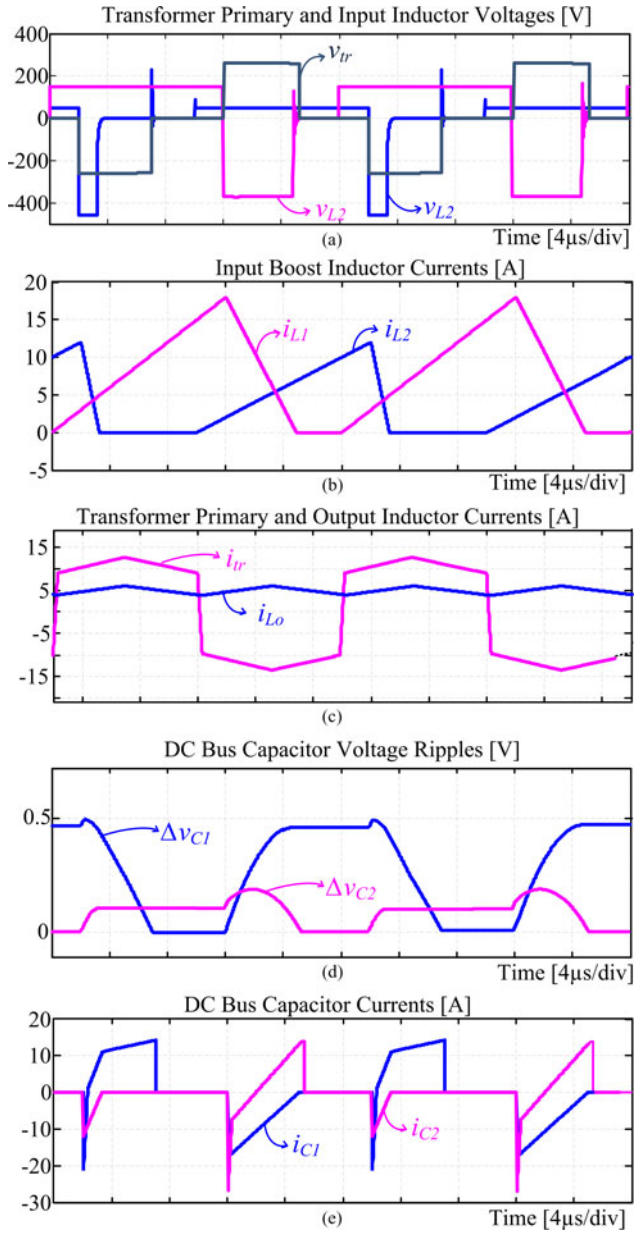

Fig. 10. Simulation waveforms when $V_1 = 150$ V, $V_2 = 50$ V, $L_1 = L_2 = 100$ μH. (a) Transformer's primary winding voltage, and input inductor voltages. (b) Input boost inductor currents. (c) Dc bus capacitor voltage ripples. (d) Dc bus capacitor currents.

input sources can be adjusted for the given reference dc link voltage.

It should be noted that this part only illustrated a design framework for DCM operation; however, as stated earlier, one of the input sources can transit to CCM mode and supply the rest of the demand power, which can be preferred in fuel cell applications. Another point is that advantages of the proposed converter become more apparent when input voltages and dc link voltages are higher. The voltage specifications given for this design procedure and simulation results given in the following section are determined rather low to be suitable with the designed low voltage proof-of-concept prototype.

IV. Simulation and Experimental Results

The simulations are performed to illustrate the operation of the converter with different set of parameters in MATLAB using SimPower Toolbox. The first simulation is conducted for same input voltage and different inductances, while the second one aims to illustrate the operation when inductances are the same with different voltages. The first set of parameters as follows: $V_1 = V_2 = 150$ V, $L_1 = 200$ μH, $L_2 = 100$ μH, $C_1 = C_2 = 100\mu$F, $L_o = 330$ μH, $f_{sw} = 50$ kHz. The results are shown in Fig. 9. The second set of parameters

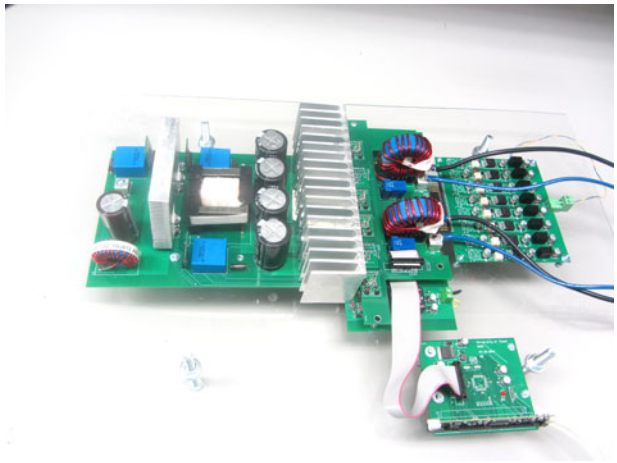

Fig. 11. Photo of the designed prototype.

are: $V_1 = 150$ V, $V_2 = 50$ V, $L_1 = L_2 = 100$ μH, $C_1 = C_2 = 100$ μF, $L_o = 330$ μH, $f_{sw} = 50$ kHz.

In Fig. 9(a), it can be observed that even though same voltage is applied to the inductors, the output power contribution is different due to the chosen different inductances. For this case, the output power is 1.6 kW and $i_{L2,pk} > i_{L1,pk}$. The charging/discharging current of C_2 is higher than that of C_1, resulting in asymmetrical voltage ripples across two dc bus capacitors.

The corresponding results for latter simulation are given in Fig. 10. As it can be seen from Fig. 10(a), the applied voltages are different while the chosen inductances are same. For this case, $i_{L1,pk} > i_{L2,pk}$ and the capacitor charging currents and thereby the capacitor voltage ripples are replaced. It is worth mentioning that the feedback voltage signal should be averaged over the switching period for capacitor voltage balancing.

Due to the asymmetry of the voltage source, the capacitor currents are different, resulting in different capacitor voltage ripples. Like in any other multilevel converter, the capacitor voltages should be balanced. For the proposed converter, this can be achieved by adding a compensating signal to the duty ratio of S_1 and S_4, which either extends or shortens its effective duty ratio.

A low voltage laboratory built prototype has been designed and tested, as shown in Fig. 11, to serve as a proof-of-concept. The input inductances ($L_1 = L_2$) are 87 μH each, dc link capacitances ($C_1 = C_2$) are 470 μF each. The output capacitor (C_o) is 220 μF and output inductor (L_o) is 200 μH. The secondary side of the transformer has a tapped winding configuration followed by a half-bridge rectifier. The transformer has 1:1 turns ratio for each secondary winding. The ratings of the switches are 600 V/22 A. The switching frequency is 50 kHz. The pulse pattern is generated using Texas Instrument's floating point DSP.

The tests are conducted for two different duty cycles. The experimental results are verified with simulation results under the same operation conditions. Fig. 12 portrays the switching pattern when $D_1 = 0.6$ and $D_2 = 0.35$. It should be noted that the inverse of the gating signals are shown here due to the hardware configuration. The experimental and simulation results for $V_1 = 70$ V and $V_2 = 90$ V are shown in Figs. 13 and 14, respectively. The peak current of the first inductor is 9.5 A, whereas the peak of the second inductor is 12.5 A. In this case, the power ratio of the second source to the first one is 1.8. The output voltage and current are around 75 V, and 9.2 A, respectively, as shown in Fig. 15. On the other hand, the output voltage is little higher in the simulation due to ideal and lossless components as well as the precise transformer ratio, as it can be seen from Fig. 16.

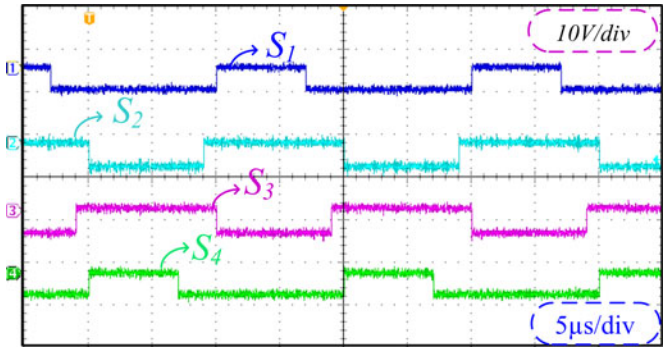

Fig. 12. Experimental waveforms of gate signals when $D_1 = 0.6, D_2 = 0.35$.

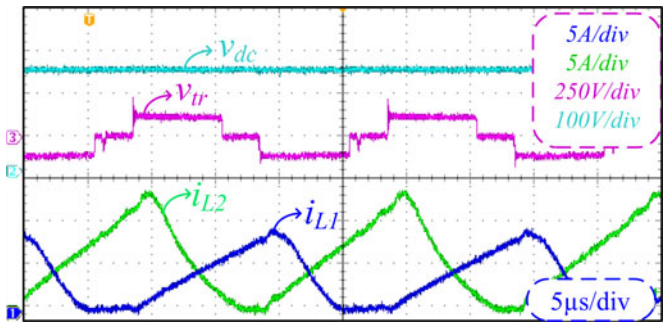

Fig. 13. Experimental results of dc link voltage, transformer voltage, input inductor currents when $D_1 = 0.6, D_2 = 0.35, V_1 = 70$ V and $V_2 = 90$ V.

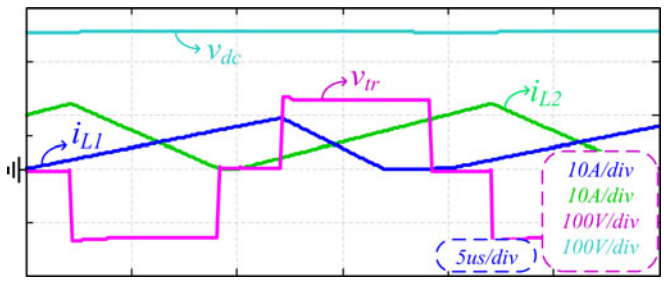

Fig. 14. Simulation results of dc link voltage, transformer voltage, input inductor currents when $D_1 = 0.6, D_2 = 0.35, V_1 = 70$ V and $V_2 = 90$ V.

In the second set of experiments, D_1 and D_2 are adjusted to 0.7 and 0.25, respectively. The first source voltage is varied between 60–70 V, while the second source voltage is swept from 70–110 V. The gating signals of the switches are given in Fig. 17. In Figs. 18 and 19, both input source voltages are set to 70 V. As seen from the figures, both sources supply 9.5-A peak current, and share the load demand equally. In Figs. 20 and 21, the second source voltage is set to 100 V. The peak current is increased to 14.5 A. The power distribution of the second source to the first source becomes 2.15. In Figs. 22 and

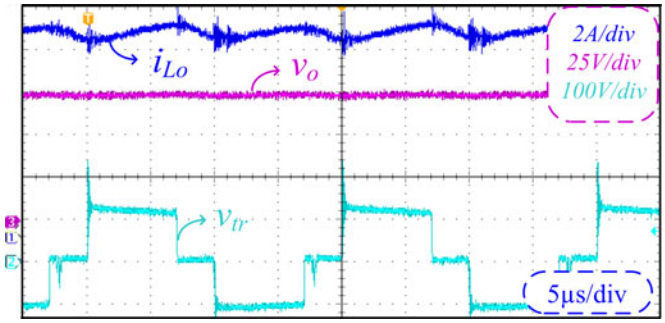

Fig. 15. Experimental results of output voltage, transformer voltage, output inductor current when $D_1 = 0.6, D_2 = 0.35, V_1 = 70$ V and $V_2 = 90$ V.

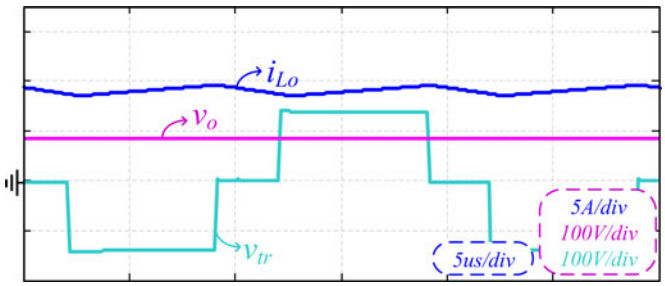

Fig. 16. Simulation results of output voltage, transformer voltage, output inductor current when $D_1 = 0.6, D_2 = 0.35, V_1 = 70$ V and $V_2 = 90$ V.

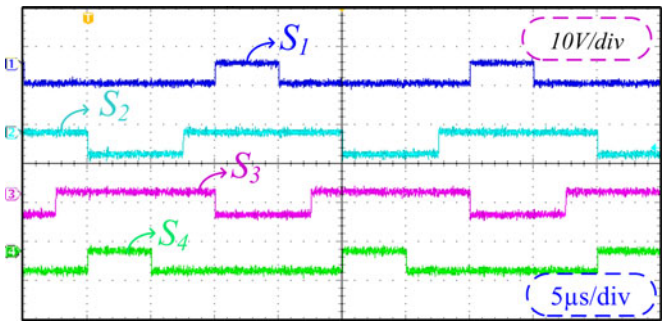

Fig. 17. Experimental waveforms of gate signals when $D_1 = 0.7, D_2 = 0.25$.

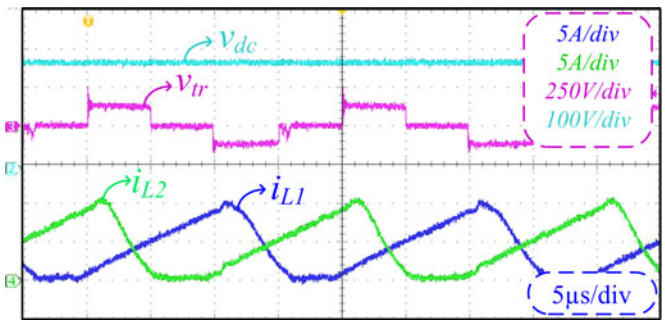

Fig. 18. Experimental results of dc link voltage, transformer voltage, input inductor currents when $D_1 = 0.7, D_2 = 0.25, V_1 = 70$ V and $V_2 = 70$ V.

23, the experimental and simulation results for $V_1 = 60$ V and $V_2 = 110$ V are given, from which a large difference between the provided powers can be clearly observed. The peak current of the second source is 17.5 A, whereas the first one provides peak current of 7 A. The power distribution is 3.75.

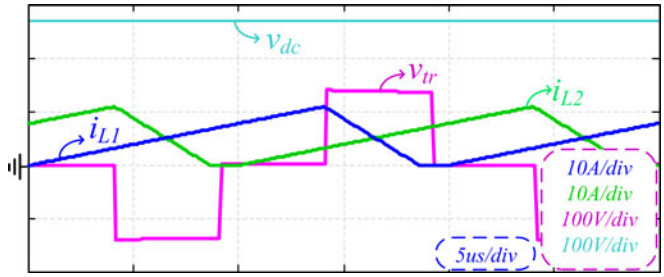

Fig. 19. Simulation results of dc link voltage, transformer voltage, input inductor currents when $D_1 = 0.7, D_2 = 0.25, V_1 = 70$ V and $V_2 = 70$ V.

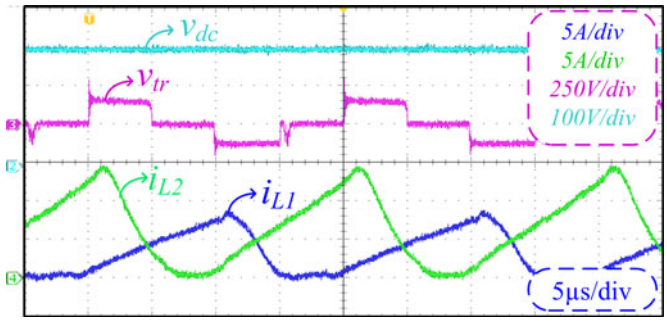

Fig. 20. Experimental results of dc link voltage, transformer voltage, input inductor currents when $D_1 = 0.7, D_2 = 0.25, V_1 = 70$ V and $V_2 = 100$ V.

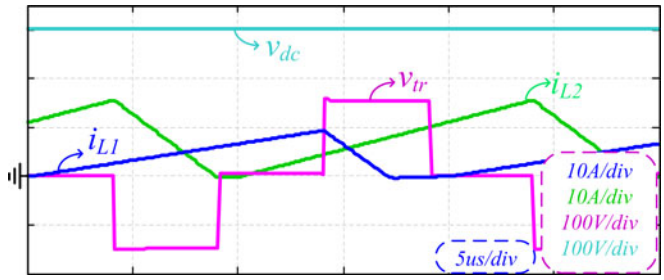

Fig. 21. Simulation results of dc link voltage, transformer voltage, input inductor currents when $D_1 = 0.7, D_2 = 0.25, V_1 = 70$ V and $V_2 = 100$ V.

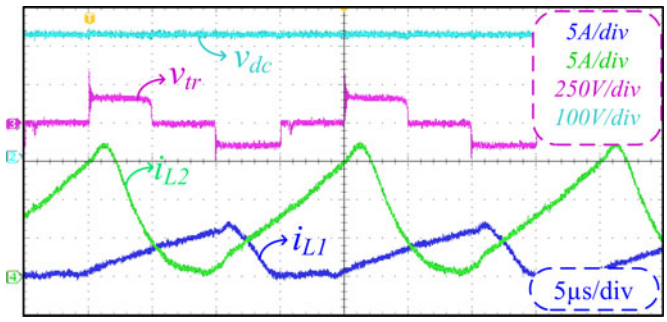

Fig. 22. Experimental results of dc link voltage, transformer voltage, input inductor currents when $D_1 = 0.7, D_2 = 0.25, V_1 = 60$ V and $V_2 = 110$ V.

The experimental efficiency data of the converter under three different operating conditions are presented in Table I, and divided into its individual loss components. The proposed converter exhibited 87–88.6% efficiency under the given test conditions. For a fair comparison, a two-stage counterpart is built by unplugging the input sources from the power terminals, and connecting two interleaving boost legs to the dc link. The

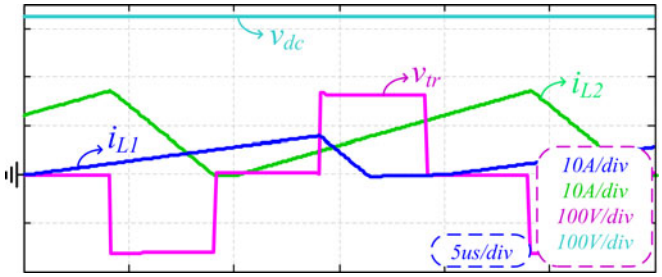

Fig. 23. Simulation results of dc link voltage, transformer voltage, input inductor currents when $D_1 = 0.7, D_2 = 0.25, V_1 = 60$ V and $V_2 = 110$ V.

switching scheme and operating conditions are kept same as of the proposed converter. The two-stage counterpart exhibits higher efficiency than the proposed one, between 89.4–90.1%. Thus, the efficiency of the proposed single-stage converter is 1.5–2.4% lower than the two-stage counterpart. The slightly reduced efficiency is the main disadvantage in single-stage converters in general, opposed to the low cost feature, including the eliminated switches, and corresponding gate driver circuits. In Table I, $P_{\mathrm{BD\_}Sn}, P_{D\_\mathrm{Boostn}}, P_{\mathrm{Con\_}BtSn}$ and P_{D_Blockn} denote the losses of the body diodes of the switches, boost diodes and boost switches present in two-stage converter, and blocking diodes in series with the inductors in the proposed converter, respectively. The other losses such as core losses and parasitic capacitance losses are summed and given under $P_{\mathrm{un-meas}}$. As it can be seen from Table I, although additional switches introduce extra losses in the two-stage counterpart, conduction and switching losses of the middle two switches in the proposed converter surpass the other losses, and reduces the converter's overall efficiency. This is due to the single-stage operation as both the rms and the peak currents of the middle two switches increase significantly. In addition, the transition voltages across the middle two switches are equal to bus voltage, which increases the turn-off switching losses. On the other hand, the currents passing through the upper and lower switches reduce due to single-stage operation. Nevertheless, this reduction does not compensate the additional losses caused by the middle two switches.

V. Conclusion

In this study, a new multiinput dc/dc converter having same number of active switches as of three-level isolated dc/dc converter without introducing additional switching actions is proposed. The circuit analysis and design consideration has been provided in detail. With proper selection of input inductors, autonomous load sharing can be achieved. To verify the operation of the converter, simulations of different parameters have been performed. A low voltage laboratory built prototype has been designed and tested under varying input voltages and duty cycles. The results prove the effective integrated operation of input sources with three-level isolated dc/dc structure, through operating four switches in a phase-shifted manner without introducing control complexity.

TABLE I
Efficiency Comparison Data

	$V_1 = 70$ V $V_2 = 90\,V$ $D_1 = 60$ $D_2 = 35$		$V_1 = 70$ V $V_2 = 100\,V$ $D_1 = 70$ $D_2 = 25$		$V_1 = 60$ V $V_2 = 70\,V$ $D_1 = 70$ $D_2 = 25$	
	Two-Stage	Prop. Conv.	Two-Stage	Prop. Conv.	Two-Stage	Prop. Conv.
Conduction Losses [W]						
$P_{\mathrm{BD\_}S1}$	0.02	0.9	0.02	0.7	0.01	0.75
$P_{\mathrm{BD\_}S2}$	0.02	0.15	0.03	0.13	0.02	0.07
$P_{\mathrm{BD\_}S3}$	0.01	0.05	0.01	0.02	0.01	0.02
$P_{\mathrm{BD\_}S4}$	0.04	1.3	0.05	1.2	0.02	0.9
P_{D_Clamp1}	0.9	0.86	1.6	1.6	1.1	1.1
P_{D_Clamp2}	0.8	0.78	1.6	1.5	1.06	1.06
P_{D_Boost1}	0.6	–	0.4	–	0.5	–
P_{D_Boost2}	1.2	–	1.1	–	0.78	–
P_{D_Block1}	–	2.3	–	2.8	–	2.1
P_{D_Block2}	–	3.4	–	4.4	–	2.7
P_{D_Bridge}	10.3	10.2	12.1	12	8.1	8.2
$P_{\mathrm{Con\_}S1}$	6.1	3.4	5.3	2.7	2.4	2.1
$P_{\mathrm{Con\_}S2}$	7	14.2	10.3	18.6	4.3	11.7
$P_{\mathrm{Con\_}S3}$	6.8	20.2	10.3	28.3	4.3	14.5
$P_{\mathrm{Con\_}S4}$	3.4	5.7	7.3	5.8	2.9	2.9
$P_{\mathrm{Con\_}BtS1}$	2.9	–	4.6	–	3.3	–
$P_{\mathrm{Con\_}BtS2}$	4.8	–	9.4	–	4.6	–
Switching Losses [W]						
$P_{\mathrm{swt\_}S1}$	3	2.7	5.7	4.2	2.8	1.9
$P_{\mathrm{swt\_}S2}$	2	7.8	2.2	11.2	0.9	5.5
$P_{\mathrm{swt\_}S3}$	2.1	9	2.1	14.7	0.9	6.2
$P_{\mathrm{swt\_}S4}$	3.4	2.4	5.6	4.1	2.7	1.7
$P_{\mathrm{swt\_}BstS1}$	5.7	–	8.7	–	5.5	–
$P_{\mathrm{swt\_}BstS2}$	7.3	–	11.2	–	6	–
$P_{\mathrm{un-meas}}$	14.5	11	15.5	12.5	10.5	7
Total Losses [W]						
$P_{\mathrm{loss\_total}}$	82.9	96.3	115.1	122	62.7	70.4
P_{in1}	281	277	334	330	261	256
P_{in2}	528	517	752	746	375	363
η [%]	89.7	87	89.4	88.6	90.1	88.6

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