A Maximum Power Density Design Method for Nine Switches Matrix Converter Using SiC-MOSFET

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***Abstract*—This paper presents a matrix converter design for achieving maximum power density using a SiC device based on a front-loading design. To design the matrix converter to achieve maximum power density, the conduction loss and the switching loss of the matrix converter are theoretically derived and validated by simulation and experiment. Based on these formulas, the relationship between the efficiency and power density are revealed by using a Pareto–Front curve in order to solve the tradeoff problem between the power density and the efficiency. Moreover, in order to promote the widespread use of the matrix converter instead of a BTB system, it is quantitatively evaluated that the power density in the matrix converter is increased by 4.19 kW/dm^3 in comparison to the BTB system. Moreover, the power density of the matrix converter that uses a SiC-MOSFET (ROHM) as the switching device with natural air cooling is 95.0% (2.1 kW/dm^3) of the calculated maximum power density. Thus, the power density of the matrix converter is improved by 57.5% by the maximum power density design method. Based on the results, the design method for a high power density ac–ac direct converter is established according to the requisite specifications.**

***Index Terms*—Front-loading design, loss analysis, matrix converter, maximum power density design, Pareto–Front curve.**

I. Introduction

THE matrix converter which can convert an ac power supply voltage directly into another ac output voltage of variable amplitude and frequency without any large energy storages, such as electrolytic capacitors, is one of the solutions to achieve the high power density and high efficiency [1]–[11]. The key advantages of the matrix converter compared with the back-to-back (BTB) converter system, which consists of a PWM rectifier and a PWM inverter are as follows: 1) reduced size, light weight, and long lifetime owing to the absence of the large electrolytic capacitor in the main circuit; 2) high efficiency because the single-stage power converter results in less switching loss compared with a two-stage power converter, and 3) low current stress on the switching devices in the low output frequency operation owing to no current concentration. Given these advantages, it is expected that the matrix converter can be applied to ac–ac conversion applications, such as industry motor drives, hybrid electric vehicle systems, and wind energy conversion systems [10], [11]. At present, the BTB system is more commonly used in ac–ac conversion applications instead of the matrix converter. In order to promote the widespread use of the matrix converter, the validity of the matrix converter should be quantitatively evaluated by comparing its efficiency and power density with that of the BTB system. Furthermore, in ac–ac conversion applications, in order to install the matrix converter in the limited space that is typically available, high power density is a major requirement.

In several studies, methods of achieving high efficiency and high power density of the power converter, which includes the matrix converter, have been discussed [12]–[17]. In order to achieve optimized maximum power density of the matrix converter, a silicon carbide (SiC), which has higher rated voltage, lower switching loss, and higher switching speed, is used in the matrix converter [12]–[15]. For optimized design, the prototypes are manufactured after many modifications in the design and specifications of the power converter. Manufacturing a large number of prototypes results in high development costs and long development periods. To solve this problem, the front-loading design, that estimates the loss, size, and electromagnetic compatibility before manufacturing the prototype, is adopted in the power converter design [16]. In the front-loading design, the prototype needs to be manufactured only once owing to the prior estimation of the performance. As a result, the developing cost as well as the process time can be reduced.

The front-loading design in terms of the efficiency and power density requires the use of techniques for estimating loss and volume using mathematical formulas. Two methods generally used for loss analysis are as follows. 1) The loss is calculated from the device current and the drain-source voltage using a circuit simulator [18]. 2) The loss is theoretically obtained from the derived formulas using device parameters [19]. In method 1 , it is difficult to optimize the converter loss when the loss is analyzed under several conditions simultaneously. This is because considerable simulation time is required to determine the minimum loss condition through trial and error. On the other hand, in method 2, it is easy to optimize the circuit because analysis time and trial time are considerably reduced.

Some derivation methods of the converter loss of an ac–ac direct converter have been proposed [19]–[25]. In [21], the conduction loss and the switching loss of an indirect matrix converter are theoretically calculated. The converter loss of the direct matrix converter composed of nine switches has been discussed [22], [23]. Nevertheless, it is difficult to understand the switching loss formulas because a coefficient of the switching loss has not been revealed. Moreover, the validity of the converter loss is not enough by experiment because the converter loss has been measured at only rated current. In earlier studies, the volumes of the matrix converter and the BTB system have

Manuscript received October 31, 2014; revised February 9, 2015; accepted March 29, 2015. Date of publication April 7, 2015; date of current version September 29, 2015. This work was supported in part by the Industrial Technology Grant Program in 2011 from the New Energy and Industrial Technology Development Organization of Japan. Recommended for publication by Associate Editor J. R. Espinoza.

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Digital Object Identifier 10.1109/TPEL.2015.2420660

been quantitatively compared using the loss formulas [24]–[26]. Nevertheless, the effectiveness of the design method based on which the direct matrix converter is designed at maximum power density point has not been confirmed by experiments. In addition, the performances such as the efficiency and the power density using a SiC device have not been theoretically revealed. In other words, when the matrix converter is designed using a SiC device, the effect for the design is not figured out.

This paper proposes a maximum power density design method for the matrix converter using loss formulas and clarifies its design procedure in detail. In addition, the validity of the proposed design method is revealed by experiments. In order to validate the design method, the prototype of the matrix converter is demonstrated at maximum power density point using a SiC-MOSFET. It is easy for anyone to design the matrix converter at required power density point with proposed maximum power density design method. Thus, to promote the widespread use of the matrix converter is expected owing to its advantages of energy saving and size reduction. Moreover, the requirement improving the performance for SiC device can be revealed in terms of the application sides. This is because the formulas, which include the SiC parameters, are validated. Finally, even when widebandgap devices, such as SiC and gallium nitride devices are practically used, the design method is effectiveness in terms of an optimum design because the volume and loss can be calculated similar to silicon (Si) device.

The remainder of this paper is organized as follows. First, in Section II, the circuit configurations of the BTB system and matrix converter are introduced. In Section III, the conduction loss and the switching loss of the matrix converter are theoretically derived. Additionally, the validity of the loss formulas is confirmed by experiment using the first prototype with 2-kW rated power. Second, the maximum power density design method is introduced in terms of loss formulas. Subsequently, the volumes of the heat sink, input *LC* filter, boost-up inductor, and dc-link capacitor are calculated. Thus, the validity of the matrix converter is evaluated by comparing the power density of the first prototype with the BTB system. Next, a Pareto–Front curve is drawn using loss and volume formulas when the switching frequency is changed. It has to be noted that the SiC-MOSFET, with 1200-V rated voltage and 120-A rated current, is used as the switching device. Based on the Pareto–Front curve, the second prototype with 10-kW rated power is designed and manufactured at the maximum power density point. Finally, the operation of the matrix converter is demonstrated by experiments with a 9.5-kW *RL* load. Based on the experimental result, the validity of the maximum power density design method, which can obtain the required power density using the SiC or Si devices, is confirmed.

II. Circuit Configuration

A. BTB System

Fig. 1 shows the circuit diagram of a BTB converter, which consists of a PWM rectifier and an inverter. This system requires a large electrolytic capacitor in the dc link part to reduce the ripple voltage formed by the rectifier. The electrolytic capacitor is

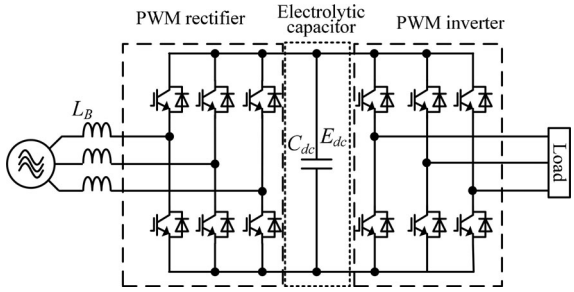

Fig. 1. Circuit configuration of a BTB system consisting of boost-up inductor, electrolytic capacitor, PWM rectifier, and PWM inverter.

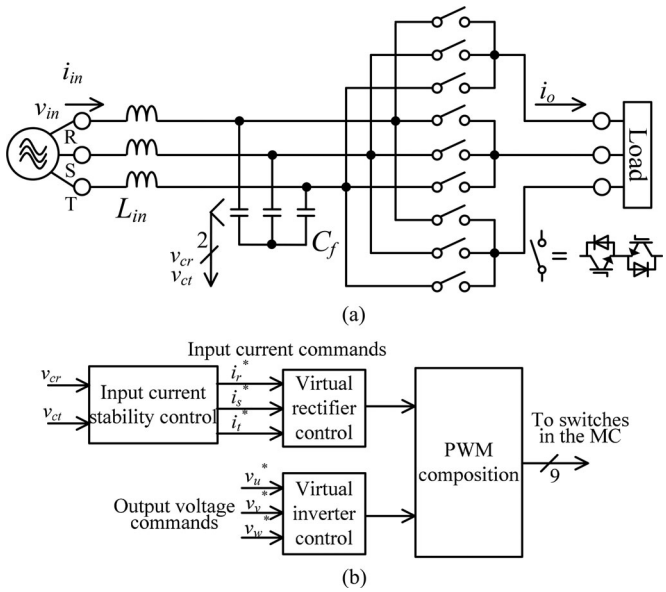

Fig. 2. Circuit configuration and virtual indirect control diagram of a nine-switch matrix converter. (a) Circuit configuration of a matrix converter. (b) Control diagram of the matrix converter.

of a large capacity and low cost; however, has a large equivalent series resistance and low performance for a frequency characteristic. Moreover, it is necessary to maintain the performance of the electrolytic capacitor periodically owing to its short lifetime.

In general, the PWM rectifier requires an automatic current regulator (ACR) to control the input current. Besides, an automatic voltage regulator (AVR) for the dc-link voltage is required to obtain the input current command. The minimum capacitor value is constrained by the control response of the dc-link voltage and the input current according to the AVR and the ACR.

B. Matrix Converter

Fig. 2(a) shows the circuit configuration of the matrix converter. Note that the bidirectional switches in the matrix converter can be used with two MOSFETs. In addition, in order to suppress the input filter resonance, the damping resistor is connected to the input inductor in parallel or input current stability control, such as damping control is adopted. It is noted that the damping resistor and the damping control gain are determined after designing the parameters of the input *LC* filter. Thus, the input *LC* filter can be stably designed. For this reason,

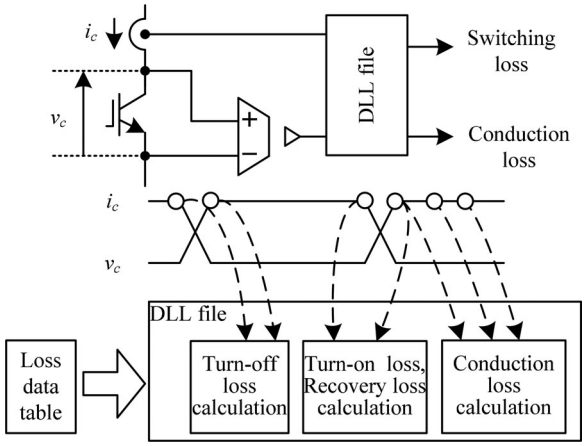

Fig. 3. Loss analysis method by simulator. The loss data table is obtained from the datasheet of the switching device or the switching test.

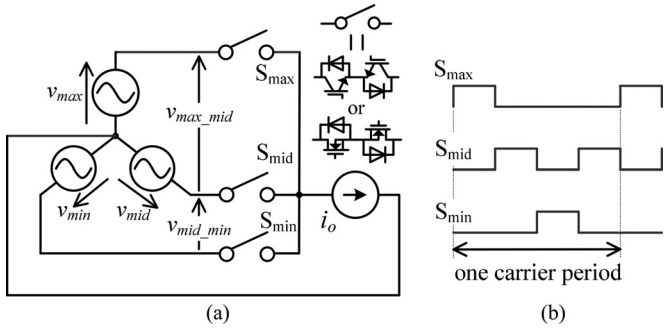

Fig. 4. Equivalent single-phase model of the matrix converter. The matrix converter losses are discussed as the maximum phase, middle phase, and minimum phase switches. (a) Equivalent circuit. (b) Switching pattern by a three-phase modulation.

in this study, the stability of the matrix converter is not taken into consideration to design the input *LC* filter. Here, the loss and volume of the damping resistor do not affect the total loss and volume.

Fig. 2(b) shows the control diagram of the matrix converter. In this study, a virtual indirect control proposed in [6] is adopted. In the virtual indirect control, the input current and the output voltage can be independently controlled. For this reason, a conventional control technique that uses a rectifier and an inverter is easily applied. Moreover, the switching loss is reduced by fixing the switching pulse patterns [7] because the fluctuated voltage owing to switching is decreased. Accordingly, the pulse pattern, in which the switching changes directly from the maximum voltage phase to the minimum voltage phase, is not taken into consideration. It has to be noted that the maximum, middle, and minimum voltage phases depend on the relationship among each input phase voltage. In order to simplify the loss analysis, a three-phase modulation scheme is adopted. Furthermore, the dead time is not taken into consideration. The input current command in the virtual rectifier is also set to unity power factor.

In order to design high efficiency and high power density of the matrix converter, it is necessary to optimize the switching device and the switching frequency by analyzing the loss.

III. Loss Analysis Method for Matrix Converter

Fig. 3 shows the loss analysis method that uses a simulator. The device voltage ν_c and current i_c are detected. Next, the conduction and switching losses are calculated from the measurement value and the loss data table. In this method, it is easy to analyze the loss of the matrix converter using the loss model of the switching device. However, it is still difficult to optimize the converter loss because the loss is analyzed under multiple conditions. This is because considerable simulation time is required to determine the minimum loss condition by trial and error.

Fig. 4(a) shows the equivalent single-phase model of the matrix converter for the derivation of loss. When the relationship among the input phase voltages is R $>$ S $>$ T, then the maximum phase switch $\mathrm{S_{max}}$ is the R-phase switch, the middle phase switch is the S-phase switch, and the minimum phase switch $\mathrm{S_{min}}$ is the T-phase switch. In other words, the matrix converter loss is derived by each $\mathrm{S_{max}}$, $\mathrm{S_{mid}}$, and $\mathrm{S_{min}}$.

Fig. 4(b) shows the pulse pattern of the single-phase in the matrix converter. According to this figure, the switching loss of the matrix converter is calculated by assuming that the middle-phase switch is turned ON when the pulse pattern is changed from the maximum phase switch (or the minimum phase switch) to the minimum phase switch (or the maximum phase switch) during one control period.

A. Conduction Loss

The conduction loss in the matrix converter P_{con} can be expressed as [22], [23]

$$P_{\mathrm{con}} = \frac{1}{\pi}\int_{\theta_o}^{\pi+\theta_o} v_{\mathrm{on}} \cdot i_o \; d\omega_o t = \frac{1}{2}k_{\mathrm{con1}}{I_o}^2 + \frac{2}{\pi}k_{\mathrm{con2}}I_o. \tag{1}$$

Here, ω_o is the output angular frequency. In this paper, the total conduction loss of each phase P_{con} is derived. Consequently, the on-duty command of each phase is definitely 1. Thus, it can be revealed that the two switches are not in the on-state when the other switch is turned ON. It is assumed that switching devices with the same characteristics are used. It is noted that k_{con1} and k_{con2} are obtained from the on-state voltage characteristic in the datasheet. Concretely, the drain-source voltage ν_{on} characteristic corresponding to the drain current mentioned in the datasheet is approximated to a primary by (2). In other words, k_{con1} is an intercept value, and k_{con2} is a gradient for the drain current

$$v_{\mathrm{on}} = k_{\mathrm{con2}}i_o + k_{\mathrm{con1}}. \tag{2}$$

In addition, the instantaneous value of the output current i_o is expressed by (3) in terms of the maximum load current I_o and the load angle θ_o

$$i_o = I_o \sin(\omega_o t - \theta_o). \tag{3}$$

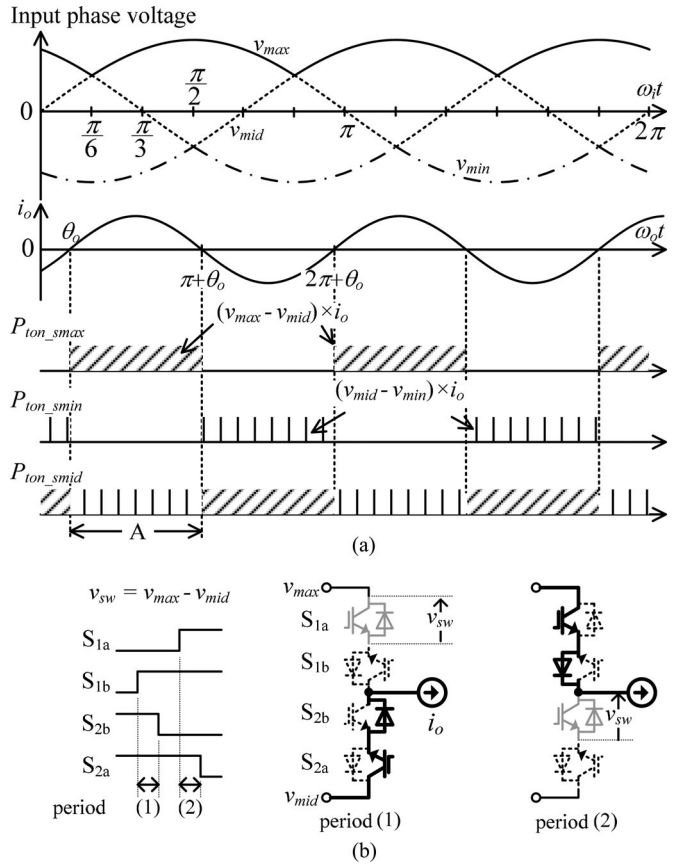

Fig. 5. Integral period of each switching loss of the matrix converter. The turn-on loss of the maximum phase switch occurs when the sign of the output current is positive. (a) Occurrence region of turn-on loss. (b) Mechanism of turn-on loss occurrence during "A."

B. Switching Loss

In this section, the turn-on loss of maximum phase $P_{\mathrm{ton\_smax}}$ is derived. First, the general turn-on loss is expressed as

$$P_{\mathrm{sw\_loss}} = \frac{1}{2\pi}\int_0^{\pi} \frac{f_s}{V_s} e_{\mathrm{on}} v_{\mathrm{sw}}\ d\omega_o t \tag{4}$$

where T is the cycle of i_o, f_s is the switching frequency, V_s is the tested voltage when the switching loss was measured, and ν_{sw} is the drain-source voltage of the device. In addition, the instantaneous turn-on loss e_{on} is expressed by

$$e_{\mathrm{on}} = k_{\mathrm{ton3}} {i_o}^2 + k_{\mathrm{ton2}} i_o + k_{\mathrm{ton1}}. \tag{5}$$

Similarly, k_{ton1}, k_{ton2}, and k_{ton3} are obtained from the turn-on loss characteristic in the datasheet by approximating to a polynomial.

Fig. 5(a) shows the integral period to calculate the switching loss. The integral period is different among switching devices owing to sign of i_o. In other words, $P_{\mathrm{ton\_smax}}$ occurs when the sign of i_o is positive.

Fig. 5(b) shows the mechanism by which the turn-on loss of the maximum phase switch occurs. It is noted that the current path in Fig. 5(b) is the path when the pulse pattern is changed from the middle phase switch to the maximum phase switch. In addition, the period (1) and (2) are the current paths on the right portion of the figure, respectively. Moreover, the sign of the output current i_o is positive. During (1), the current flows through the switch (S_{2a}, S_{2b}), which is connected to the middle phase. The differential voltage between the maximum phase and the middle phase ν_{sw} is dropped on the switch S_{1a}. On the other hand, during (2), the current path becomes the maximum phase switch (S_{1a}, S_{1b}) because the switch S_{1a} is turned ON. Now, the dropped voltage on S_{1a} becomes zero and the differential voltage ν_{sw} is dropped on the switch S_{1b}. As a result, the turn-on loss of S_{1a} occurs. It is noted that the maximum phase turn-on loss $P_{\mathrm{ton\_smax}}$ does not occur when the sign of the output current is negative. This is because the current, which flows into S_{1a}, passes through a fly-wheeling diode (FWD).

Furthermore, the drain-source voltage ν_{sw} is different among each switching devices. Accordingly, the drain-source voltage of $S_{\max}$ is the differential voltage ($\nu_{\max} - \nu_{\mathrm{mid}}$) between the maximum phase voltage $\nu_{\max}$ and the middle phase voltage ν_{mid}

$$v_{\mathrm{sw}} = v_{\max} - v_{\mathrm{mid}} = V_{\mathrm{in}} \sin\left(\omega_i t + \frac{5}{6}\pi\right),\ 0 \le \omega_i t < \frac{\pi}{6}. \tag{6}$$

It is noted that V_{in} is the maximum input line voltage. In addition, ω_i is the input angular frequency. Thus, $P_{\mathrm{ton\_smax}}$ is expressed as

$$\begin{aligned} P_{\mathrm{ton\_smax}} = \frac{f_s}{4\pi^2 V_s}\int_{\theta_o}^{\pi+\theta_o} \Bigg\{ \int_0^{\frac{\pi}{6}} e_{\mathrm{on}}(\omega_o t)\cdot(v_{\max}(\omega_i t) \\ - v_{\mathrm{mid}}(\omega_i t))\ d\omega_i t + \\ \cdots + \int_{-\frac{\pi}{6}}^{2\pi} e_{\mathrm{on}}(\omega_o t)\cdot(v_{\max}(\omega_i t) \\ - v_{\mathrm{mid}}(\omega_i t))\ d\omega_i t \Bigg\} d\omega_o t \end{aligned} \tag{7}$$

$$P_{\mathrm{ton\_smax}} = \frac{3 f_s V_{\mathrm{in}}}{4\pi^2 V_s}\left(\frac{\pi}{2} k_{\mathrm{ton3}} {I_o}^2 + 2 k_{\mathrm{ton2}} I_o + k_{\mathrm{ton1}}\pi\right) \tag{8}$$

On the other hand, the dropped voltage of the minimum phase switch is the differential voltage between the middle phase voltage and the minimum phase voltage ($\nu_{\mathrm{mid}} - \nu_{\min}$). Now, the dropped voltage of the middle phase switch, which depends on the output current, is ($\nu_{\max} - \nu_{\mathrm{mid}}$) or ($\nu_{\mathrm{mid}} - \nu_{\min}$). Similar to the turn-on loss of the maximum phase switch, the middle phase, and the minimum phase turn-on losses are calculated as

$$P_{\mathrm{ton\_smid}} = \frac{3 f_s V_{\mathrm{in}}}{2\pi^2 V_s}\left(\frac{\pi}{2} k_{\mathrm{ton3}} {I_o}^2 + 2 k_{\mathrm{ton2}} I_o + k_{\mathrm{ton1}}\pi\right) \tag{9}$$

$$P_{\mathrm{ton\_smin}} = \frac{3 f_s V_{\mathrm{in}}}{4\pi^2 V_s}\left(\frac{\pi}{2} k_{\mathrm{ton3}} {I_o}^2 + 2 k_{\mathrm{ton2}} I_o + k_{\mathrm{ton1}}\pi\right). \tag{10}$$

C. Confirmation of Matrix Converter Loss Formulas

In order to validate the conduction and switching loss equations, the calculation results are compared with the loss simulation results obtained by PLECS. Table I lists the calculation parameters. In the loss simulation, the stray inductance,

TABLE I
DEVICE PARAMETERS AND SIMULATION CONDITION TO CALCULATE MATRIX CONVERTER LOSSES

Parameters of switching device (SK80GM063)		
On-state voltage characteristic	k_{con1} (V)	0.977
	k_{con2} (V/A)	0.018
Switching loss characteristic	k_{ton1} (J)	0.0
	k_{ton2} (J/A)	5×10^{-5}
	k_{ton3} (J/A^2)	0.0
Input power factor		1.0
Maximum input line voltage V_{in}		283 V
Switching frequency f_s		10 kHz
Test voltage V_s		300 V

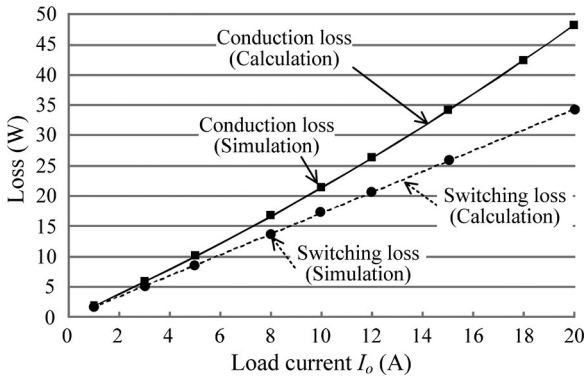

Fig. 6. Conduction loss and switching loss-load current characteristics between calculation and simulation. The difference between the values obtained by calculation and simulation are within 0.02%.

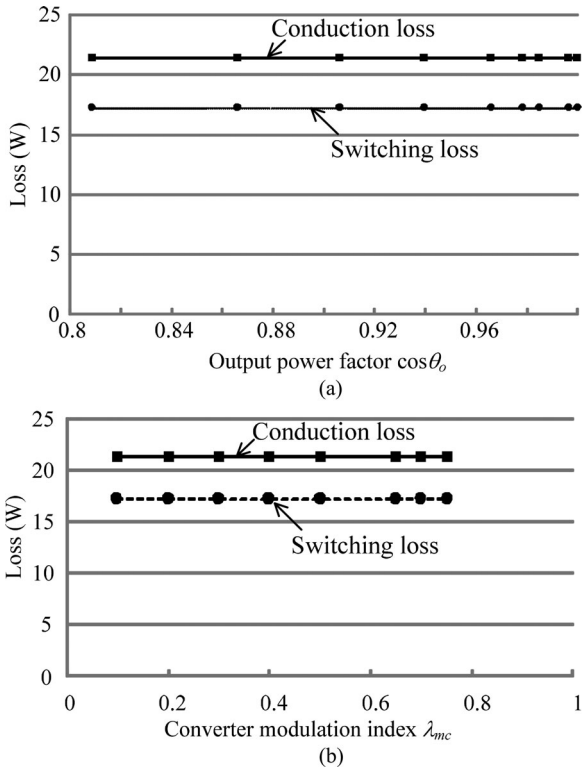

Fig. 7. Conduction and switching loss characteristics between calculation and simulation. The matrix converter losses do not depend on the output power factor and modulation ratio. (a) Loss-output power factor characteristics. (b) Loss-modulation index characteristics.

the stray capacitance, and an input *LC* filter are not taken into consideration.

Fig. 6 shows the conduction and switching losses of the matrix converter obtained by the theoretical calculation and the simulation. Note that the solid line and the square point in Fig. 6 show the calculated conduction loss. On the other hand, the dash line and the circle point show the switching loss of the calculation and simulation results, respectively. As a result, the calculation result of the conduction loss agrees well with the simulation result. The conduction and turn-on loss errors between the calculation and simulation are within 0.02%. Thus, the validity of the derived loss formulas is confirmed. On the other hand, the error of the switching loss between the calculation and simulation is 2.4% at 20-A output current when the input *LC* filter is connected. This is caused by the voltage ripple resulting from switching. Thus, the loss margin needs to be considered owing to the ripple voltage when the matrix converter is designed.

Fig. 7(a) shows the matrix converter losses based on the output power factor. In addition, Fig. 7(b) shows the matrix converter losses based on the modulation ratio. As the results show, the conduction and switching losses do not depend on the output power factor and the modulation index. If it assumes that the switching devices have the same on-resistance, are used, then the total conduction loss is not dominated by the on-duty command. Accordingly, the output power factor is not related to the conduction loss. Moreover, the switching loss of each switches occurs during a half period of the output current. On the other hand, the switching loss is decided from the drain-source voltage ν_{sw} and output current. The drain-source voltage of $\mathrm{S}_{\mathrm{max}}$ is the differential voltage ν_{sw} at the input side. In other words, the drain-source voltage does not depend on the output voltage. Thus, the converter loss is not changed when the output power factor, modulation index, or output frequency is changed. In other words, the efficiency is adversely affected because the output power becomes lower. In order to improve the efficiency, the output power factor and the modulation index are increased.

Note that the voltage transfer ratio of the matrix converter is limited to 0.75 when three-phase modulation is adopted in a virtual inverter control. In order to increase the output voltage, the two-phase modulation should be applied. In the two-phase modulation scheme, the switching loss can be reduced to two thirds because one of the output phases is not operated in comparison with a three-phase modulation. In other words, the switching loss is calculated by multiplying (8)–(10) by 2/3 when two-phase modulation is adopted. Furthermore, the switching loss depends on the modulation strategy. However, it is expected that the switching loss can be calculated by considering the drain-source voltage even when the other modulation strategy is adopted.

Finally, the validity of the loss formulas is confirmed with the first prototype.

Fig. 8 shows the first prototype of the matrix converter board using the Si-MOSFET. Table II lists the parameters of the MOSFET and the experimental conditions. The switching loss of a

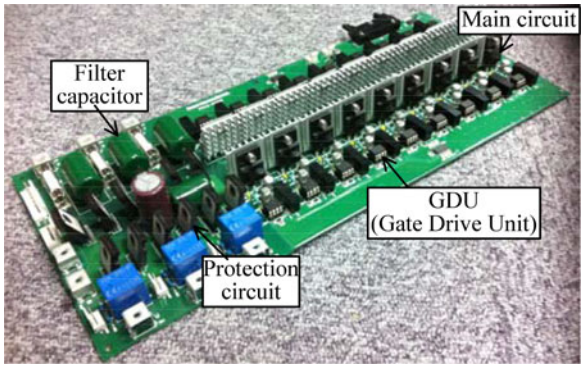

Fig. 8. Board of a 2-kW matrix converter. The size of this board is 358 mm × 155 mm × 40 mm. A Si-MOSFET (ROHM: R6046FNZ) is used as the switching device.

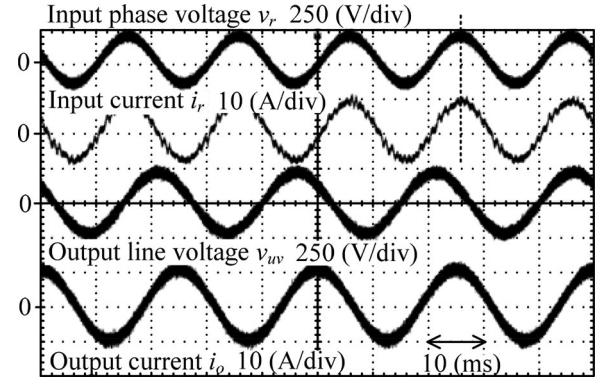

Fig. 9. Steady operation at rated power during the experiment. As a result, unity power factor is obtained and the input current THD is 7.4%.

TABLE II
DEVICE PARAMETERS AND EXPERIMENTAL CONDITIONS

Parameters of R6046FNZ			Input line voltage $V_{\rm in}$	283 V
On-state voltage characteristic	$k_{\rm con1}$ (V)	0.0	Output power $P_{\rm out}$	2 kW
	$k_{\rm con2}$ (V/A)	0.08	Output frequency f_o	40 Hz
Turn-on loss characteristic	$k_{\rm ton1}$ (J)	0.0	Commutation method	4-step voltage
	$k_{\rm ton2}$ (J)	9×10^{-6}	Load inductance	5 mH
Turn-off loss characteristic	$k_{\rm toff1}$ (J/A)	3×10^{-6}	Input inductor	2 mH
	$k_{\rm toff2}$ (J/A)	3×10^{-5}	Filter capacitor	18.9 μF
Recovery loss characteristic	$k_{\rm trr1}$ (J)	0.0		
	$k_{\rm trr2}$ (J/A)	1.65×10^{-5}		
No-load loss and snubber loss		10 W		

The no-load loss and snubber loss were measured in experiment.

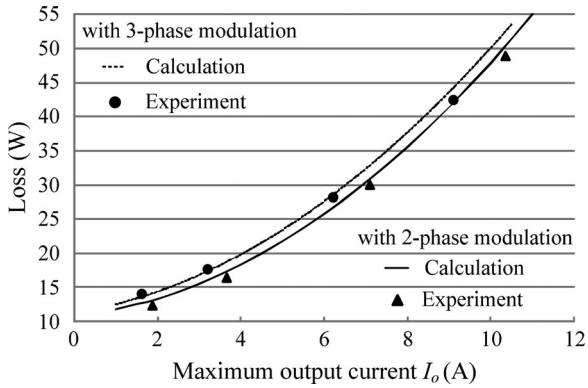

Fig. 10. Total loss characteristics comparison between calculation and experimental result. The loss error between the calculation value and the measured value is 2.77% at the rated current.

MOSFET is twice as that of an IGBT, the reason being that the switching loss of a MOSFET does not depend on the sign of $i_{\rm o}$. In other words, the device current flows into MOSFET which has low resistance. Thus, when the MOSFETs are used as a bidirectional switch, the switching loss occurs at all of region. This board consists of the main circuit, filter capacitor, protection circuit for the surge voltage, and drive circuit. The size of this board is 358 mm × 155 mm × 40 mm. IC-0526B (RYOSAN) is used as the heat sink.

Fig. 9 shows the operation waveforms using a 2-kW *RL* load. The output line voltage was observed through a low-pass filter with the cut-off frequency of 1.5 kHz. Two-phase modulation was adopted in the virtual inverter control. In addition, four-step voltage commutation is adopted as the commutation method [27]. As a result, the unity power factor is obtained, and the input current total harmonic distortion (THD) is 7.4%. Thus, satisfactory fundamental operation of the matrix converter can be confirmed.

Fig. 10 shows the loss characteristics for the maximum output current. It can be seen that the calculated total loss includes the conduction loss, turn-on loss, turn-off loss, and recovery loss of the FWD. Accordingly, the calculation results almost agree to the simulation and experimental results. In particular, the total loss error at the rated power (rated current) is important because each device is selected at the rated power during the matrix converter design. It can be confirmed that the loss error is 2.77% at the rated output current. Moreover, the measured loss is less than the calculated value. This is because the middle phase switch is often not operated. In the experiment, in order to avoid the pulse pattern, which is below the switching time for the switching device, the threshold value is set to the pulse width. In the first prototype, the switch is not operated when the width of the pulse pattern is below 1 μs because the threshold value is set to 1 μs. Thus, the pulse pattern of the middle phase switch, which is less than 1 μs, is eliminated. Consequently, the measured switching loss is less than the calculated value.

Based on these results, the validity of loss formulas can be confirmed in experiment.

D. Design Procedure for Matrix Converter Using Loss Formulas

Based on the formulas (1), (8), (9), and (10), it is easy to design the matrix converter with optimized efficiency and reduced size. It is noted that the design method depends on whether high efficiency or high power density. When the matrix converter is designed in terms of high power density, the switching frequency is increased. As a result, the input *LC* filter becomes smaller. In this case, the size of the heat sink is large because the switching

loss increases. Furthermore, the switching loss is more dominant than the conduction loss. Thus, the switching device, which has small parameters $k_{\rm ton1}$ and $k_{\rm ton2}$, is selected in reference to the datasheets. Accordingly, high power density is obtained even if the switching frequency is increased. This is because the volume of heat sink can be reduced owing to lower switching loss. On the other hand, when the matrix converter is designed in terms of high efficiency, the conduction loss dominates owing to lower switching frequency. Therefore, the switching device, which has small parameters $k_{\rm con1}$ and $k_{\rm con2}$, is selected from the datasheet. As a result, high efficiency can be obtained because conduction loss is low. Besides, the switching device in the matrix converter can be selected depending on the efficiency required in an application. First, circuit specifications such as the rated power, rated voltage, rated current, and switching frequency are arbitrarily determined. Second, the on-state voltage parameters $k_{\rm con1}$ and $k_{\rm con2}$ as well as switching loss parameters $k_{\rm ton1}$ and $k_{\rm ton2}$, that the demanded efficiency is obtained, are calculated using (1), (8), (9), and (10). Next, based on the calculated parameters, the switching device is selected from the datasheet. Finally, the efficiency determined in the experiment agrees with that of the design value when the matrix converter is manufactured using the selected device.

IV. Design of Maximum Power Density Based on Front Loading

Based on these formulas, the maximum power density design method for the matrix converter is introduced in this section.

Fig. 11 shows the design flowchart of the matrix converter for achieving maximum power density. First, the volume of the heat sink $\rm Vol_{heat}$ is calculated. The thermal resistance $R_{\rm th}$ and the cooling system performance index (CSPI) [28], which indicates the cooling performance of the heat sink, are needed in order to calculate $\rm Vol_{heat}$. Second, the volume of the input *LC* filter is obtained. Then, the capacitance value C_f is calculated from the voltage ripple $V_{\rm rip}$ on the filter capacitor. As a result, the volume of the filter capacitor $\rm Vol_C$ can be calculated. On the other hand, the inductance value of the input inductor *L* is decided from C_f and the cut-off frequency f_c. Moreover, the volume of the input inductor is calculated based on an area product [30]. Next, the Pareto–Front curve is drawn from the volume of the system and the efficiency. It is noted that the maximum power density design method is not determined by the protection circuit. In other words, the switching frequency obtained the maximum power density does not depend on the volume of the protection circuit. From the Pareto–Front curve, f_s at the maximum power density is obtained. In other words, the specification of the matrix converter is decided. Finally, the inductor, the capacitor, and the heat sink are selected. Note that $\rm Vol_{heat}$ is recalculated when the required heat sink is not found.

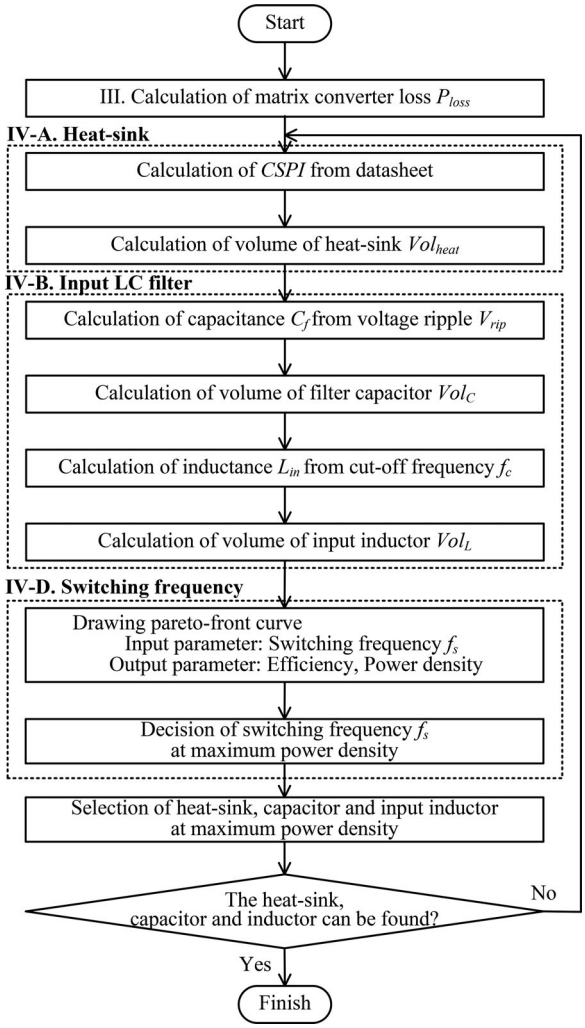

Fig. 11. Design flowchart of the matrix converter for the maximum power density based on the front-loading design.

A. Heat Sink

First, $\rm Vol_{heat}$ is calculated from the CSPI [28]. Note that the CSPI is decided from the datasheet of the heat sink. The CSPI depends on the cooling condition. For example, the CSPI ranges from 3 to 10 W/Kdm^3 when a forced air cooling system is adopted. In fact, the heat sink is selected by considering the required heat resistance, and the CSPI is calculated from the volume of the heat sink. Finally, the heat sink, which has a larger CSPI, should be selected.

As a result, $\rm Vol_{heat}$ is expressed as

$$\rm Vol_{heat} = \frac{1}{CSPI \times R_{th}} \tag{11}$$

where $R_{\rm th}$ is expressed in terms of the device loss $P_{\rm loss}$, maximum junction temperature T_j, and ambient temperature T_a

$$R_{\rm th} = \frac{T_j - T_a}{P_{\rm loss}}. \tag{12}$$

B. Input LC Filter

Next, the volume of the input *LC* filter in the matrix converter is calculated. It is assumed that f_c is one-fifth of f_s and $V_{\rm rip}$ is 4% or less. Accordingly, C_f is expressed as

$$C_f = \frac{I_o}{\pi \omega_s V_{\rm rip}} \sin \pi D \tag{13}$$

where ω_s is the switching angular frequency and *D* is the on-duty cycle of the converter. In the matrix converter, *D* cannot be obtained because *D* varies with time. In this study, C_f is designed considering the worst-case condition. Thus, *D* is set to 0.5. Moreover, when I_o is decided, the output power factor for a real application should be taken into consideration. Accordingly, Vol_C is obtained from electrostatic energy *E* as

$$E = \frac{1}{2}\varepsilon_0\varepsilon_s {k_z}^2 \mathrm{Vol}_C = \frac{1}{2} C_f {V_{\mathrm{in}}}^2 \tag{14}$$

$$\mathrm{Vol}_C = \frac{C_f {V_{\mathrm{in}}}^2}{\varepsilon_0\varepsilon_s {k_z}^2}. \tag{15}$$

It is assumed that the filter capacitor is connected by delta winding. Accordingly, the dropped voltage on the filter capacitor is the input line voltage. In other words, V_{in} is the maximum input line voltage. In addition, the dielectric constant of the material ε_s and the breakdown voltage coefficient k_z depend on the material of the capacitor. In addition, ε_0 is the dielectric constant of the vacuum. ε_s is 2.2, and k_z is expressed from the film of thickness *d* and breakdown voltage *V* as

$$k_z = \frac{V}{d} = \frac{400}{20 \times 10^{-6}} = 2 \times 10^7. \tag{16}$$

On the other hand, the volume of the inductor is calculated from area product [30], [31]

$$\mathrm{Vol}_L = K_{\mathrm{vol}} \left[\frac{L_{\mathrm{in}} {I_{\mathrm{in}}}^2}{K_u B_m J} \right]^{\frac{3}{4}}. \tag{17}$$

Here, the capacitor voltage ripple depends on the modulation strategy. However, the design of the input filter is not dominated by the modulation strategy. This is because the input filter is designed in the worst case. The capacitor voltage ripple becomes large when the switch is turned on at the maximum point of an output current and the duty is 0.5. According to (13), the filter capacitance is calculated by assuming that the output current and the duty are the maximum value and 0.5, respectively. Thus, the measured capacitor voltage is less than that of the designed value.

The area product is the evaluation method for the volume of a core, which can be quantitatively, calculated from the effective cross section A_e and the window section A_{win}. In addition, the core coefficient K_{vol} depends on the type of the core, K_u is a space factor of winding, B_m is the maximum flux density, and *J* is the current density. Furthermore, the input inductance is calculated by assuming that the cut-off frequency is one-fifth of the switching frequency. The input current ripple then becomes 4% owing to the cut-off frequency of the input *LC* filter.

C. Boost-Up Inductor and DC-Link Capacitor

The boost-up inductor and the dc-link capacitor are not necessary for the matrix converter. On the other hand, the BTB system has a boost-up inductor and a dc-link capacitor. First, the volume of the boost-up inductor and the dc-link capacitor are calculated. Second, the capacitance value of the dc-link capacitor is designed by assuming that the fluctuating voltage, when the output power is rapidly changed from P_1 to P_2, is less than 3% of the dc-link voltage. When the BTB system is used in real-life applications, the response angular frequency ω_{AVR} and disturbances are taken into consideration. Thus, the dc-link capacitance C_{dc} is calculated as [32], [33]

$$C_{\mathrm{dc}} = \frac{(P_2 - P_1)T_p - \frac{\sqrt{3}V_{\mathrm{in}}\Delta V}{2}\left(K_p \frac{T_p}{2} + K_i f_s \frac{{T_p}^2}{3}\right)}{E_{\mathrm{dc}}\Delta V - \frac{1}{2}\Delta V^2}. \tag{18}$$

Note that K_p and K_i are the proportional and integral gains of the AVR, respectively. In addition, T_p is an overshoot time of the dc-link voltage when the load is rapidly changed and is expressed as

$$T_p = \frac{\pi}{\omega_{\mathrm{AVR}}\sqrt{1-\zeta^2}} \tag{19}$$

where the damping factor ζ is set to 0.7. Additionally, the response angular frequency for the AVR ω_{AVR} is one-tenth of the response angular frequency for the ACR ω_{ACR}. Moreover, ω_{ACR} is limited to one-tenth of the switching frequency f_s. According to (18), in order to calculate the required capacitance for the BTB system, it takes the fluctuation voltage, response speed, control gain, and stability control into consideration.

On the other hand, the boost-up inductance is calculated assuming that the inductor current ripple is below 4% owing to the design condition of the input inductor in the matrix converter

$$L_B = \frac{E_{\mathrm{dc}}}{\pi\omega_s I_{\mathrm{rip}}} \sin \pi D = \frac{E_{\mathrm{dc}}}{\pi\omega_s I_{\mathrm{rip}}}. \tag{20}$$

Similar to the input inductor, the volume of the boost-up inductor is calculated by (17). On the other hand, it is necessary to calculate the dc-link capacitor volume $\mathrm{Vol}_{C\mathrm{dc}}$ from the effective value of the switching ripple current I_{rip_fs} when the electrolytic capacitor is used as the dc-link capacitor. Thus, the electrolytic capacitor is selected based on the required ripple current I_{rip_fs} from the datasheet. Finally, the relationship between the volume $\mathrm{Vol}_{C\mathrm{dc}}$ and the dc-link capacitance C_{dc} is expressed as

$$\mathrm{Vol}_{C\mathrm{dc}} = k_{\mathrm{vol2}} C_{\mathrm{dc}} + k_{\mathrm{vol1}}. \tag{21}$$

Moreover, I_{rip_fs} is obtained as [29]

$$I_{\mathrm{rip}\_fs} = \frac{I_o}{\pi} \sin \pi D. \tag{22}$$

According to (22), the required electrolytic capacitor is selected assuming that I_{rip_fs} is the maximum value and *D* is set to 0.5.

D. Decision of Switching Frequency

Fig. 12 shows the Pareto–Front curve of the matrix converter. Table III lists the calculation conditions considered to decide the specification of the matrix converter at the maximum power density point. Note that the switching devices are the same as the switching device of the first prototype. In addition, the calculated efficiency includes the conduction loss, switching loss, and copper loss of the input or boost-up inductor. Moreover, the conduction loss ($P_{\mathrm{con}S}$, $P_{\mathrm{con}D}$) and the switching loss $P_{\mathrm{ton}S}$

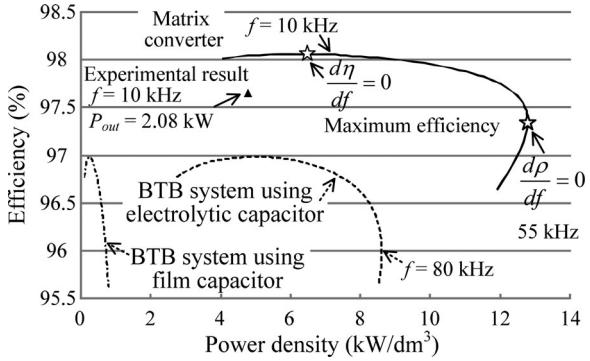

Fig. 12. Pareto–Front curves of the matrix converter and the BTB system (Rated power = 2 kW) using the film capacitor or electrolytic capacitor.

TABLE III
CALCULATION PARAMETERS TO DETERMINE THE POWER LOSS AND VOLUME OF THE MATRIX CONVERTER AND BTB SYSTEM

Rated power P_n	2 kW	Input current $I_{\rm in}$		5.77 A
C_f voltage ripple $V_{\rm rip}$	8.49 V (3%)	Current ripple $I_{\rm rip}$		0.23 A
CSPI (W/Kdm^3)	14.2	DC-link voltage $E_{\rm dc}$		350 V
Core coefficient $K_{\rm vol}$	17.3	Fluctuated voltage ΔV		10.5 V
Space factor K_u	0.5	Previous output power P_1		1 kW
Current density J	4 A/mm^2	Output power P_2		2 kW
Flux density B_m	1.23 Wb/m^2	Switching ripple current $I_{{\rm rip}\_fs}$		1.84 A
Junction temperature T_j	120 °C	Capacitor volume coefficient	$k_{\rm vol1}$ (dm^3)	1.31×10^{-3}
Ambient temperature T_a	20 °C		$k_{\rm vol2}$ (dm^3/J)	1.74×10^{-3}

of a BTB system are calculated as [34]

$$P_{{\rm con}S} = k_{{\rm cons}1} {I_o}^2 \left(\frac{1}{8} + \frac{\lambda}{3\pi}\cos\theta_o\right) + k_{{\rm cons}2} I_o \left(\frac{1}{2\pi} + \frac{\lambda}{8}\cos\theta_o\right) \quad (23)$$

$$P_{{\rm con}D} = k_{{\rm cond}1} {I_o}^2 \left(\frac{1}{8} - \frac{\lambda}{3\pi}\cos\theta_o\right) + k_{{\rm cond}2} I_o \left(\frac{1}{2\pi} - \frac{\lambda}{8}\cos\theta_o\right) \quad (24)$$

$$P_{{\rm ton}S} = \frac{E_{\rm dc} f_s}{2\pi V_s}\left(2k_{{\rm ton}1} I_o + k_{{\rm ton}2}\pi\right). \quad (25)$$

Similar to (2), $k_{\rm cons1}$, $k_{\rm cons2}$ and $k_{\rm cond1}$, $k_{\rm cond2}$, which are the on-state voltage coefficients of the switching device and the diode, respectively, are obtained from the datasheet, and λ is the modulation index. The power density design of the matrix converter takes the input *LC* filter, the switching device, and the heat sink into consideration. On the other hand, the power density design of the BTB system takes the boost-up inductor, dc-link capacitor (film capacitor or electrolytic capacitor), the switching device, and the heat sink into consideration.

TABLE IV
CONDITIONS TO DESIGN MAXIMUM POWER DENSITY FOR THE SECOND-ORDER PROTOTYPE USING SIC-MOSFET

Parameters of switch (BSM00003A)			Rated power P_n	10 kW
Turn-on loss characteristic	$k_{\rm ton1}$ (J)	8.31×10^{-5}	Input line voltage $V_{\rm in}$	283 V
	$k_{\rm ton2}$ (J/A)	3.61×10^{-5}	Rated output current I_o	47.1 A
	$k_{\rm ton3}$ (J/A^2)	-3.14×10^{-8}	Rated input current $I_{\rm in}$	40.8 A
Turn-off loss characteristic	$k_{\rm toff1}$ (J)	1.90×10^{-4}	Voltage ripple $V_{\rm rip}$	8.49 V (3%)
	$k_{\rm toff2}$ (J/A)	1.60×10^{-6}	CSPI (W/Kdm^3)	0.496
	$k_{\rm toff3}$ (J/A^2)	1.9×10^{-7}	Cooling system	Natural air
	$k_{\rm toff4}$ (J/A^3)	-7.52×10^{-10}	Junction temperature T_j	120 °C
On-state voltage characteristic	$k_{\rm con1}$ (V)	0.0	Ambient temperature T_a	20 °C
	$k_{\rm con2}$ (V/A)	0.0164	Core coefficient $K_{\rm vol}$	71
Volume of switching device	$D : 122 \times W : 45.6 \times H : 21.1$ (mm)		Space factor K_u	0.5
			Current density J	4 A/mm^2

As shown in Fig. 12, it can be confirmed that the maximum power density in the matrix converter and the BTB system are attained at 55 and 80 kHz, respectively. The efficiency and the maximum power density in the matrix converter are 97.4% and 12.8 kW/dm^3, respectively. On the other hand, the efficiency and the power density in the BTB system are 96.0% and 8.61 kW/dm^3, respectively. Thus, it is quantitatively evaluated that the power density in the matrix converter is increased by 4.19 kW/dm^3 in comparison to the BTB system. In addition, the optimized frequency depends on the converter type. In other words, it is necessary to determine the switching frequency of each of the converters by the Pareto–Front curve.

The experimental result is plotted in Fig. 12 for the switching frequency and the output power of 10 kHz and 2.08 kW, respectively. Nevertheless, the power density of the first prototype is either half of the maximum power density or less. In other words, the first prototype is designed at a low power density point. Hence, in order to improve the power density, it is necessary to design and manufacture the second prototype by the maximum power density design method.

E. Maximum Power Density Design for Second Prototype

Table IV lists the design conditions for the second prototype. Note that SiC-MOSFET (BSM00003A), with 1200-V rated voltage and 120-A rated current, is used as the switching device. It is noted that $k_{\rm toff1} - k_{\rm toff4}$ are each coefficients of the turn-off loss $e_{\rm off}$ characteristic. Thus, $k_{\rm toff1} - k_{\rm toff4}$ are obtained by the turn-off loss characteristics by polynomial approximation

$$e_{\rm off} = k_{\rm toff4} {i_o}^3 + k_{\rm toff3} {i_o}^2 + k_{\rm toff2} i_o + k_{\rm toff1}. \quad (26)$$

Fig. 13 shows the Pareto–Front curve of the matrix converter using SiC. According to the switching device, the rated power of the system is set to 40 kW. The cooling system of the heat sink and the rated output power are considered as follows: 1)

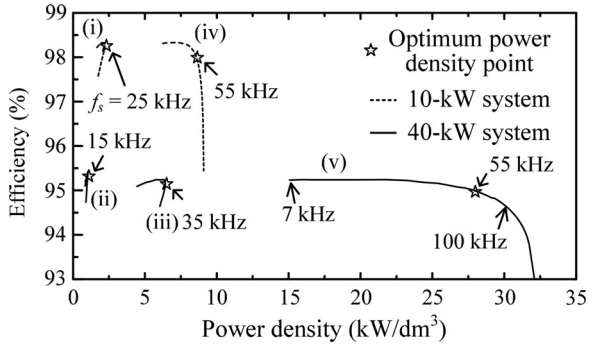

Fig. 13. Pareto–Front curve of the matrix converter using SiC-MOSFET according to output power and cooling method. (i) natural air (10 kW), (ii) natural air (40 kW), (iii) forced air (40 kW), (iv) water (10 kW), and (v) water (40 kW).

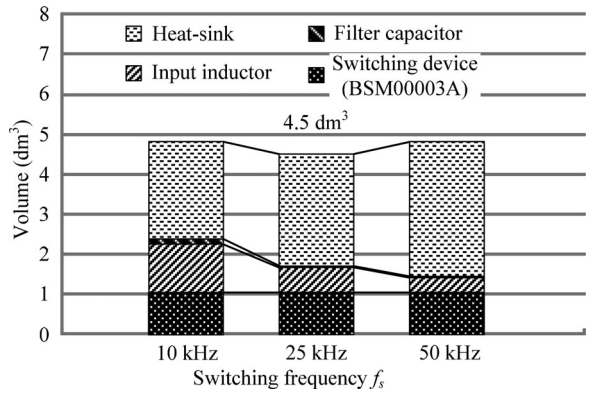

Fig. 14. Volume comparison for the switching frequency. The volume of the heat sink and input *LC* filter is a tradeoff for a given switching frequency.

the natural air cooling system and 10-kW output power, 2) the natural air cooling system (40 kW), 3) the forced air cooling system (40 kW), 4) the water cooling system (10 kW), and 5) the water cooling system (40 kW). Note that the CSPI in 3 and 4, 5 are 4.0 and 270, respectively [28]. Additionally, the conduction loss, the switching loss, no-load loss, and the copper loss of the input inductor are taken into consideration in order to evaluate the efficiency. On the other hand, the volumes of the input *LC* filter, heat sink, and switching devices are taken into consideration in order to evaluate the power density. It is confirmed that a power density of 30 kW/dm^3 can be achieved when the water cooling system is adopted.

Fig. 14 shows the volume comparison for each switching frequency. According to the result, when the switching frequency is 25 kHz, the total volume of the second prototype is less compared to that with other values of switching frequency. Although the volume of the heat sink is less at 10-kHz switching frequency, the input *LC* filter is large. On the other hand, the input *LC* filter becomes smaller when the switching frequency is 50 kHz. Nevertheless, the volume of the heat sink increases now because of the converter loss. Thus, the volumes of the heat sink, and the input *LC* filter are a tradeoff.

In this study, the prototype is manufactured with 10-kW rated power owing to the limitation of the experimental environment. From the result, it is confirmed that f_s at the maximum power density is 25 kHz. Additionally, the maximum power density is 2.21 kW/dm^3 included the protection circuit. Therefore, the

TABLE V
SPECIFICATION OF THE SECOND-ORDER PROTOTYPE USING SIC-MOSFET DESIGNED AT MAXIMUM POWER DENSITY

Maximum power density $\rho_{\max}$	2.21 kW/dm^3	Design value of the size (mm)	
Inductance value $L_{\rm in}$	110 μH	Input inductor	$D65 \times W65 \times H48$
Capacitance value C_f	8.44 μF	Filter capacitor	$D20 \times W20 \times H36$
Cooling system	Natural air	Heat-sink	$D147 \times W450 \times H42$
Switching frequency f_s	25 kHz	Switching device (BSM00003A)	$D122 \times W46 \times H:21$
Heat resistance $R_{\rm th}$	0.752 K/W	Total volume	4.5 dm^3
Efficiency	98.3%	Maximum snubber voltage $V_{\rm snu}$	450 V
Maximum surge	960 V	% Load inductance	10%
Maximum output current $I_{\max}$	84.9 A	Time constant of $C_{\rm snu}$ and $R_{\rm dc}$	10 s
D–S stray capacitance $C_{\rm snu}$	450 V	Snubber capacitance $C_{\rm ds}$	136 μF
Discharge resistor $R_{\rm dc}$	73 kΩ	Snubber loss $P_{\rm snu}$	1.0 W

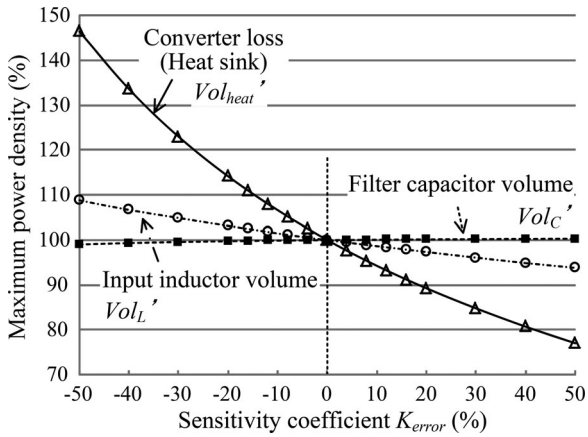

Fig. 15. Sensitivity analysis for a maximum power density design method.

input *LC* filter and the heat sink are selected for the switching frequency of 25 kHz. As a result, C_f and $L_{\rm in}$ are designed to be 8.44 μF and 110 μH. Table V lists the specification of the second prototype designed at 25-kHz switching frequency.

Fig. 15 shows a sensitivity analysis result for the maximum power density in order to validate the Pareto–Front curve when the error $K_{\rm error}$ from -50% to 50% is taken into consideration. It is noted that each maximum power densities in Fig. 15 are calculated by

$$P'_{\rm loss} = (1 + 0.01K_{\rm error})(P_{\rm con} + P_{\rm sw\_loss}) \tag{27}$$

$$\mathrm{Vol}'_L = (K_{\rm vol}(1 + 0.01K_{\rm error}))\left[\frac{L_{\rm in}{I_{\rm in}}^2}{K_u B_m J}\right]^{\frac{3}{4}} \tag{28}$$

$$\mathrm{Vol}'_C = \frac{C_f {V_{\rm in}}^2}{\varepsilon_0 \varepsilon_s (k_z(1 + 0.01K_{\rm error}))^2}. \tag{29}$$

Here, according to (11) and (12), the volume of the heat sink is determined by the converter loss $P\prime_{\rm loss}$. Thus, the error occurs to the volume of the heat sink by changing the converter loss.

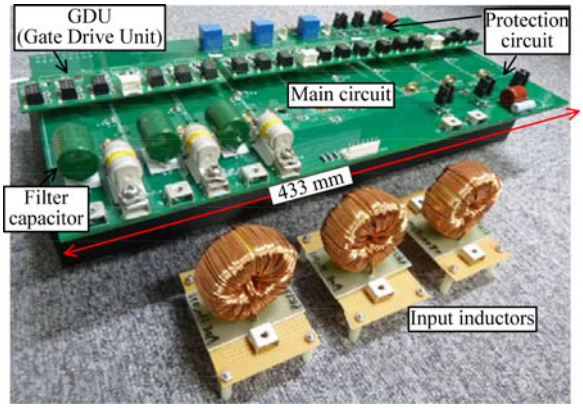

Fig. 16. 10-kW matrix converter using SiC-MOSFET (ROHM: BSM00003A). PCB size is 433 mm × 233 mm × 4 mm. The input inductance is 110 μH at 25-kHz switching frequency and 30 A. The wire resistance of the input inductors is 6 mΩ.

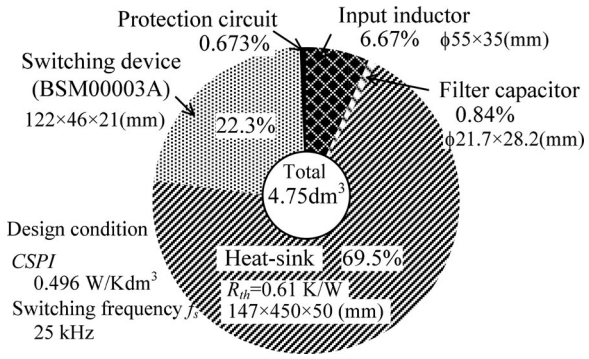

Fig. 17. Property of the volume of the matrix converter with the natural air cooling system. The volume of the heat sink is larger than other devices because the natural air cooling system is adopted in the heat sink.

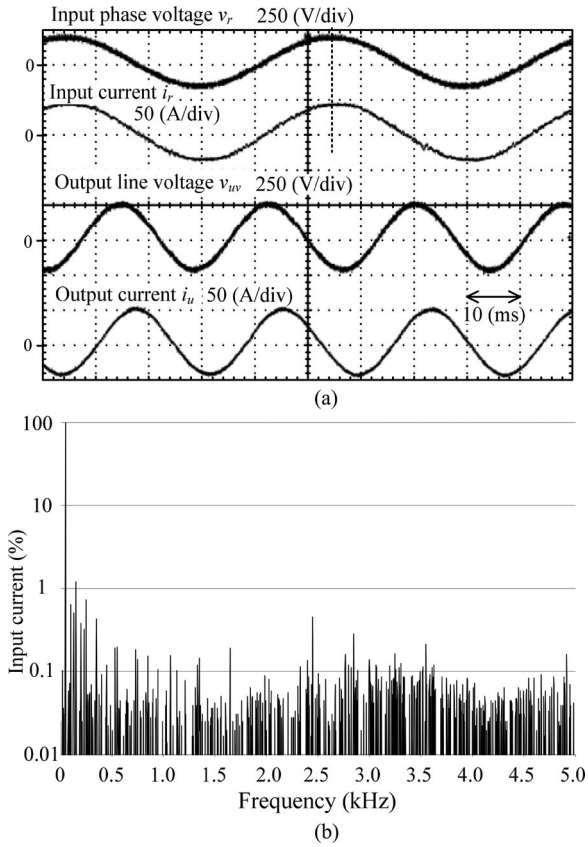

Fig. 18. Steady operation at 9.5-kW output power in the experiment. The waveforms and the input current spectrum are measured by oscilloscope (Tektronix: MSO5054). The input current THD is 2.9%. The vertical axis is normalized to 28.2-A fundamental current. (a) Input and output waveforms of the second prototype. (b) Spectrum of the input current.

As the result, it is confirmed that the error for the converter loss dominates the maximum power density. On the other hand, the error for the input *LC* filter volume is suppressed within 10% of the designed maximum power density. This is because the volume of the heat sink is larger owing to the natural air cooling system in comparison with that of the input *LC* filter. Thus, the required maximum power density can be designed when the error of the converter loss is less. In other words, the validity of the maximum power density design method can be proved.

Fig. 16 shows the second prototype and the input inductors. In order to reduce the stray inductance, the second prototype is manufactured with a printed circuit board (PCB) of size 433 mm × 233 mm × 4 mm. The switching devices, fuses, filter capacitors, current sensors, and snubber circuit are mounted on the PCB.

Fig. 17 shows the property of the volume of the second prototype. The power density of the second prototype is 2.1 kW/dm^3 included the volume of the protection circuit. Accordingly, it is confirmed that the second prototype can be manufactured at 95.0% of the calculated maximum power density point. In other words, the power density of the matrix converter is improved by 57.5% by the maximum power density design method. Thus, the validity of the maximum power density design method is confirmed by the experimental results. Nevertheless, there is a difference between the experimental value and the design value because of the difference in the design value and the manufactured value of the size of the heat sink. Moreover, the volume of the switching device is large. In order to increase power density, it is important to design the package of the switching device [35].

Thus, it is confirmed that the heat sink is bulky. In order to reduce the total volume, the forced air or water cooling system is adopted and junction temperature T_j should be higher owing to SiC device when the heat sink is designed. Accordingly, the size of the heat sink and the input *LC* filter can be reduced because the CSPI and ω_s are increased.

V. Experimental Results

Fig. 18(a) shows the operation waveforms using a 9.5-kW *RL* load. Table VI lists the experimental condition for second-order prototype. It is noted that the switching frequency is 25 kHz. In addition, two-phase modulation was adopted in the virtual inverter control. Moreover, the four-step hybrid commutation, which combines the voltage and current commutations, was adopted [27]. As a result, the unity power factor is successfully obtained.

TABLE VI
EXPERIMENTAL CONDITIONS

Input line voltage $V_{\rm in}$	200 V	Input frequency $f_{\rm in}$	50 Hz
Rated power P_n	10 kW	Output frequency f_o	90 Hz
Modulation index $\lambda_{\rm mc}$	0.866	Switching frequency $f_{\rm sw}$	25 kHz
Output line voltage $V_{\rm out}$	173 V	Load inductance	0.65 mH
Modulation method	Two-phase	Input inductor $L_{\rm in}$	110 μH
Commutation method	Four-step hybrid	Filter capacitance C_f	8.44 μF
Damping resistor R_d	–	Deadtime compensation	Adopt

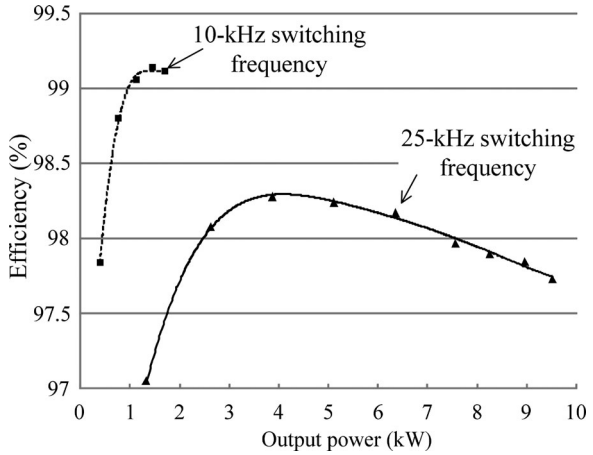

Fig. 19. Efficiency characteristics at 10- and 25-kHz switching frequency. The efficiency at maximum point are 99.1% and 98.3% at 10- and 25-kHz switching frequency, respectively.

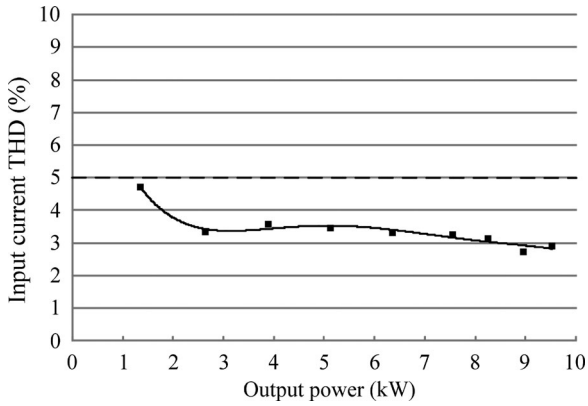

Fig. 20. Input current THD characteristic at 25-kHz switching frequency. The input current THD is below 5% when the output power is over 1 kW.

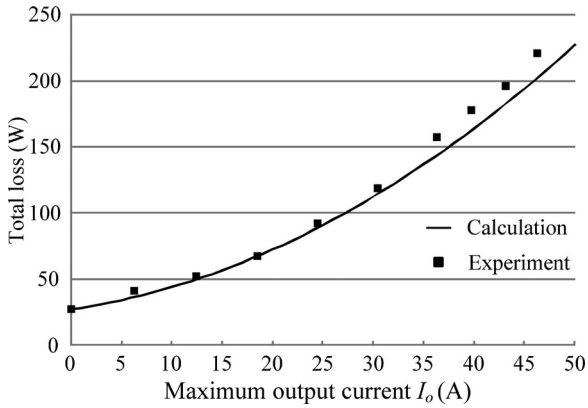

Fig. 21. Total loss characteristics comparison between the calculation and experimental result. The maximum error of the total loss is 10.6% at 6.29-A output current. This is because the harmonic component is included in the output current.

Fig. 18(b) shows the spectrum of the input current obtained by a fast Fourier transform. Note that the input current value is normalized with respect to the fundamental current, which is equal to 28.2 A. Accordingly, a large harmonic distortion does not occur. In particular, the fifth- and seventh-order harmonic components are low because the commutation failure does not occur owing to the hybrid commutation scheme employed. Moreover, the input current THD is 2.9%. Thus, the fundamental operation of the second prototype is confirmed.

Fig. 19 shows the efficiency characteristics at 10- and 25-kHz switching frequency. It is confirmed that the maximum efficiency is 99.1% at 1.5-KW output power and 10-kHz switching frequency. Nevertheless, with light loads, the efficiency becomes low owing to no-load loss. Furthermore, the total efficiency achieved in the experiment is lower than the designed efficiency. In this study, the second prototype was designed because the output power factor is unity in order to validate the maximum power density design method. That is, the output current is increased because the output power factor is low in the experiment. Thus, it is necessary to take the output power factor into consideration when the matrix converter is designed in practical applications.

Fig. 20 shows the input current THD characteristics at 25-kHz switching frequency. The input current THD is less than 5.0% over 1-kW output power. In addition, the input current THD becomes low when the output power is increased. This is because the ratio of the harmonic component to the fundamental component is degraded by the increasing output power.

Fig. 21 shows the loss characteristics for the maximum output current determined by using a power meter (YOKOGAWA: WT1600). It is noted that the total loss measured by a power meter includes the input inductor and filter capacitor loss, snubber loss, wiring loss, and converter loss. In the calculation result, the copper loss of the input inductor is included. It is confirmed that the maximum error of the total loss is 10.6% at 6.29-A output current. This is because the harmonic component is included in the output current. According to Table VI, the load inductance is set to 0.65 mH. In addition, the load resistance is 23 Ω when the loss error is measured to 10.6%. Then, the time constant of *RL*-load is calculated to 28.6 μs (35 kHz). Thus, the switching ripple of the output current is not suppressed. As the result, owing to the output current distortion, the measured output power becomes low by power meter. Moreover, there is also the other cause of loss error except for the harmonic component, such as the iron loss of the input inductor, filter capacitor loss, and wire loss. These losses, which are less in comparison with the converter loss, are not included in the calculation result.

Furthermore, the loss error increases over 36-A output current. This is caused by the snubber, wire resistor, and fuse. Thus, the interface loss should be included into the calculated loss when a large capacity power converter is designed. It is noted that the temperature characteristic for SiC device is not almost changed in comparison with that of Si device. For this reason, the total loss error is not influenced by temperature characteristic for the SiC device. However, the proposed maximum power density design method for the matrix converter is validated even when the large capacity matrix converter is designed. This is because the heat sink volume is only dominated by the switching device loss.

According to Fig. 21, the loss error between the measured value and calculated value is 18.8 W at the rated current. In the loss error, the snubber loss is increased by 1.3 W, and the loss due to the wire resistor and the fuse is 5.7 W. As a result, the device loss error is 11.8 W (5.87%). Thus, the loss error does not depend on the maximum power density design method because the switching frequency at the maximum power density point is almost unchanged. Furthermore, the proposed maximum power density design method is also validity for SiC application. The converter loss can be decreased by SiC device. As a result, the total loss depends on the passive component loss. Nevertheless, if the converter loss is decreased by adopting the SiC device, the switching frequency can be increased owing to the reduced size of heat sink. Accordingly, the passive component can be smaller. In other words, using the SiC device can reduce not only the converter loss but also the passive component loss.

Based on these results, the loss of the matrix converter can be easily estimated by loss formulas, which do not depend on the kind of switching devices. Moreover, the matrix converter can be easily designed at the maximum power density point with a Pareto–Front curve because the maximum power density of the second prototype is 95.0% of the calculated maximum power density. Thus, it is expected that the application areas of the matrix converter can be expanded owing to its advantages of energy saving and reduced size.

VI. Conclusion

In this paper, the derivation methods for the conduction loss and the switching loss in the matrix converter were presented for experiment and simulation. As the result, it was confirmed that the total loss error between the calculated and experimental results is 2.77% at the rated current with the first prototype, which is 2-kW rated power. The loss error does not depend on the maximum power density design method because the switching frequency at the maximum power density point is almost unchanged. Thus, the loss formulas for the matrix converter were validated in the experiment.

Next, the maximum power density design method for the matrix converter was proposed based on the front-loading design in order to improve power density. As the result, it was quantitatively evaluated that the power density in the matrix converter is increased by 4.19 kW/dm^3 in comparison to the BTB system. However, the power density of first prototype was 37.5% of the maximum power density point. In order to design the matrix converter at the maximum power density point, the second prototype was designed and manufactured by the maximum power density design method. Accordingly, the power density of the second prototype that uses a SiC-MOSFET as the switching device in the experiment is 95.0% (2.1 kW/dm^3). Thus, the power density of the matrix converter was improved by 57.5% by the maximum power density design method in comparison to the first prototype.

Based on these results, the loss of the matrix converter can be easily estimated by loss formulas when not only Si device but also SiC device is used. Moreover, the matrix converter can be easily designed at the maximum power density point with a Pareto–Front curve because the calculated maximum power density is 95% agreed to the experimental result. Thus, it is expected that the application areas of the matrix converter to be expanded, given its advantages of energy saving and size reduction.

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