Steady-State Analysis and Design of Class-D ZVS Inverter at Any Duty Ratio

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***Abstract*—This paper presents steady-state analytical expressions of the class-D zero-voltage switching inverter at any duty ratio along with a design example. The obtained expressions include stead-state voltage and current waveforms, output power capability, peak switch voltage, peak switch current, output power, and power conversion efficiency as functions of the duty ratio. Additionally, switching-timing allowance due to antiparallel diodes of switching devices can be predicted from the analytical results. The analytical expressions are verified by showing quantitative agreements with PSpice simulations and circuit experiments.**

***Index Terms*—Class-D ZVS inverter, duty ratio, output power, power conversion efficiency, steady-state analysis, voltage and current waveforms.**

I. Introduction

THE class-D zero-voltage switching (ZVS) inverter [1]–[21] is an improved version of the class-D inverter [22]–[24]. The class-D ZVS inverter not only maintains the inherent strengths of the basic class-D inverter, such as simple circuit architecture and low switch voltage stress, but also possesses its own advantages, for instance, low switching loss, low switching noise, and high power conversion efficiency by adopting the ZVS technology. Therefore, the class-D ZVS inverter has been a main choice in various applications. Typical applications for the class-D ZVS inverter can be found in dc–dc converters [2], ozone generators [3], induction heating [4]–[7], electrodeless fluorescent lamps [8], [9], contactless battery chargers [10], electronic discharge machining [11], etc. In the class-D ZVS inverter, the duty ratio is one of major factors for determining the circuit performance, which depends on the applications. In past designs of the class-D ZVS inverter, there are cases that the duty ratio is far from 50% [5]–[8], in particular, for high-frequency applications. Most analysis and design approaches of the class-D ZVS inverter are, however, for approximately 50% duty ratio [1]–[4], [10]–[13]. There are only a few analyses and designs of the class-D ZVS inverter at any duty ratio [5]–[8].

Generally, two approaches can be considered for analyses and designs of the switching inverter. One is transient analysis-based designs [5]–[8], [10]–[16], and the other is steady-state analysis-based ones [1]–[4], [9], [17]–[25]. In our knowledge, all the analysis approaches of the class-D ZVS inverter at any duty ratio presented till now are classified into the transient analysis. The transient analysis gives accurate waveforms and design values. If analytical waveform equations are necessary, however, the inverter should be expressed by piece-wise linear differential equations. When the differential equations are solved numerically [7], high calculation cost is necessary for obtaining the steady state from the transient analysis. This is because the resonant inverter usually takes long transient time for converging to the steady state. Additionally, the circuit parameters are usually included in the waveform equations, which are transcendental equations. Therefore, it is difficult for designers to comprehend the relationships between the circuit parameters and responses intuitively.

On the other hand, the steady-state analysis is based on the assumption that the output voltage and current are expressed as periodic functions. The fundamental-frequency-component approximation, which is one of the typical steady-state analysis methods, limits the parameter ranges, where the analytical results can be applied. This is because there are cases that the output current includes many harmonic components, e.g., when the duty ratio of the upper switch is different from that of the bottom one, and when the operating (switching) frequency is much different from the resonant frequency of the output network. The steady-state analysis, however, gives simple and easy-to-use equations for understanding the relationships between the circuit parameters and responses. In addition, it is possible to obtain a simple step-by-step design from the steady-state analytical expressions. Therefore, it can be stated that it is useful and valuable to carry out the steady-state analysis of the class-D ZVS inverter at any duty ratio, even though the accuracy of the waveform expressions is low compared with the differential equation approaches by applying the fundamental-frequency-component approximation.

In the switching-mode circuits, it is difficult to realize ideal turn on/off switching, especially for the upper switch at high frequencies. Additionally, there is a possibility that the ZVS operation cannot be achieved because of component tolerances in the implemented circuits. Non-ZVS operation yields switching losses and power conversion efficiency degradation. Generally, two strategies are considered against this problem. One is that

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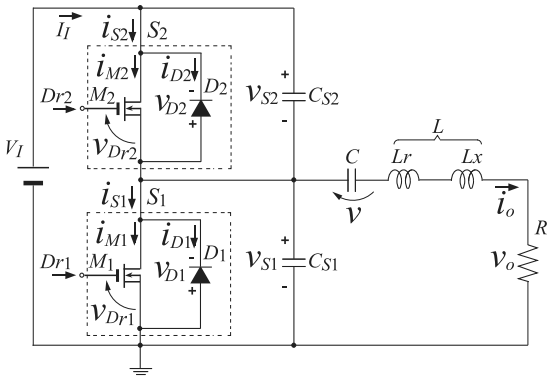


Fig. 1. Circuit topology of the class-D ZVS inverter.

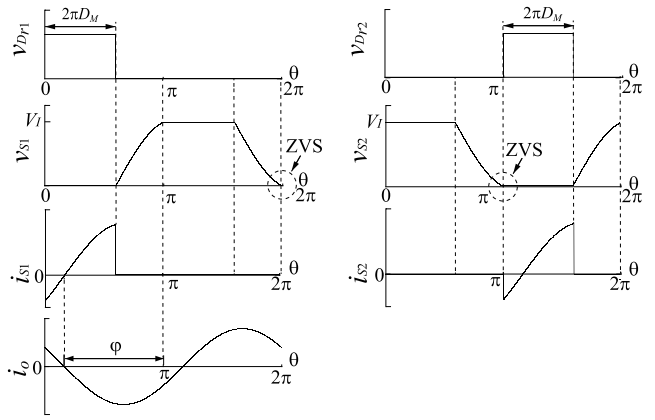


Fig. 2. Nominal waveforms of the class-D ZVS inverter.

the zero-derivative switching (ZDS) is applied to the class-D ZVS inverter, which is known as the class-DE inverter [18]–[21]. The other strategy is that a switching-timing allowance for maintaining the ZVS operation is included in the switching pattern by using the antiparallel diode of the switching devices. When the switch turns on during the time that the antiparallel diode is in on-state, it is regarded that the class-D inverter achieves the ZVS operation. Therefore, the switching time has an allowable duration by considering the antiparallel diode. The antiparallel diode, however, may generate more conduction losses than the MOSFET. Namely, there is a tradeoff relationship between the switching-timing allowance and the power conversion efficiency. Therefore, it is also helpful and valuable to predict the switching-timing allowance and power conversion efficiency of the class-D ZVS inverter analytically.

This paper presents a steady-state analysis for the class-D ZVS inverter at any duty ratio. By applying the fundamental-frequency-component approximation of the output current, it is possible to obtain simple design equations, which contribute to the intuitive understanding of the relationships between the circuit parameters and responses. The obtained analytical expressions include voltage and current waveforms, output power capability, peak switch voltage, peak switch current, output power, and power conversion efficiency as functions of the duty ratio. In addition, the switching-timing allowance can be predicted easily from the analytical expressions. A simple step-by-step design procedure by using the analytical expressions is also given. The presented analytical expressions are verified by showing quantitative agreements with PSpice simulations and circuit experiments. The designed inverter achieved the specified output power and the ZVS condition. In the laboratory measurements, the designed inverter obtained 97.4% power conversion efficiency at 100-kHz operating frequency and 10-W output power with 40% duty ratio.

II. Class-D ZVS Inverter

Fig. 1 shows a circuit topology of the class-D ZVS inverter. This circuit is composed of input voltage source V_I, two MOSFETs M_1 and M_2 with their antiparallel diodes D, and series resonant filter L–C–R. C_{S1} and C_{S2} are shunt capacitances, which include MOSFET parasitic capacitances. This paper focuses on the class-D ZVS inverter with symmetric switching operation. Namely, the duty ratio of the bottom MOSFET M_1 is the same as that of the upper one M_2.

A. Class-D ZVS Inverter

Fig. 2 shows the nominal waveforms of the class-D ZVS inverter. In this figure, $\theta = \omega t = 2\pi f t$ represents the angular time, where f is the operating frequency. The MOSFETs M_1 and M_2 turn ON and OFF alternatively. For achieving the ZVS operation, the dead time, in which both the MOSFETs are in off-state, is necessary. Namely, the duty ratio of the MOSFET D_M should be less than 0.5. There are two dead-time intervals every period in the class-D inverter operation. In the dead-time intervals, the output current discharges one of the shunt capacitance and charges the other one. Additionally, the MOSFETs M_1 and M_2 are turned on when their shunt-capacitance voltages reach zero, which is ZVS operation. Because of the ZVS operation, high power conversion efficiency can be achieved in the class-D ZVS inverter.

It is, however, difficult to realize ideal turn on/off switching, especially for the upper MOSFET at high frequencies. Additionally, there is a possibility that the ZVS operation cannot be achieved because of component tolerances in the implemented circuits. When the switching point, at which the switch voltage is zero, is shifted to the right side in Fig. 2, the ZVS operation cannot be achieved and power conversion efficiency is degraded. Generally, two strategies are considered against this problem. One is that the ZDS is applied to the class-D ZVS inverter, which is known as the class-DE inverter. The other strategy is to design the class-D ZVS inverter with a switching-timing allowance for maintaining the ZVS operation by using the antiparallel diodes of the MOSFETs.

B. Class-DE Inverter

Fig. 3 shows the nominal waveforms of the class-DE inverter. In the class-DE inverter, the switch voltage is zero and its derivative is also zero at the switch-turn-on instant, which is called the class-E ZVS/ZDS conditions. The ZDS condition realizes a zero-current switching at turn-on instant. Because there is no

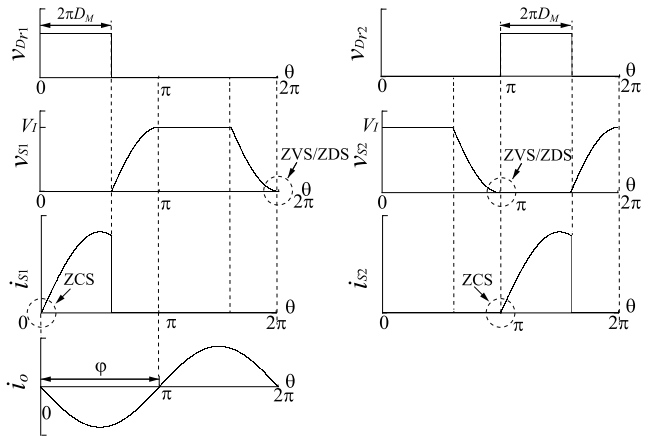


Fig. 3. Nominal waveforms of the class-DE ZVS inverter.

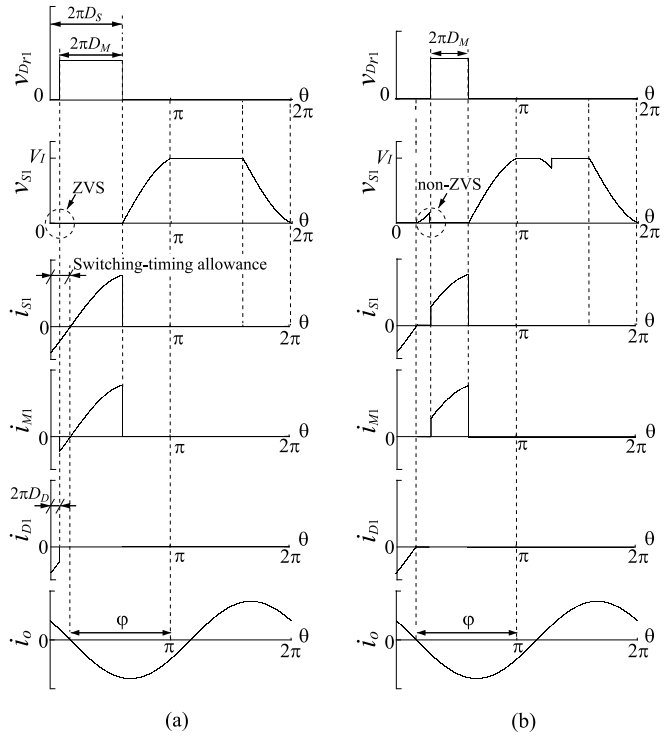


Fig. 4. Example waveforms of class-D inverter with antiparallel-diode conduction. (a) ZVS operation. (b) Non-ZVS operation.

discontinuous waveform jump of not only the switch voltage but also the switch current at turn-on instant, the class-DE inverter has strength against the switching delay and the component tolerances.

C. Class-D ZVS Inverter With Antiparallel-Diode Conduction

Fig. 4(a) shows the example waveforms of the class-D ZVS inverter with the antiparallel-diode conduction. In Fig. 4(a), the switch voltage v_{S1} reduces to be zero at $\theta = 2\pi$, namely prior to the turn-on instant of the MOSFET M_1. In this case, the antiparallel diode D_1 turns on and a negative current i_{D1} flows through the diode as shown in Fig. 4(a). Because the on-state antiparallel diode keeps the switch voltage $v_{\rm S1}$ equal to a small built-in potential, it is regarded that the switch voltage $v_{\rm S1}$ is approximately zero. Namely, it is regarded that the ZVS condition can be achieved when the MOSFET turns on during the time interval in which the antiparallel diode is in the on-state. In other words, the MOSFET M_1 has switching-timing allowance in the range of $0 \le \theta \le \pi - \varphi$ as shown in Fig. 4(a), where φ is an initial phase of the output current. Similar operation appears at the MOSFET M_2. The switching-timing allowance also has strength for the switching delay and component tolerances. In this operation, the sum of the on-duty ratio of the antiparallel diode and that of the MOSFET is expressed as the on-duty ratio of the switching device, namely $D_S = D_D + D_M$.

On the other hand, if the MOSFET M_1 turns on after the switch current changes from the negative to positive, namely at the point of $\theta > \pi - \varphi$, the switch voltage $v_{\rm S1}$ returns to positive, as shown in Fig. 4(b). In this operation mode, the ZVS operation cannot be achieved. Namely, both the turn-on switching loss and the conduction loss in the antiparallel diode yield in this non-ZVS operation mode. For avoiding this operation mode, it is useful to predict the switching-timing allowance.

III. Circuit Analysis

A. Assumptions

In this paper, the analytical expressions of the class-D ZVS inverter at any duty ratio are given. The purpose of the analysis is to obtain the relationships between the circuit parameters and circuit responses and the design equations for achieving the ZVS in the class-D inverter with simple formulations. Therefore, the analysis of the class-D inverter, which does not achieve the ZVS condition, is outside scope of this paper. The analysis of the class-D ZVS inverter presented in this paper is based on the following assumptions:

1) All the passive components work as linear components.
2) All the components have no parasitic resistances.
3) The MOSFETs and antiparallel diodes work as ideal switches. Therefore, zero-switching time, zero on-resistances, and infinite off-resistances are assumed.
4) Only the fundamental-frequency component passes through the resonant filter. It is well known that the resonant filter should be inductive for achieving the ZVS condition. Therefore, the resonant inductance L is divided into L_r and L_x virtually. The resonant filter $L_r - C$ is an ideal filter at the operating frequency f, that is, $f = 1/(2\pi\sqrt{L_r C})$. Additionally, L_x yields a phase shift of the output current.
5) The loaded quality factor Q of the series resonant filter L–C–R, which is defined as
$$Q = \frac{\omega L}{R} \tag{1}$$
is sufficiently high.
6) The duty ratio of the upper MOSFET is the same as that of the bottom one.
7) The class-D inverter achieves the ZVS operation and the waveforms as shown in Fig. 4(a). Namely, the switch

TABLE I
SWITCHING PATTERNS IN CLASS-D ZVS INVERTER

		S_1		S_2	
		D_1	M_1	D_2	M_2
$0 < \theta \le 2\pi D_S$	$0 < \theta \le 2\pi D_D$	ON	OFF	OFF	OFF
	$2\pi D_D < \theta \le 2\pi(D_D + D_M)$	OFF	ON	OFF	OFF
	$2\pi D_S < \theta \le \pi$	OFF	OFF	OFF	OFF
$\pi < \theta \le \pi + 2\pi D_S$	$\pi < \theta \le \pi + 2\pi D_D$	OFF	OFF	ON	OFF
	$\pi + 2\pi D_D < \theta \le \pi + 2\pi(D_D + D_M)$	OFF	OFF	OFF	ON
	$\pi + 2\pi D_S < \theta \le 2\pi$	OFF	OFF	OFF	OFF

voltages satisfy

$$v_{\rm S1}(2\pi) = 0 \quad \text{and} \quad v_{\rm S2}(2\pi) = V_I \tag{2}$$

and

$$v_{\rm S1}(\pi) = V_I \quad \text{and} \quad v_{\rm S2}(\pi) = 0. \tag{3}$$

8) Because of the assumptions (5) and (6), the output current is expressed by a pure sinusoidal waveform, namely

$$i_o(\theta) = I_m \sin(\theta + \varphi) \tag{4}$$

where I_m is the absolute value of the output current amplitude.

B. Waveform Equations

Because of the assumptions (6) and (7), the switching patterns in this analysis are fixed as given in Table I. The MOSFET and its antiparallel diode can be expressed as one switch S_1 and S_2 as shown in Fig. 1 because of the assumption (3).

By the KCL, the basic equation is given as

$$i_{\rm S2} + i_{C_{S2}} - i_{S1} - i_{C_{S1}} = i_o = I_m \sin(\theta + \varphi). \tag{5}$$

For $0 < \theta \le 2\pi D_S$, the switch S_1 is in the on-state. Namely, MOSFET M_1 or antiparallel diode D_1 is ON and the switch S_2 is OFF. Therefore, the normalized switch voltages are given as

$$\frac{v_{\rm S1}}{V_I} = 0 \quad \text{and} \quad \frac{v_{\rm S2}}{V_I} = 1. \tag{6}$$

Additionally, the currents through the switch S_2 and the shunt capacitances for $0 < \theta \le 2\pi D_S$ are

$$i_{\rm S2} = i_{C_{S1}} = i_{C_{S2}} = 0. \tag{7}$$

From (5) and (7), the current through the switch S_1 is

$$i_{\rm S1} = -i_o = -I_m \sin(\theta + \varphi). \tag{8}$$

For $2\pi D_S < \theta \le \pi$, both switches S_1 and S_2 are OFF. Therefore, the switch currents are

$$i_{\rm S1} = i_{\rm S2} = 0. \tag{9}$$

Additionally, by considering the relationship between the two switch voltages

$$\frac{v_{\rm S1}}{V_I} = 1 - \frac{v_{\rm S2}}{V_I} \tag{10}$$

and from (5) and (9), we have

$$i_{C_{S2}} - i_{C_{S1}} = \omega(C_{S1} + C_{S2})\frac{dv_{\rm S1}}{d\theta} = -I_m \sin(\theta + \varphi). \tag{11}$$

When we define

$$C_S = C_{S1} + C_{S2}. \tag{12}$$

Equation (11) can be rewritten as

$$\begin{aligned} \omega C_S R \frac{dv_{\rm S1}/V_I}{d\theta} &= -\frac{RI_m}{V_I}\sin(\theta + \varphi) \\ &= -\frac{V_m}{V_I}\sin(\theta + \varphi) \end{aligned} \tag{13}$$

where V_m is the absolute value of the output voltage amplitude and V_m/V_I is normalized amplitude of the output voltage. By integrating both sides of (13) with $v_{\rm S1}(2\pi D_S) = 0$, the normalized switch voltage is obtained as

$$\frac{v_{\rm S1}}{V_I} = \frac{1}{\omega C_S R}\frac{V_m}{V_I}[\cos(\theta + \varphi) - \cos(2\pi D_S + \varphi)]. \tag{14}$$

For $\pi < \theta \le \pi + 2\pi D_S$, the switch S_1 is OFF and the switch S_2 is ON. Therefore, the normalized switch voltages are

$$\frac{v_{\rm S2}}{V_I} = 0 \quad \text{and} \quad \frac{v_{\rm S1}}{V_I} = 1 - \frac{v_{\rm S2}}{V_I} = 1. \tag{15}$$

From (15), we have

$$i_{\rm S1} = i_{C_{S1}} = i_{C_{S2}} = 0. \tag{16}$$

Therefore, the switch current $i_{\rm S2}$ is expressed as

$$i_{\rm S2} = i_o = I_m \sin(\theta + \varphi). \tag{17}$$

For $\pi + 2\pi D_S < \theta \le 2\pi$, both switches S_1 and S_2 are OFF. Therefore, the two switch currents $i_{\rm S1}$ and $i_{\rm S2}$ are

$$i_{\rm S1} = i_{\rm S2} = 0. \tag{18}$$

Following a similar procedure in the interval $2\pi D_S < \theta \le \pi$, the normalized switch voltage is expressed as

$$\frac{v_{\rm S1}}{V_I} = 1 + \frac{1}{\omega C_S R}\frac{V_m}{V_I}[\cos(\theta + \varphi) + \cos(2\pi D_S + \varphi)]. \tag{19}$$

C. ZVS Condition

From (2) and (19), we have

$$\frac{RI_m}{V_I} = \frac{V_m}{V_I} = -\frac{\omega C_S R}{2\cos(\pi D_S + \varphi)\cos\pi D_S}. \tag{20}$$

Equation (20) is a relationship of the normalized amplitude of the output voltage when the ZVS condition is achieved. In the mathematical sense, however, two patterns of operations are included in (20). One is that the voltage reaches zero from the positive potential and the other is that it does from the negative potential.

In this analysis, the derivative of the switching voltage is used as a parameter. The derivative of the switching voltage reflects on the current jump at turn-on instant. When the derivative is zero, the class-E ZVS/ZDS conditions are satisfied. From (19), the derivative of the normalized switch voltage v_{S1}/V_I at $\theta = 2\pi$ can be expressed as

$$\alpha = \left.\frac{dv_{S1}(\theta)/V_I}{d\theta}\right|_{\theta=2\pi} = -\frac{1}{\omega C_S R}\frac{RI_m}{V_I}\sin\varphi. \tag{21}$$

Substituting (20) into (21), we obtain

$$\alpha = \frac{\sin\varphi}{2\cos(\pi D_S+\varphi)\cos\pi D_S}. \tag{22}$$

In the real circuit with the ZVS operation, the switch voltage needs to fall naturally from a positive potential to zero. Namely, one of the necessary conditions for the ZVS is

$$\alpha \le 0. \tag{23}$$

D. Fourier Analysis

The normalized voltages across the resistance R and the reactance L_x are expressed as

$$\frac{v_o}{V_I} = \frac{Ri_o}{V_I} = \frac{RI_m}{V_I}\sin(\theta+\varphi) = \frac{V_m}{V_I}\sin(\theta+\varphi) \tag{24}$$

and

$$\begin{aligned}\frac{v_{L_x}}{V_I} &= \frac{\omega L_x}{R}\frac{dRi_o/V_I}{d\theta} = \frac{\omega L_x}{R}\frac{RI_m}{V_I}\cos(\theta+\varphi)\\ &= \frac{V_{L_x}}{V_I}\cos(\theta+\varphi)\end{aligned} \tag{25}$$

where $V_{L_x} = \omega L_x I_m$ is the amplitude of the voltage across the reactance L_x.

From the assumption (4), the output voltage of the resonant filter has only the fundamental-frequency component of the switch voltage v_{S1}. Therefore, the normalized amplitudes V_m/V_I and V_{L_x}/V_I are obtained from Fourier series expansion for v_{S1}

$$\begin{aligned}\frac{V_m}{V_I} &= \frac{RI_m}{V_I} = \frac{1}{\pi}\int_0^{2\pi}\frac{v_{S1}}{V_I}\sin(\theta+\varphi)d\theta\\ &= -\frac{2\sin(\pi D_S+\varphi)\sin\pi D_S}{\pi}\end{aligned} \tag{26}$$

and

$$\begin{aligned}\frac{V_{L_x}}{V_I} &= \frac{1}{\pi}\int_0^{2\pi}\frac{v_{S1}}{V_I}\cos(\theta+\varphi)d\theta\\ &= \frac{1}{\pi}\{2\sin\varphi + [\sin 2\pi D_S\cos 2(\pi D_S+\varphi) - \pi + 2\pi D_S\\ &\quad - 4\cos(2\pi D_S+\varphi)\sin(\pi D_S+\varphi)\cos\pi D_S]\\ &\quad \times [2\cos(\pi D_S+\varphi)\cos\pi D_S]^{-1}\}.\end{aligned} \tag{27}$$

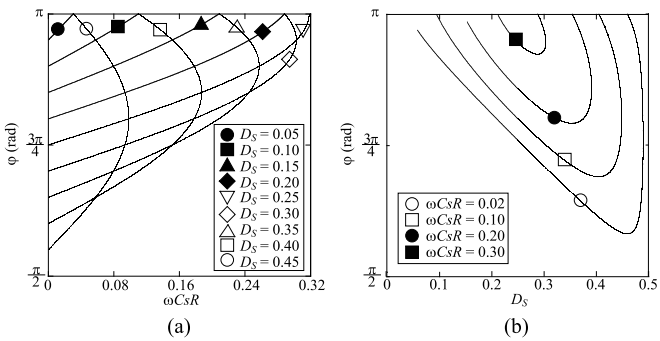


Fig. 5. φ as a function of $\omega C_S R$ and D_S. (a) φ for fixed D_S. (b) φ for fixed $\omega C_S R$.

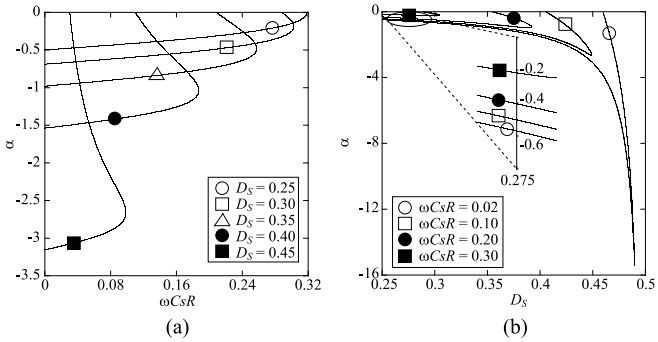


Fig. 6. α as a function of $\omega C_S R$ and D_S. (a) α for fixed D_S. (b) α for fixed $\omega C_S R$.

From (20) and (26), we obtain

$$\omega C_S R = \frac{\sin 2(\pi D_S+\varphi)\sin 2\pi D_S}{\pi}. \tag{28}$$

It can be seen from (28) that φ is a function of $\omega C_S R$ and D_S. Namely, φ is obtained when $\omega C_S R$ and D_S are fixed. It is also seen from (22) that α can be obtained from D_S and φ. In the mathematical sense, however, there are multiple solutions for φ because of the trigonometric functions. We have conditions of I_m in (20), α in (22), and $\omega C_S R$ in (28) for achieving the ZVS, namely $I_m \ge 0$, $\alpha \le 0$, and $\omega C_S R \ge 0$. From the above three conditions, the range of φ can be limited to

$$\pi(1-D_S) \le \varphi \le \pi. \tag{29}$$

Figs. 5 and 6 show φ and α as functions of $\omega C_S R$ for fixed D_S and as functions of D_S for fixed $\omega C_S R$, respectively. It is seen from Fig. 5 that the $\omega C_S R$ increases as the duty ratio decreases from $D_S = 0.5$ to 0.25. This result means that it is possible to design high-frequency class-D ZVS inverter by reducing the load resistance R and/or shunt capacitance C_S. There is, however, the minimum shunt-capacitance value, which is the same as the output capacitance of the MOSFET. When the shunt capacitance is composed of only the MOSFET output capacitance, the operating frequency can be increased by decreasing the duty ratio. Additionally, it is seen that the highest frequency can be obtained at $D_S = 0.25$ and $\varphi = \pi$. It is also seen from Fig. 5 that the $\omega C_S R$ increases as the duty ratio decreases from 0.25.

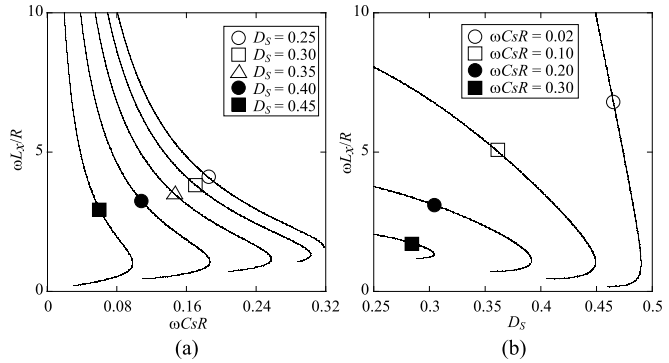


Fig. 7. $\omega L_x/R$ as a function of $\omega C_S R$ and D_S. (a) $\omega L_x/R$ for fixed D_S. (b) $\omega L_x/R$ for fixed $\omega C_S R$.

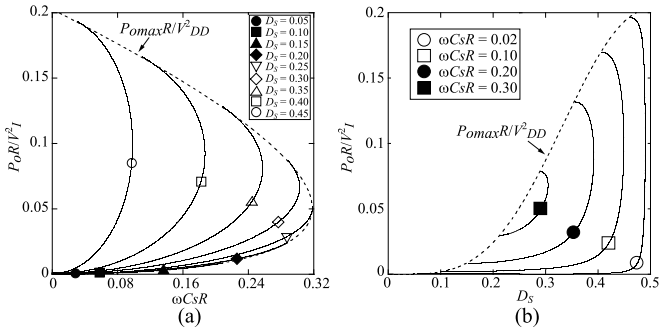


Fig. 8. Normalized output power $P_o R/V_I^2$ as a function of $\omega C_S R$ and D_S. (a) $P_o R/V_I^2$ for fixed D_S. (b) $P_o R/V_I^2$ for fixed $\omega C_S R$.

In Fig. 6, $\alpha = 0$ means that the class-D inverter achieves not only the ZVS condition but also ZDS condition. Namely, the class-D inverter for $\alpha = 0$ is the class-DE inverter. It is seen from (22) that φ of the class-DE inverter is always π at any D_S. We can confirm that all the equations for $\alpha = 0$ and $\varphi = \pi$ agree with those in [18]–[21], which is one of the proofs for validating the analytical expressions presented in this paper.

When the MOSFET M_1 and M_2 are in the off-state and the switch current is negative, the antiparallel diode is in on-state and keeps the switch voltage to be zero. Therefore, the MOSFETs do not need to turn on at $\theta = 0$ or $\theta = \pi$ strictly. Namely, the necessary condition of the diode duty ratio for achieving the ZVS is

$$0 \le 2\pi D_D < \pi - \varphi \tag{30}$$

as shown in Fig. 4(a). It can be stated from Fig. 5(a) that the permissible switching-timing allowance increases as φ decreases at any D_S and $\omega C_S R$.

From (20) and (27), we have

$$\begin{aligned}\frac{\omega L_x}{R} = & -[4\sin\varphi\cos(\pi D_S+\varphi)\cos\pi D_S - \pi + 2\pi D_S \\ & - 4\cos(2\pi D_S+\varphi)\sin(\pi D_S+\varphi)\cos\pi D_S \\ & + \sin 2\pi D_S \cos 2(\pi D_S+\varphi)]/(\pi\omega C_S R). \end{aligned} \tag{31}$$

Fig. 7 shows $\omega L_x/R$ as a function of $\omega C_S R$ for fixed D_S and as a function of D_S for fixed $\omega C_S R$. It is seen from this figure that there are maximum values of $\omega C_S R$ and D_S under the ZVS condition. Additionally, it should be noted that the L_x is used for yielding the phase shift of the output current. When L_x is not sufficiently small compared with L, namely, when $\omega L_x R$ is not sufficiently small compared with Q, the output filter characteristics does not satisfy the assumption (4).

E. Power Relations

By considering input power, output power, and their relationships, it is possible to obtain the analytical relationships between the circuit parameters and circuit responses.

The input current I_I is given by the average value of the current from the input voltage source. Therefore, we have

$$\begin{aligned} I_I = & \frac{1}{2\pi}\int_0^{2\pi}(i_{S2}+i_{C_{S2}})d\theta \\ = & \frac{1}{2\pi}\int_{\pi}^{\pi+2\pi D_S} I_m\sin(\theta+\varphi)d\theta \\ = & -\frac{I_m\sin(\pi D_S+\varphi)\sin\pi D_S}{\pi}. \end{aligned} \tag{32}$$

From (32), the normalized input resistance is

$$\omega C_S R_i = \omega C_S \frac{V_I}{I_I} = \frac{2\pi}{\tan(\pi D_S+\varphi)\tan\pi D_S}. \tag{33}$$

From (26) and (32), the normalized input power is

$$\frac{P_I R}{V_I^2} = \frac{V_I I_I R}{V_I^2} = \frac{2\sin^2(\pi D_S+\varphi)\sin^2\pi D_S}{\pi^2}. \tag{34}$$

On the other hand, the normalized output power can be obtained from (26) as

$$\frac{P_o R}{V_I^2} = \frac{1}{2}\left(\frac{V_m}{V_I}\right)^2 = \frac{2\sin^2(\pi D_S+\varphi)\sin^2\pi D_S}{\pi^2}. \tag{35}$$

It is seen from (35) that the maximum normalized output power $P_{o\max}R/V_I^2$ can be obtained for $\varphi = \pi$, i.e., when the class-D inverter achieves the ZVS/ZDS conditions. The normalized maximum output power is

$$\frac{P_{o\max}R}{V_I^2} = \frac{2\sin^4\pi D_S}{\pi^2}. \tag{36}$$

From (34) and (35), the power conversion efficiency of the ideal class-D ZVS inverter is

$$\eta = \frac{P_o}{P_I} = 1. \tag{37}$$

Fig. 8 shows the normalized output power $P_o R/V_I^2$ as a function of $\omega C_S R$ for fixed D_S and as a function of D_S for fixed $\omega C_S R$, respectively. The validity of (36) is confirmed from Fig. 8. The maximum output power increases as $\omega C_S R$ decreases and D_S increases. It is also seen from Fig. 8(a) that there is the peak value of $\omega C_S R$ for $P_o R/V_I^2$. It can be stated from Fig. 8 that it is possible to realize various applications

by changing $\omega C_S R$ and D_S of the class-D ZVS inverter. For example, it is effective to use a high D_S for high-power applications. It is, however, difficult to increase both the operating frequency and the output power. There is a limitation for obtaining high output power at high frequencies from the single class-D inverter. In this case, it is necessary to consider the other topologies such as push-pull topology.

Additionally, it is seen from Figs. 5 and 8 that both the operating frequency and the output power decreases as the duty ratio decreases from 0.25 to 0. There is no advantage of the class-D ZVS inverter in the range of $0 < D \leq 0.25$ for operating frequency and/or output power enhancements. As a result, it can be stated that the ZVS class-D inverter should be designed for $0.25 \leq D < 0.5$.

F. Design Equations

From above analytical expressions, the design equations of C_S in (28) and L_x in (31) are obtained. Therefore, design equations for L_r and C are necessary for designs of a class-D ZVS inverter.

From (1) and (31), we have

$$\begin{aligned}\frac{\omega L_r}{R} &= \frac{\omega L}{R} - \frac{\omega L_x}{R} \\ &= Q + [4\sin\varphi\cos(\pi D_S + \varphi)\cos\pi D_S - \pi + 2\pi D_S \\ &\quad - 4\cos(2\pi D_S + \varphi)\sin(\pi D_S + \varphi)\cos\pi D_S \\ &\quad + \sin 2\pi D_S \cos 2(\pi D_S + \varphi)]/(\pi\omega C_S R). \end{aligned} \tag{38}$$

From the assumption (4) and (38), the normalized resonant capacitance ωCR is

$$\begin{aligned}\omega CR &= \frac{R}{\omega L_r} \\ &= \pi\omega C_S R/[\sin 2\pi D_S \cos 2(\pi D_S + \varphi) + \pi\omega C_S RQ \\ &\quad + 4\sin\varphi\cos(\pi D_S + \varphi)\cos\pi D_S - \pi + 2\pi D_S \\ &\quad - 4\cos(2\pi D_S + \varphi)\sin(\pi D_S + \varphi)\cos\pi D_S]. \end{aligned} \tag{39}$$

IV. Power Output Capability and Power Conversion Efficiency

In this section, analytical predictions of the power output capability and power conversion efficiency of the class-D ZVS inverter at any duty ratio are derived at any duty ratio.

A. Power Output Capability

The definition of the power output capability C_p is

$$\begin{aligned}C_p &= \frac{P_o}{|V_{\mathrm{S1max}} I_{\mathrm{S1max}}| + |V_{\mathrm{S2max}} I_{\mathrm{S2max}}|} \\ &= \frac{P_o R}{V_I^2 \left(\left| \frac{V_{\mathrm{S1max}}}{V_I} \frac{RI_{\mathrm{S1max}}}{V_I} \right| + \left| \frac{V_{\mathrm{S2max}}}{V_I} \frac{RI_{\mathrm{S2max}}}{V_I} \right| \right)}, \end{aligned} \tag{40}$$

where V_{S1max}, V_{S2max}, I_{S1max}, and I_{S2max} are the peak values of voltages and currents at the switches S_1 and S_2. Because the maximum switch voltage is the same as the input voltage, we have

$$\frac{V_{\mathrm{S1max}}}{V_I} = \frac{V_{\mathrm{S2max}}}{V_I} = 1. \tag{41}$$

In the range of $\pi(1 - D_S) \leq \varphi < 3\pi/2 - 2\pi D_S$, the switch turns off prior to the peak current of the output current flows through the switch. On the other hand, the peak point appears during the switch-on state when $3\pi/2 - 2\pi D_S \leq \varphi \leq \pi$ is satisfied. Therefore, the normalized maximum current of the switch is obtained by using (26) as

$$\begin{aligned}\frac{RI_{\mathrm{S1max}}}{V_I} &= \frac{RI_{\mathrm{S2max}}}{V_I} \\ &= \begin{cases} \left| \frac{RI_m}{V_I} \sin 2\pi D_S \right| \\ = \left| -\frac{2\sin(\pi D_S + \varphi)\sin 2\pi D_S \sin\pi D_S}{\pi} \right|, \\ \text{for } \pi(1 - D_S) \leq \varphi < \frac{3\pi}{2} - 2\pi D_S \\ \left| \frac{RI_m}{V_I} \right| = \left| -\frac{2\sin(\pi D_S + \varphi)\sin\pi D_S}{\pi} \right|, \\ \text{for } \frac{3\pi}{2} - 2\pi D_S \leq \varphi \leq \pi \end{cases} \end{aligned} \tag{42}$$

Therefore, the power output capability can be rewritten as

$$\begin{aligned}C_p &= \frac{P_o R}{2V_I^2 \left| \frac{RI_{\mathrm{S1max}}}{V_I} \right|} \\ &= \begin{cases} \left| \frac{\sin(\pi D_S + \varphi)\sin\pi D_S}{2\pi \sin 2\pi D_S} \right|, \\ \text{for } \pi(1 - D_S) \leq \varphi < \frac{3\pi}{2} - 2\pi D_S \\ \left| -\frac{\sin(\pi D_S + \varphi)\sin\pi D_S}{2\pi} \right|, \\ \text{for } \frac{3\pi}{2} - 2\pi D_S \leq \varphi \leq \pi. \end{cases} \end{aligned} \tag{43}$$

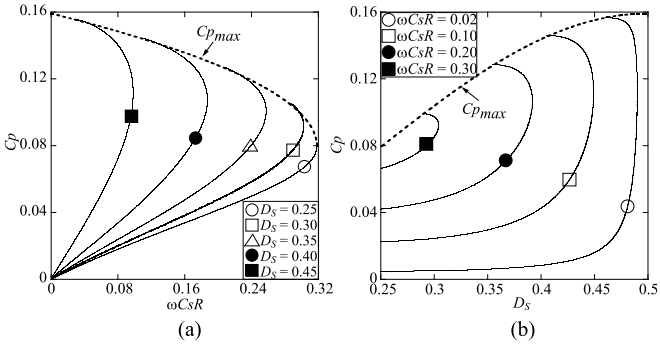


Fig. 9. Power output capability C_p as a function of $\omega C_S R$ and D_S. (a) C_p for fixed D_S. (b) C_p for fixed $\omega C_S R$.

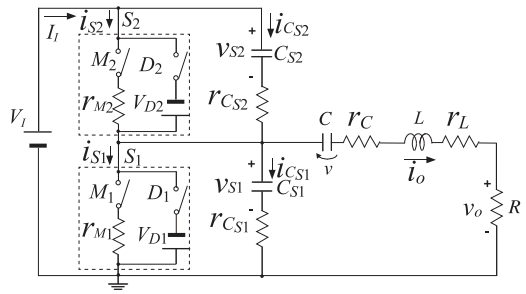


Fig. 10. Equivalent circuit of class-D inverter including ESR.

It is seen from (43) that the maximum power output capability $C_p\text{max}$ can be obtained for $\varphi = \pi$, namely

$$C_p\text{max} = \frac{\sin^2 \pi D_S}{2\pi}. \tag{44}$$

Fig. 9(a) and (b) shows the power output capability C_p and $C_p\text{max}$ as a function of $\omega C_S R$ for fixed D_S and as a function of D_S for fixed $\omega C_S R$, respectively. It is seen from Fig. 9 that the maximum output power capability increases as $\omega C_S R$ decreases and D_S increases.

We would like to emphasize that all the graphs from Figs. 6–9 are drawn by using the normalized dimensionless parameters. Namely, these are the general characteristics of the class-D ZVS inverter, which are independent of power levels and operating frequencies. It is too difficult to obtain these dimensionless-parameter graphs from the transient analysis-based approach. Much information about relationships between the circuit parameters and responses can be obtained from these figures, which show the usefulness and effectiveness of the analysis with the fundamental-frequency-component approximation.

B. Power Conversion Efficiency

In real circuits, the power losses occur in the parasitic resistance of each component. In this paper, we consider the power losses in MOSFET-on resistances r_{M1} and r_{M2}, on-state antiparallel diodes, equivalent series resistances (ESRs) of the loaded network r_L and r_C, and shunt capacitances $r_{C_{S1}}$ and $r_{C_{S2}}$ as shown in Fig. 10. It is assumed that the parasitic resistances are small enough not to affect the waveforms.

For $2\pi D_S < \theta \le 2\pi$, the switch current i_{S1} is zero. From (8), the power loss in the diode D_1 of the switch S_1 is

$$\begin{aligned} P_{r_{D1}} &= \frac{1}{2\pi}\int_0^{2\pi} -V_{D1} i_{S1}\, d\theta \\ &= \frac{1}{2\pi}\int_0^{2\pi D_D} -V_{D1}[-I_m \sin(\theta+\varphi)]\, d\theta \\ &= \frac{V_{D1} I_m}{\pi} \sin\pi D_D \sin(\pi D_D + \varphi) \end{aligned} \tag{45}$$

where V_{D1} is the forward voltage drop of the antiparallel diode. Because of symmetric operation, we have

$$P_{r_{D2}} = P_{r_{D1}}. \tag{46}$$

The power losses in the MOSFET-on resistances are

$$\begin{aligned} P_{r_{M1}} &= P_{r_{M2}} = \frac{1}{2\pi}\int_0^{2\pi} r_{M1} i_{S1}^2\, d\theta \\ &= \frac{1}{2\pi}\int_{2\pi D_D}^{2\pi D_S} r_{M1}[-I_m \sin(\theta+\varphi)]^2\, d\theta \\ &= \frac{r_{M1} I_m^2}{4\pi}\{2\pi(D_S - D_D) - \sin 2\pi(D_S - D_D) \\ &\quad \cos 2[\pi(D_S + D_D) + \varphi]\}. \end{aligned} \tag{47}$$

The power loss in the ESRs of the resonant circuit is

$$P_{r_{LC}} = \frac{1}{2\pi}\int_0^{2\pi} (r_C + r_L) i_o^2\, d\theta = \frac{(r_C + r_L) I_m^2}{2}. \tag{48}$$

Finally, the power losses in the ESRs of the shunt capacitances are given by

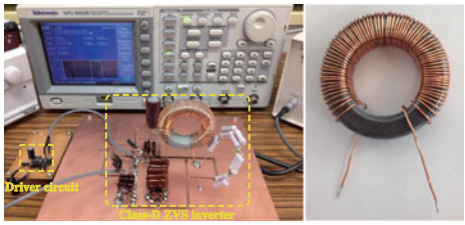
$$\begin{aligned} P_{r_{C_{S1}}} &= P_{r_{C_{S2}}} = \frac{1}{2\pi}\int_0^{2\pi} r_{C_{S1}} i_{C_{S1}}^2\, d\theta \\ &= \frac{1}{2\pi}\int_{2\pi D}^{\pi} r_{C_{S1}} \left(\omega C_{S1} \frac{dv_{S1}}{d\theta}\right)^2 d\theta \\ &= \frac{r_{C_{S1}} I_m^2}{8\pi}\left[\int_{2\pi D_S}^{\pi} \sin^2(\theta+\varphi) \right. \\ &\quad \left. + \int_{\pi+2\pi D_S}^{2\pi} \sin^2(\theta+\varphi)\right] \\ &= \frac{r_{C_{S1}} I_m^2}{8\pi}[\pi(1-2D_S) + \sin 2\pi D_S \cos 2(\pi D_S + \varphi)]. \end{aligned} \tag{49}$$

From (45) to (49), the power conversion efficiency is

$$\begin{aligned} \eta = {} & P_o \times (P_o + P_{r_{LC}} + P_{r_{D1}} + P_{r_{D2}} + P_{r_{M1}} + P_{r_{M2}} \\ & + P_{r_{C_{S1}}} + P_{r_{C_{S2}}})^{-1} \\ = {} & P_o \times (P_o + P_{r_{LC}} + 2P_{r_{D1}} + 2P_{r_{M1}} + 2P_{r_{C_{S1}}})^{-1} \\ = {} & \left\langle 1 + \frac{r_C + r_L}{R} - \frac{2V_{D1}}{R}\frac{\sin\pi D_D \sin(\pi D_D + \varphi)}{\sin\pi D_S \sin(\pi D_S + \varphi)} \right. \\ & + \frac{r_{M1}}{\pi R}\{2\pi(D_S - D_D) - \sin 2\pi(D_S - D_D) \\ & \times \cos 2[\pi(D_S + D_D) + \varphi]\} + \frac{r_{C_{S1}}}{2\pi R}[\pi(1-2D_S) \\ & \left. + \sin 2\pi D_S \cos 2(\pi D_S + \varphi)]\right\rangle^{-1}. \end{aligned} \tag{50}$$

V. Design Example

This section shows a step-by-step design example and confirms the validity of the analytical expressions by comparing with PSpice-simulation and experimental results. The design specifications of the class-D ZVS inverter are: input voltage $V_I = 80$ V, operating frequency $f = 100$ kHz, loaded quality factor $Q = 3$, output power $P_o = 10$ W, and load resistance $R = 50\ \Omega$.



(a) (b)

Fig. 11. Experimental setup. (a) Overview of implemented circuit. (b) Resonant inductor.

The IRF510 MOSFETs were used as switching devices. In addition, $D_S = 0.4$ is also given.

From (35), we have $\varphi = 2.6$ rad. Substituting φ into (28), $\omega C_S R$ is calculated as

$$\omega C_S R = \frac{\sin 2(\pi D_S + \varphi)\sin 2\pi D_S}{\pi} = 0.0925. \quad (51)$$

Therefore, the shunt capacitance is

$$C_S = \frac{\omega C_S R}{\omega R} = 5.89 \text{ nF}. \quad (52)$$

From (1), the resonant inductance is obtained as

$$L = \frac{QR}{\omega} = 239\ \mu\text{H}. \quad (53)$$

From (39), we have

$$\begin{aligned} C = {} & \pi C_S / [\sin 2\pi D_S \cos 2(\pi D_S + \varphi) + \pi \omega C_S R Q \\ & + 4\sin\varphi \cos(\pi D_S + \varphi)\cos\pi D_S - \pi + 2\pi D_S \\ & - 4\cos(2\pi D_S + \varphi)\sin(\pi D_S + \varphi)\cos\pi D_S] \\ = {} & 18 \text{ nF}. \end{aligned} \quad (54)$$

From (20), the output current amplitude is given as

$$I_m = -\frac{\omega C_S R}{2\cos(\pi D_S + \varphi)\cos\pi D}\frac{V_I}{R} = 0.632 \text{ A}. \quad (55)$$

Because the condition that $3\pi/2 - 2\pi D_S = 2.20 < (\varphi = 2.6) < \pi$ is satisfied, the maximum switch current can be obtained from (42) as

$$I_{\text{S1max}} = I_m = 0.632 \text{ A}. \quad (56)$$

It is confirmed that $I_{S\text{max}}$ is much smaller that the permissible drain current of the IRF510 MOSFET, which is 5.6 A. Therefore, it is estimated that the MOSFETs of the designed class-D inverter can work at the room-temperature. From (43) and (56), the output power capability is

$$C_p = \frac{P_o R}{2V_I^2 \left| \frac{R I_{\text{S1max}}}{V_I} \right|} = 0.0988. \quad (57)$$

Fig. 11 shows the overview of the implemented circuit and resonant inductor. The Micrometals iron-powder toroidal core T-200-3 was used as a core of the resonant inductor. Additionally, the polyurethane copper wire whose diameter is 0.65 mm was used as the winding wire with 74 turns. After implementing

TABLE II
PARAMETER VALUES FOR POWER CONVERSION EFFICIENCY ESTIMATIONS

r_L	r_{M1}	V_{D1}
0.836 Ω	0.54 Ω	0.8 Ω

the resonant inductor, $r_L = 0.836\ \Omega$ was measured by HP4194A impedence/gain-phase analyzer at 100 kHz. The HP4194A provides the ESR values from the total power loss of an inductor, which consists of the winding loss and the core loss. Additionally, $r_{M1} = r_{M2} = 0.54\ \Omega$ were obtained from the datasheet of IRF510 MOSFET. Because it can be estimated that the MOSFETs of the class-D inverter works at the room-temperature in this experiment, the usage of the datasheet value is of relevance for confirming the accuracy of the analytical predictions. Furthermore, the ESRs of capacitances were ignored in this design because they are much smaller than the other ESRs. Table II gives the parameter values for power conversion efficiency estimations. From (50), the power conversion efficiency can be predicted as

$$\begin{aligned} \eta = {} & \left\langle 1 + \frac{r_L}{R} - \frac{2V_{D1}}{R}\frac{\sin\pi D_D \sin(\pi D_D + \varphi)}{\sin\pi D_S \sin(\pi D_S + \varphi)} \right. \\ & + \frac{r_{M1}}{\pi R}\{2\pi(D_S - D_D) - \sin 2\pi(D_S - D_D) \\ & \left. \times \cos 2[\pi(D_S + D_D) + \varphi]\} \right\rangle^{-1} \\ \approx {} & 97.5\%. \end{aligned} \quad (58)$$

Table III gives parameters and characteristics from analytical expressions, PSpice simulations, and experimental measurements for the designed inverter with $D_M = 0.4$ and $D_D = 0$. This table also give the PSpice-simulation and experimental results for $D_M = 0.35$ and $D_M = 0.2$. In Table III, the power conversion efficiency of the PSpice simulation and experimental measurements were obtained from

$$\eta = \frac{P_o}{P_I} = \frac{V_o^2}{RV_I I_I} \quad (59)$$

where V_o is the root-mean-square value of the output voltage. In the experimental measurements, V_o, V_I, and I_I were measured by LeCroy's WavePro7000 1-GHz Oscilloscope and the current probe of Hioki3272 power supply. In the PSpice simulations, the input current and the output voltage could be calculated by

$$I_I = \frac{1}{2\pi}\int_0^{2\pi} (i_{S2} + i_{CS2}) d\theta \quad (60)$$

and

$$V_o = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} v_o^2 d\theta} \quad (61)$$

respectively. In addition, the experimental power-added efficiency η_{PAE} is obtained from

$$\eta_{\text{PAE}} = \frac{P_o - P_{\text{Dr1}} - P_{\text{Dr2}}}{P_I} = \frac{P_o - P_{\text{Dr1}} - P_{\text{Dr2}}}{V_I I_I} \quad (62)$$

TABLE III
DESIGN VALUES OF CLASS-D ZVS INVERTER

	Analytical	Simulated	Measured	Analytical	Simulated	Measured	Analytical	Simulated	Measured
	$D_M = 0.4$			$D_M = 0.35$			$D_M = 0.2$		
C_S	5.89 nF	5.89 nF	5.93 nF	5.89 nF	5.89 nF	5.93 nF	5.89 nF	5.89 nF	5.93 nF
L	239 μH	239 μH	236 μH	239 μH	239 μH	236 μH	239 μH	239 μH	236 μH
C	18.0 nF	18.0 nF	18.0 nF	18.0 nF	18.0 nF	18.0 nF	18.0 nF	18.0 nF	18.0 nF
R	50.0 Ω	50.0 Ω	50.3 Ω	50.0 Ω	50.0 Ω	50.3 Ω	50.0 Ω	50.0 Ω	50.3 Ω
V_I	80.0 V	80.0 V	80.3 V	80.0 V	80.0 V	80.4 V	80.0 V	80.0 V	80.6 V
I_I	0.125 A	0.125 A	0.126 A	0.125 A	0.127 A	0.126 A	0.091 A	0.110 A	0.111 A
V_{S1max}	80.0 V	80.6 V	81.9 V	80.0 V	80.7 V	81.9 V	80.0 V	80.7 V	83.2 V
V_{S2max}	80.0 V	80.6 V	83.0 V	80.0 V	80.7 V	83.2 V	80.0 V	80.7 V	83.2 V
I_{S1max}	0.632 A	0.611 A	0.612 A	0.632 A	0.612 A	0.610 A	0.571 A	0.552 A	0.6 A
I_{S2max}	0.632 A	0.611 A	0.611 A	0.632 A	0.612 A	0.608 A	0.571 A	0.551 A	0.6 A
φ	2.60 rad	2.63 rad	2.64 rad	2.60 rad	2.63 rad	2.64 rad	2.55 rad	2.64 rad	2.63 rad
V_o	22.4 V	22.1 V	22.3 V	22.4 V	22.2 V	22.3 V	20.2 V	19.7 V	19.8 V
P_o	10.0 W	9.77 W	9.85 W	10.0 W	9.87 W	9.85 W	8.16 W	7.76 W	7.79 W
P_{Dr1}	–	–	24.0 mW	–	–	23.4 mW	–	–	14.5 mW
P_{Dr2}	–	–	27.8 mW	–	–	26.0 mW	–	–	17.3 mW
C_p	0.0988	0.0996	0.0976	0.0988	0.0999	0.0979	0.0892	0.0869	0.0713
η	97.5%	97.5%	97.4%	97.3%	97.1%	97.2%	90.7%	88.2%	87.1%
η_{PAE}	–	–	96.8%	–	–	96.7%	–	–	86.7%

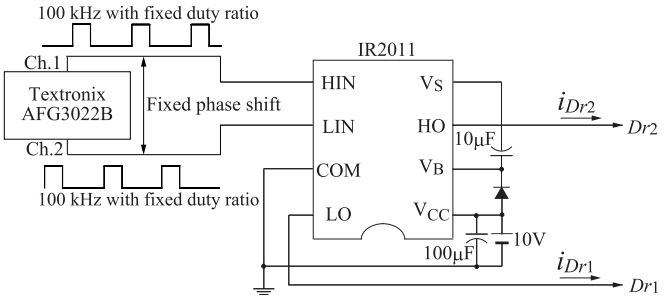


Fig. 12. Driver circuit.

where $P_{\mathrm{D}rk}$ is the driving power to the MOSFET M_k. Fig. 12 shows the driver circuit in the experiment. The driver circuit was built by the dual-channel function generator Textronix AFG3022B, which generates two kinds of arbitral signals with a fixed phase shift, and the IR2011 high- and low-side driver. The measured driving power given in Table III could be obtained from

$$P_{\mathrm{D}rk} = \frac{1}{2\pi}\int_0^{2\pi} v_{\mathrm{D}rk} i_{\mathrm{D}rk} d\theta \tag{63}$$

where $i_{\mathrm{D}rk}$ is the output current of the driver circuit, which was measured by LeCroy's WavePro7000 1-GHz Oscilloscope and the current probe of Hioki3272 Power Supply. The passive element values including the parasitic resistances in Table III were measured by the HP4194A Impedence/Gain-Phase Analyzer.

Fig. 13 shows the waveforms from the analytical expressions, PSpice simulations, and experimental measurements for $D_M =$ 0.4, 0.35, and 0.2. The results for $D_M = 0.35$ and $D_M = 0.2$ were obtained by changing the on-duty ratio of the driving voltage from $D_M = 0.4$. The analytical waveforms for $D = 0.2$, which is non-ZVS operation, is obtained from fundamental-frequency-component approximation. Because of page limitation, the waveform equations with non-ZVS operation are not given in this paper. The LeCroy's WavePro7000 1-GHz Oscilloscope with the current probe of Hioki3272 Power Supply was used for the current-waveform measurements.

It is seen from Fig. 13 that the analytical waveforms agreed with both the PSpice simulation and experimental waveforms quantitatively. In Fig. 13(a), all the waveforms satisfy the ZVS condition and specified output power. It is also confirmed from Table III that the analytical predictions of the power conversion efficiency and the output power capability showed the good agreements with the PSpice-simulation and experimental results. These results verified the presented analytical expressions. In the experimental measurements, 97.4% power conversion efficiency was achieved at the 10 W output power and 100-kHz operating frequency. In addition, it is seen from Fig. 13(a) and (b) that waveforms for $D_M = 0.35$ are almost the same as those for $D_M = 0.4$ except driving voltages. Because of $\varphi =$ 2.6 rad, the switching allowance $\pi - \varphi = 0.54$ rad is obtained. Namely, the maximum D_D and the minimum D_M are 0.09 and 0.31, respectively, for achieving the ZVS operation. Therefore, waveforms for $D_M = 0.35$ showed the quantitative agreements with those for $D_M = 0.4$. It can be stated from these results that the designed class-D ZVS inverter had a switching-timing allowance for achieving the ZVS condition and high power conversion efficiency could be kept due to the ZVS technology. The power conversion efficiency for $D_M = 0.35$, however, reduced slightly compared with that for $D_M = 0.4$ as given in Table III. This is because the conduction loss causes in the antiparallel diode. It is seen from Fig. 13(c) that the ZVS was not achieved because the switch turns on after the switch current changes sign. The output current was still a sinusoidal waveform and all the waveforms from the analytical expressions, PSpice simulation, and circuit experiment showed quantitative agreements.

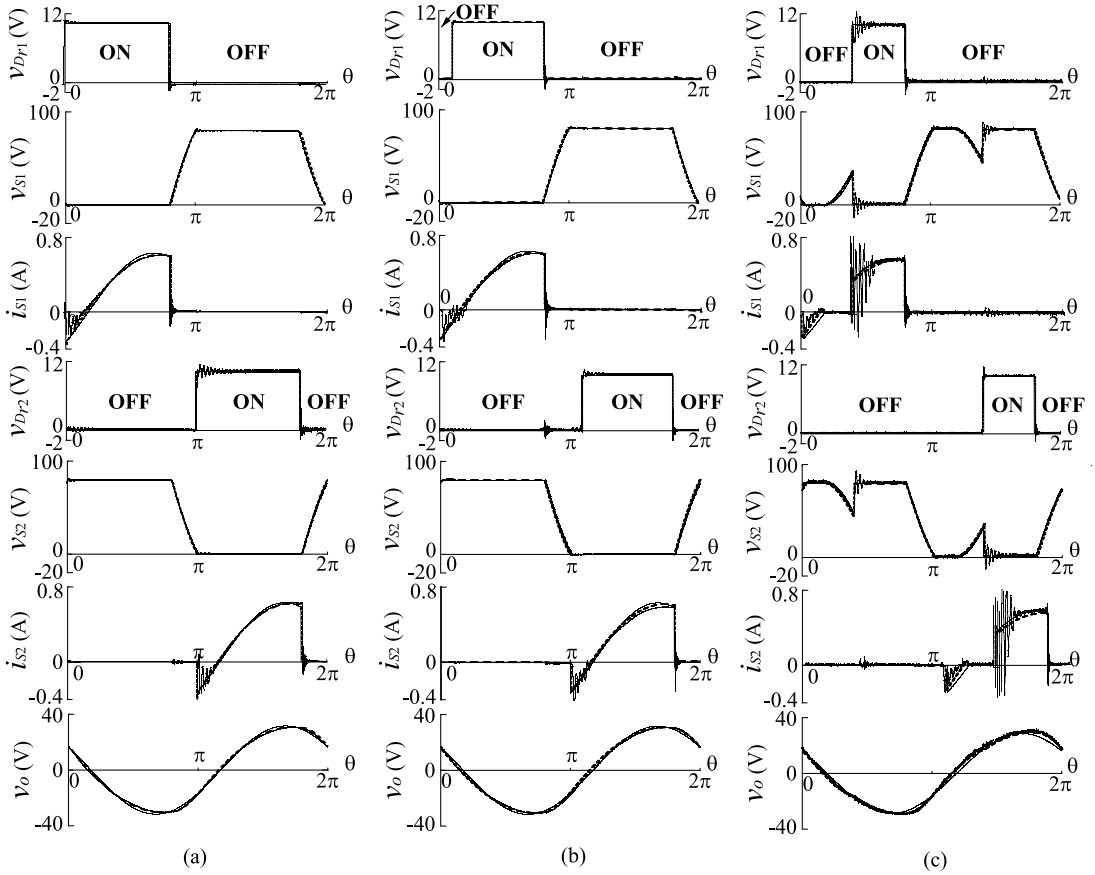


Fig. 13. Waveforms obtained from analytical expressions (solid line), PSpice simulations (dashed line), and circuit experiments (dotted line). (a) For $D_M = 0.4$. (b) For $D_M = 0.35$. (c) For $D_M = 0.2$.

Therefore, it can be stated that the analytical expressions based on the fundamental-frequency-component approximation are valid for low duty ratio. The implemented inverter was designed for $Q = 3$, which is not high Q value. The fundamental-frequency-component approximation is usually invalid for low Q, for example, in the class-E inverter [25]. However, the fundamental-frequency-component approximation was valid in this case because of the symmetric operation of the class-D inverter.

VI. Conclusion

This paper has presented the steady-state analytical expressions of the class-D ZVS inverter at any duty ratio. By applying the fundamental-frequency-component approximation of the output current, the simple design equations and the relationships between the circuit parameters and responses are derived. From the obtained expressions, output power capability, peak switch current and voltage, and power conversion efficiency can be obtained analytically. The simple step-by-step design procedure is also given along with PSpice-simulation and experimental results. The analytical expressions were verified by the quantitative agreements with both the PSpice simulations and the circuit experiments. In the laboratory measurements, the designed inverter achieved 97.4% power conversion efficiency at 100-kHz operating frequency and 10-W output power with 40% duty ratio. The analytical predictions showed good agreement with PSpice simulation and experimental results.

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