Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter

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***Abstract*—Switched-capacitor (SC) converters are gaining popularity due to their high power density and suitability for on-chip integration. Soft-charging and resonant techniques can be used to eliminate the current transient during the switching instances, and improve the power density and efficiency of SC converters. In this paper, we propose a split-phase control scheme that enables the Dickson converter to achieve complete soft-charging (or resonant) operation, which is not possible using the conventional two-phase control. An analytical method is extended to help in the analysis and design of split-phase controlled Dickson converters. The proposed technique and analysis are verified by both simulation and experimental results. An 8-to-1 step-down Dickson converter with an input voltage of 150 V and rated power of 36 W is built using GaN FETs. The converter prototype demonstrated a five fold reduction in the output impedance (which corresponds to conduction power loss) compared to a conventional Dickson converter, as a result of the split-phase controlled soft-charging operation.**

***Index Terms*—Dickson, GaN, soft-charging, switched-capacitor converter, split-phase control.**

I. Introduction

INDUCTORS and transformers are essential in conventional switch-mode power converters for voltage conversion. However, because the magnetic components have relatively low energy density, they often dominate the size and cost of a converter. On the other hand, switched-capacitor (SC) converters use only capacitors to transfer energy and consequently can have higher power density and greater suitability for on-chip integration compared to magnetic-based converters. They can also achieve a higher efficiency at large voltage conversion ratios compared to their magnetic counterparts, due to lower component rating and less extreme duty ratio requirements [1]. These advantages make SC converters desirable for a broad range of applications, including voltage balancing [2], [3], energy buffering [4], CMOS integrated power conversion [5]–[7] and renewable energy harvesting [8]. However, SC converters also have some drawbacks, which limit their performance in some applications [9]. Since the capacitors are directly charged/discharged by other capacitors or voltage sources, large transient current spikes can occur, which reduce the efficiency of the converter. Moreover, these transient effects increase the device stress and can cause undesirable electromagnetic interference problems. To mitigate the current spikes, either large capacitors or higher switching frequencies have to be employed, neither of which is a satisfactory solution. Interleaved designs [10]–[12] can reduce the current spike at the output and input terminals, but do not solve the fundamental efficiency concerns.

Recently, merged two-stage converters have been demonstrated, which can eliminate the current transient using soft-charging operation, while simultaneously improving the efficiency [13], [14]. In this architecture, the output capacitor of a step-down SC converter stage is removed and a second-stage buck converter is cascaded to the output of the SC converter to act as a controlled current load. As a result, the SC stage is allowed to operate with a larger capacitor voltage ripple without adversely affecting the efficiency, which improves the energy utilization of the capacitors. The second-stage buck converter operates with a low voltage stress, enabling an increase in the switching frequency, thereby reducing the magnetic component size. The soft-charging technique can result in significant power density and efficiency improvements [14]–[16]. A formal method was presented in Ref. [17] to aid in the design of such soft-charging SC converters. In addition, it has been shown that an inductor alone at the output of the SC converter can replace the second-stage converter while soft-charging operation can still be achieved [17]–[19]. There are also other similar techniques of using inductors to eliminate the current transient, such as resonant soft-switching techniques, based on various SC converter topologies [2], [20]–[24]. In addition, it has been shown in Ref. [17] that any two-phase step-down SC converter that is able to achieve soft-charging operation is also able to achieve resonant operation with a single inductor at the output.

Among the various SC converter topologies, the Dickson converter [5], [25], [26], whose schematic is shown in Fig. 2, has efficient utilization of switches but poor utilization of capacitors [18]. This is because the voltage ratings on the switches are either $2V_{\rm out}$ or $V_{\rm out}$, but the voltage ratings of the flying capacitors (C_1, C_2, ..., C_N) are $V_{\rm out}$, $2V_{\rm out}$, ..., $NV_{\rm out}$, respectively, where $V_{\rm out}$ is the output voltage of a step-down configuration and N is the voltage step-down ratio. A variant of the Dickson converter is the multilevel modular capacitor clamped converter (MMCCC) [27]. MMCCC converters have the same equivalent circuits as the Dickson converters, but resort to a more modular realization at the cost of increased number of

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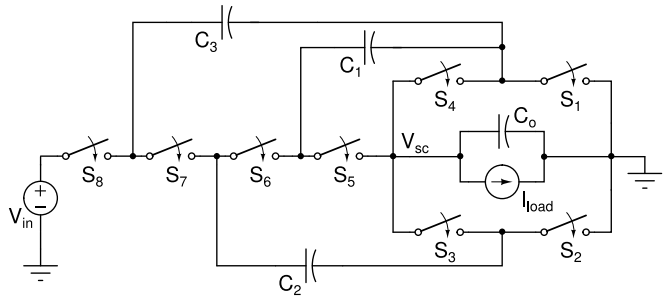

Fig. 1. 4-to-1 Dickson topology.

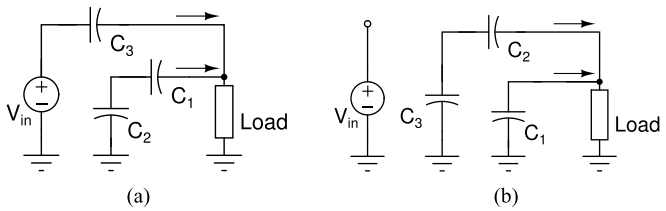

Fig. 2. Two-phase operation of a 4-to-1 Dickson converter. (a) Phase 1. (b) Phase 2.

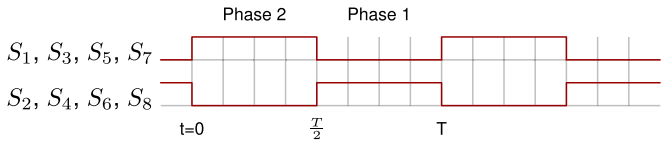

Fig. 3. Gate signals of switches for two-phase operation of Dickson converter. High represents ON and low represents OFF.

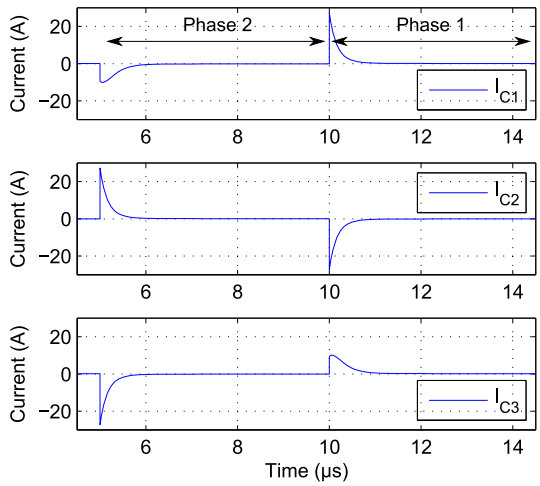

Fig. 4. Capacitor current waveforms of the Dickson SC converter in conventional *two-phase hard-charging* operation. Simulation parameters are given in Table I.

switches. Since soft-charging or resonant operation eliminates the current transient and allows smaller flying capacitor values without adversely affecting the efficiency, the power density of the Dickson converter can be significantly improved with such techniques. However, it has been demonstrated that the Dickson SC converter cannot achieve complete soft-charging operation with conventional, two-phase control and a single inductor [28]. Likewise, resonant zero current switching operation for MM-CCC converters to date has only been achieved with multiple inductors in the circuit [22], [23]. In this study, it is shown that complete soft-charging operation with a single inductor is possible for the Dickson (and the MMCCC) converter, something that to date has not been demonstrated. A technique to achieve complete soft-charging operation is proposed, by splitting the original two switching phases into four phases [29]. The proposed technique does not introduce any additional components to the two-phase soft-charging converter, and can be realized with a small additional control effort. The proposed technique and analysis are confirmed by simulation as well as experimental measurements of a converter prototype. This study represents an expansion of our earlier conference paper [30], and includes a more extensive analysis of the proposed control method, with detailed derivations of the operation of the converter. Moreover, we provide additional experimental results that clearly illustrate the performance improvements enabled by the proposed method.

The remainder of this paper is organized as follows: Section II describes the operation of conventional Dickson converters. It explains why complete soft-charging operation is not achievable using the original two-phase control, and proposes the split-phase control technique so that complete soft-charging operation is achieved. In Section III, existing analytical methods are expanded to aid in the analysis and design of split-phase Dickson converters. Section IV presents the simulation results as well as experimental results based on a 36-W split-phase controlled soft-charging Dickson converter prototype. Finally, the conclusions are given in Section V.

II. Achieving Complete Soft-charging Operation of Dickson Converter

A. Conventional Dickson SC Converter

A conventional 4-to-1 step-down Dickson SC converter is shown in Fig. 1 and the two conventional switching phases are shown in Fig. 2. It should be clarified that "phase" in this paper refers to the state of the switching circuit [1] and should not be confused with the use of "multi-phase", which is sometimes used to mean interleaved SC designs [12]. The control signals for the two-phase operation are given in Fig. 3, and as can be seen, the converter simply operates at a 50% duty ratio. For conventional (hard-charging) operation, the flying capacitor network is directly connected to the output, with a large output capacitance C_o acting as a voltage-source load. Thus, a large current transient occurs during the phase switching instances due to the capacitor voltages mismatch and the resultant charge redistribution process. This is the characteristic of the slow switching limit (SSL) of SC converters [1]. The current waveforms for the capacitors of the converter in SSL operation are shown in Fig. 4, using the simulation parameters given in Table I. It can be seen that there is a large impulse current through each capacitor (and thus through switches) at phase transitions. To minimize the voltage mismatch among the capacitors and the resultant current impulse, large capacitors or high switching

TABLE I
SIMULATION PARAMETERS

V_{in}	40 V
I_{load}	2 A
f_{sw}	100 kHz
$R_{ds,\text{on}}$	10 mΩ
R_{ESR}	1 mΩ
C_1, C_2, C_3	10 μF
$C_{o,\text{hard-charging}}$	100 μF
$C_{o,\text{soft-charging}}$	None

frequency has to be employed such that the converter operates in the fast switching limit (FSL) [1].

B. Incomplete Soft-charging Operation with Conventional Two-Phase Control

In soft-charging operation, the output capacitance is removed so that the output voltage of the SC stage can change instantaneously to compensate for the difference in capacitor voltages. By eliminating the voltage mismatch and the resultant current impulse, soft-charging SC converters exhibit the same behavior as an SC converter in FSL, while operating at a switching frequency corresponding to the SSL region of a conventional design. As a result, the flying capacitors are allowed to have larger voltage ripples without reducing the efficiency, and this increases the energy utilization of the capacitors and thus the power density of SC converters. In order to shield the load from the large voltage ripple at the output port of the soft-charging SC converter, an interfacing element must be placed between the SC stage and the load. Practical implementations of the interfacing element can be either a low voltage magnetic converter [13] or an LC filter [17]–[19], but for the purpose of clear illustration, the simulation in this section simply removes the output capacitor and uses a constant current source to represent the combination of the interfacing element and the voltage-source load.

While the current load ensures that there is no transient current drawn from the SC converter due to the voltage mismatch between the capacitor network and the final output node, complete soft-charging operation also requires that there is no voltage mismatch among the internal capacitor connections of the SC stage, so that there is no charge redistribution within the flying capacitor network [17]. For example, by applying KVL to the equivalent circuits in Fig. 2, the following requirements can be found for complete soft-charging operation

$$\text{Phase 1} : V_{\text{in}} - V_{C_3} = V_{C_2} - V_{C_1} \quad (1)$$

$$\text{Phase 2} : V_{C_3} - V_{C_2} = V_{C_1}. \quad (2)$$

However, constraints (1) and (2) *cannot* be satisfied during the transition between phases when the Dickson converter is operated with a conventional, two-phase control scheme. Fig. 5 shows the voltage and current waveforms of interest during the transition from Phase 2 to Phase 1. It can be seen that, due to the charging and discharging process in Phase 2, the two voltage values, $(V_{\text{in}} - V_{C_3})$ and $(V_{C_2} - V_{C_1})$ are different

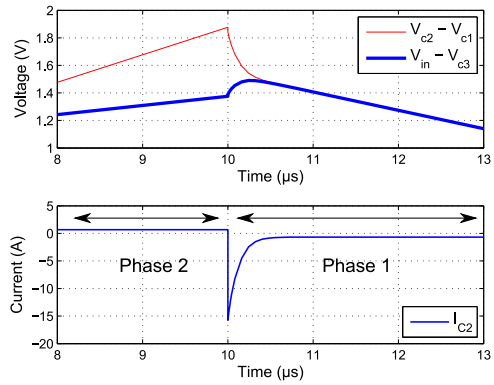

Fig. 5. Voltage and current waveforms for two-phase soft-charging operation of the Dickson converter.

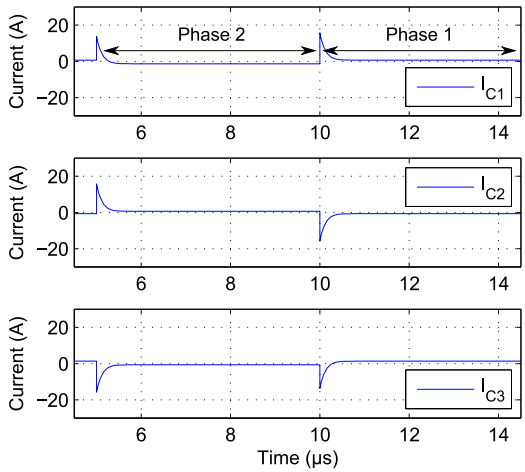

Fig. 6. Capacitor current waveforms of the Dickson SC converter in *two-phase soft-charging* operation. Simulation parameter are given in Table I.

and diverging. Thus, when the converter transitions to Phase 1 and forces the two nodes to have the same voltage, charge redistribution occurs. This results in the large current impulse as seen in the bottom plot of Fig. 5, which shows the current through capacitor C_2 of Fig. 1. A similar scenario happens at the start of Phase 2, when $(V_{C_3} - V_{C_2})$ is always greater than V_{C_1}, making it also a hard-charging transition from Phase 1 to Phase 2.

From a circuit intuition point-of-view, the voltage mismatch is due to the asymmetry in the capacitor connection, particularly for the outer most (C_3) and inner most capacitor (C_1). As can be seen in Fig. 2, these two capacitors are in series with another capacitor in one phase but not in the other phase. As a result, not all current paths have the same equivalent capacitance, giving rise to voltage mismatch when transitioning to the other phase of operation. Therefore, unlike topologies such as series-parallel and Fibonacci, the Dickson SC converter cannot achieve complete soft-charging operation, despite using a current load. The current waveforms of all capacitors for the Dickson converter with a current-source load are plotted in Fig. 6. Comparing it to the hard-charging case in Fig. 4, while the magnitude and width of the current impulse are reduced with two-phase soft-charging

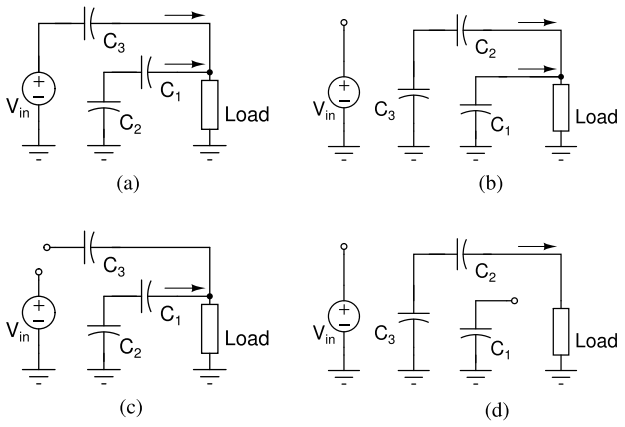

Fig. 7. Split-phase operation of a 4-to-1 Dickson converter. Switching sequence: 1b→1a→2b→2a. (a) Phase 1a. (b) Phase 2a. (c) Phase 1b. (d) Phase 2b.

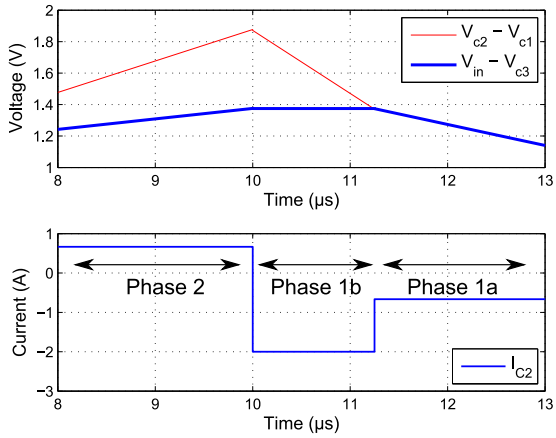

Fig. 8. Voltage and current waveforms for split-phase soft-charging operation of the Dickson converter.

operation, there is still significant transient effect and associated losses, owing to the internal capacitor voltage mismatch.

C. Complete Soft-Charging Operation with Proposed Split-Phase Control

To ensure that each branch in the capacitor network results in the same voltage at the output node, we propose the split-phase control of the Dickson converter, with two secondary phases introduced [29], [30], as shown in Fig. 7. Phase 1a and 2a are the same as Phase 1 and Phase 2 in the original operation, while the Phase 1b configuration is a subset of Phase 1 and the Phase 2b configuration is a subset of Phase 2. The switching sequence is Phase 1b → Phase 1a → Phase 2b → Phase 2a. As can be seen from the schematic in Fig. 7(c), in Phase 1b, C_2 discharges and C_1 charges, and thus $(V_{C_2} - V_{C_1})$ decreases while $(V_{\rm in} - V_{C_3})$ remains constant. The circuit can transition from Phase 1b to Phase 1a when $(V_{C_2} - V_{C_1})$ equals $(V_{\rm in} - V_{C_3})$, i.e., when (1) is satisfied. This process is illustrated in the voltage and current waveforms of Fig. 8. As can be seen, with the introduction of the additional "buffer" phase, 1b, KVL is satisfied during phase transitions and the current transient can be eliminated.

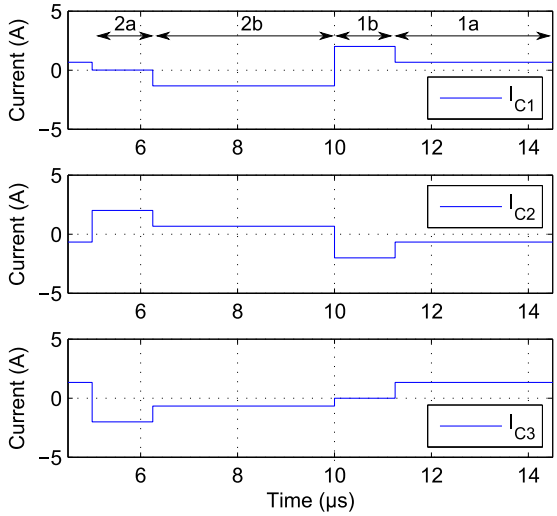

Fig. 9. Capacitor current waveforms of the Dickson SC converter in *split-phase soft-charging* operation. Simulation parameters are given in Table I.

TABLE II
THE AVERAGE, RMS AND PEAK VALUES OF CURRENT OF CAPACITOR C_2 IN A SINGLE HALF PERIOD

Configuration	Average (A)	RMS (A)	Peak (A)
Hard-charging	1.00	3.52	27.3
Soft-charging two-phase	1.00	1.91	15.8
Soft-charging split-phase	1.00	1.15	2.00

Simulation Parameters are given in Table I.

Similarly, the circuit transitions from Phase 2b to Phase 2a when (2) is satisfied. The effect on the overall current waveform can be seen in Fig. 9, which shows the currents through all the capacitors in one complete switching cycle. It can bee seen that, in contrast to the waveforms in Figs. 4 and 6, all of the currents have no transient component, and are of a constant value in each phase.

To quantify the improvement in the power transfer, the average, RMS and peak values of capacitor current for a half-period duration are calculated and tabulated in Table II. For SC converters, the average capacitor current represents the delivered power, and is hence held fixed in this comparison. The RMS current reflects the conduction loss of the switches and capacitors, and should be as close to the average value as possible for high efficiency operation. It can be seen that two-phase soft-charging operation reduces the RMS and peak values of the capacitor current, but to a limited extent. On the other hand, the proposed split-phase control achieves both the lowest RMS values and the lowest peak values. By eliminating the current transient, the converter efficiency can be improved and the current stress of the devices reduced.

The switch control signals to achieve the proposed split-phase operations are shown in Fig. 10. It can be seen that compared to the original two-phase control in Fig. 3, the proposed switching sequence only delays the turn-on of two switches (S_5 and S_8). Thus, generating the extra phases in the split-phase operation

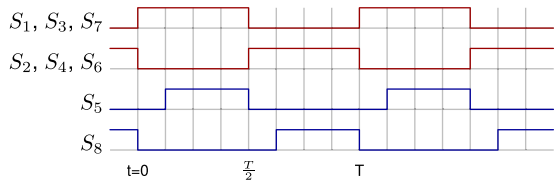

Fig. 10. Gate signal for split-phase operation of the Dickson converter. High represents ON and low represents OFF.

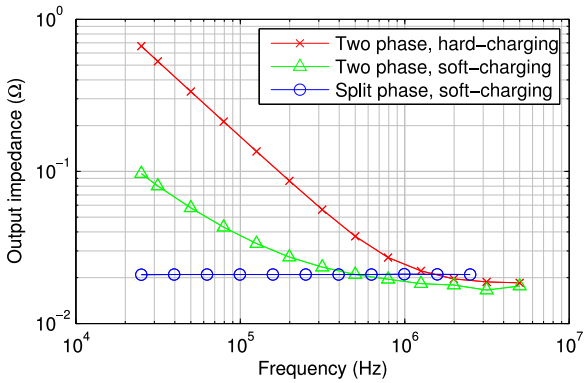

Fig. 11. Simulated output impedance of the Dickson converter.

does not increase the switching frequency of the switches, and therefore introduces no added switching loss. Another advantage of the proposed split-phase control is the scalability of the technique. Even though the technique is illustrated with a 4-to-1 Dickson converter with only three flying capacitors, it can be applied to Dickson converters with larger conversion ratios without introducing more secondary phases [29]. This is because only the switch that connects to the input voltage and the switch that connects to the innermost capacitor (C_1) needs to be delayed. Additional switches for higher conversion ratios follow the original gate signals as do switch S_6 and S_7. Therefore, there is no increase in control complexity as the conversion ratio increases.

D. Output Impedance Comparison

The output referred impedance of an SC converter encapsulates both the capacitor charge transfer loss and the conduction loss of the converter and is widely used to characterize the performance of such converters [31]–[33]. The output impedance can be calculated as

$$R_{\text{out}} = \frac{\frac{V_{\text{in}}}{N} - V_{\text{out}}}{I_{\text{out}}} \tag{3}$$

where N is the conversion ratio. For a given switching frequency and converter volume, it is desirable to have an output impedance that is as low as possible. To illustrate the benefit of the split-phase soft-charging operation, the 4-to-1 step-down Dickson converter shown in Fig. 1 is simulated using Spice with simulation parameters given in Table I. In the hard-charging operation, the duty ratio is fixed to 0.5 (as is convention) while the duty ratio of the split-phase operation is as found analytically in Section III. The output impedance is plotted against switching frequency in Fig. 11. It can be seen that the conventional hard-charging Dickson converter shows two regions of asymptotic behaviors as found in the previous literature [1]. At low frequencies (slow switching limit, SSL), when the power loss due to the current transient dominates, the impedance decreases as the switching frequency increases. The impedance reaches a constant at high frequencies (fast switching limit, FSL), when the resistive conduction loss dominates. With two-phase soft-charging operation, the impedance in the SSL region is reduced significantly, owing to the current-source load. However, there is still nonnegligible frequency dependent behavior since complete soft-charing operation cannot be achieved with two-phase Dickson converter. With the proposed split-phase control, however, it can be seen that now the output impedance is both low and independent of the switching frequency, due to the complete elimination of the charge transfer losses. Therefore, using split-phase control, soft-charging Dickson converters can achieve significant efficiency and power density improvement. It should be noted that the impedance at high frequencies in split-phase operation is slightly higher than the FSL impedance of the conventional two-phase operation. This is due to the fact that in the added phases (Phase 1b and Phase 2b), there is one path less that delivers current to the load, resulting in a slightly increased effective switch resistance. However, this increase in conduction loss will diminish as the converter conversion ratio increases.

III. Analysis

While Section II presents an intuitive understanding why the split-phase control eliminates the current transient in the operation of the Dickson converter, it is beneficial to formulate a general analysis. Existing numerical analysis methods such as proposed in Ref. [34] can provide accurate predictions on the performance of SC converters. Instead, this paper focuses more on analytical tools that provide additional insights on the operation of the proposed control. An analytical method was presented in Ref. [28] that determines whether an arbitrary SC topology is able to achieve complete soft-charging operation. However, the method in Ref. [28] was developed for an SC converter with two phases, and for the proposed split-phase control, a total of four different circuit states are present. Hence, the method in Ref. [28] is extended in this section to a higher number of phases. With a higher number of phases, the duty ratio of each phase is not known. Therefore, unlike in Ref. [28], where the capacitor values required by soft-charging operation are found given the expected duty ratio, the objective here is to find the corresponding duty ratios for complete soft-charging operation, given a set of capacitor values.

As explained in Section II, complete soft-charging can be achieved if and only if the internal capacitor network satisfies KVL at all times, including at phase transitions. The aim of the analysis is thus to find the set of charge flow vectors for the capacitors, such that the corresponding capacitor voltage changes result in node voltages that satisfy KVL during all phase transitions. To represent the KVL constraint, a voltage vector is first defined for the circuit elements as

$$\mathrm{v} = \begin{bmatrix} v_{\text{in}} & \mathbf{v_c}^{\mathrm{T}} & v_{\text{out}} \end{bmatrix}^{\mathrm{T}}, \tag{4}$$

TABLE III
DUTY RATIO OF EACH PHASE FOR THE DICKSON TOPOLOGY AT DIFFERENT CONVERSION RATIOS

Conversion ratio	4:1	6:1	8:1	N:1
D_{1a}	$3/8$	$4/12$	$5/16$	$(N+2)/4N$
D_{2a}	$3/8$	$4/12$	$5/16$	$(N+2)/4N$
D_{1b}	$1/8$	$2/12$	$3/16$	$(N+2)/4N$
D_{2b}	$1/8$	$2/12$	$3/16$	$(N+2)/4N$

where $\mathbf{v_c}$ is a column vector of the capacitor voltages. In each phase of Fig. 7, the circuit consists of a number of closed loops, where a KVL equation can be written for each loop. These KVL equations can be lumped into a matrix-vector product form [35] as

$$\mathbf{A_i v^i} = \mathbf{0} \tag{5}$$

where $\mathbf{A_i}$ is called the reduced loop matrix for the ith phase. In this analysis, the entries of the loop matrices are positive if the circuit element is traversed from the negative terminal to the positive terminal and vice versa. At the end of phase i, the voltage vector becomes $\mathbf{v^i} + \mathbf{\Delta v^i}$, due to charge being delivered to the load, and the KVL equations become

$$\mathbf{A_i}(\mathbf{v^i} + \mathbf{\Delta v^i}) = \mathbf{0}. \tag{6}$$

From (5) and (6), we have from the property of linear circuits:

$$\mathbf{A_i \Delta v^i} = \mathbf{0}. \tag{7}$$

Similar to the voltage vector, a charge flow vector is defined as the vector of charge that flows into the positive terminal of each element in the circuit and is given in the form of

$$\mathbf{q} = \begin{bmatrix} q_{\rm in} & \mathbf{q_c}^{\rm T} & q_{\rm out} \end{bmatrix}^{\rm T} \tag{8}$$

where $\mathbf{q_c}$ is a column vector of charges that flow into the flying capacitors. In the ith phase, KCL equations can be expressed by

$$\mathbf{B_i q^i} = \mathbf{0}, \tag{9}$$

where $\mathbf{B_i}$ represents the reduced incidence matrix of the topology [35]. Entries of $\mathbf{A_i}$ and $\mathbf{B_i}$ can be directly obtained from KVL and KCL equations of the circuit. Moreover, for a capacitor, the change in voltage and the charge flow is related by

$$q_c = C\Delta v_c\,. \tag{10}$$

In addition, for periodic steady-state operation, there is also a condition being that the net charge that flows into a capacitor in a period is zero

$$\sum_{\rm phase} \mathbf{q_c^i} = \mathbf{0}. \tag{11}$$

Combining the constraints given by (7), (9), (10) and (11), a set of nonzero charge vectors ($\mathbf{q^i}$) required for soft-charging operation can be obtained. A detailed derivation of the charge flow vectors from the constraints for the four-phase Dickson converter in Fig. 7 is provided in the appendix and only the result is given in this section. Using equal flying capacitor values, the final charge vectors are found to be

$$\mathbf{q^i} = \begin{bmatrix} q_{\rm in} \\ q_{c3} \\ q_{c2} \\ q_{c1} \\ q_{\rm out} \end{bmatrix}, \mathbf{q^{1a}} = \begin{bmatrix} -2 \\ 2 \\ -1 \\ 1 \\ 3 \end{bmatrix}, \mathbf{q^{2a}} = \begin{bmatrix} 0 \\ -1 \\ 1 \\ -2 \\ 3 \end{bmatrix}$$
$$\mathbf{q^{1b}} = \begin{bmatrix} 0 \\ 0 \\ -1 \\ 1 \\ 1 \end{bmatrix}, \mathbf{q^{2b}} = \begin{bmatrix} 0 \\ -1 \\ 1 \\ 0 \\ 1 \end{bmatrix}. \tag{12}$$

From the definition in (8), the last entries in the charge vectors are the amount of charge delivered to the load. Assuming a constant current load, the last entry of each of the charge vectors is thus in proportion to the relative duration of each phase. Since the total charge delivered to the load in a period is 8 units ($3+3+1+1$), we derive that for complete soft-charging operation of the Dickson converter with equal flying capacitance, the duty ratio of each phase is

$$D^{1a} = \frac{3}{8},\ D^{2a} = \frac{3}{8},\ D^{1b} = \frac{1}{8},\ D^{2b} = \frac{1}{8}. \tag{13}$$

These duty ratios are what were used to obtain the simulation results in Fig. 9. In addition, the required duty ratio for complete soft-charging operation varies with the native conversion ratio. Similar analysis has been carried out for conversion ratios of 6:1 and 8:1, and the results are shown in Table III. It can be seen that, as the conversion ratio increases, the duty ratios of the "a" phases approach 0.25 each and those of "b" phases approach 0.25 each. Thus, there is no extreme duty ratio as the conversion ratio increases.

Another useful result that can be obtained from the analysis is that soft-charging operation can be achieved regardless of the order of the switching phases, since the preceding derivation does not rely on the sequence of the phases. With the proposed split-phase control, there are four phases. These four phases can be ordered to form six distinct periodic sequences in total, and three representative ones are shown below. While Sequence 1 is the same sequence obtained from the voltage balance intuition in Section II, Sequence 2 is the reverse of Sequence 1; and in Sequence 3, the two original phases (Phase 1a and 2a) are adjacent instead of being separated by the secondary phases. The duration of each phase is still given by the constraint of (13).

Switching sequences:

1) Phase 1b → Phase 1a → Phase 2b → Phase 2a.
2) Phase 2a → Phase 2b → Phase 1a → Phase 1b.
3) Phase 1a → Phase 2a → Phase 1b → Phase 2b.

Fig. 12 shows the simulated current waveforms for these switching sequences. It can be seen that all three of the switch-

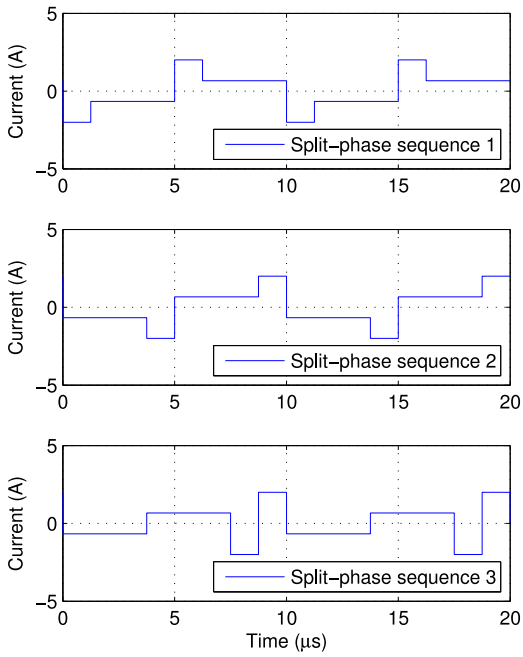

Fig. 12. Current waveform of capacitor C_2 of the Dickson SC converter under different switching sequences.

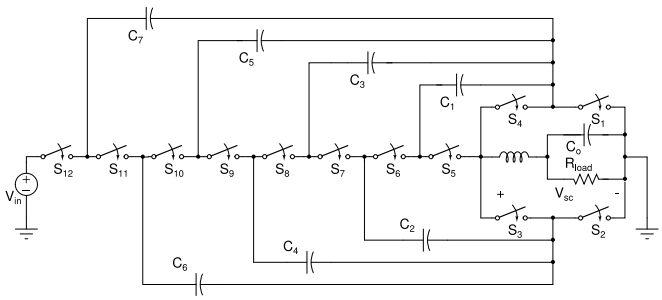

Fig. 13. The schematic of the proposed experimental prototype 8-to-1 Dickson converter.

ing sequences result in a nonimpulse current, showing that complete soft-charging operation can be achieved for each switching sequence. This is a particularly useful result: as will be discussed in Section IV, the intuitively devised sequence (Sequence 1), cannot be easily implemented due to practical constraints, whereas other sequences may yield practical and feasible solutions.

IV. Experimental Results

Hardware prototypes have been implemented for the proposed split-phase controlled soft-charging Dickson SC converter, with a voltage step-down ratio of 8 to 1. The schematic of the converter is shown in Fig. 13. The prototype uses 12 GaN switches and seven flying capacitors. With an input voltage of 150 V, the nominal output voltage of the converter is 18.75 V. The switch ratings of the Dickson converter are either $V_{\rm out}$ or $2V_{\rm out}$, plus additional voltage stress caused by the ripple of the capacitors. With the chosen parameters, the ripple is about 8 V at 2 A load current. Corresponding 40 and 100 V GaN FETs are

TABLE IV
Design Specifications and Parameters

	Hard-charging	Soft-charging Prototype 1	Soft-charging Prototype 2
$V_{\rm in}$	150 V DC	150 V DC	150 V DC
$I_{\rm load}$	2 A	2 A	2 A
$V_{\rm out}$	18 V DC	18 V DC	18 V DC
f_{sw}	250 kHz	250 kHz	50 kHz
Inductor	-	3.3 μH	3.3 μH
Flying capacitors	2.2 μF	0.47 μF	2.2 μF

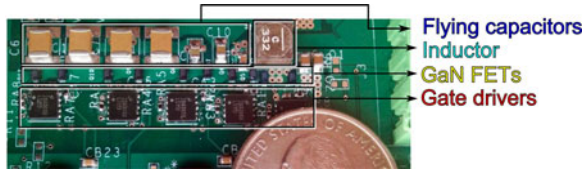

Fig. 14. Photo showing the power stage of the hardware prototype of the proposed 8-to-1 Dickson SC converter. A US quarter is included for perspective.

TABLE V
Component Listing of the Converter Prototype in Soft-Charging Configuration 1

Component	Part number	Parameters
S_{12}, S_5 - S_1	EPC2014	40 V, 16 mΩ, 10 A
S_{11} - S_6	EPC2007	100 V, 30 mΩ, 6 A
C_4 - C_7	C4532X7R2E474K230KA	250 V, 0.47 μF
C_1 - C_3	C3216X7R2A474K160AA	100 V, 0.47 μF
C_o	C3216X5R1V226M160AC	35 V, 22 μF
Inductor	XAL5030-332	3.3 μH
Level-shifting	ADUM5210	
Micro-controller	TI C2000 Piccolo	

selected conservatively to satisfy the voltage ratings. A nominal switching frequency is chosen and the flying capacitors and inductor are selected such that

$$f_{sw} \geq \frac{1}{2\pi\sqrt{LC}} \tag{14}$$

where C is the equivalent capacitance in series with the inductor in each phase [17]. The prototype has been implemented, and tested in three configurations, among which one is conventional hard-charging and two are soft-charging. The tested specifications and parameters for different configurations are given in Table IV. The first soft-charging configuration is to demonstrate the power density improvement by reducing the flying capacitance, while the second soft-charging configuration is to demonstrate efficiency improvement by reducing the switching frequency and keeping the same capacitance compared to hard-charging. It should be noted that in practice, a soft-charging converter is most likely designed to achieve a combination of both. A photo of the power stage of the prototype in soft-charging configuration 1 is shown in Fig. 14 and its component listing is provided in Table V.

The waveforms in this section are captured with soft-charging configuration 1. The voltage V_{sc} (from Fig. 13) as well as the

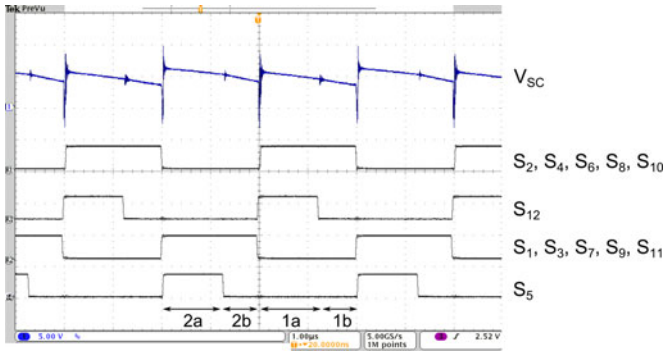

Fig. 15. Output voltage (V_{sc} in Fig. 13) (top) and switching functions (lower). Bandwidth of the waveform capture is 1 Gsamples/s.

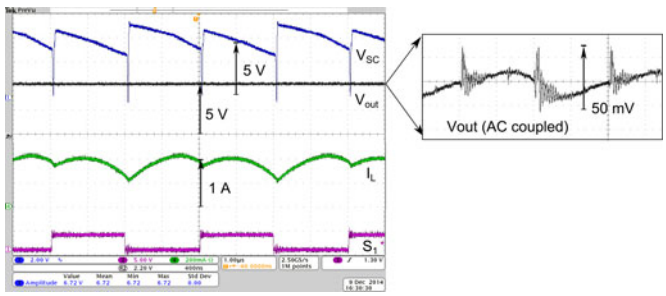

Fig. 16. Converter voltage before (V_{sc} in Fig. 13)) and after ($V_{\rm out}$) the LC filter, as well as inductor current. $V_{\rm in} = 40$ V and $I_{\rm load} = 1$ A. Waveform capture is band-limited to 25 Msamples/s for the ac coupled waveform.

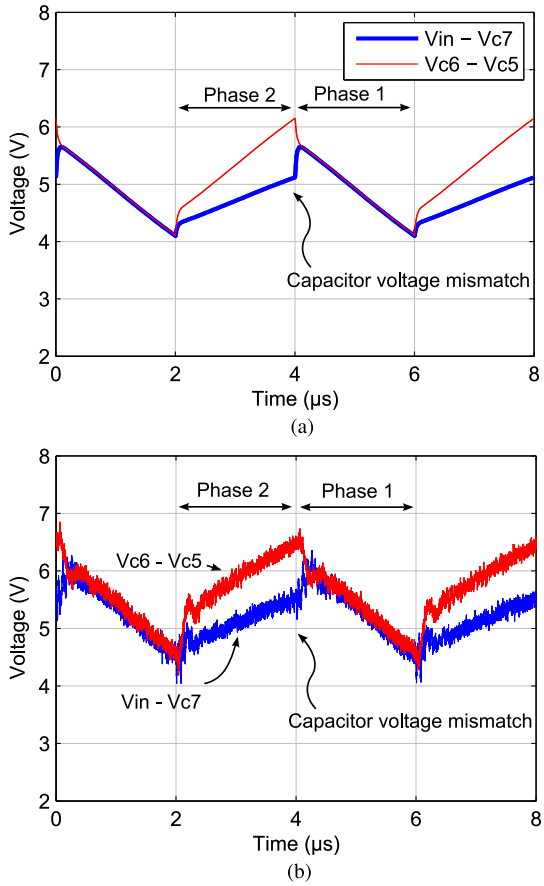

Fig. 17. Capacitor voltage mismatch during *two-phase* soft-charging operation. (a) Simulation. (b) Experiment.

switch gate signals are shown in Fig. 15. V_{sc} decreases during each phase due to the charging and discharging of capacitors, and jumps up after each major transition. Therefore V_{sc} resembles a sawtooth waveform. It can be seen that V_{sc} has a relatively large ripple, which is the result of the increased voltage ripple on the flying capacitors. This increased ripple is the key to enable smaller capacitors in soft-charging SC converters. The absolute slope of V_{sc} increases as load current increases. The flying capacitor and switching frequency should be chosen such that the voltage ripple on V_{sc} is a reasonable value, say $10\%-20\%$ of the maximum output voltage value, since the ripple magnitude adds to the voltage stress of the switches. It can also be seen from the V_{sc} waveform in Fig. 15, that V_{sc} goes to about -2.0 V at every major phase transition. This is due to the dead-time implemented to prevent current shoot-through. During the dead-time, the equivalence of the body diode of the GaN devices is forced to conduct by the inductor, and the forward voltage of roughly 1.4 V [36] appears negatively on V_{sc}. The dead-time can be tuned to achieve the maximum efficiency of the converter [36], but the process is not carried out for this prototype. In addition, the output LC filter should be designed such that the ripple on V_{sc} in worst load condition results in an acceptable output voltage ripple at the output of the LC filter. This however, can be easily achieved since the ripple on V_{sc} is much smaller than what is commonly present at the input of the LC filter of a PWM magnetic converter. The output voltage after the inductor ($V_{\rm out}$) is shown in Fig. 16. It can be seen that the ripples on V_{sc} are filtered by the LC circuit and the output is a steady dc voltage with 50 mV of ripple at 1A of load current.

The switching signals as seen in Fig. 15 are slightly different from what are used in simulation (see Fig. 10). This is because using the original phase sequence (1b $\rightarrow$ 1a $\rightarrow$ 2b $\rightarrow$ 2a) results in negative V_{ds} voltages across some of the switches, due to the large voltage ripples during the operation. Bidirectional blocking switches would have to be used, which would increase the complexity of the circuit and reduce the efficiency. Since it has been shown by the analysis in Section III, that complete soft-charging operation can be achieved regardless of the switching sequence, the actual sequence used by the hardware prototype is Sequence 2 in Section III (i.e., 2a $\rightarrow$ 2b $\rightarrow$ 1a $\rightarrow$ 1b). This switching sequence results in no negative V_{ds} voltage on any of the switches so that the converter operates properly using the GaN FETs.

To demonstrate the soft-charging operation, the capacitor voltages are measured for both two-phase control and split-phase control. The simulated and measured waveforms for two-phase control are shown in Fig. 17. The experimental waveform clearly shows the mismatch in voltage $V_{\rm in} - V_{c7}$ and $V_{c6} - V_{c5}$ during the transition between Phase 2 and Phase 1, as expected from the analysis and simulation. On the other hand, as shown in Fig. 18, the voltage mismatch has been eliminated by using the proposed split-phase control, as the two sets of voltages converge right before the switching occurs.

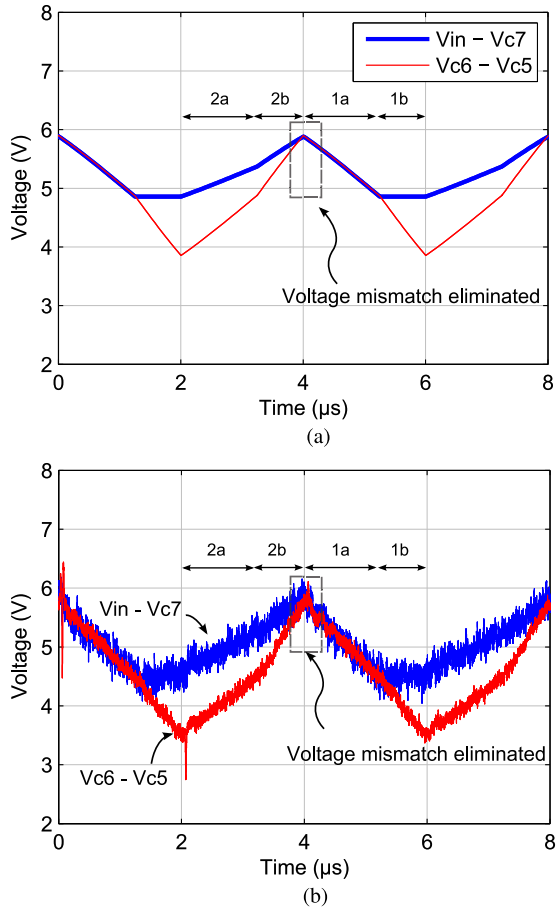

Fig. 18. Capacitor voltage mismatch eliminated with *split-phase* soft-charging operation. (a) Simulation. (b) Experiment.

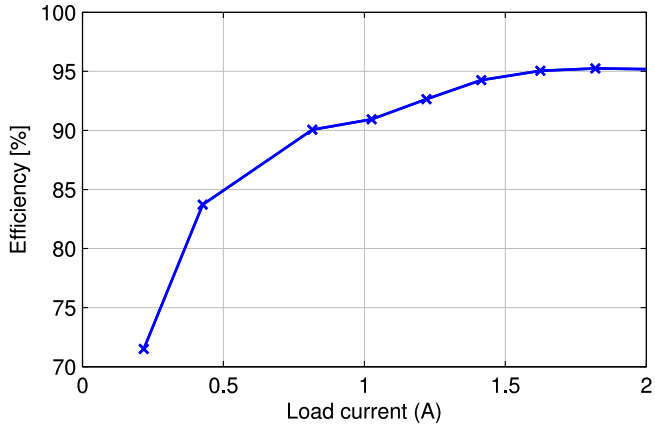

Fig. 19. Measured efficiency of converter prototype in split-phase operation with soft-charging configuration 1, at $V_{\rm in} = 150$ V.

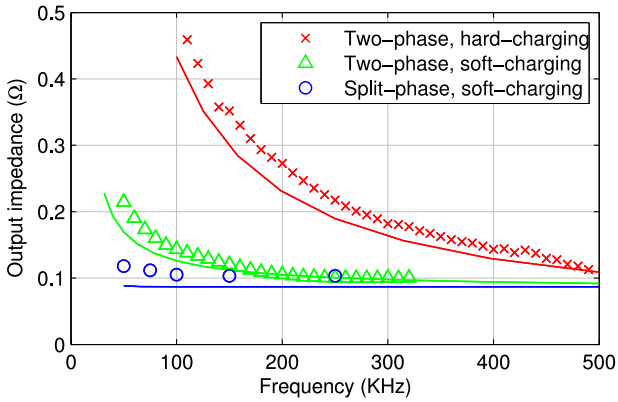

Fig. 20. Output impedance calculated from measured data. Simulated values are shown as solid lines for reference.

The efficiency of the soft-charging converter configuration 1 in split-phase operation is plotted in Fig. 19. It can be seen that the converter achieves a peak efficiency of 95% at the rated load. It should be noted that the efficiency at light load can be improved by scaling down the switching frequency, provided that the constraint given in (14) is still satisfied.

For a direct comparison of the output impedance, the second soft-charging configuration is used, since it has the same capacitor values as the hard-charging converter. The only difference between this prototype and the hard-charging one is the extra inductor to make the LC filter. The additional inductor incurs an approximately 10% increase in the components volume of the power stage, but the penalty in volume is much less when the total enclosed box volume of the power stage is considered. The output impedance is plotted against the switching frequency inFig. 20, and is calculated from (3) using the measured data. It can be seen that similar to the simulation results, the output impedance in hard-charging operation increases as frequency decreases. Two-phase soft-charging operation reduces the impedance at low switching frequencies while the proposed split-phase operation results in the lowest output impedance. For example, to achieve the same output impedance as the split-phase operation at 100 kHz, the two-phase soft-charging operation requires a switching frequency of approximately 200 kHz while the hard-charging converter has to switch at over 500 kHz. Moreover, it can be seen in Fig. 20 that the measured data closely match the simulated values, especially at higher switching frequencies. At lower switching frequencies, the experimental values of all three cases are larger than expected. This can be attributed to the tolerance of the flying capacitor used (up to 20%). Since the split-phase control assumed equal capacitor values for soft-charging operation, different capacitor values will result in some degree of capacitor charging/discharging loss and is not modeled in the simulation.

In addition, the efficiencies of the converters in the SSL region are compared in Fig. 21, using the soft-charging converter configuration 2. It can be seen that soft-charging operation brings significant efficiency improvement while the proposed split-phase control has the highest efficiency. The split-phase soft-charging operation also has the smallest drop in efficiency as the load increases, due to its smallest output impedance. At a load current of 2 A, the split-phase reduces power loss by 30% compared to two-phase soft-charging operation, and by 75% compared to the projected power loss with the hard-charging operation. It should be noted that both the output impedance measurements and the efficiency measurements are obtained

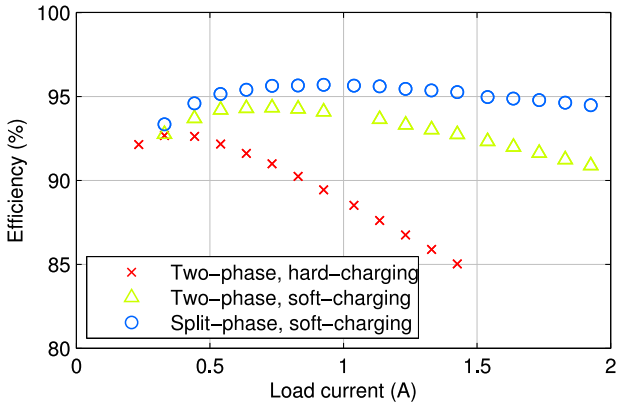

Fig. 21. Measured efficiency of the Dickson converter in deep SSL region. $V_{\rm in} = 40$ V, $f_{sw} = 100$ kHz.

using reduced input voltage and output current rather than the rated values. This is to prevent the conventional hard-charging converter from breaking due to the excessive heat when the converter is operating inefficiently with high output impedance in the SSL region. The hardware results also demonstrated that indeed the split-phase control is effective for a Dickson converter with a conversion ratio that is higher than the analyzed 4-to-1.

V. Conclusions

In this paper, we proposed a split-phase control method that enables the Dickson SC converter to operate in complete soft-charging mode. With complete soft-charging operation, the proposed converter has no current transient and thus can achieve superior efficiency and/or power density compared to conventional SC converters. The existing analysis is extended to account for the split-phase control technique and the desired duty ratio for each phase is found. In addition to supporting simulation results, the proposed technique was experimentally verified with an 8-to-1 Dickson converter. The hardware prototype in soft-charging operation has been shown to exhibit significantly lower output impedance and higher efficiency in SSL region than conventional SC converters.

Appendix
Derivation of the Charge Flow Vector for a 4-to-1 Dickson Converter

For the 4-to-1 Dickson converter in Fig. 1, the voltage change vector is defined as

$$\mathbf{\Delta v} = \begin{bmatrix} \Delta v_{\rm in} \\ \mathbf{\Delta v_c} \\ \Delta v_{\rm out} \end{bmatrix} = \begin{bmatrix} \Delta v_{\rm in} \\ \Delta v_{c3} \\ \Delta v_{c2} \\ \Delta v_{c1} \\ \Delta v_{\rm out} \end{bmatrix}. \tag{15}$$

Using the KVL equations defined in (5) and examining each loop in Fig 7, the following reduced loop matrices can be found:

$$\mathbf{A_{1a}} = \begin{bmatrix} 1 & -1 & 0 & 0 & -1 \\ 0 & 0 & 1 & -1 & -1 \end{bmatrix}$$
$$\mathbf{A_{2a}} = \begin{bmatrix} 0 & 1 & -1 & 0 & -1 \\ 0 & 0 & 0 & 1 & -1 \end{bmatrix}$$
$$\mathbf{A_{1b}} = \begin{bmatrix} 0 & 0 & 1 & -1 & -1 \end{bmatrix}$$
$$\mathbf{A_{2b}} = \begin{bmatrix} 0 & 1 & -1 & 0 & -1 \end{bmatrix}. \tag{16}$$

In addition, since $\Delta V_{\rm in}$ is considered zero for a constant voltage-source input, a row of $\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}$ can be added to each of the reduced loop matrices, resulting in the modified reduced loop matrix $\mathbf{A_{1am}}$, $\mathbf{A_{2am}}$, $\mathbf{A_{1bm}}$ and $\mathbf{A_{2bm}}$. The solution to (7) and (16) represents the possible change in values that the voltages of the circuit elements can take, constrained by KVL. By definition, the solution is the nullspace of each of the modified reduced loop matrix[1], and is shown below

$$\mathbf{w^{1a}} = \begin{bmatrix} 0 \\ 0.1225 \\ 0.6325 \\ 0.7550 \\ -0.1225 \end{bmatrix} \begin{bmatrix} 0 \\ -0.6205 \\ 0.4472 \\ -0.1733 \\ 0.6205 \end{bmatrix} \tag{17}$$

$$\mathbf{w^{2a}} = \begin{bmatrix} 0 \\ -0.2124 \\ -0.6968 \\ 0.4844 \\ 0.4844 \end{bmatrix} \begin{bmatrix} 0 \\ 0.7449 \\ 0.3383 \\ 0.4066 \\ 0.4066 \end{bmatrix}$$

$$\mathbf{w^{1b}} = \begin{bmatrix} 0 \\ -0.5774 \\ 0.6667 \\ 0.3333 \\ 0.3333 \end{bmatrix} \begin{bmatrix} 0 \\ 0.5774 \\ 0.3333 \\ 0.6667 \\ -0.3333 \end{bmatrix} \begin{bmatrix} 0 \\ 0.5774 \\ 0.3333 \\ -0.3333 \\ 0.6667 \end{bmatrix} \tag{18}$$

$$\mathbf{w^{2b}} = \begin{bmatrix} 0 \\ 0.5774 \\ 0.7887 \\ 0 \\ -0.2113 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1.000 \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ 0.57740 \\ -0.2113 \\ 0 \\ 0.7887 \end{bmatrix}. \tag{19}$$

[1]The nullspace can be found, for example, by using the *null* command in Matlab.

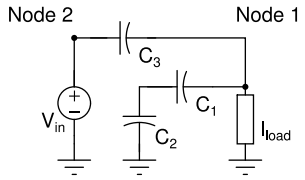

Fig. 22. Phase 1 of the split-phase Dickson converter.

In addition, for soft-charging operation, the output voltage is able to change instantaneously to accommodate the change in the terminal voltage during phase transitions, and thus, it is no longer a state in the linear circuit being analyzed. Therefore, Δv_{out} is excluded from the analysis. The basis corresponding to the capacitor voltage change ($\mathbf{\Delta v_c}$) are obtained from the middle elements of the $\mathbf{w^i}$ vectors.

$$\mathbf{w_c^{1a}} = \begin{bmatrix} 0.1225 \\ 0.6325 \\ 0.7550 \end{bmatrix} \begin{bmatrix} -0.6205 \\ 0.4472 \\ -0.1733 \end{bmatrix} \tag{20}$$

$$\mathbf{w_c^{2a}} = \begin{bmatrix} -0.2124 \\ -0.6968 \\ 0.4844 \end{bmatrix} \begin{bmatrix} 0.7449 \\ 0.3383 \\ 0.4066 \end{bmatrix}$$

$$\mathbf{w_c^{1b}} = \begin{bmatrix} -0.5774 \\ 0.6667 \\ 0.3333 \end{bmatrix} \begin{bmatrix} 0.5774 \\ 0.3333 \\ 0.6667 \end{bmatrix} \begin{bmatrix} 0.5774 \\ 0.3333 \\ -0.3333 \end{bmatrix} \tag{21}$$

$$\mathbf{w_c^{2b}} = \begin{bmatrix} 0.5774 \\ 0.7887 \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 1.000 \end{bmatrix} \begin{bmatrix} 0.57740 \\ -0.2113 \\ 0 \end{bmatrix}. \tag{22}$$

The charge vector for the 4-to-1 Dickson converter is defined as

$$\mathbf{q} = \begin{bmatrix} q_{\text{in}} \\ \mathbf{q_c} \\ q_{\text{out}} \end{bmatrix} = \begin{bmatrix} q_{\text{in}} \\ q_{c3} \\ q_{c2} \\ q_{c1} \\ q_{\text{out}} \end{bmatrix}. \tag{23}$$

Taking the Phase 1 schematic repeated in Fig. 22 as an example, by applying KCL to Node 1, Node 2 and the ground node respectively, the following equations can be found:

$$\begin{cases} q_{c3} + q_{c1} - q_{\text{out}} = 0 \\ -q_{\text{in}} - q_{c3} = 0 \\ q_{\text{in}} + q_{c2} + q_{\text{out}} = 0. \end{cases} \tag{24}$$

The number of independent KCL equations for a circuit is given by $n-1$, where n is the number of nodes in the circuit [35]. Therefore, only three nodes from the circuit in Fig. 22 are used to generate the KCL equations. Expressing these KCL equations using the matrix-vector product form given in (9) yields the reduced incidence matrix $\mathbf{B_{1a}}$. The same process is repeated for the other phases and all four of the reduced incidence matrices are given below

$$\mathbf{B_{1a}} = \begin{bmatrix} 0 & 1 & 0 & 1 & -1 \\ -1 & -1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 \end{bmatrix} \tag{25}$$

$$\mathbf{B_{2a}} = \begin{bmatrix} 0 & -1 & -1 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$\mathbf{B_{1b}} = \begin{bmatrix} 0 & 0 & -1 & -1 & 0 \\ 0 & 0 & 0 & 1 & -1 \\ -1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \tag{26}$$

$$\mathbf{B_{2b}} = \begin{bmatrix} 0 & -1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & -1 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 \end{bmatrix}. \tag{27}$$

The solution for the possible capacitor charge vectors that satisfy (9) and (27) are found to be

$$\mathbf{u^{1a}} = \begin{bmatrix} 0.2443 \\ -0.2443 \\ -0.6109 \\ 0.6109 \\ 0.3666 \end{bmatrix} \begin{bmatrix} -0.5615 \\ 0.5615 \\ -0.0432 \\ 0.0432 \\ 0.6047 \end{bmatrix} \mathbf{u^{2a}} = \begin{bmatrix} 0 \\ 0.6325 \\ -0.6325 \\ -0.3162 \\ -0.3162 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 0 \\ -0.7071 \\ -0.7071 \end{bmatrix}$$

$$\mathbf{u^{1b}} = \begin{bmatrix} 0 \\ 0 \\ -0.5774 \\ 0.5774 \\ 0.5744 \end{bmatrix} \mathbf{u^{2b}} = \begin{bmatrix} 0 \\ -0.5774 \\ 0.5774 \\ 0 \\ 0.5744 \end{bmatrix}. \tag{28}$$

Similar to the preceding analysis of the voltage vector, only the elements that correspond to the charge through the capacitors ($\mathbf{q_c}$) are of interest. Again, the corresponding elements are

grouped in to a set of new vectors, defined as $\mathbf{u_c^i}$

$$\mathbf{u_c^{1a}}=\begin{bmatrix}-0.2443\\-0.6109\\0.6109\end{bmatrix}\begin{bmatrix}0.5615\\-0.0432\\0.0432\end{bmatrix}\mathbf{u^{2a}}=\begin{bmatrix}0.6325\\-0.6325\\-0.3162\end{bmatrix}\begin{bmatrix}0\\0\\-0.7071\end{bmatrix}$$

$$\mathbf{u_c^{1b}}=\begin{bmatrix}0\\-0.5774\\0.5774\end{bmatrix}\mathbf{u_c^{2b}}=\begin{bmatrix}-0.5774\\0.5774\\0\end{bmatrix}. \tag{29}$$

Since each basis in (22), $\mathbf{w^i}$ represent a set of voltage changes, they can be related to the charge transferred by multiplying with the respective capacitor values. The result can be represented by

$$\mathbf{c} * \mathbf{w_c^i} \tag{30}$$

where $*$ represents element-wise multiplication and $\mathbf{c}$ is given by

$$\mathbf{c}=\begin{bmatrix}C_3\\C_2\\C_1\end{bmatrix}. \tag{31}$$

Since the $\mathbf{u_c^i}$ vectors in (29) represent the possible charge transfer constrained by KCL and the $\mathbf{c} * \mathbf{w_c^i}$, vectors in (30) represent the possible charge transfer due to the change in capacitor voltage constrained by KVL, the actual charge transfer values must satisfy both. To find the actual charge flow, the common space spanned by $\mathbf{u_c^i}$ and $\mathbf{c} * \mathbf{w_c^i}$, can be found, and is defined as $\mathbf{p_c^i}$. Therefore, $\mathbf{p_c^i}$ can be expressed as

$$\mathbf{p_c^i}=\sum_j \beta_j \mathbf{u^i_{c(j)}} + \gamma_j \mathbf{c} * \mathbf{w^i_{c(j)}} \tag{32}$$

where i is the phase number and j represents the jth basis. For $C_1 = C_2 = C_3$, (32) can be solved for β and γ, and the charge vectors are found as

$$\mathbf{p_c^{1a}} = \begin{bmatrix}0.3714\\-0.1857\\0.1857\end{bmatrix}\mathbf{p_c^{2a}} = \begin{bmatrix}0.2000\\-0.2000\\0.4000\end{bmatrix}$$

$$\mathbf{p_c^{1b}} = \begin{bmatrix}0\\-0.5774\\0.5774\end{bmatrix}\mathbf{p_c^{2b}} = \begin{bmatrix}-0.5774\\0.5774\\0\end{bmatrix}. \tag{33}$$

These are the basis for the charge vectors which satisfy KCL and which also result in a capacitor voltage change that satisfies KVL. To find the actual values of the charge transfered, the steady-state condition given in (11) results in the following equation:

$$\alpha_{1a}\mathbf{p_c^{1a}} + \alpha_{2a}\mathbf{p_c^{2a}} + \alpha_{1b}\mathbf{p_c^{1b}} + \alpha_{2b}\mathbf{p_c^{2b}} = 0. \tag{34}$$

Equation (34) can be used to find the values of the α's. Finally, the actual charge flow vectors are given by

$$\mathbf{q_c^{1a}} = \alpha_{1a}\mathbf{p_c^{1a}},\ \mathbf{q_c^{2a}} = \alpha_{2a}\mathbf{p_c^{2a}} \tag{35}$$

$$\mathbf{q_c^{1b}} = \alpha_{1b}\mathbf{p_c^{1b}},\ \mathbf{q_c^{2b}} = \alpha_{2b}\mathbf{p_c^{2b}}. \tag{36}$$

It should be noted that even though the coefficient values (α, β, γ) are obtained using only the basis whose elements correspond to the capacitors ($\mathbf{u_c^i}$ and $\mathbf{w_c^i}$), their values are also valid for the original basis, $\mathbf{u^i}$ and $\mathbf{w^i}$, which contain the elements corresponding to the input and output source. The overall charge vectors, which also contain the charge flow through the input and output element, can be found using the same set of coefficients and the resultant values are given as in (12).

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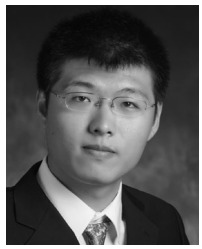

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