High-Frequency-Link-Based Grid-Tied PV System With Small DC-Link Capacitor and Low-Frequency Ripple-Free Maximum Power Point Tracking

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***Abstract*—This paper proposes a grid-tied photovoltaic (PV) system consisting of modular current-fed dual-active-bridge (CF-DAB) dc–dc converter with cascaded multilevel inverter. The proposed converter allows a small dc-link capacitor in the three-phase wye-connected PV system; therefore, the system reliability can be improved by replacing electrolytic capacitors with film capacitors. The low-frequency ripple-free maximum power point tracking (MPPT) is also realized in the proposed converter. First of all, to minimize the influence resulting from reduced capacitance, a dc-link voltage synchronizing control is developed. Then, a detailed design of power mitigation control based on CF-DAB dynamic model is presented to prevent the large low-frequency voltage variation propagating from the dc-link to PV side. Finally, a novel variable step-size MPPT algorithm is proposed to ensure not only high MPPT efficiency, but also fast maximum power extraction under rapid irradiation change. A downscaled 5-kW PV converter module with a small dc-link capacitor was built in the laboratory with the proposed control and MPPT algorithm, and experimental results are given to validate the converter performance.**

***Index Terms*—Current-fed dual-active-bridge (CF-DAB), high-frequency link (HFL), low-frequency ripple, maximum power point tracking (MPPT), small dc-link capacitor.**

I. Introduction

PHOTOVOLTAIC (PV) energy has become one of the most popular sustainable energy sources nowadays [1]. Due to continuous cost reduction and government incentives, the installation of grid-integrated PV system has grown rapidly in the past few years [2]. As a promising topology for grid-tied PV system, the cascaded multilevel inverter (CMI) has many advantages, such as modularity, high ac voltage application with low device rating, low harmonic spectra and low electromagnetic interference, etc. [3], [4]. In addition, distributed maximum power point tracking (MPPT) terminal for segmented PV arrays can be achieved by a CMI PV converter [5], [6].

In MW-scale high-voltage grid-tied PV systems, galvanic isolation between the PV panel and the grid is required to prevent electric shock on PV panel due to insulation damage and to suppress leakage current. Hence, compared to single-stage CMI converter, the cascaded multilevel inverter integrated with high-frequency-link (HFL)-based dc–dc converters has advantage of providing galvanic isolation between the PV panel and the grid without using bulky line-frequency transformer. However, in a three-phase wye-connected CMI PV system with dc–dc stage, electrolytic capacitors are used as the dc-link energy buffers between dc–dc stage and inverter stage to provide the double-line-frequency (2ω) power to the grid [7]. Though electrolytic capacitor has high capacitance density, it has been considered as a particularly unreliable component, which is on average 30 times less reliable than nonelectrolytic capacitor under identical conditions [8], [9]. Therefore, capacitance reduction is highly desirable in order to achieve high reliability with nonelectrolytic film capacitor [10]–[12], especially for the high-voltage CMI PV system. Nonetheless, the small dc-link capacitance will make the converter suffer from large 2ω voltage ripple on the dc-link. If this voltage ripple propagates to the PV side, it will deteriorate the MPPT performance and decrease the MPPT efficiency [13]–[15]. To solve this issue, current-fed isolated dc–dc converters have inherent advantages over the voltage-fed types because the input current of current-fed converter can be controlled directly, and thus, it is possible to eliminate the input low-frequency power ripple in the PV side by special designed current control.

Several isolated current-fed dc–dc converters have been studied for various applications [16]–[22]. Jiang *et al.* [16] have proposed a current-fed boost-half-bridge PV microinverter; due to the high reverse recovery loss of the diodes at transformer secondary side, the switching frequency is relatively low. To alleviate the loss on the diodes, a resonant operating mode with ZCS condition based on the same topology is proposed in [17]. Nonetheless, the dc-link capacitor is still large and the lower switch suffers from hard switching of high peak current. The current-fed full-bridge converters are suitable for high-power applications [18], however, start-up circuits are needed since the duty cycle can never be smaller than 0.5. Active clamp circuits are usually adopted to extend the duty-cycle range as well as enable ZVS operating [19], [20]. In [21], a three-phase current-fed dual-active-bridge (CF-DAB3) converter is proposed for PV application on a dc distributed system. Although it has high power capability, the converter faces phase current unbalancing issues. The current-fed dual-half-bridge (CF-DHB) converter with small dc-link capacitor for fuel cell applications has

Manuscript received October 19, 2014; revised December 22, 2014; accepted February 22, 2015. Date of publication March 11, 2015; date of current version September 21, 2015. Recommended for publication by Associate Editor L. Chang.

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Digital Object Identifier 10.1109/TPEL.2015.2411858

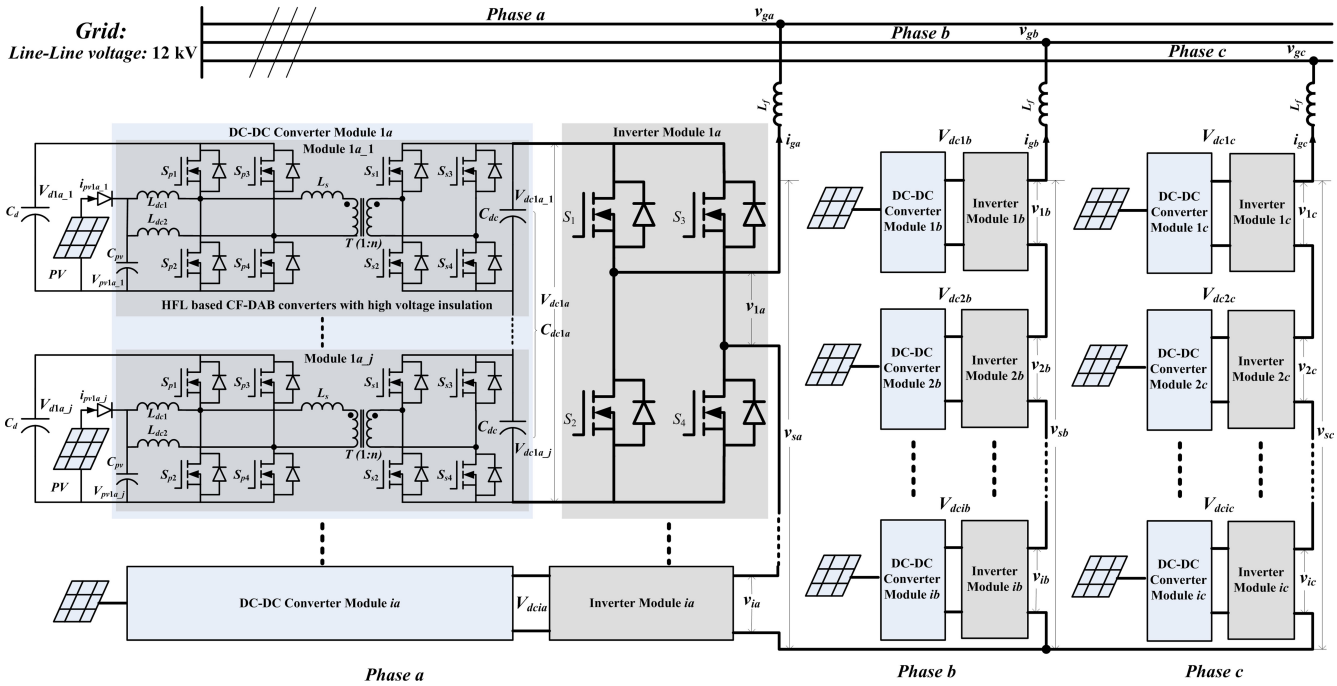


Fig. 1. Grid-tied cascaded multilevel PV inverter system based on CF-DAB dc-dc converters.

been proposed by authors in [22], and the input low-frequency ripple current is successfully mitigated by applying direct feedback compensation in the phase-shift control. Unfortunately, the half-bridge topology will suffer from unbalanced capacitor voltage if the duty cycle is not 0.5. Moreover, low-frequency resonance may occur between the reduced dc-link capacitor and transformer magnetic inductor, resulting in large transformer current.

This paper proposes a grid-tied CMI PV system based on a current-fed dual-active-bridge (CF-DAB) dc–dc converter that enables using small film capacitors. A dc-link voltage synchronizing control, i.e., "$d = 1$" control, is applied to reduce the high current stress and consequent loss in the converter resulting from unbalanced dc-link voltage between primary side and secondary side of the transformer [23]. With low-frequency power mitigation control, the 2ω ripple on the input PV voltage can be greatly attenuated. Therefore, low-frequency ripple-free power can be extracted from the PV array. Furthermore, other characteristics such as the inherent zero-voltage switching (ZVS), high step-up ratio, interleaved structure, and wide input voltage capability make CF-DAB converter very suitable for PV applications. Therefore, the proposed CF-DAB-based CMI PV converter is an optimal candidate for MW-scale PV systems.

To achieve maximum solar energy harvest, the MPPT strategy should satisfy both high steady-state MPPT efficiency and fast MPPT. Among numerical MPPT methods, the variable step-size incremental conductance (INC) method is attractive due to its advantages in compromising steady-state MPPT efficiency and transient tracking speed [24]–[26]. The variable step-size of INC is accurate at steady state, but the dynamic of the MPPT is not good mainly due to the degression of the iteration step size [25]. A modified variable step-size INC MPPT with an adaptive scaling factor is utilized in [26] to improve tracking speed during the transient. However, this modification increases the computational burden and still may have MPPT failure during rapid irradiation change [24]. In this paper, the variable step-size INC MPPT algorithm is improved in several aspects. First, the PV voltage is kept unchanged during rapid irradiation change to avoid possible failure of MPPT. Second, a maximum step size is adapted right after the short transient, and when approaching the new maximum power point (MPP), variable step size with an adaptive scaling factor related to PV power is adopted for fast tracking.

The rest of this paper is organized as follows. In Section II, a CF-DAB module-based MW-scale grid-tied CMI PV system is introduced and the corresponding low-frequency ripple power is analyzed. In Section III, a detailed low-frequency ripple power mitigation control as well as synchronizing dc-link voltage control is proposed. An MPPT strategy that is able to achieve both high steady-state efficiency and fast tracking speed under rapid irradiation change is also presented. A downscaled 5-kW module of the proposed PV system has been built in the laboratory, and experimental verifications are given in Section IV. Finally, Section V summarizes the conclusions.

II. System Configuration and Low-Frequency Ripple Power

Fig. 1 presents the system configuration of a proposed MW-scale grid-tied PV system with CF-DAB dc–dc converters [5]. It consists of *i* cascaded multilevel inverter modules for each phase and each inverter module is connected to *j* cascaded CF-DAB converter modules. Compared with traditional PV systems, this system shows many advantages. Because of the high-frequency isolated dc–dc converters, the PV system can be directly connected to the high-voltage ac grid without bulky line-frequency

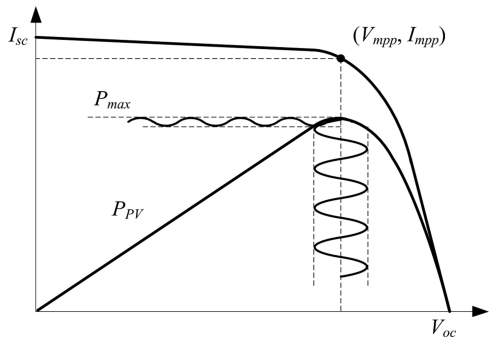


Fig. 2. Low-frequency ripple effect on the MPPT.

transformer, and the converter output voltage is scalable due to the modular structure. Each dc–dc module is interfaced with segmented PV arrays having independent MPPT; therefore, the solar energy harvesting can be maximized. Moreover, flexible control strategies are able to be explored and applied in this topology. By using the reactive power compensation and optimization strategy in [6], the proposed converter can reduce the over modulation of the PV inverter output voltage caused by unsymmetrical active power generation from PV arrays, and thus, improve the system power quality and reliability. In addition, due to the isolated CF-DAB converter, the ground leakage current is effectively suppressed. Particularly, this converter can reduce the dc-link capacitance and enable film capacitor implementation by allowing large voltage ripple on the dc-link; hence, the PV system reliability is greatly improved.

The dc-link capacitance is mainly determined by the allowed voltage ripple on the dc-link in specific system. For the PV system in Fig. 1, the instantaneous power flow through each phase leg contains 2ω fluctuating power. The dc-link capacitance required to buffer the energy can be calculated by (1) as derived in [23].

$$C_{\mathrm{dc1}a} = \frac{S_{1p}}{\omega_g \Delta V_{\mathrm{dc1}a} V_{\mathrm{dc1}a}} \tag{1}$$

where S_{1p} is the apparent output power flow through the single phase leg, ω_g is line frequency, $V_{\mathrm{dc1}a}$ and $\Delta V_{\mathrm{dc1}a}$ are the average voltage and the allowed peak-to-peak ripple voltage on the dc-link, respectively.

As illustrated in (1), the required dc-link capacitance is inversely proportional to the dc-link voltage and the allowed voltage ripple. With selected bus voltage, small capacitance will result in large voltage ripple on the capacitor. This large low-frequency voltage ripple on the dc-link imposes challenges on the PV system operation, especially on the dc–dc stage. The ripple significantly increases the peak current inside the CF-DAB converter module if unbalanced bus voltage occurs between primary side and secondary side [27]. Moreover, this large 2ω voltage ripple can decrease the MPPT efficiency if it propagates to PV side. Fig. 2 illustrates how the low-frequency voltage ripple affects the PV power generation. It can be seen that the PV output power will be typically diminished from the maximum power at (V_{mpp}, I_{mpp}) if the PV voltage or current has low-frequency ripple. As mentioned in [14], the voltage ripple should be kept below 8.5% to get 98% utilization factor of PV array. With the CF-DAB dc–dc converter interface adopted in this paper, the low-frequency voltage ripple can be effectively attenuated in the PV side through the power mitigation control discussed in the Section III, thus large voltage ripple on dc-link is allowed without influence on the PV power.

With low-frequency ripple-free PV voltage, high effective MPPT become possible. Using the autonomous variable step-size MPPT strategy proposed in Section III, the proposed PV system can achieve high efficient MPPT in steady state and fast tracking under rapid irradiation change.

In this paper, the application scenario is a 3-MW/12-kV PV system. The CMI module number *i* is selected to be 4, considering the tradeoffs among the cost, lifetime, passive components, switching devices, and frequency selection. As a result, power rating of each inverter module is 250 kW. The dc-link voltage of each inverter module is 3 kV based on grid voltage, power devices selection as well as power quality. The switching frequency of inverter stage is 5 kHz, and the PV inverter will generate nine-level output voltage with equivalent 40-kHz PWM frequency for each phase using phase-shift carrier-based PWM control. The line filtering inductance is 0.8 mH. As for the dc–dc converter modules, four CF-DAB modules are in series, where each module has a power rating of 62.5 kW and dc-link voltage of 750 V. The 2ω voltage ripple on the dc-link is allowed to be 30% of dc-link voltage at rated power, resulting in a 250 μF total capacitance requirement for $C_{\mathrm{dc1}a}$. The low capacitance makes it possible for film capacitor implementation to improve the system lifetime. The switching frequency for dc–dc stage is 50 kHz. The leakage inductor L_s is designed at 2 μH, while the input dc inductor L_{dc1} is 10 μH considering the cost and size, and system efficiency over wide operating range. C_d is 250 μF, and C_{pv} is 120 μF to limit the switching frequency ripple voltage within 1%. In addition, the cascaded modular structure enables using SiC devices for both inverter stage and dc–dc stage to improve system efficiency and reliability.

III. Low-Frequency Power Mitigating Control and MPPT

To simplify the analysis, a PV system including one single dc–dc module and one inverter module, namely $i = 1$ and $j = 1$ for the PV system of Fig. 1, is selected for investigation. The control system for the proposed CF-DAB-converter-based PV system is described in Fig. 3, which can be divided into CF-DAB converter control system and full-bridge inverter control system. The dc-link voltage v_{dc} is controlled by the inverter module. A detailed active and reactive power compensation and optimization strategy for the inverter control has been reported in [5] and [6]; therefore, this paper only focuses on the control for dc–dc module. Duty-cycle plus phase-shift control is employed for the CF-DAB converter. The PV voltage v_{pv} is regulated by the duty cycle *D*, while the low voltage side (LVS) voltage v_d is controlled by the phase-shift angle ϕ. To minimize the peak current of the transformer, "$d = 1$" control using PI + Resonant (PIR) controller is applied to synchronize the LVS and high voltage side (HVS) dc-link voltage. A low-frequency

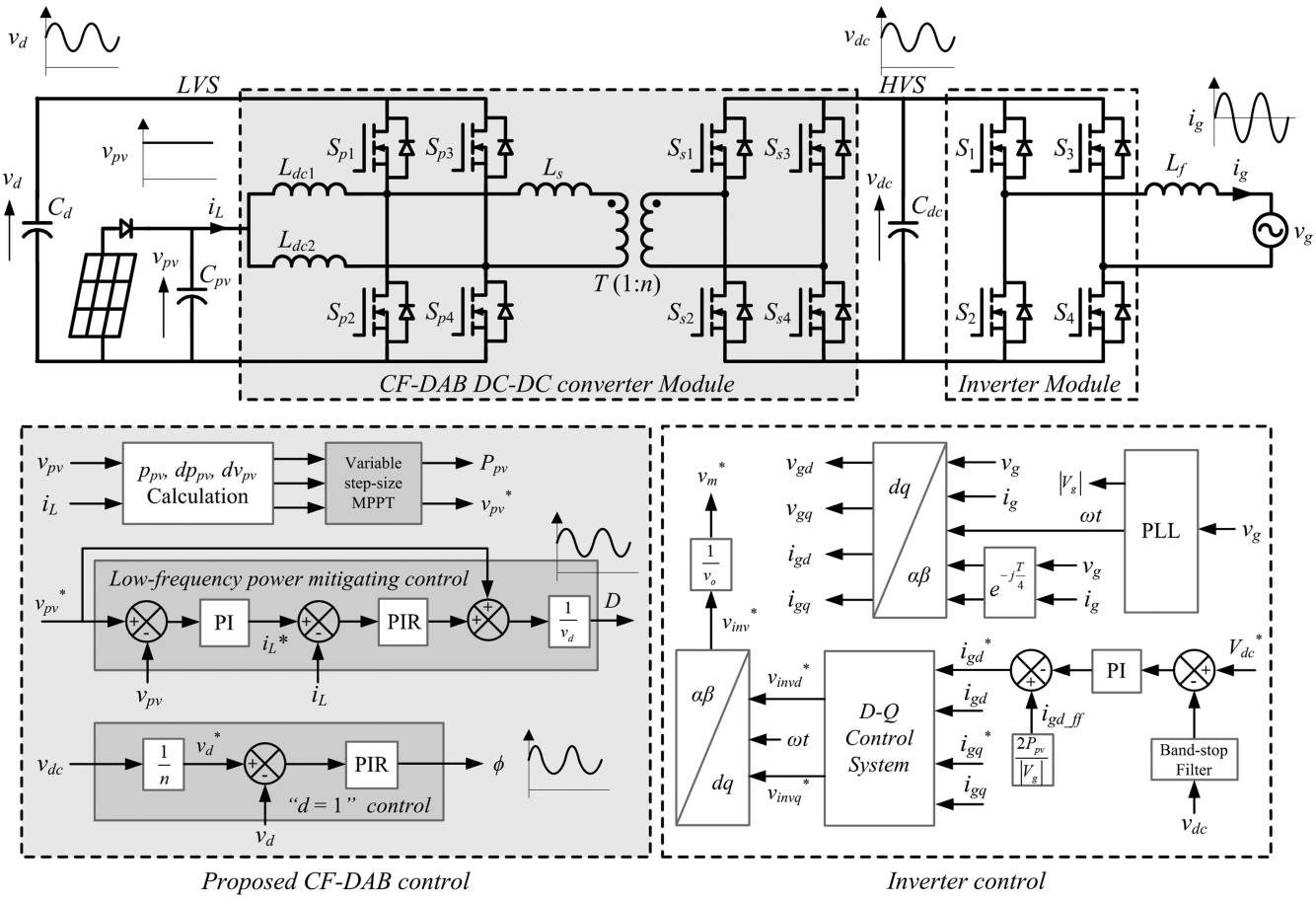


Fig. 3. Control system diagram of proposed PV converter.

power mitigation strategy using dual-loop control with dc-link voltage fed forward is developed for the PV voltage control; hence, low-frequency ripple-free PV power can be realized. The PV voltage $v_{\rm pv}$ and the inductor current i_L are used to calculate the PV voltage variation $dv_{\rm pv}$, PV power $p_{\rm pv}$, and PV power variation $dp_{\rm pv}$. And the PV voltage reference $v^*_{\rm pv}$ is generated from MPPT block, which is implemented with an autonomous variable step-size MPPT strategy that can achieve high efficiency and fast MPPT under rapid irradiation change.

A. Dynamics Analysis of CF-DAB-Based PV System

The operation principles of the CF-DAB converter have been presented in [23]. The operation ranges and some key waveforms are redrawn here in Figs. 4 and 5, respectively. Fig. 4 shows that there are seven subareas that can be combined into four operating modes symmetrically, and each one has two conditions: $D < 0.5$ and $D > 0.5$. In real application, the duty cycle is usually limited within 0.25–0.75 in order to achieve high efficiency, and the phase-shift angle should be smaller than $\pi/3$ for low circulating loss. Therefore, the converter will mainly operate in mode I and II. Fig. 5 depicts the key waveforms of the CF-DAB converter under mode I and mode II. $v_{\rm pri}$ and $v'_{\rm sec}$ are primary-side voltage and primary referred secondary-side voltage of the transformer, respectively. $i_{L\rm dc1}$ is the current of the dc–dc converter inductor, and i_{Ls} is transformer primary-side current.

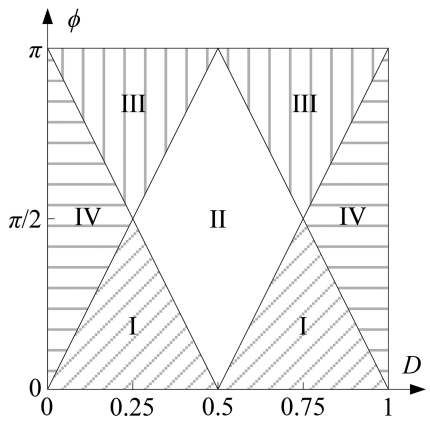


Fig. 4. Operating ranges of CF-DAB converter.

Based on the periodicity and symmetry of the waveforms, the power flow equation of the CF-DAB can be derived as

$$P=\begin{cases}\frac{V_d V_{\rm dc}}{n\omega L_s}\phi\left(2D^T-\frac{\phi}{2\pi}\right)\\ \text{Mode I}:0<\phi<\min\left\{2D^T\pi,\pi-2D^T\pi\right\}\\ \frac{V_d V_{\rm dc}}{n\omega L_s}\left[\phi\left(1-\frac{\phi}{\pi}\right)-\frac{\pi}{2}\left(1-2D^T\right)^2\right]\\ \text{Mode II}:2D^T\pi<\phi<\pi-2D^T\pi, D^T>0.25\end{cases}\tag{2}$$

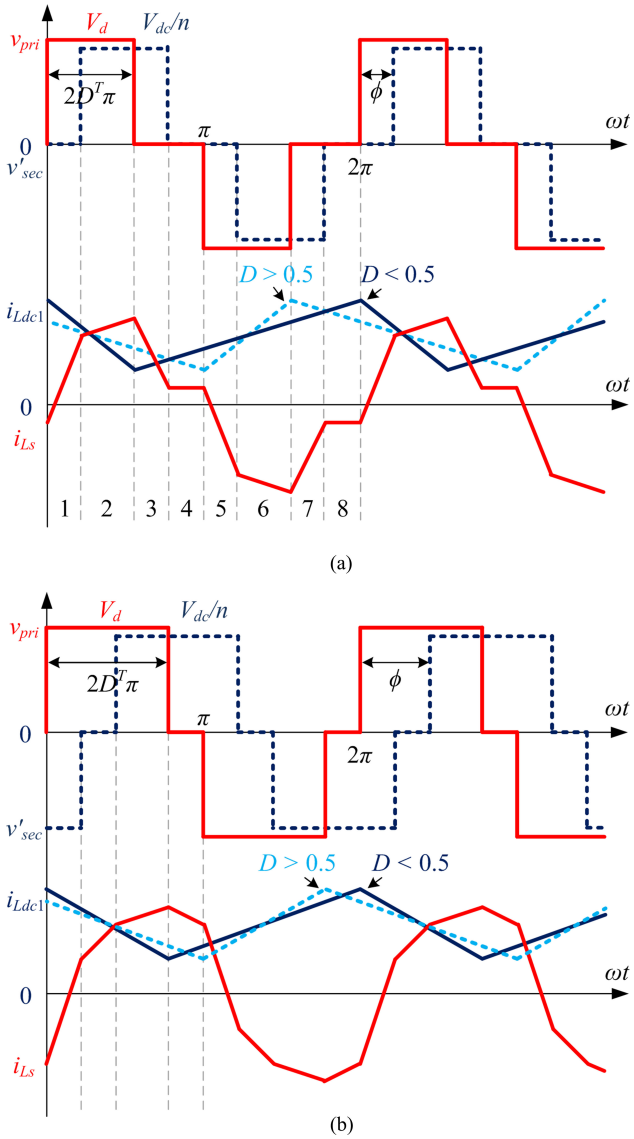


Fig. 5. Key waveforms of CF-DAB converter: (a) mode I, where $0 < D^T < 0.5$, $\phi < \min\{2D^T\pi, \pi - 2D^T\pi\}$, and (b) mode II, where $0.25 < D^T \leq 0.5$, $2D^T\pi < \phi < \pi - 2D^T\pi$. $D^T = \min\{D, 1-D\}$.

where V_d, $V_{\rm dc}$ are dc-link voltage at the LVS and HVS, n is the turns ratio of the transformer, ω is the switching frequency, D is the duty cycle, ϕ is the phase-shift angle between the HVS and LVS, and D^T is the minimal value of D and $(1-D)$.

The CF-DAB converter can be considered as a boost converter cascaded by a voltage-fed DAB converter whose power flow follows (2). The corresponding averaged model is constructed in Fig. 6 where the PV array is modeled as a current source paralleled with an equivalent output resistor of PV array operating at MPP, that is $R_{\rm mpp} = V_{\rm mpp}/I_{\rm mpp}$ [24]. Since the control cycle is the same as switching cycle in this paper, the step-delay effects are not considered and all the analyses are under s-domain. Based on the developed equivalent circuit model, the small-signal state-space equations can be derived in appendix (A-1)–(A-3). Accordingly, the control-to-output transfer functions $G_{v{\rm pv}\_d}(s)$, $G_{vd\_\phi}(s)$ are summarized in (3) and (4).

$$G_{v_{\rm pv}\_d}(s) = \begin{cases} \dfrac{2V_dC_ds + 4D\left[I_{L\,{\rm dc}1} - {\rm sgn}(0.5-D)\phi V_{\rm dc}/n\omega L_s\right]}{(sC_{\rm pv} + 1/R_{\rm mpp})\left[L_{\rm dc1}C_ds^2 + R_{L\,{\rm dc}1}C_ds + 2D^2\right] + 2C_ds} \\ \qquad {\rm Mode\,I}: 0 < \phi < \min\{2D^T\pi, \pi - 2D^T\pi\} \\ \dfrac{2V_dC_ds + 4D\left[I_{L\,{\rm dc}1} - {\rm sgn}(0.5-D)(1-2D^T)\pi V_{\rm dc}/n\omega L_s\right]}{(sC_{\rm pv} + 1/R_{\rm mpp})\left[L_{\rm dc1}C_ds^2 + R_{L\,{\rm dc}1}C_ds + 2D^2\right] + 2C_ds} \\ \qquad {\rm Mode\,II}: 2D^T\pi < \phi < \pi - 2D^T\pi, D^T > 0.25 \end{cases} \tag{3}$$

$$G_{vd\_\phi}(s) = \begin{cases} \dfrac{-(V_{\rm dc}/n\omega L_s)(2D^T - \phi/\pi)\left[(sL_{\rm dc1} + R_{L\,{\rm dc}1})(sC_{\rm pv} + 1/R_{\rm mpp}) + 2\right]}{(sC_{\rm pv} + 1/R_{\rm mpp})\left[L_{\rm dc1}C_ds^2 + R_{L\,{\rm dc}1}C_ds + 2D^2\right] + 2C_ds} \\ \qquad {\rm Mode\,I}: 0 < \phi < \min\{2D^T\pi, \pi - 2D^T\pi\} \\ \dfrac{-(V_{\rm dc}/n\omega L_s)(1 - 2\phi/\pi)\left[(sL_{\rm dc1} + R_{L\,{\rm dc}1})(sC_{\rm pv} + 1/R_{\rm mpp}) + 2\right]}{(sC_{\rm pv} + 1/R_{\rm mpp})\left[L_{\rm dc1}C_ds^2 + R_{L\,{\rm dc}1}C_ds + 2D^2\right] + 2C_ds} \\ \qquad {\rm Mode\,II}: 2D^T\pi < \phi < \pi - 2D^T\pi, D^T > 0.25. \end{cases} \tag{4}$$

As can be seen, the converter is a third-order system that has three poles, including a pair of conjugated poles due to the *LC* resonant network. The natural frequency ω_n of the *LC* network can be determined by

$$\omega_n = \sqrt{\frac{2(C_d + D^2C_{\rm pv})}{L_{\rm dc1}C_dC_{\rm pv}}}. \tag{5}$$

With given *LC* parameters, the resonant characteristic mainly varies with $R_{\rm mpp}$ and the control variable (D, ϕ), which are determined by the PV operating condition ($V_{\rm pv}$, P). To illustrate the impact of PV operating condition on the system dynamic, bode plots of $G_{v{\rm pv}\_d}(s)$, $G_{vd\_\phi}(s)$ under different ($V_{\rm pv}$, P) are shown in Fig. 7. Experimental circuit parameters of a down-scaled 5-kW prototype as listed in Table I in Section V are used in calculation. To verify the small-signal model, ac sweep results from circuit simulation in PSIM are also depicted in Fig. 7. The small-signal gains of the derived model matches well with the simulation results, demonstrating good accuracy of the derived model. As can be seen, the operating condition has less impact on $G_{v{\rm pv}\_\phi}(s)$ compared to $G_{v{\rm pv}\_d}(s)$ due to the cancellation effect of the near pairs of conjugated zeros and poles. The natural damping frequencies ω_d of the PV system under different operating conditions are close to ω_n at around 6.2 kHz, which is above 1/10 of switching frequency of dc–dc stage and 1/2 of that of the inverter stage. Moreover, the resonant peak magnitude varies significantly with operating conditions. When input voltage is high and the power is low, the converter presents as a very low damping system. And these two characteristics make the controller design of PV voltage control difficult in compromising between the high control bandwidth and high system stability.

B. Low-Frequency Power Mitigating Control

To make the control system more robust, a dual-loop control is adopted for PV voltage control. Within the PV voltage loop control, input inductor current feedback control is inserted as an inner-loop control. With the introduced state feedback control,

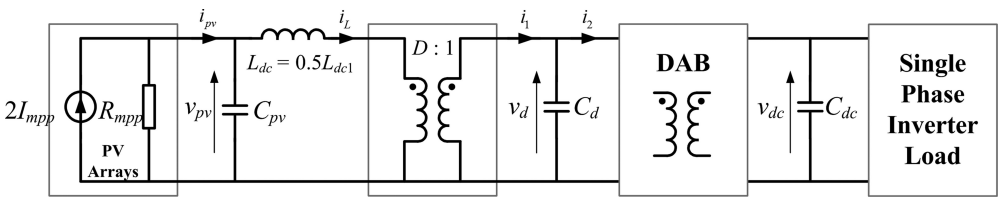


Fig. 6. Averaged equivalent circuit of CF-DAB-based PV converter operating at MPP.

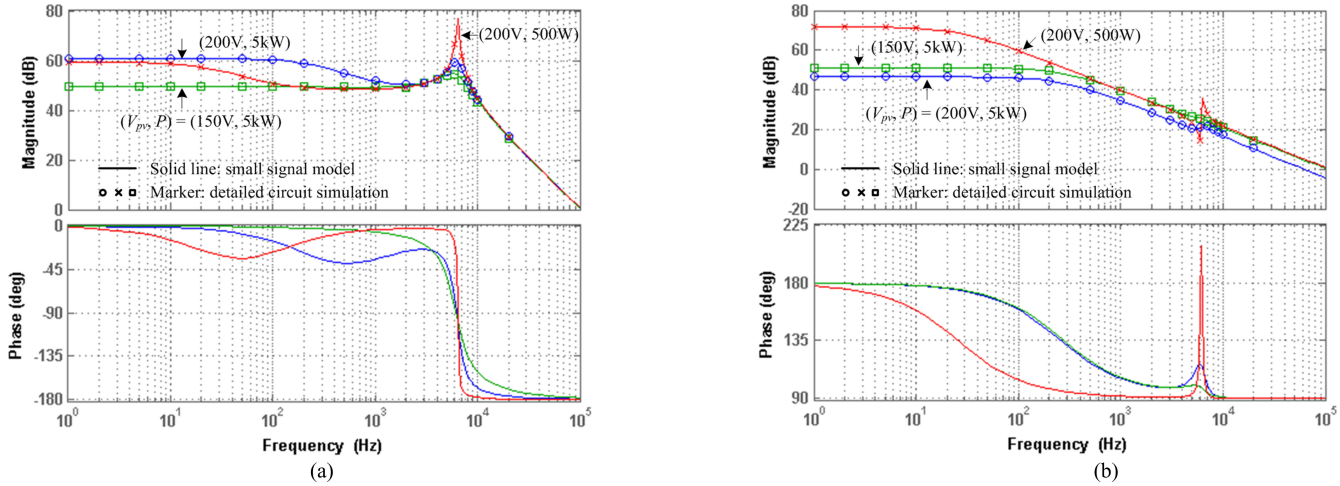


Fig. 7. Bode plots of control-to-output transfer functions under different conditions: (a) $G_{v\mathrm{pv}\_d}(s)$, and (b) $G_{vd\_\phi}(s)$.

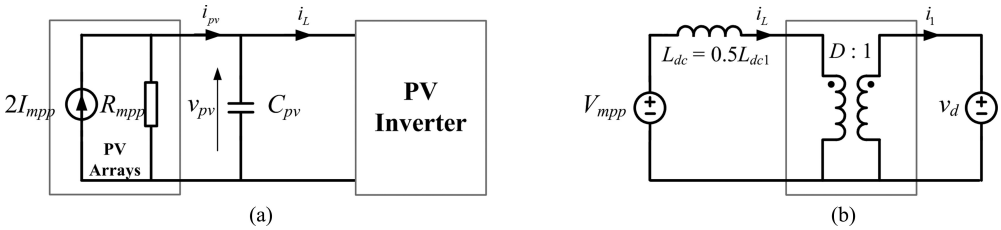


Fig. 8. Equivalent circuit model for PV voltage dual-loop control: (a) PV voltage loop, and (b) inductor current loop.

the system order degrades from 3 to 2, which simplifies the system dynamic response. In addition, v_d is fed forward to cancel the impact of the disturbance on the bus voltage so that the current loop of i_L with duty-cycle control is decoupled from the voltage loop of v_d with phase-shift control. As a result, the system order is further reduced for the duty-cycle control loop, which greatly simplifies the controller design. The simplified system diagram is shown in Fig. 8. In the inner current loop, the PV is considered as a constant voltage source due to its slow dynamic response, while v_d is a voltage disturbance source. With a high-bandwidth inner current loop, the inductor current can be well regulated such that low-frequency ripple can be eliminated. Consequently, the PV voltage loop are freed from ripple voltage control; hence, a much lower bandwidth loop can be used, which make the system more robust.

Based on the developed equivalent circuit model, the system control block diagram is described in Fig. 9. $H_r(s)$ is the transfer function of the feedback filter, which in experiment is a first-order low-pass filter with corner frequency of 1/3 switching frequency. $G_{cv}(s)$, $G_{ci}(s)$ are the compensators for PV voltage loop and inductor current loop, respectively, which are given in (6) and (7). PI controllers are implemented for both control loops. Particularly, a resonant controller is inserted to current loop in order to boost the control loop gain at 2ω such that 2ω ripple in the inductor current can be neglected

$$G_{cv} = -0.05 - \frac{10\pi}{s} \tag{6}$$

$$G_{ci} = -1 - \frac{0.0002}{s} - \frac{200\pi s}{s^2 + 4\pi s + (2\omega)^2}. \tag{7}$$

The bode plots of the compensated loop gain at $v_{\mathrm{pv}} = 150$ V and $P = 5$ kW are shown in Fig. 10. The current loop has a cut-off frequency of 2.36 kHz and a gain of 59 dB at 2ω (i.e., 120 Hz), while the PV voltage loop has a low bandwidth of 23 Hz, which satisfies both 2ω component attenuation and MPPT. The pole-zero locus of the closed PV voltage loop are also given in Fig. 11 to evaluate the control system stability and performance

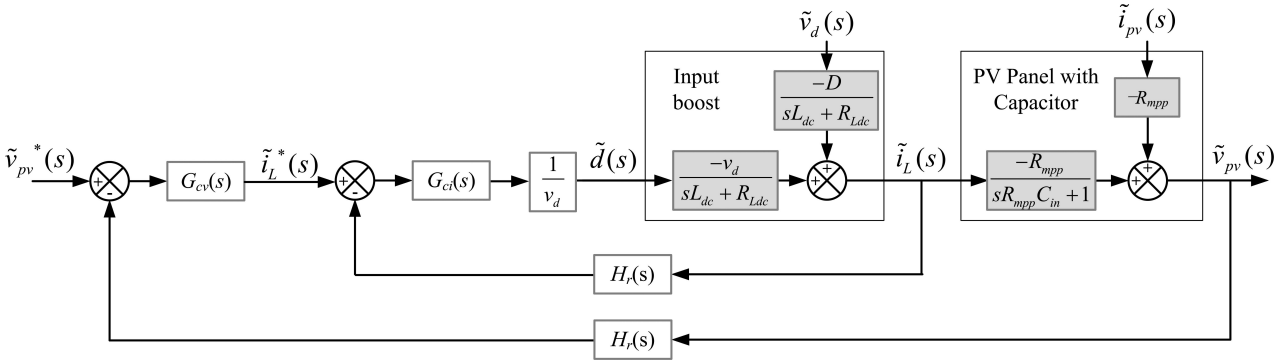


Fig. 9. Control block diagram of the PV voltage control.

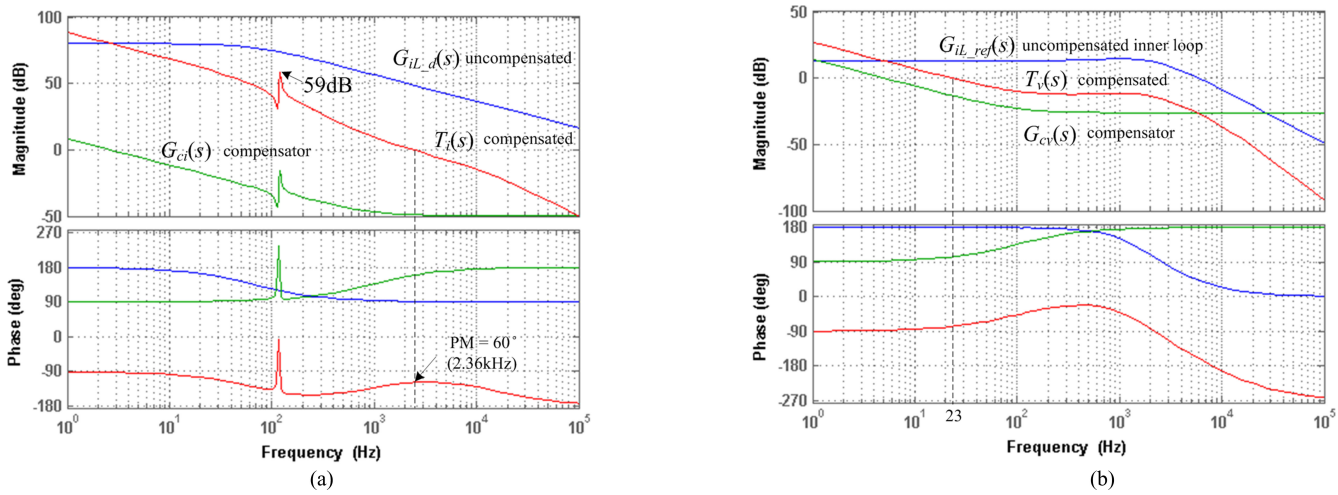


Fig. 10. Bode plots of control system when $v_{\rm pv} = 150$ V, $P = 5$ kW: (a) inductor current loop and (b) PV voltage loop.

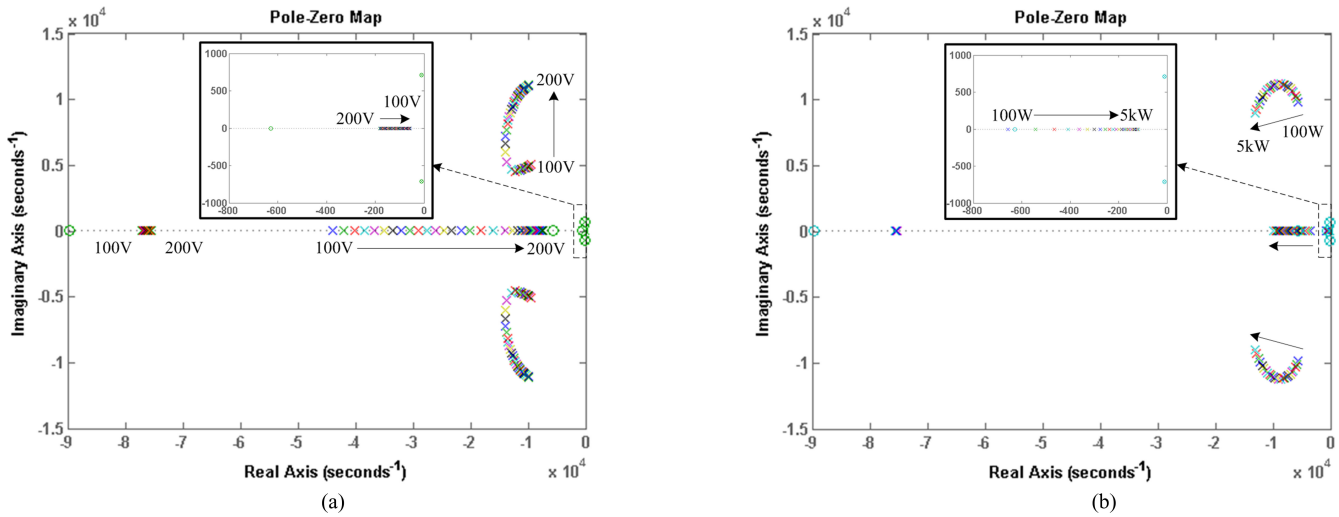


Fig. 11. Pole-zero locus of transfer function from $v_{\rm pv}{}^{*}$ to $v_{\rm pv}$: (a) $P = 5$ kW, $v_{\rm pv}$ varies from 100 V to 200 V and (b) $v_{\rm pv} = 150$ V, P varies from 100 W to 5 kW.

with PV array under different operating conditions. The system is always stable in the designed operating range since all the poles of the closed-loop system are in the left half plane. However, as seen from zoomed poles locus, the system shows slower dynamic response at condition of lower input voltage or higher power.

C. DC-Link Voltage Synchronizing Control

Due to large voltage variation on the HVS side, dc-link voltage synchronizing control, i.e., "$d = 1$" control, is applied to the LVS bus voltage control to avoid large peak current inside the converter resulting from voltage mismatch between the LVS

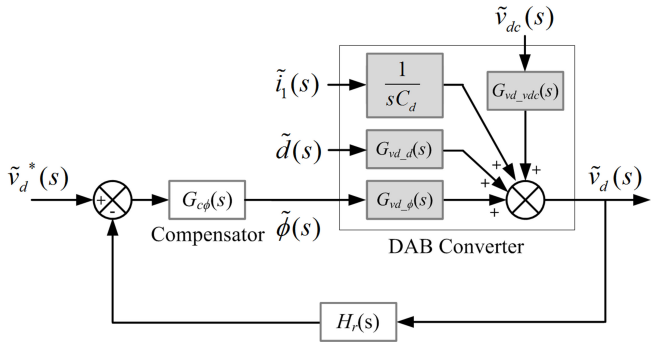


Fig. 12. Control block diagram for LVS voltage loop.

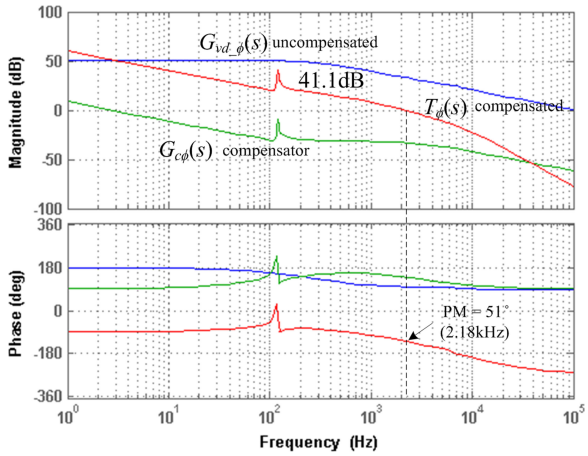


Fig. 13. Bode plots of LVS bus voltage loop when $v_{\rm pv} = 150$ V, $P = 5$ kW.

and HVS side. The transfer function $G_{vd\_\phi}(s)$ derived in (4) is directly used for the phase-shift controller design. The corresponding control block diagram is shown in Fig. 12. $G_{vd\_d}(s)$, $G_{vd\_i{\rm pv}}(s)$, $G_{vd\_v{\rm dc}}(s)$ are the transfer functions from disturbance sources to bus voltage v_d, and $G_{c\phi}(s)$ is the transfer functions of the phase-shift controller.

A modified PI with plugged resonant controller in (8) is selected to compensate the phase-shift loop. A pole at -6000π rad/s, around half of the natural frequency, is placed to attenuate the possible resonant peak resulting from the conjugated poles at low power condition as shown in Fig. 7(b). In addition, the resonant controller ensures system with enough gain at 2ω frequency so that the LVS voltage is well synchronized with the HVS voltage. Therefore, the transformer peak current can be minimized, resulting in low current stress and improved system efficiency [23]

$$G_{c\phi} = \frac{-514(s+200\pi)}{s(s+6000\pi)} + \frac{-1.26\pi s}{s^2+4\pi s+(2\omega)^2}. \qquad (8)$$

Fig. 13 shows the bode plots of the LVS bus voltage control loop at $v_{\rm pv} = 150$ V and $P = 5$ kW. As shown, the phase-shift control loop has a cut-off frequency at 2.18 kHz with 51° phase margin after compensation. And with the inserted resonant controller, the system has a gain of 41.1 dB at 2ω (i.e., 120 Hz).

D. Variable Step-Size MPPT With Fast Tracking

The proposed variable step-size MPPT strategy based on an INC method is sketched in Fig. 14. To realize fast MPPT, an online step-size calculation algorithm adapted to the PV system operating conditions is developed in Fig. 14(b). $dv_{\rm pv}$, $di_{\rm pv}$, $dp_{\rm pv}$, and $p_{\rm pv}$ are first calculated using the filtered PV voltage and inductor current to avoid sensing noise in the circuit. Then, according to $dp_{\rm pv}$, the step-size algorithm is divided into two separate paths. If the changed power is above the threshold $dP_{\rm th}$ for two times in succession, rapid irradiation change mode is detected, otherwise the converter continues with step-size calculation in slow irradiation change mode.

Fig. 15 shows the operating paths of the INC method under rapid irradiation change. During rapid irradiation change, the operating PV curves change dramatically. Ideally, if the PV converter can follow the operating path *a*, all the available power can be extracted from the PV array. However, this extra power change due to irradiation variation may confuse the MPPT algorithm, which may lead to MPPT failure and energy waste as illustrated in operating path *b* and *b'*. To avoid possible MPPT failure, the PV voltage is kept unchanged as long as the rapid irradiation change is detected, as shown in operating path *c*. Since the MPP voltage does not vary much for different irradiation level, this unchanged PV voltage is close to new MPP voltage; therefore, most of the power generated can still be extracted. Once the irradiation change become slowly, a large MPPT step $V_{\rm fast}$ will be used at first for fast tracking of the new MPP. After the new MPP is crossed twice, the voltage step size is scaled down by factor k_s in each MPPT cycle. When the step size is smaller than $V_{\rm th}$, the MPPT exits the rapid irradiation change mode, switching to slow irradiation change mode. With this algorithm, the energy waste during rapid irradiation change is reduced, and the system achieves fast tracking under rapid irradiation change without failure.

As for slow irradiation change mode, $v_{\rm step}$ is calculated online in (9) according to the PV power and voltage variations

$$v_{\rm step} = f(p_{\rm pv}, dp_{\rm pv}, dv_{\rm pv}) = (k_1 - k_2 p_{\rm pv})\frac{dp_{\rm pv}}{dv_{\rm pv}} \qquad (9)$$

where k_1 and k_2 are the coefficients related to the PV system parameters and dynamics. When the PV voltage is far away from the MPP voltage, a large $v_{\rm step}$ will be applied. In addition, a scale factor negatively correlated with PV power is multiplied to balance the performance in low-power or high-power condition. With properly selected k_1 and k_2, fast MPPT with low steady-state variation can be achieved. In experiment, $k_1 = 0.001$ and $k_2 = 0.0000001$. To smooth the PV voltage change, $v_{\rm step}$ is limited by

$$0.5 \cdot v_{\rm step}(k-1) \le v_{\rm step}(k) \le 2 \cdot v_{\rm step}(k-1). \qquad (10)$$

IV. Experimental Results

A downscaled 5-kW PV system prototype including one dc–dc converter module and one inverter module using SiC MOSFETs was built in the laboratory as shown in Fig. 16. PV emulators from Magna-Power were used to emulate a

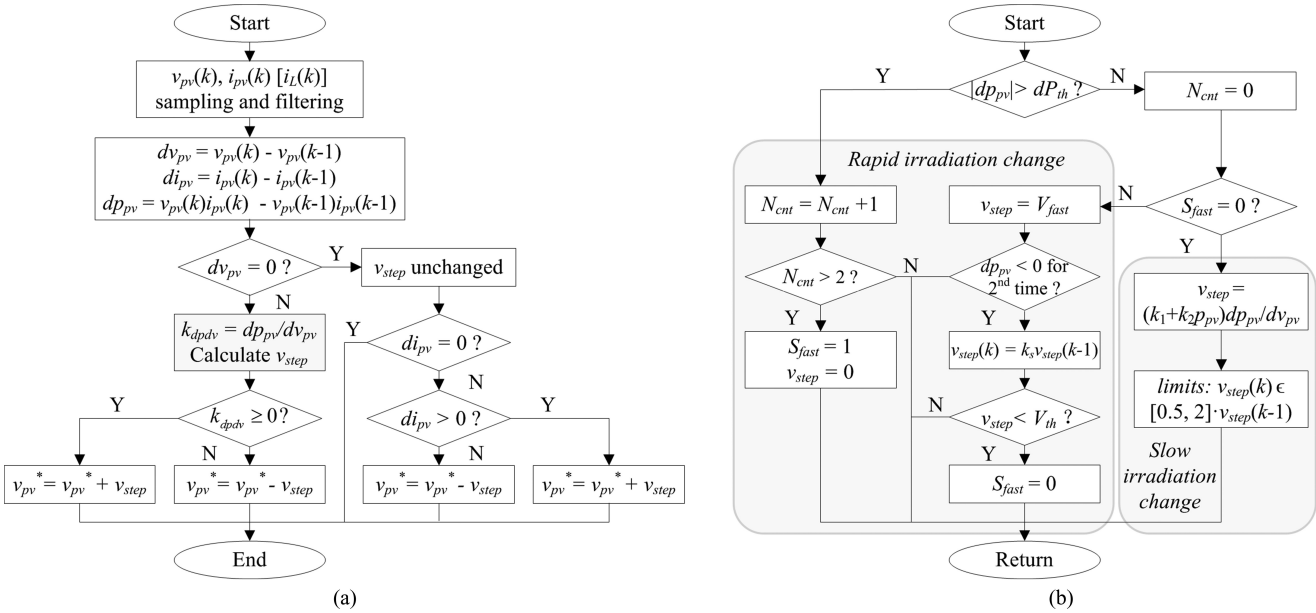


Fig. 14. Flow chart of proposed variable step-size INC MPPT strategy: (a) INC algorithm, and (b) variable step-size algorithm.

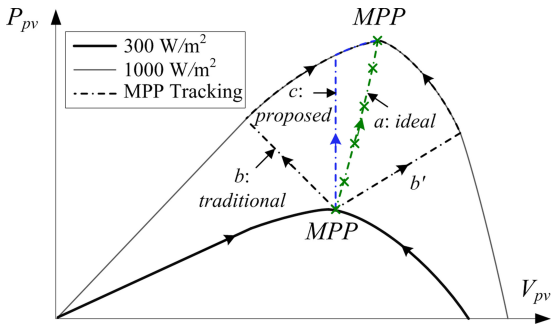


Fig. 15. Operating paths of INC MPPT method under rapid irradiation change.

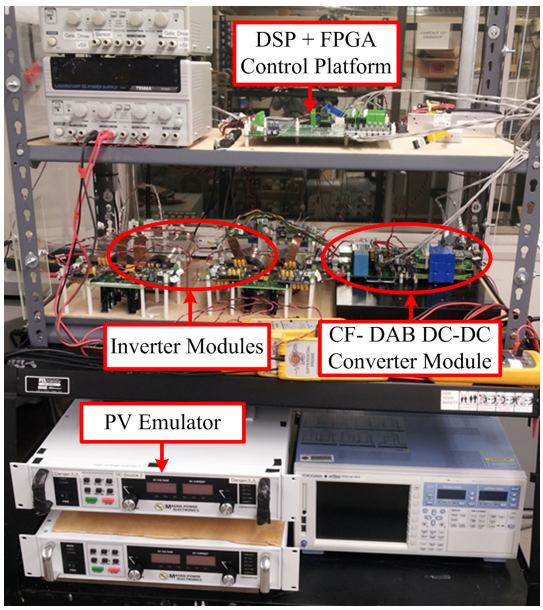


Fig. 16. Laboratory PV system prototype including one dc–dc module and one inverter module.

TABLE I
CIRCUIT PARAMETERS OF THE PV SYSTEM PROTOTYPE

Items	Descriptions	Value
V_{pv}	MPPT voltage range	100–200 V
V_d	Nominal LVS dc-link voltage	300 V
V_{dc}	Nominal HVS dc-link voltage	600 V
V_g	Grid RMS voltage	208 V
n	Transformer turns ratio	32:16
L_s	Leakage inductance of dc–dc converter	28.5 μH
L_{dc1}, L_{dc2}	DC inductor of dc–dc converter	143 μH
L_f	Line filter inductor of inverter	2 mH
C_{pv}	Input capacitor of dc–dc converter	10 μF
C_d	LVS dc-link capacitor	30 μF
C_{dc}	HVS dc-link capacitor	120 μF
S_p	LVS switches	FCH76N60N
S_s	HVS switches	CMF20120D
f_{sw1}	Switching frequency of dc–dc stage	50.4 kHz
f_{sw2}	Switching frequency of inverter stage	10.08 kHz
f_{mppt}	MPPT frequency	10 Hz

150-V / 4.1-kW PV string under the standard irradiance (1000 W/m^2) and the room temperature (25 °C). The proposed control strategy was implemented in digital signal processors and field-programmable gate array control platform. The system circuit parameters are listed in Table I, where the HVS dc-link voltage is reduced to 600 V due to low grid voltage of 208 V. The following experimental results are provided to demonstrate the performance of the proposed PV system.

Fig. 17 shows the steady state and dynamic performance of the PV system with disabled MPPT. In Fig. 17(a), the irradiation level increased from 300 to 1000 W/m^2 within 1.5 s. Fig. 17(b) and (c) are the zoomed waveforms at steady state under the irradiation of 300 W/m^2 and 1000 W/m^2, respectively. As can be seen, with a small dc-link capacitor (120 μF), a large voltage variation of 146 V is observed on the dc-link at 1000 W/m^2 (4.1 kW), which is 24.3% of the normal voltage. And with the

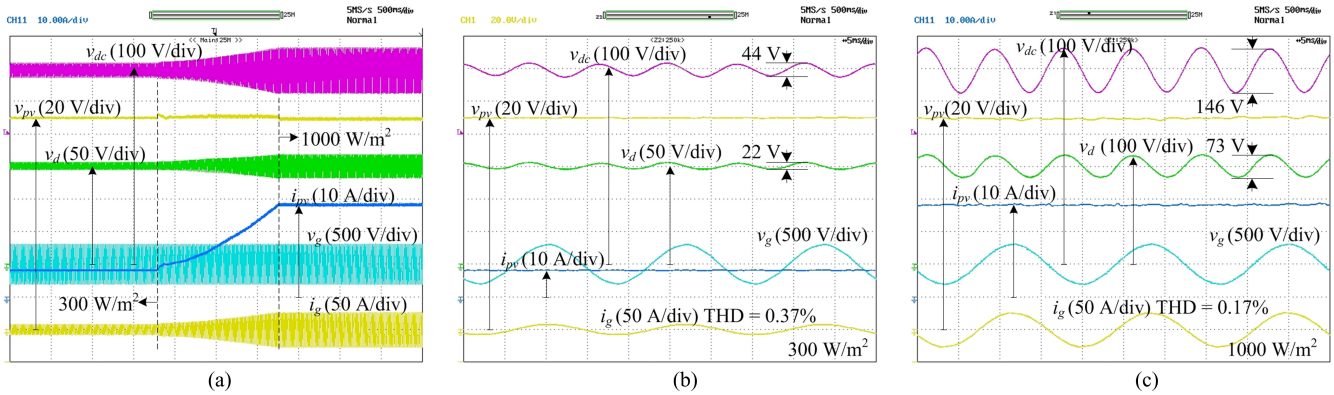


Fig. 17. Steady state and dynamic responses of the PV system under solar irradiance change: (a) dynamics response under irradiance change from 300 to 1000 W/m^2, (b) zoomed steady-state waveforms at 300 W/m^2, and (c) zoomed steady-state waveforms at 1000 W/m^2.

proposed PIR controller, the LVS voltage follows stiffly with the HVS voltage. The PV voltage is well regulated at 150 V in steady state without low-frequency ripple, which demonstrates the high performance of the proposed low-frequency power mitigation control. During the transient, the HVS and LVS ripple voltage, and the grid current increase smoothly with the PV current; and the PV voltage shows a negligible variation, which can be further improved with an increased bandwidth of the control loop. The total harmonic distortion of grid current is less than 1% for both 300 and 1000 W/m^2 irradiation level.

Fig. 18 illustrates the transformer current and ZVS waveforms of the CF-DAB dc-dc module under proposed control strategy. As the dc-link voltage swings at 120 Hz, the transformer current also shows a swinging envelope. However, the LVS dc-link voltage is synchronized with the HVS dc-link voltage using "$d = 1$" control, thus the transformer current in each switching cycle has a flat top or bottom as shown in the zoomed waveforms. Therefore, the peak current stress on the transformer and switching devices are minimized. It can also be seen that ZVS are achieved in both LVS switches and HVS switches, demonstrating the converter has low switching loss.

Fig. 19 demonstrates the performance of the PV system with the proposed variable step-size MPPT strategy. Fig. 19(a) shows the steady-state and dynamic MPPT waveforms, while Fig. 19(b) depicts the corresponding MPPT trajectories of *P–V* and *I–V* curves. In steady state, the PV voltage ripple around the MPP is less than 2 V at 300 W/m^2 and 4 V at 1000 W/m^2. This small variation ensures the MPPT efficiency higher than 99.5%. The dynamic MPPT process under rapid irradiation change is also captured as shown from $t_0 - t_3$. From $t_0 - t_1$, the rapid irradiation change is detected with the $dp_{\rm pv}$ larger than 50 W. During this period, the PV voltage is regulated as unchanged. Then, from $t_1 - t_2$, the MPPT step size is set to 2 V in order for fast tracking the new MPP. At t_2, where the converter crosses the MPP for the second time, the MPPT step size begins to decrease by a factor of 0.6 in each MPPT cycle. And finally, at t_3, the MPPT step size is less than 0.2 V and the MPPT algorithm switches to slow irradiation change mode.

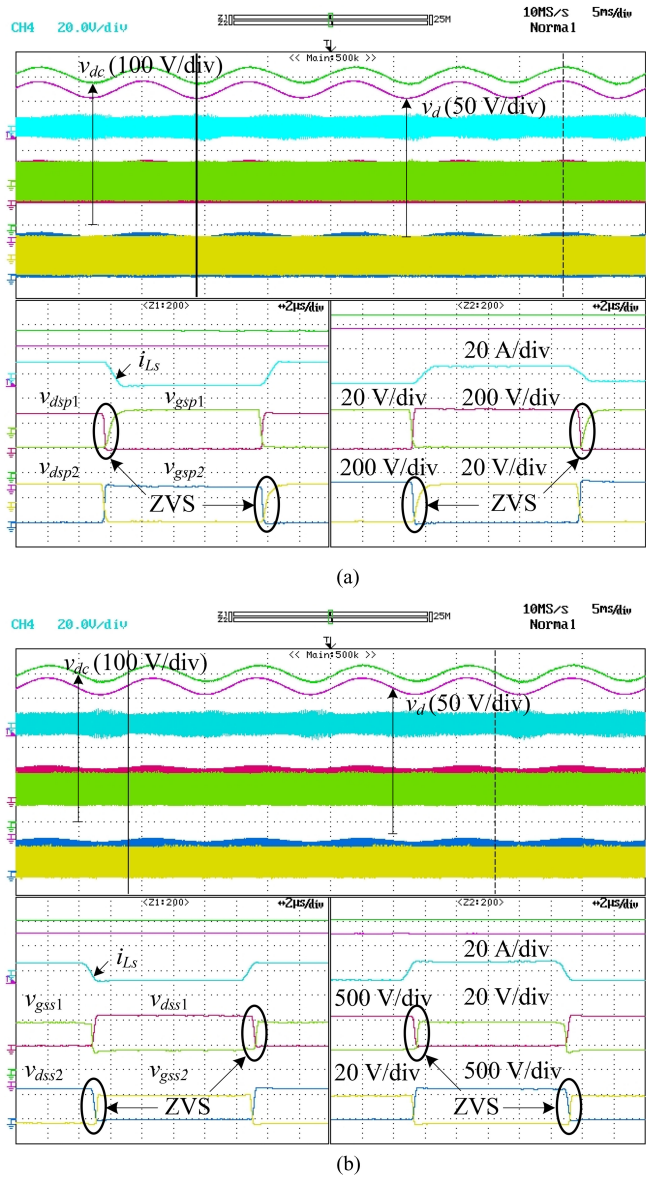
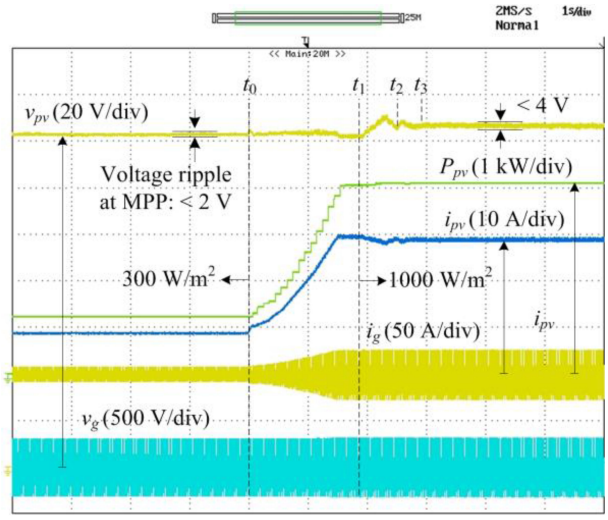
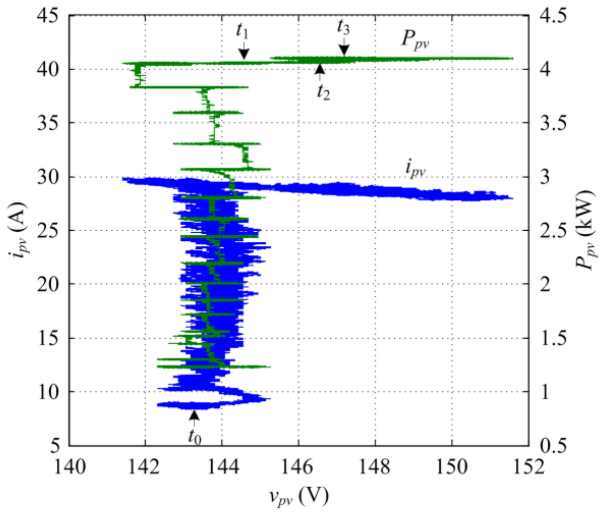


Fig. 18. ZVS operating waveforms of CF-DAB converter: (a) S_{p1} and S_{p2}, (b) S_{s1} and S_{s2}.



(a)



(b)

Fig. 19. MPPT of the PV inverter under solar irradiance change (a) input and output waveforms, and (b) MPPT trajectories.

V. Conclusion

In this paper, a grid-tied CMI PV system based on CF-DAB dc-dc converters using small dc-link capacitors has been proposed. "$d = 1$" control was applied to minimize the peak current stress in the converter by synchronizing the LVS dc-link voltage with HVS dc-link voltage. A detailed low-frequency power mitigation control for the CF-DAB converter was proposed based on the dynamic model of the converter. With the proposed dual-loop control using PIR controller, the large low-frequency voltage ripple on the dc-link can be blocked away from the PV side. This proposed power mitigation control can be extended to other current-fed topologies, e.g., CF-DHB and CF-DAB3. An autonomous variable step-size INC MPPT method was also proposed. Fast tracking speed under rapid irradiation change and high MPPT efficiency (>99.5%) were realized for the PV system. Experimental results of the 5-kW PV converter module were given to verify the power mitigation control and MPPT method.

Appendix

State-space equations for the small-signal model of a CF-DAB dc–dc converter

$$\begin{cases} \dot{\tilde{x}} = A\tilde{x} + B\tilde{u} \\ y = C\tilde{x} \end{cases}, \begin{cases} x = [i_{\mathrm{Ldc1}}, v_{\mathrm{pv}}, v_d]^T \\ y = [v_{\mathrm{pv}}, v_d]^T \end{cases} \tag{A-1}$$

$$A = \begin{bmatrix} -\frac{R_{L\mathrm{dc1}}}{L_{\mathrm{dc1}}} & \frac{1}{L_{\mathrm{dc1}}} & -\frac{D}{L_{\mathrm{dc1}}} \\ -\frac{2}{C_{\mathrm{pv}}} & -\frac{1}{R_{\mathrm{mpp}} C_{\mathrm{pv}}} & 0 \\ \frac{2D}{C_d} & 0 & 0 \end{bmatrix}, C = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{A-2}$$

Mode I

$$B = \begin{bmatrix} \frac{-V_d}{L_{\mathrm{dc1}}} & 0 & 0 \\ 0 & 0 & 0 \\ X & \frac{V_{\mathrm{dc}}(\phi - 2\pi D^T)}{\pi n \omega L_s C_d} & \frac{\phi(\phi - 4\pi D^T)}{\pi n \omega L_s C_d} \end{bmatrix}$$

where

$$X = \frac{2n\omega L_s I_{L\mathrm{dc1}} - \mathrm{sgn}(0.5 - D) 2\phi V_{\mathrm{dc}}}{n\omega L_s C_d}.$$

Mode II

$$B = \begin{bmatrix} \frac{-V_d}{L_{\mathrm{dc1}}} & 0 & 0 \\ 0 & 0 & 0 \\ Y & \frac{(2\phi - \pi)V_{\mathrm{dc}}}{\pi n \omega L_s C_d} & \frac{\pi^2 (1 - 2D^T)^2 - 2\phi(\pi - \phi)}{2\pi n \omega L_s C_d} \end{bmatrix}$$

where

$$Y = \frac{2n\omega L_s I_{L\mathrm{dc1}} - \mathrm{sgn}(0.5 - D) 2\pi (1 - 2D^T) V_{\mathrm{dc}}}{n\omega L_s C_d}. \tag{A-3}$$

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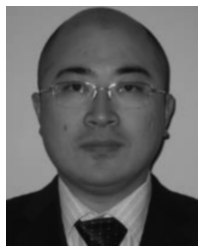

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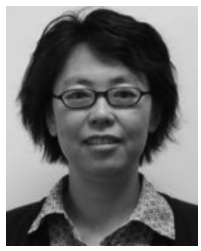

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