Dual Switches DC/DC Converter With Three-Winding-Coupled Inductor and Charge Pump

Yu Tang, *Member, IEEE*, Dongjin Fu, Jiarong Kan, *Member, IEEE*, and Ting Wang

***Abstract*—In order to obtain a high step-up voltage gain, high-efficiency converter, this paper proposed a dual switches dc/dc converter with three-winding-coupled inductor and charge pump. The proposed converter composed of dual switches structure, three-winding-coupled inductor, and charge pump. This combination facilitates realization of high step-up voltage gain with a low voltage/current stress on the power switches. Meanwhile, the voltage across the diodes is low and the diode reverse-recovery problem is alleviated by the leakage inductance of the three-winding-coupled inductor. Taking all these into consideration, the efficiency can be high. This paper illustrated the operation principle of the proposed converter; discussed the effect of leakage inductance on voltage gain; the conditions of zero current shutting off of the diodes are illustrated; the voltage and current stress of the power devices are shown; a comparison between the performance of the proposed converter and previous high step-up converters was conducted. Finally, a prototype rated at 500 W has been established, and the experimental results verify the correctness of the analysis.**

***Index Terms*—Charge pump, dual switches, high step-up voltage gain, three-winding-coupled inductor.**

I. Introduction

FACING the pressure from environment protection and energy shortage, development of the green energy is a most effective solution. Unfortunately, the output of the green energy source, such as photovoltaic cell and fuel cell, is relatively low (usual lower than 50 VDC) compared to the dc bus voltage (200 or 400 VDC). Thus, a high step-up voltage gain dc/dc converter with high efficiency should be introduced to boost the voltage, then the green energy can be connected to the grid. Considering isolated topologies may decrease the efficiency and increase the system volume, the nonisolated topologies seem to be more attractive choices [1]–[5].

Among the nonisolated dc–dc converters, the boost converter is usually used for voltage step up. However, the duty cycle will approach to 1 when the output voltage is much higher than the input voltage. Thus, the current ripple of the inductor and current stress of the power device are large, which results in large conduction loss, switching loss, and low efficiency [6]. In order to extend the voltage gain, lots of researches have been done. Generally speaking, the common high step-up voltage gain dc/dc converter can be classified into four species: the cascade Boost topology, the switched-cell Boost topology, the coupled-inductor Boost topology, and the mixture of these three. By cascading another boost converter, a high voltage gain can be easily obtained, but too many components are required, leading to high cost and low overall efficiency [7]. With the transition in series and parallel connection of the switched cell, an inherent high voltage gain can be achieved. However, the voltage-conversional ratio is difficult over ten times and the pulsating voltage or pulsating current will result in more electromagnetic interference. According to the kind of energy storage element, switched-cell Boost converters can be generalized into switched-inductor Boost converter (SL-C) [8]–[10] and switched-capacitor Boost converter (SC-C) [11], [12]; the voltage stress across the power devices of the SL-C is relatively high, while the current through the power switch of the SC-C is high, which have a big influence on the efficiency. Aiming to solve these problems, coupled-inductor Boost converters have been discussed [13]–[20]. Lots of researches have been done on this topic, the voltage ratio can be increased by raising the turns ratio, the reverse-recovery problem of the diodes is partly solved due to the leakage inductor. In fact, these converters are the derivations of the tradition Boost converter, which inheriting the disadvantages of the Boost converter, the RMS current through the switch is relatively high and the voltage stress across the output diode is high.

Yang *et al.* [21] have proposed a dual-switch converter, which compared to the Boost converter can provide a higher voltage gain with a lower voltage/current stress of the switches. Based on [21], this paper propose a dual switches dc/dc converter with three-winding-coupled inductor and charge pump. The proposed converter can provide a relatively high voltage conversion ratio with a high efficiency, the dual switches structure reduce the voltage/current stress of the switches; the magnetic components can be integrated into one magnetic core, which is helpful to simplify the structure; take the advantages of the leakage

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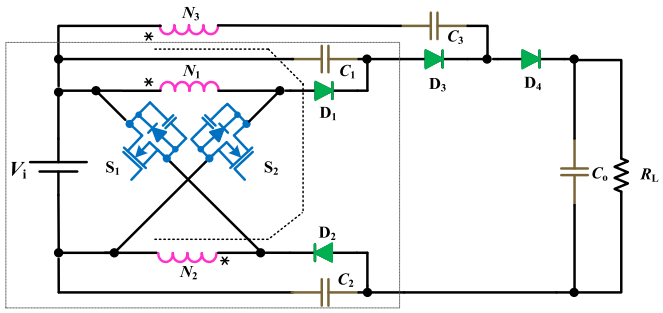

Fig. 1. Circuit diagram of the proposed converter.

inductor, all the diodes can realize the ZCS to reduce the loss. A prototype with 30–50 V input/400 V output/500 W power is established in the lab, and experiments have been done to verify the analysis.

II. Operation Principle of the Proposed Converter

Fig. 1 shows the topology of dual switches dc/dc converter with three-winding-coupled inductor and charge pump. The switches S_1 and S_2 share the same operation signal; the capacitors C_1 and C_2 are used to absorb the energy of leakage inductor and clamp the voltage across S_1 and S_2; C_3 is the capacitor of charge pump, which is used to add the voltage conversion ratio; N_1, N_2, and N_3 are the windings of the three-winding-coupled inductor.

The turns ratio of N_1, N_2, and N_3 is 1:1:n; In order to simplify the analysis, some assumptions have been made:

1) since the dual switches structure in the dotted box is a symmetrical topology, all the symmetrical components of the dual switches structure are exactly share the same operation modes;
2) the capacitance of C_1, C_2, and C_o are largely enough, that the voltage v_{c1}, v_{c2}, and v_o could be treated as a constant.

Fig. 2 illustrated the operation waveforms of the proposed converter; a resonance loop is formed by the leakage L_k and the capacitor C_3. According to the relationship between the resonance period and the on-state period (DT_s), the proposed converter can operates in two modes: while $\pi\sqrt{L_kC_3} > DT_s$, the converter operates in the below resonance frequency mode (BRF mode), while $\pi\sqrt{L_kC_3} < DT_s$, the converter operates in the over resonance frequency mode (ORF mode). Fig. 3 shows the corresponding equivalence circuits. In BRF mode, the equivalence circuits are shown in Fig. 3(a)–(f); in ORF mode, the equivalence circuits are shown in Fig. 3(a), (b), (b′), and (c)–(f).

A. BRF Mode

1) Mode 1 [t_0–t_1]: During this stage, the power switches S_1 and S_2 start to conduct, the equivalence circuit is shown in Fig. 3(a). The voltage across the switches decreases to 0. With the help of leakage inductor L_k, the current through the turns N_1 and N_2 increase from 0, which is helpful to reduce the switching loss. The diodes D_1, D_2, and D_3 are reverse-biased, while D_4 is conducted; the leakage inductor L_k and capacitor C_3 begins to resonant, considering that this time interval is extremely short, the leakage inductor current i_{Lk} drops almost at a constant slope.

2) Mode 2 [t_1–t_2]: During this stage, S_1 and S_2 remains in conduction, the equivalence circuit is shown in Fig. 3(b). At the time of t_1, the leakage inductor current i_{Lk} decreases to zero, D_4 turns OFF with ZCS, and then, i_{Lk} keeps falling, D_3 turns ON, L_k and C_3 are still in resonance state.

The state equations of resonant circuit from t_1 to t_2 can be written as follows:

$$\begin{cases} L_k \dfrac{di_{\mathrm{Lk}}}{dt} = v_{C3} - nV_i - V_{C1} \\ C_3 \dfrac{dv_{C3}}{dt} = -i_{\mathrm{Lk}}. \end{cases} \tag{1}$$

Simplifying (1) gives

$$\begin{cases} i_{\mathrm{Lk}} = \dfrac{v_{C3}(t_1) - nV_i - V_{C1}}{Z_r} \sin\omega_r(t-t_1) \\ v_{C3} = -(nV_i + V_{C1}) + \left[nV_i + V_{C1} - v_{C3}(t_1)\right] \\ \qquad \sin\omega_r(t-t_1) \end{cases} \tag{2}$$

where Z_r and ω_r are defined as: $Z_r = \sqrt{L_k/C_3}$, $\omega_r = \sqrt{1/L_kC_3}$.

3) Mode 3 [t_2–t_3]: The equivalence circuit is shown in Fig. 3(c). At the time of t_2, S_1 and S_2 are turned OFF. N_1 and N_2 transfer energy to the parasitic capacitors of S_1 and S_2, the parasitic capacitors keep charging until D_1 and D_2 begin to conduct.

4) Mode 4 [t_3–t_4]: The equivalence circuit is shown in Fig. 3(d). At the time of t_3, N_1 and N_2 transfer energy to the clamping capacitors C_1 and C_2. C_3 charges the leakage inductor L_k in a resonance way, considering this time interval is extremely short, the leakage inductor current i_{Lk} rises almost at a constant slope.

5) Mode 5 [t_4–t_5]: The equivalence circuit is shown in Fig. 3(e). At the time of t_4, the leakage inductor current i_{Lk} rise to zero, D_3 turns OFF with ZCS, then i_{Lk} keeps rising and turns to positive, N_1 and N_2 keeps transferring energy to the clamping capacitors C_1 and C_2.

L_k and C_3 are still in resonance state, the state equations of resonant circuit can be written as follows:

$$\begin{cases} L_k \dfrac{di_{\mathrm{Lk}}}{dt} = nV_{C1} + V_i + V_{C2} + v_{C3} - V_o \\ C_3 \dfrac{dv_{C3}}{dt} = -i_{\mathrm{Lk}}. \end{cases} \tag{3}$$

Simplifying (3) gives

$$\begin{cases} i_{\mathrm{Lk}} = \dfrac{nV_{C1} + V_i + V_{C2} + v_{C3}(t_4) - V_o}{Z_r} \sin\omega_r(t-t_1) \\ v_{C3} = (nV_{C1} + V_i + V_{C2} - V_o) \\ \qquad -[nV_{C1} + V_i + V_{C2} + v_{C3}(t_4) - V_o]\sin\omega_r(t-t_1). \end{cases} \tag{4}$$

6) Mode 6 [t_5–t_6]: The equivalence circuit is shown in Fig. 3(f). At the time of t_5, the current through N_1 and N_2 decrease to 0, D_1 and D_2 turn OFF with ZCS.

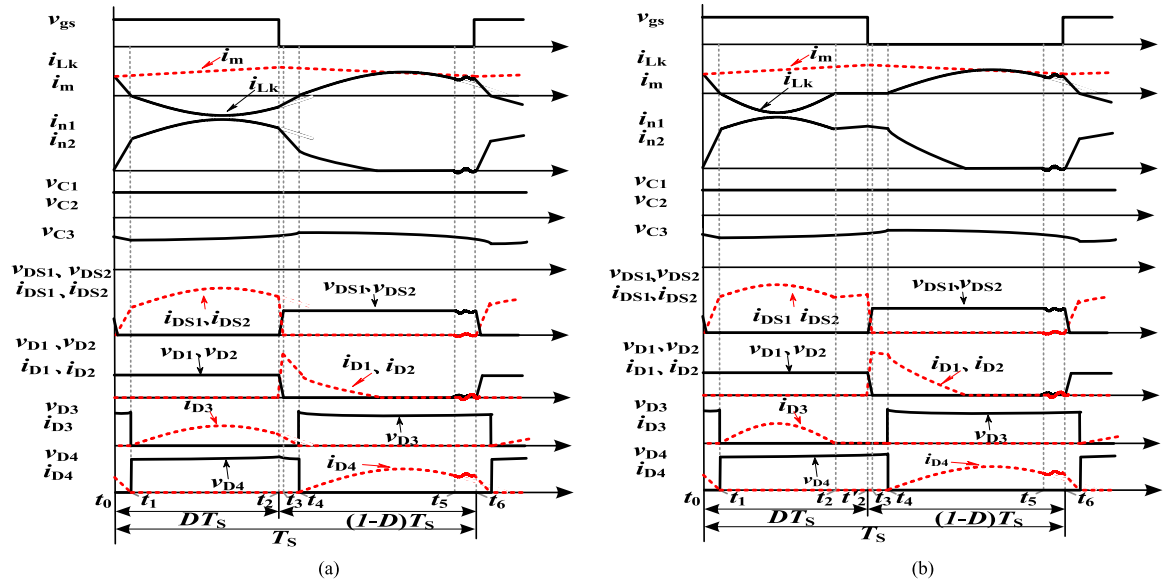

Fig. 2. Equivalent circuits of the converter.

B. ORF Mode

ORF is similar to that of BRF; the only difference is that ORF contains a new mode between the mode 2 and mode 3 of BRF:

2′) Mode 2′[$t_2 - t_2'$]: The equivalence circuit is shown in Fig. 3(b′). At the time of t_2, the current through D_3 decrease to zero and turns off with ZCS.

III. Analysis of the Proposed Converter

A. Voltage Gain

In ideal situation, the coupled inductors are well coupled and the leakage inductance is zero, the operation mode can be simplified to two modes.

When S_1 and S_2 turns ON, the magnetizing inductor is charged, the voltage across the magnetizing inductor could be expressed as

$$V_{Lm} = nV_i. \tag{5}$$

Obviously, the turns N_2, the power switch S_1, the diode D_2, and the clamping capacitor C_2 forms a Buck–Boost converter; the turns N_1, the power switch S_2, the diode D_1, the clamping capacitor C_1, and the capacitor C_o forms a Boost converter

$$\begin{cases} V_{C1} = \dfrac{1}{1-D}V_i - V_i = \dfrac{D}{1-D}V_i \\ V_{C2} = \dfrac{D}{1-D}V_i. \end{cases} \tag{6}$$

The voltage across the capacitor C_3 is

$$V_{C3} = \frac{D}{1-D}V_i + nV_i. \tag{7}$$

While during the OFF state, the magnetizing inductor is discharged, the voltage across the magnetizing inductor is

$$V_{Lm} = V_i + V_{C2} + V_{C3} - V_o = \frac{1+D}{1-D}V_i + nV_i - V_o. \tag{8}$$

Based on the voltage–second balancing of the magnetizing inductors, the voltage conversion ratio of the converter in ideal situation is

$$G_{\text{ideal}} = \frac{V_o}{V_i} = \frac{1+n+D}{1-D}. \tag{9}$$

However, the leakage inductor would causes some duty-cycle loss and leads to a voltage gain loss. In order to simplify the calculation, the extremely short time interval $[t_0 - t_1]$, $[t_2 - t_4]$ is ignored; the magnetizing inductor L_m is largely enough so that the magnetizing current I_{Lm} is treated as a constant. Fig. 4 shows the simplified waveforms of the proposed converter.

The simplified waveforms can be classified into three modes: During time interval $[t_0 - t_2]$, S_1, S_2, D_2, and D_5 are conducted, while D_1, D_3, and D_4 are reverse biased, the peak current of D_3 can be expressed as

$$i_{\text{peak}-D3} = \frac{2I_o}{D}. \tag{10}$$

During time stage $[t_0 - t_2]$, magnetizing current I_{Lm} is treated as a constant, the voltage across the leakage inductor is

$$V_{\text{Lk}(0-2)} = L_k \frac{-i_{\text{peak}-D3} - 0}{DT_s} = -\frac{2L_k I_o f_s}{D^2}. \tag{11}$$

From (7)) and (11), the voltage across C_3 in real situation can be calculated as

$$V_{C3}' = nV_i - \frac{2L_k I_o f_s}{D^2} + \frac{D}{1-D}V_i. \tag{12}$$

During the time interval $[t_2 - t_5]$, since the turns ratio of N_1, N_2, and N_3 is 1:1:n and the dual switches structure is a symmetrical topology, the current through N_1, N_2, and N_3 could be defined as n:n:2, the peak current of D_1 and D_2 is

$$i_{\text{peak}-D1} = i_{\text{peak}-D2} = \frac{n}{2}I_{LM}. \tag{13}$$

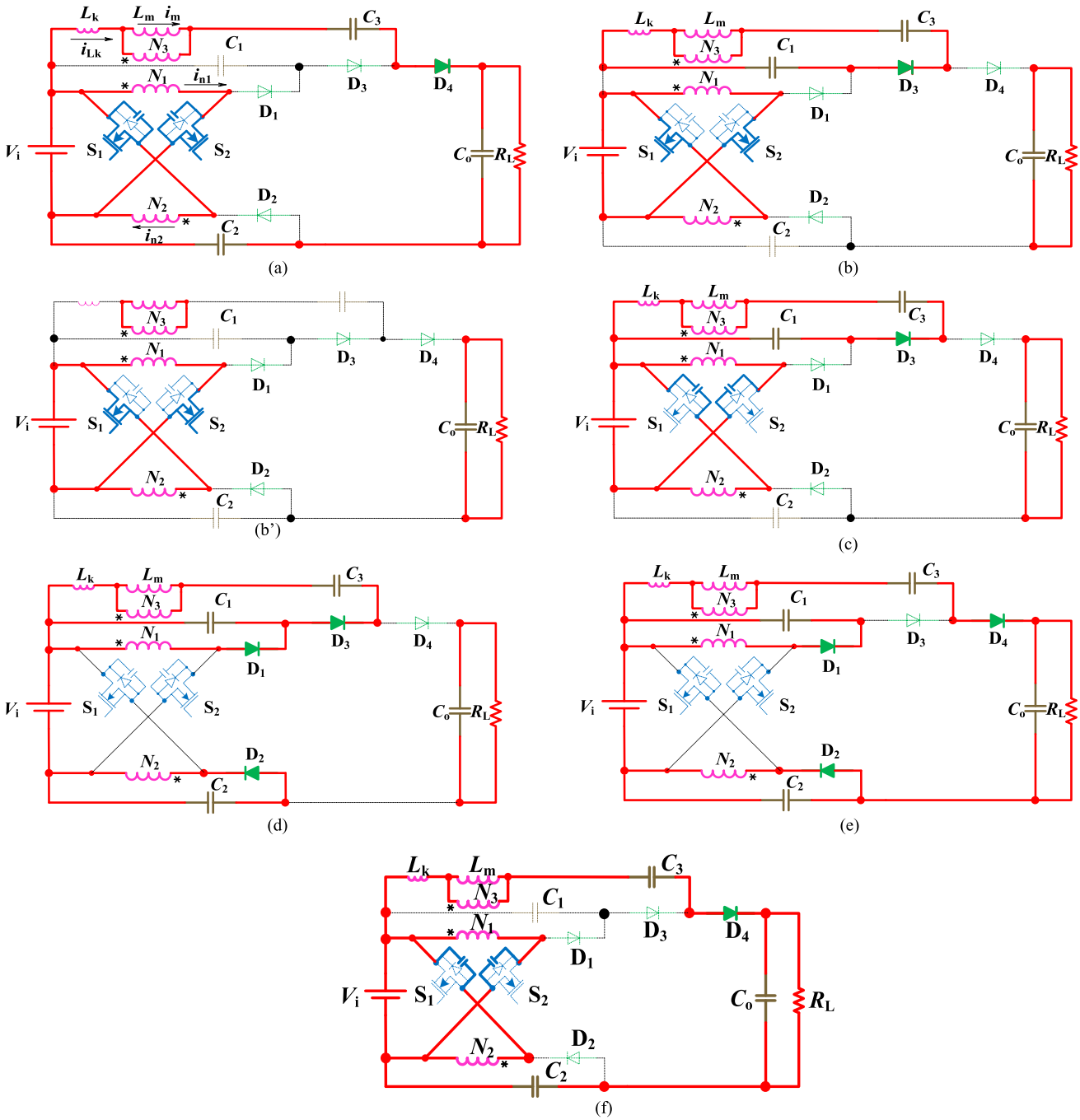

Fig. 3. Equivalent circuits of the converter.

Assuming the duration of mode 2 $[t_2 - t_5]$ is t, the electric through D_1 and D_2 is

$$Q_1 = \frac{1}{2} \cdot \frac{n}{2} I_{LM} \cdot t \tag{14}$$

During the time stage $[t_2 - t_6]$, the electric charge through D_4 can be defined as

$$Q_2 = \frac{1}{2} I_{Lm} \cdot t + [(1-D)T_s - t] \cdot I_{Lm}. \tag{15}$$

During one switching period, the electric charge through the capacitors is zero, thus the relationship between Q_1 and Q_2 is $Q_1 = Q_2 = I_o T_s$, from (14) and (15)

$$\begin{cases} t = \dfrac{4}{n+2}(1-D)T_s \\ I_{Lm} = \dfrac{n+2}{n(1-D)} I_o. \end{cases} \tag{16}$$

From the aforementioned equation, the voltage across the leakage inductor during $[t_2 - t_5]$ is obtained

$$V_{\mathrm{Lk}(2-5)} = L_k \frac{I_{Lm} - 0}{t} = \frac{(n+2)^2 L_k I_o f_s}{4n(1-D)^2}. \tag{17}$$

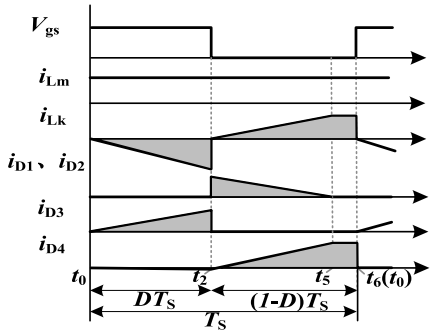

Fig. 4. Simplified waveforms.

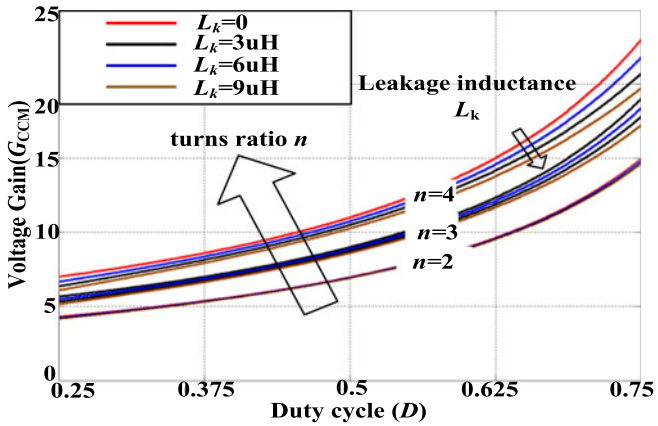

Fig. 5. Effort of leakage inductance on voltage gain.

According to (6) and (17), the output voltage in real situation can be expressed as

$$V_o = V_i + V_{C2} + V'_{C3} + nV_{C1} - V_{\mathrm{Lk}(2-5)}. \tag{18}$$

Define τ as $\tau = \frac{L_k f_s}{R_L}$. According to (6), (12), and (17), (18) can be simplified as

$$V_o = V_i \frac{1+n+D}{1-D} \cdot \frac{1}{1+2\tau/D^2+(n+2)^2\tau/[4n(1-D)^2]}. \tag{19}$$

Fig. 5 plots the graph that the voltage gain verse different leakage inductance and different turns ratio in the condition that the output power is 500 W, output voltage is 400 V, and the switching frequency is 50 kHz. As the figure shows, with the rise of the leakage inductance and the decrease of the turns ratio, the voltage conversion ratio is decreasing.

B. Condition of ZCS for D_1 and D_2

With the help of the leakage inductance, the turn-off current falling rate of D_3 and D_4 is limited by the leakage inductor; moreover, the diode current of D_1 and D_2 is reduced to zero before it turns OFF, which solves the reverse-recovery problem. According to the aforementioned analysis, the prerequisite of the ZCS for D_1 and D_2 is that the existence of Mode 6. According to (16), the requirement of the existing the mode 6 is that

$$t = \frac{4}{n+2}(1-D)T_s \le (1-D)T_s. \tag{20}$$

Simplifying (20), the following conclusion can be deducted: while the turns ratio of the coupled inductor n meets the condition that $n \ge 2$, D_1 and D_2 can realize the ZCS turn OFF.

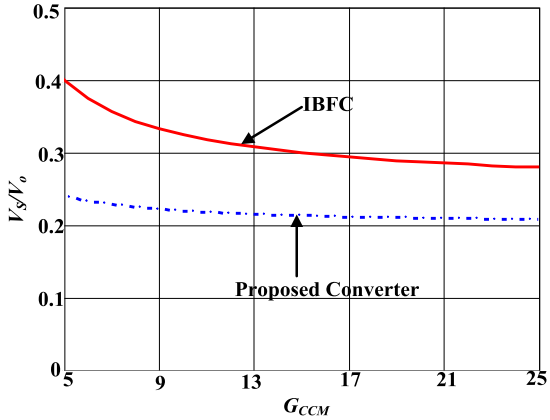

Fig. 6. Comparison of voltage stress.

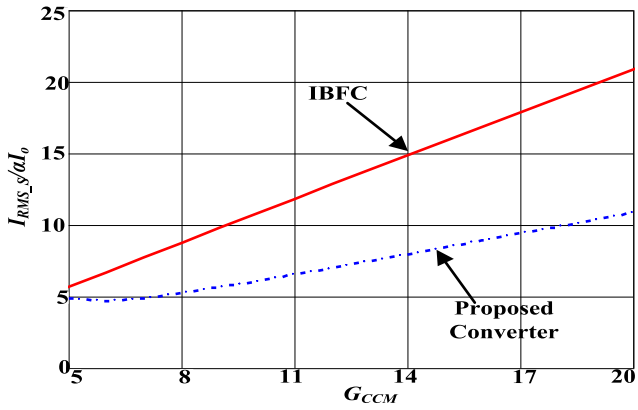

Fig. 7. Comparison of current stress.

C. Voltage/Current Stress of the Power Devices

According to the aforementioned analysis, the voltage stress across the power switches and the diodes can be obtained as

$$\begin{cases} V_{S1} = V_{S2} = \frac{1}{1-D}V_i = \frac{1}{1+n+D}V_o \\ V_{D1} = V_{D2} = \frac{1}{1-D}V_i = \frac{1}{1+n+D}V_o. \end{cases} \tag{21}$$

The comparison of switch voltage stress between the proposed converter and integrated boost-flyback converter (IBFC) [13] is shown in Fig. 6. To realize the same voltage ratio, the IBFC presents the high voltage stress across the switches; while the switch voltage stress is greatly decreased in the proposed converter. That means the switches with low R_{DS_on} can be utilized, which is beneficial to the efficiency and cost.

The average current through D_1 and D_2 is

$$I_{\mathrm{avg-D1}} = I_{\mathrm{avg-D2}} = I_o. \tag{22}$$

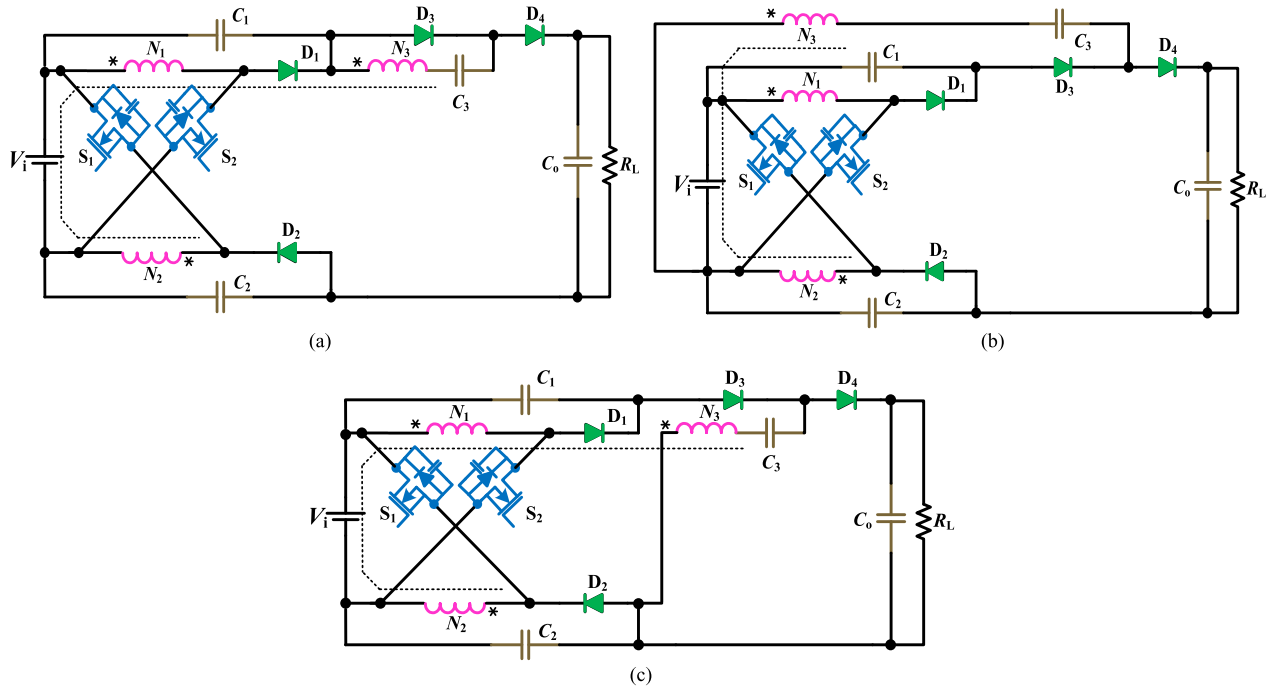

Fig. 8 Variations of the proposed converter.

TABLE I
UTILIZED COMPONENTS AND PARAMETERS OF THE CONVERTER

Components	Parameters
V_i (input voltage)	30–50 V
V_o (output voltage)	400 V
P_o (rated power)	500 W
f_s (switching frequency)	50 kHz
$N_1 : N_2 : N_3$ (turns ratio)	27:27:81
L_m (magnetizing inductor, N3 side)	1530 μH
L_k (N3 side)	25 μH
inductor core material	PPF306060
core part number	2
S_1, S_2 (power switches)	IRFP4568
D_1, D_2 (clamping diodes)	SF33
D_3, D_4	FR304
C_1, C_2 (clamping capacitor)	4.7 uF/63 V
C_3 (capacitor of charge pump)	1 μF/250 V (ORF Mode) 3 μF/250 V (BRF Mode)
C_o (filter capacitor)	470 μF/450 V (electrolytic) 1.5 μF/450 V (CBB)

According to the flux balance and the Fig. 4, the following equation can be deducted:

$$N_1 I_{s(\mathrm{a-b})} + N_2 I_{s(\mathrm{a-b})} - N_3 \frac{I_o}{D} = N_1 \frac{I_o}{1-D} + N_2 \frac{I_o}{1-D} + N_3 \frac{I_o}{1-D}. \quad (23)$$

Where $I_{s(0-2)}$ is the average current through N1 and N2, simplified (23), $I_{s(0-2)}$ can be obtained as

$$I_{s(0-2)} = \frac{0.5n + D}{D(1-D)} I_o. \quad (24)$$

According to (24), the RMS value of S_1 and S_2 is

$$\begin{aligned} I_{\mathrm{RMS}-S1} &= I_{\mathrm{RMS}-S2} \\ &= \sqrt{\frac{1}{T_s}\int_0^{DT_s} \left(I_{s(0-2)} - \frac{1}{2}\Delta i_L + \frac{\Delta i_L}{DT_s} t \right)^2 dt} \\ &= \frac{0.5n + D}{\sqrt{D}(1-D)} \cdot \frac{P_o}{V_o} \cdot \sqrt{\frac{1}{12}K_i^2 + 1} \end{aligned} \quad (25)$$

where K_i is the coefficient of the inductor current ripple, which is defined as $\Delta i_L = K_i I_{s(0-2)}$.

The comparison of the RMS current (where $\alpha = \sqrt{\frac{1}{12}K_i^2 + 1}$) between the proposed converter and IBFC is shown in Fig. 7. As can be seen, the RMS current through the switches is decreased greatly. Though two switches are utilized in the proposed converter, the conduction loss (proportioned to I_{RMS}^2) and switching loss (nearly proportioned to $V_S * I_{\mathrm{RMS}}$) will be decreased obviously.

The voltage stress and current stress of D_3 is

$$\begin{cases} V_{D3} = V_o - V_i - V_{C1} - V_{C2} = \dfrac{n}{1+n+D} V_o \\ I_{\mathrm{avg}-D3} = I_o. \end{cases} \quad (26)$$

The voltage stress and current stress of D_4 is

$$\begin{cases} V_{D4} = V_o - V_i - V_{C1} - V_{C2} = \dfrac{n}{1+n+D} V_o \\ I_{\mathrm{avg}-D4} = I_o. \end{cases} \quad (27)$$

D. Topology Deduction

Changing the connection point of the turns, some equivalence topologies can be obtained, which are shown in Fig. 8. The

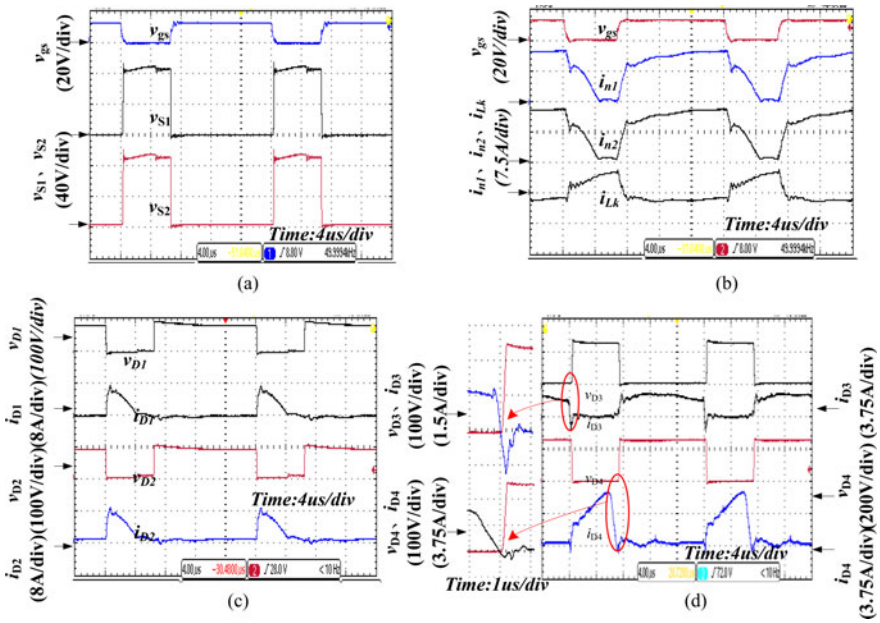

Fig. 9. Experimental waveforms when $V_i = 30$ V under BRF operation.

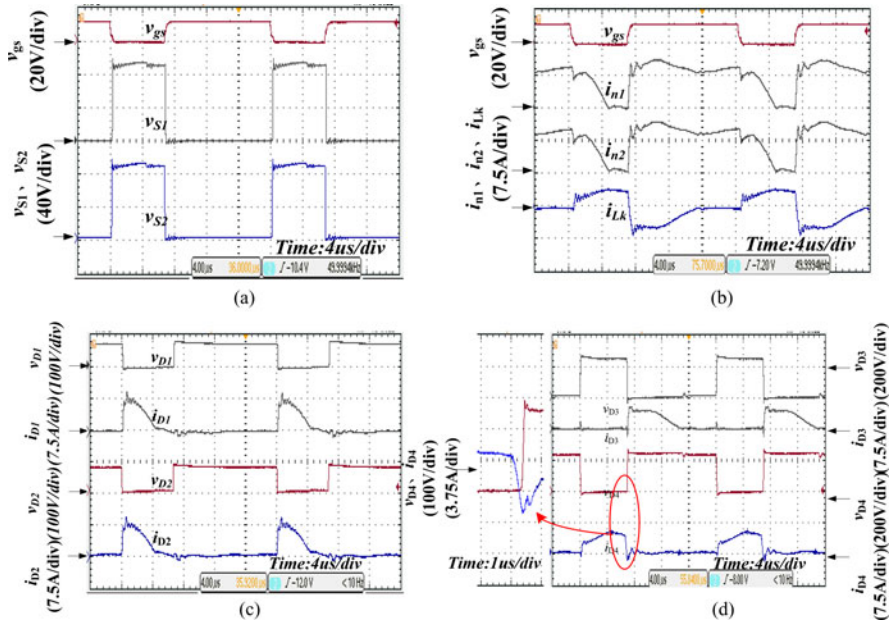

Fig. 10. Experimental waveforms when $V_i = 30$ V under ORF operation.

operation principles of these converters are similar to that of Fig. 1 shown, which shares the same voltage and current stress of the power devices and the same voltage conversion ratio. The difference between these converters is that the current flow path and the voltage across the capacitor C_3.

IV. Experimental Results

In order to verify the correctness of the analysis, some experiments have been conducted. The experimental conditions, utilized components and parameters of the converter are shown in Table I.

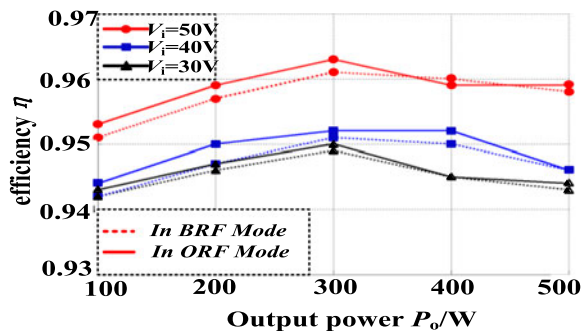

Fig. 11. Efficiency curves of the proposed converter.

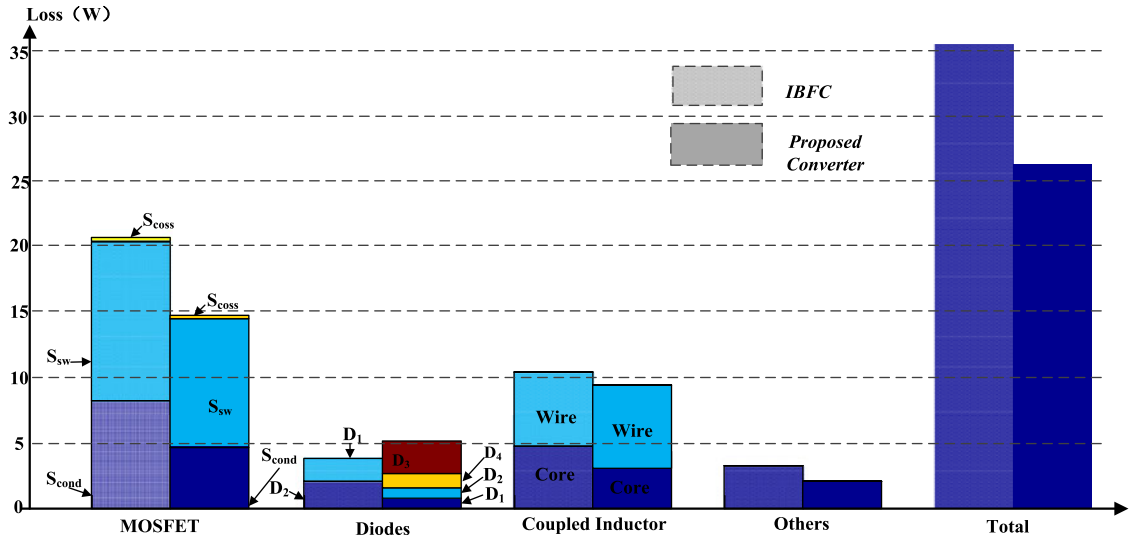

Fig. 12. Loss breakdown.

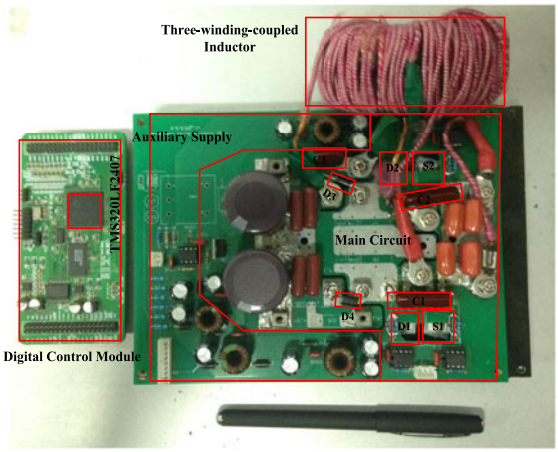

Fig. 13. Prototype board.

Fig. 9 shows the waveforms under the condition that the input voltage is 30 V, output voltage is 400 V, and output power is 500 W with BRF mode. The switching signal $V_{\rm gs}$, the switches voltage $V_{\rm ds1}$ and $V_{\rm ds2}$ are given in Fig. 9(a). The two active switches bear the same voltage stress about 86 V. The switching signal $V_{\rm gs1}$, the inductor current i_{n1}, i_{n2}, and i_{n3} are shown in Fig. 9(b), when the switches are ON, i_{n1} and i_{n2} increases; when the switches are OFF, i_{n1} and i_{n2} decreases. Fig. 9(c) shows the waveforms of the voltage and the current of D_1 and D_2; the diode current of D_1 and D_2 decreases to zero before they block voltage built, the ZCS of D_1 and D_2 helps to reduce the loss. Fig. 9(d) shows the waveforms of the voltage and the current of D_3 and D_4, the turn-off current falling rate of D_3 and D_4 is limited by the leakage inductor, which is good to improve the efficiency.

Fig. 10 shows the waveforms under the condition that the input voltage is 30 V, output voltage is 400 V, and output power is 500 W with ORF mode.

Fig. 11 illustrates the measured efficiency with different input voltage of the proposed converter in ORF mode and BRF mode, where the solid line presents the ORF mode and the dotted line presents the BRF mode. As can be seen, the efficiency is higher with the increase of input voltage, the efficiency of two modes is relatively close. When the converter operates with $V_{\rm in} = 30$ V, the maximum efficiency is nearly 95%, and the efficiency at 500-W full load is about 94.5% in both mode. When the input voltage increases to 50 V, the efficiency at full load is 95.9% in ORF mode and 95.8% in BRF mode, the maximum efficiency is 96.4% in ORF mode and 96.1% in BRF mode. It can be seen that a high efficiency can be achieved with different input voltage during a wide load range.

Fig. 12 illustrates the loss breakdown comparison of the proposed converter and the IBFC showed in [22]. The operation conditions are: $V_{\rm in} = 40$ V, $V_{\rm out} = 400$ V, $P_o = 500$ W, and $f_s = 50$ kHz. It can be seen that the main losses of the converter come from the switches. The loss of switches mainly contains: switching losses ($S_{\rm SW}$), conduction losses $S_{\rm cond}$, and capacitive losses $S_{\rm coss}$. As can be seen, the proposed converter's conduction losses can be outstandingly reduced due to the MOSFET of lower $R_{DS-{\rm on}}$ was applied. Also the switching losses are reduced since the voltage stress and current stress were much lower than those of the IBFC. Although the proposed converter has higher diodes loss, the loss of coupled inductor is less. Therefore, the efficiency is higher in the proposed converter than in the IBFC.

Fig. 13 shows the prototype.

V. Conclusion

Based on the dual switches structure, this paper proposed a novel dual switches dc/dc converter with three-winding-coupled inductor and charge pump. The characteristics of the converters are shown as following:

1) the proposed converter can achieve a high gain with a small duty cycle, which is helpful to reduce the peak

current through the power device and helps to improve the efficiency;
2) the dual switches structure feature reduce the voltage and current stress of the power switches;
3) the voltage stress of the diodes is relatively low and the reverse problem is very small.

Experimental results have been given to verify the analysis and merits of the converter.

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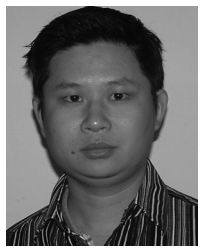

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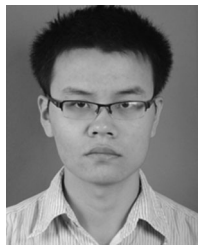

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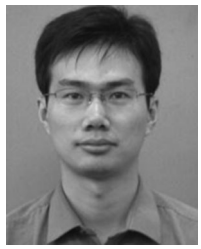

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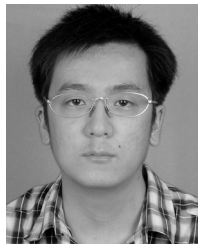

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