Deadtime Effect on GaN-Based Synchronous Boost Converter and Analytical Model for Optimal Deadtime Selection

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***Abstract*—It is widely acknowledged that gallium nitride (GaN)-based power switching devices are superior to conventional silicon (Si) devices in terms of lower semiconductor loss and faster switching speed. However, the deadtime related losses in GaN HEMT-based converters can be detrimental if not optimized, especially when operating at very high switching frequencies. This paper proposes an original analytical model for deadtime optimization for the GaN converters. The proposed model is more accurate than conventional deadtime optimization methods used in Si converters. A GaN-based synchronous boost converter is used as a case study. Circuit simulation and experimental tests are successfully performed to verify the analysis and proposed model.**

***Index Terms*—Deadtime optimization, gallium nitride (GaN) power devices, synchronous boost converter.**

I. Introduction

With the continuing trend toward higher power, higher efficiency, lighter weight, and smaller size power electronic converters in various applications, there has always been a need for better performance power switching devices. Conventional silicon (Si)-based power devices have seen tremendous improvements over the past 60 years, but their performances are limited by the physical properties of Si material [1]. In recent years, there has been a focus on wide-bandgap (WBG) semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN) [2]–[5]. Due to the superior physical properties of SiC and GaN, they are believed to be promising candidates to replace Si in the next generation of power electronics. As a new technology, some special characteristics of WBG-based power devices are still unknown to the public, rendering the usage of these devices less effective when applied in power converters. This research aims to propose an accurate model for the deadtime optimization of GaN devices. A GaN device-based phase-leg configuration synchronous boost converter is evaluated as a case study.

Compared to Si, GaN material has more favorable physical properties, such as higher electric breakdown field, lower intrinsic carrier concentration, and larger saturated electron drift velocity [6], as shown in Table I [4]. These material properties lead to the low semiconductor loss and high switching speed features of GaN-based power switching devices. As GaN device technology becomes more mature, an increasing number of GaN HEMTs of different ratings and types are presented and evaluated in the literature [7]–[9]. Many researchers have also reported high efficiency and high power density converters using GaN devices [10]–[14]. In [11], a GaN HEMT boost converter is shown to achieve 98% efficiency at 300-W output power at a switching frequency of 1 MHz. A 10-W synchronous buck converter using GaN-on-SiC HEMTs is demonstrated in [12], achieving 95% efficiency at 10-MHz switching frequency, and 90% efficiency at 40-MHz switching frequency. Yu *et al.* [13] present a 3-kW 400–800 V GaN-based boost converter showing 99% efficiency at 100-kHz switching frequency. In [14], a GaN device is used in a hybrid resonant converter with 97.5% California Energy Commission weighted efficiency.

TABLE I
Key Electronic Properties of Si, GaN [4]

Property	Si	GaN
Band gap E_g (eV)	1.12	3.43
Electron mobility μ_n (cm^2/Vs)	1400	2000
Hole mobility μ_p (cm^2/Vs)	450	30
Intrinsic carrier concentration n_i (cm^{-3}) at 300 K	1.5×10^{10}	1.9×10^{-10}
Electron saturation velocity v_{nsat} ($\times 10^7$cm/s)	1.0	2.5
Critical breakdown electric field E_{crit} (MV/cm)	0.25	3.5

To take full advantage of the benefits that GaN technology will bring to power electronics, simple direct replacement of Si devices in converters by GaN devices is far from enough. Hence, researchers are working on various aspects to optimize the performance of GaN devices in power converters. High-performance gate drive designs are studied to cope with different gate voltages and very high switching frequency requirements [15]–[17]. Parasitic inductances are also reduced in both device packages [18] and circuit layout [19] to minimize the adverse voltages induced during very fast switching transients. However, very few researchers have looked at the deadtime effect in GaN-based converters, which will severely compromise the device performance if not optimized.

Unlike conventional Si MOSFETs, GaN HEMTs have no p-n junction body diode, but the channel is capable of conducting negative current at no gate voltage when the drain-to-source is reversely biased. Device manufacturers sometimes refer to this reverse conduction ability of GaN HEMTs as a "majority carrier diode." For simplicity in the analysis, the term "body diode" will

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be used throughout this paper. This body diode of GaN HEMT features zero reverse recovery, which helps reduce the turn-on switching loss dramatically. However, the GaN body diode has very high forward voltage drop when conducting (twice that of Si MOSFET body diode), inducing considerable conduction loss during deadtime [20]. In addition, when a power converter is switching at very high frequencies, the deadtime related losses become even more prominent. As a result, GaN-based converters are more sensitive to deadtime related losses compared to Si converters, and more attention needs to be paid to this aspect. The deadtime optimization of GaN converters have been mentioned in [21] and [22]. But in these two papers, the optimal value is obtained by parametrically varying the deadtime and comparing the corresponding losses measured. These optimal deadtime values are only valid for the particular converters and operating conditions under test. Neither theoretical analysis nor specific optimization method is provided.

GaN converters require a careful investigation to understand the importance of deadtime because of its very fast turn-on and turn-off characteristics and high frequency switching capability. The nonoptimal deadtime in Si converters are less detrimental than that in the GaN converters and it can still lead to as high as 6% efficiency decrease for low output voltage and high switching frequency applications [23]. As a result, many deadtime optimization methods for Si converters have been proposed in the past decades, but they are not suitable to use for GaN devices.

The methods used for Si deadtime models can be classified into two categories: 1) based on measurements of switching quantities, such as switch node voltage and current [23]–[25]; 2) based on the measurements of low frequency quantities, such as terminal voltage and/or current (also known as sensorless methods) [26]–[28]. The methods in the first category try to sense the high frequency switch node voltage or current and use them as an indication of a switch turn-off instance, which triggers the turn-on of the complementary switch. However, in practice, the very fast and noisy switching quantities in GaN devices are always difficult to sense. In contrast, the sensorless methods only measure the converter terminal quantities, and continuously adjust the deadtime, while searching for the optimal points that achieve the highest converter efficiency or smallest duty cycle (for constant output voltage). The drawbacks of sensorless methods are their slow transient response due to the inherent searching behaviors and the relatively large dithering window due to finite searching steps.

For converters based on GaN HEMTs, deadtime optimization methods with higher accuracy and faster transient response compared to Si technology are needed. Thanks to the majority carrier nature and zero reverse recovery property of GaN HEMTs, a high accuracy model is possible and is proposed in this paper. Based on the shortcomings of the conventional methods mentioned above, a feed-forward type method, which directly generates optimal deadtime values without continuous searching or adjusting, is devised to fulfill this need. The proposed optimal deadtime calculation is based on the knowledge of device parameters and converter operating point and provides an accurate solution.

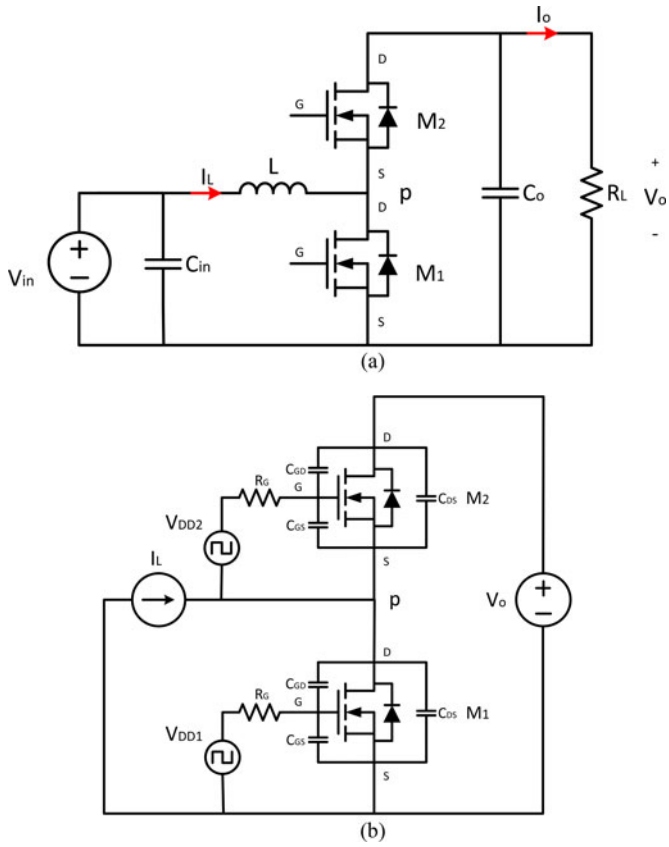

Fig. 1. Schematic of the synchronous boost converter under study. (a) Power circuit. (b) Equivalent circuit including gate drive path.

The aim of this research paper is to present an original analytical model for optimal deadtime calculation of GaN devices to contribute to close the knowledge gap for emerging GaN-based devices. Circuit simulation and experimental tests are carried out to verify the given model. This paper is organized in the following way: Section II will present the proposed modeling for deadtime optimization for GaN devices. Section III will present the verification of deadtime model using circuit simulation and results. Then, the experimental tests will be described in detail in Section IV. Finally, conclusions and discussions will be given in Section V.

II. Proposed Modeling for Deadtime Optimization

The converter under study is a synchronous boost converter, whose schematics are shown in Fig. 1. Again, for the simplicity of the analysis, an antiparalleled body diode is used to model the reverse conduction of the GaN HEMT at zero gate voltage. The timing sequence of gate drive output voltages (V_{DD1} and V_{DD2}) is illustrated in Fig. 2. In the figure, T and D represent the switching period and duty cycle of control FET M_1, respectively. As can be seen, there are two deadtimes t_{ddon} and t_{ddoff} during one switching cycle. t_{ddon} is inserted right before the turn-on of control FET M_1 and, thus, is called turn-on deadtime, and t_{ddoff} is called turn-off deadtime since it occurs after the M_1 turn-off. In addition, t_{ddon} is included into the on-state duty cycle DT of M_1, while t_{ddoff} is in the off-state

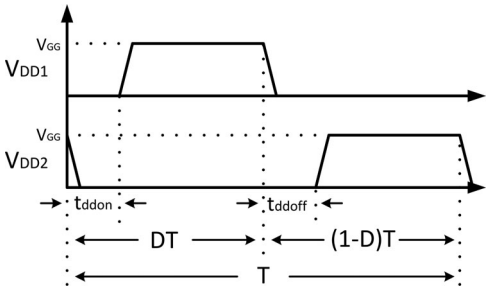

Fig. 2. Timing sequence of gate driver voltages.

cycle (1-*D*)*T*, which is consistent with the way deadtimes are generated in most digital and analog controllers. It should also be noted that the deadtime intervals defined here are based on the output voltages of gate drive rather than the digital gating signals.

A. Analysis of Deadtime Effect

In a synchronous boost converter, the deadtime intervals inserted into the complementary gating voltages are commonly used to prevent the simultaneous on-state of two switches, which will short circuit the output capacitor and cause high current spikes as well as excessive loss. This instantaneous short circuit is usually referred as a "shoot-through" or "short-through" phenomenon. However, improper gating time will not only lead to shoot-through loss, but also diode conduction loss and partial voltage turn-on loss depending on the deadtime used. All these losses can be named as deadtime related losses.

Fig. 3 illustrates the waveforms of the voltage at switch node *p* at different deadtimes. As can be seen from Fig. 3(a), in the case of too long of deadtimes, there will be periods when both switches are in the off-state, during which the inductor current has to go through the body diode of synchronous FET M_2. This diode conduction takes place during both turn-on deadtime $t_{\rm ddon}$ and turn-off deadtime $t_{\rm ddoff}$, and can be observed in switch node voltage V_p waveform. The fact that V_p is higher than output voltage $V_{\rm O}$ indicates the voltage drop across the diode. Since the GaN HEMT body diode has a high forward voltage drop, the body diode conduction losses during these times will be high.

In the case of too short deadtimes, the loss mechanisms during turn-on deadtime $t_{\rm ddon}$ and turn-off deadtime $t_{\rm ddoff}$ are quite different. When turn-on deadtime $t_{\rm ddon}$ is set to be too short, the control FET M_1 will be turned on before synchronous FET M_2 is off; thus, shoot-through takes place. An obvious decrease in the switch node voltage V_p can be observed during shoot-through events. The amplitude of V_p depends on the dynamic on-state resistance of M_1. The waveform in Fig. 3(b) shows the extreme case when M_1 is able to be fully turned on before M_2 turns off, and V_p decreases to half of $V_{\rm O}$. In most cases, M_1 will only be partially turned on during a shoot-through event.

In contrast to $t_{\rm ddon}$, the introduction of turn-off deadtime $t_{\rm ddoff}$ not only prevents the shoot-through, but also achieves the zero voltage turn-on of synchronous FET M_2. When smaller $t_{\rm ddoff}$ is used, M_2 will start to turn on before the drain-to-source voltage $V_{\rm DS1}$ of M_1 reaches $V_{\rm O}$. Hence, as M_2 is turned on, it will draw large current from the converter output $V_{\rm O}$ to expedite the charging process of device output capacitor $C_{\rm oss}$ and help finish the turn-off transition of M_1. This expedited charging can be observed in V_p waveform, as its rate of increase changes suddenly [see Fig. 3(b)]. This capacitive charging is essentially different from a shoot-through event although both events feature high current spikes and high loss. This phenomenon is referred

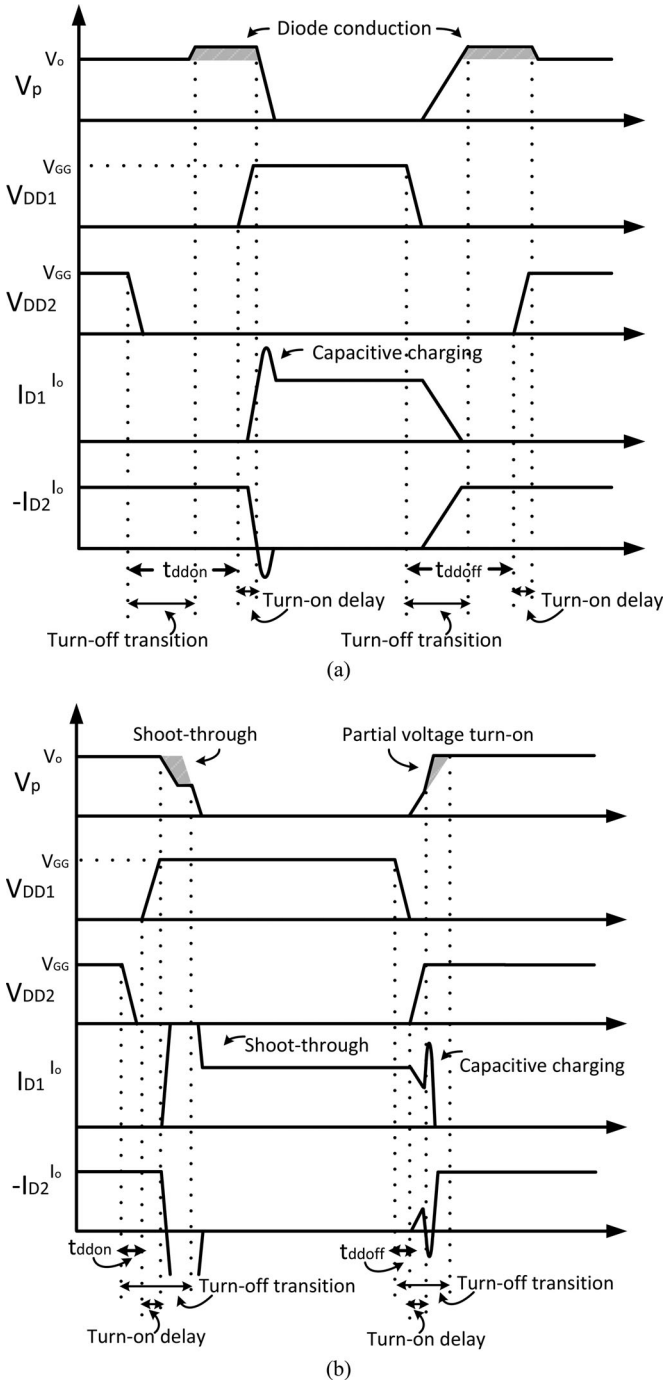

Fig. 3. Effect of deadtimes on GaN converter switching. (a) Too long deadtimes; (b) too short deadtimes. V_p, $V_{\rm DD1}$, and $V_{\rm DD2}$ stand for the switch node voltage, control FET M_1 gating voltage, and synchronous FET M_2 gating voltage, respectively. I_{D1} and I_{D2} stand for the drain current of M_1 and M_2, respectively.

to as partial voltage turn-on of the synchronous FET M_2, since M_2 starts to turn on before the voltage across it decreases to zero.

From the above analysis, the optimal turn-on deadtime should be able to avoid shoot-through, and minimize the diode conduction at the same time. Similarly, the optimal turn-off deadtime will achieve the zero voltage turn-on (ZVS) of the synchronous FET M_2 and maintain the minimal diode conduction meanwhile.

B. Optimization of Turn-On Deadtime for GaN Devices

The optimal deadtime calculation model proposed in this section is based on calculating the switching times of GaN HEMTs. To facilitate the analysis, one switching cycle of converter operation is broken down into 20 subintervals based on different switching transitions, as shown in Fig. 4. It is further assumed that proper PCB layout as suggested in [19] has been adopted to minimize the parasitic inductances in the circuit. This assumption will be validated by the experimental results in the later sections.

According to Fig. 4, one full switching cycle of length T starts from the synchronous FET conduction, when gate voltage of amplitude $V_{\rm GG}$ is applied to M_2. At time t_1, zero gate voltage is applied to M_2, the input capacitance $C_{\rm iss}(C_{\rm gs}+C_{\rm gd})$ of M_2 is being discharged through the gate resistance R_g. The gate-to-source voltage of M_2 is as follows:

$$v_{gs2} = V_{\rm GG} e^{-(t-t_1)/R_g C_{iss}}. \tag{1}$$

This stage ends at t_2 when $v_{\rm gs2}$ decreases to $V_{\rm th}+I_L/g_{\rm fs}$, where $V_{\rm th}$ is the gate threshold voltage, $g_{\rm fs}$ is the transconductance, and I_L represents the inductor current. During this interval, M_2 maintains the fully on-state, and this period is referred to as "turn-off delay period" of M_2. At t_2, $v_{\rm gs2}$ keeps decreasing according to (1). M_2 starts to turn-off, and the current is diverted from its conducting channel to its body diode. This stage ends at t_3, when $v_{\rm gs2}$ decreases to $V_{\rm th}$, and M_2 is fully off, with all current going through the diode. The length of time interval from t_1 to t_3 can be calculated by equating (1) with $V_{\rm th}$

$$(t_3-t_1)_- = R_g C_{iss}\ln(V_{\rm GG}/V_{\rm th}). \tag{2}$$

However, in order to achieve more accurate timing, the fall time of gate driver voltage t_f also needs to be taken into consideration. Considering the fact that high-performance gate drivers usually have very short fall times, t_f can be directly added to (2) to achieve a reasonable estimation. Thus,

$$t_3-t_1 = R_g C_{iss}\ln(V_{\rm GG}/V_{\rm th})+t_f. \tag{3}$$

During t_3-t_4, $v_{\rm gs2}$ discharges from $V_{\rm th}$ to 0. Similar to delay period, this period does not affect the power circuit behavior; hence, is named "after turn-off period" of M_2. The "diode conduction period 1" from t_4 to t_5 only exists in the case of too long turn-on deadtime.

At t_5, $V_{\rm GG}$ is applied to gate of M_1, to charge C_{iss} through R_g. The gate-to-source voltage of M_1 becomes

$$v_{gs1} = V_{\rm GG}(1-e^{-(t-t_5)/C_{iss}R_g}). \tag{4}$$

Before $v_{\rm gs1}$ reaches $V_{\rm th}$ at t_6, M_1 does not conduct any current. Hence, t_5-t_6 is the "turn-on delay period" of M_1. The length of this period can be obtained as

$$(t_6-t_5)_- = C_{iss}R_g\ln(V_{\rm GG}/(V_{\rm GG}-V_{\rm th})). \tag{5}$$

Compared to $(t_6-t_5)_-$, the rise time of the gate driver voltage t_r is much longer; hence, the actual turn-on delay time can be approximated as

$$t_6-t_5 = 2(t_6-t_5)_- + t_r V_{\rm th}/V_{\rm GG}. \tag{6}$$

During t_6-t_9, M_1 is turned on through three steps. From t_6 to t_7, $v_{\rm gs1}$ is increased from $V_{\rm th}$ to $V_{\rm th}+I_L/g_{\rm fs}$ according to (4). At t_7, all I_L is diverted from M_2 diode to M_1 channel. From t_7 to t_8, $v_{\rm gs1}$ continues to increase, as does the current in M_1 channel $i_{\rm ch1}$. The current component $i_{\rm ch1}-I_L$ is discharging and charging the drain-to-source capacitor $C_{\rm ds}$ of M_1 and M_2, respectively. At t_8, equilibrium is reached

$$(V_{\rm GG}-V_{gs1p})/R_g(1+(C_{ds1}+C_{ds2})/C_{gd}) = V_{gs1p}g_{fs} \tag{7}$$

and $v_{\rm gs1}$ reaches the miller plateau $V_{\rm gs1p}$ constrained by (7). From t_8 to t_9, $v_{\rm gs1}$ is kept at $V_{\rm gs1p}$, and $v_{\rm ds1}$ is discharged to the on-state value. The period of t_9-t_{10} is after turn-on period of M_1, when $v_{\rm gs1}$ is increased from $V_{\rm gs1p}$ to $V_{\rm GG}$. Then, the first half of the switching cycle is finished.

The optimal turn-on deadtime is needed such that the instance t_3, when M_2 channel ceases conducting, is directly followed by the instance t_6, when M_1 channel begins to conduct. Hence, the optimal turn-on deadtime exactly compensates for the length mismatch between sync FET turn off transition period (t_1-t_3) and control FET turn-on delay period (t_5-t_6), and can be calculated as

$$t_{\rm ddon\_opt} = t_3-t_1-(t_6-t_5). \tag{8}$$

Substituting (3), (5), and (6) into the above equation gives

$$t_{\rm ddon\_opt} = R_g C_{iss}\ln(V_{\rm GG}/V_{\rm th})+t_f-2(C_{iss}R_g \ln(V_{\rm GG}/(V_{\rm GG}-V_{\rm th})))-t_r V_{\rm th}/V_{\rm GG}. \tag{9}$$

C. Optimization of Turn-Off Deadtime for GaN Devices

The second half switching cycle $(t_{10}-T)$ is a dual process of the first half, however, with a few important differences. Hence, only M_1 turn-off periods $t_{12}-t_{15}$ will be analyzed here.

At t_{12}, the end of turn-off delay period, $v_{\rm gs1}$ has been discharged to $V_{\rm th}+I_{\rm Lmax}/g_{\rm fs}$. $I_{\rm Lmax}$ is the maximum inductor current during given switching cycle, and is used to take the inductor current ripple into account. During $t_{12}-t_{13}$, $v_{\rm gs1}$ will continue to decrease according to

$$v_{gs1} = V_{\rm GG}e^{-(t-t_{11})/R_g C_{iss}}. \tag{10}$$

The channel current of M_1 will be

$$i_{\rm ch1} = (V_{gs1}-V_{\rm th})g_{fs}. \tag{11}$$

The charging current of the output capacitors will be

$$(C_{oss1}+C_{oss2})dV_{ds1}/dt = I_{L\max}-i_{\rm ch1}. \tag{12}$$

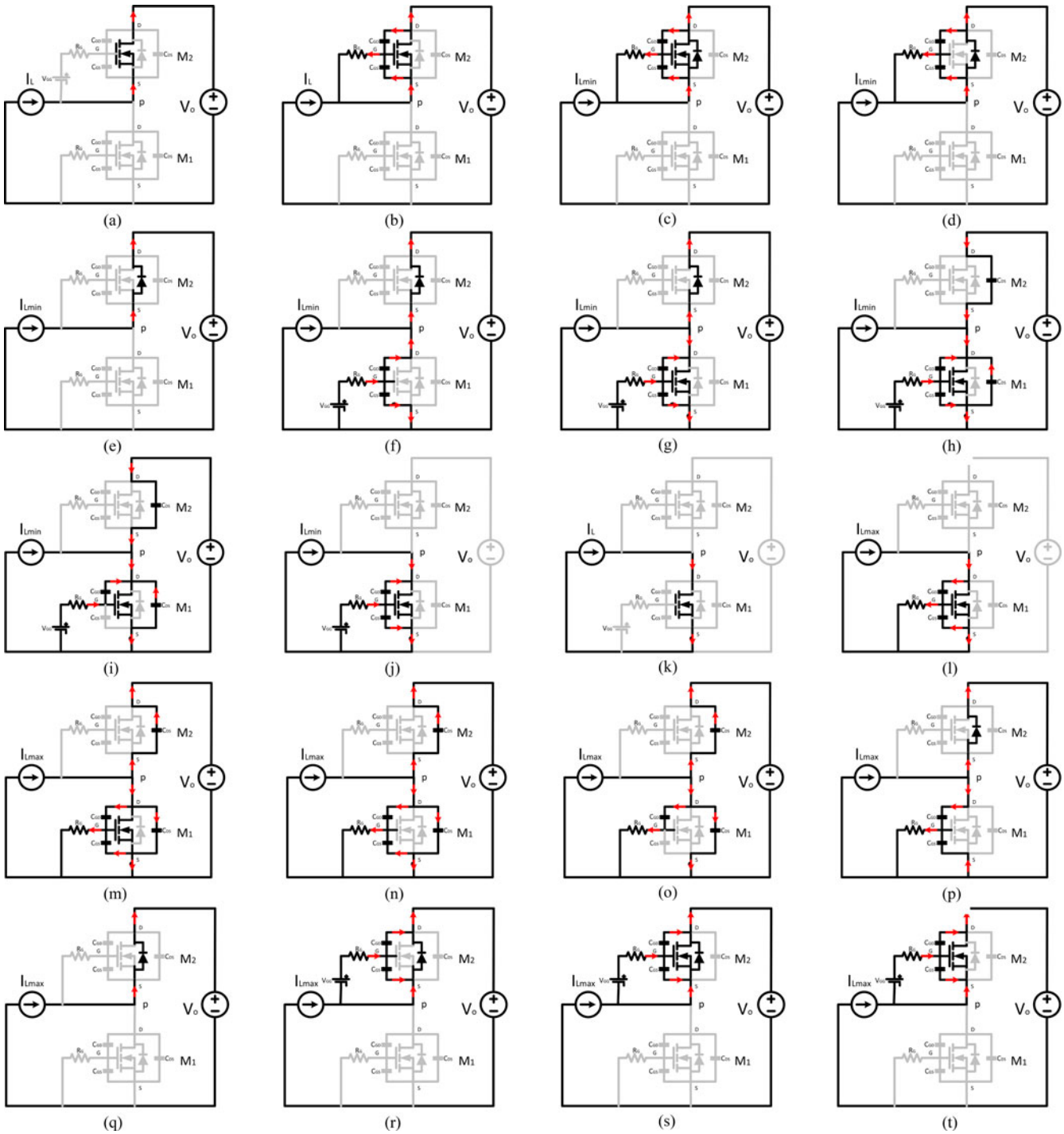

Fig. 4. Different phases of switching transition in one switching cycle in a synchronous boost converter using GaN devices. (a) $0 - t_1$: synchronous FET conduction period; (b) $t_1 - t_2$: synchronous FET turn-off delay period; (c) $t_2 - t_3$: synchronous FET turn-off period; (d) $t_3 - t_4$: after synchronous FET turn-off period; (e) $t_4 - t_5$: diode conduction period 1; (f) $t_5 - t_6$: control FET turn-on delay period; (g) $t_6 - t_7$: control FET turn-on period 1; (h) $t_7 - t_8$: control FET turn-on period 2 (i) $t_8 - t_9$: control FET turn-on period 3 (j) $t_9 - t_{10}$: after control FET turn-on period; (k) $t_{10} - t_{11}$: control FET conduction period; (l) $t_{11} - t_{12}$: control FET turn-off delay period; (m) $t_{12} - t_{13}$: control FET turn-off period 1; (n) $t_{13} - t_{14}$: control FET turn-off period 2; (o) $t_{14} - t_{15}$: control FET turn-off period 3; (p) $t_{15} - t_{16}$: after control FET turn-off period; (q) $t_{16} - t_{17}$: diode conduction period 2; (r) $t_{17} - t_{18}$: synchronous FET turn-on delay period; (s) $t_{18} - t_{19}$: synchronous FET turn-on period; (t) $t_{19} - T$: after synchronous FET turn-on period.

At t_{13}, $v_{\rm gs1}$ decreases to $V_{\rm th}$, $i_{\rm ch1}$ becomes 0. Hence, M_2 is in fully off-state after t_{13}, but the device output capacitors will keep being charged by inductor current $I_{\rm Lmax}$. During $t_{13}-t_{14}$, $v_{\rm gs1}$ continues to decrease according to (9). At t_{14}, the turn-off plateau voltage $v_{\rm gs1p}{}'$ has been reached, which is constrained by

$$V_{gs1p}{}'/R_g(1+(C_{ds1}+C_{ds2})/C_{gd})=I_{L\max}. \tag{13}$$

During $t_{14}-t_{15}$, $v_{\rm gs1}$ is kept at $V_{\rm gs1p}{}'$, and $C_{\rm ds1}$ continues to be charged by $I_{\rm Lmax}$ until $V_{\rm ds1}$ reaches converter output voltage $V_{\rm O}$ at t_{15}.

The switching times can be obtained in the following manner. Similar to (3), turn-off delay time of M_1 is

$$t_{12}-t_{11}=R_gC_{iss}\ln(V_{\rm GG}/(V_{\rm th}+I_{L\max}/g_{fs}))+t_f \tag{14}$$

and

$$t_{13}-t_{11}=R_gC_{iss}\ln(V_{\rm GG}/V_{\rm th})+t_f. \tag{15}$$

The turn-off time of M_1 can be obtained by taking time integral of (12) from t_{12} to t_{15}. This integral operation deliberately avoids dealing with the nonlinearity of $C_{\rm oss}$

$$2Q_{oss}|_0^{V_O}=I_{L\max}(t_{15}-t_{12})-\int_{t_{12}}^{t_{13}}i_{\rm ch1}dt. \tag{16}$$

In (16), $Q_{\rm oss}|_0^{Vo}$ represents the capacitive charge needed to increase the voltage of output capacitor from 0 to $V_{\rm O}$, and can be readily found in the device datasheet.

Solving (14)–(16), the value of $t_{15}-t_{11}$ will be known. Also, the length of turn-on delay period will be the same as in the first half cycle

$$t_{18}-t_{17}=t_6-t_5. \tag{17}$$

Finally, the optimal turn-off deadtime needs to eliminate the periods of $t_{15}-t_{18}$, and to ensure that M_2 channel starts to conduct right after $V_{\rm ds1}$ reaches $V_{\rm O}$. Hence, the optimized turn-off deadtime exactly compensates for the length mismatch between control FET turn off transition period ($t_{11}-t_{15}$) and sync FET turn-on delay period ($t_{17}-t_{18}$), which is

$$t_{\rm ddoff\_opt}=t_{15}-t_{11}-(t_{18}-t_{17}) \tag{18}$$

Further substitution and arrangements yield the result into (19) as shown at the bottom of the page.

D. Case Study of a 160-W GaN Converter

The optimal deadtime calculation model proposed above has been applied to a 160-W GaN-based synchronous boost converter whose specifications are listed in Table II. The GaN HEMT used in the converter is EPC 2001 and its parameters are listed in Table III. Some critical parameters of the gate drive circuit that will be needed for the calculation are also provided in Table III. In this table, the total gate resistance R_g includes a 1-Ω external gate resistance and a 0.6-Ω internal gate resistance of the device. The values of the gate driver voltage rise time t_r and fall time t_f come from the datasheet of the gate driver chip LM5113. It should also be noted that the gate threshold voltage $V_{\rm th}$ and transconductance $g_{\rm fs}$ should be temperature dependent generally; however, this dependence is very weak for the operating range of interest (0–8 A) and, thus, is negligible here.

TABLE II
SPECIFICATIONS OF THE GAN CONVERTER

Specifications	Value
Input voltage $V_{\rm in}$ (V)	24
Output voltage V_o (V)	48–80
Power rating P (W)	0–160
Switching frequency f (kHz)	400
Choke inductor L (μH)	20
Input capacitor $C_{\rm in}$ (μF)	10
Output capacitor Co (μF)	60

TABLE III
CRITICAL PARAMETERS OF GAN DEVICE (EPC2001) AND GATE DRIVER

Specifications	Value
Drain-to-source voltage $V_{\rm DS}$ (V)	100
Drain current at 25 °C I_D (A)	25
Input capacitance $C_{\rm iss}$ (pF)	900
Gate threshold voltage $V_{\rm th}$ (V)	1.4
Transconductance $g_{\rm fs}$ (S)	12.5
On-state gate voltage $V_{\rm GG}$ (V)	5
Total gate resistance R_g (Ω)	1.6
Gate driver voltage rise time t_r (ns)	7
Gate driver voltage fall time t_f (ns)	1.5

According to the parameters listed and (9), the optimal turn-on deadtime $t_{\rm ddon\_opt}$ is found to be 4.27×10^{-10} s. Hence, only 0.427 ns is needed for the turn-on deadtime, and this optimal value of turn-on deadtime is independent of the converter operation conditions, such as output voltage and loads.

On the contrary, from (19), it can be seen that the optimal turn-off deadtime $t_{\rm ddoff\_opt}$ is a function of converter output voltage $V_{\rm O}$ and peak inductor current $I_{\rm Lmax}$, which is also dependent on the load current $I_{\rm load}$. Hence, the optimal turn-off deadtime $t_{\rm ddoff\_opt}$ is evaluated for a wide range of output voltages (48–80 V) and load currents (0.4–2 A). The results are shown in Fig. 5.

As seen in the figure, the required turn-on deadtime $t_{\rm ddoff\_opt}$ decreases significantly as load current increases. For example, at the output voltage of 80 V, the optimal turn-off deadtimes for load currents of 0.5, 1, and 2 A are 36.82, 22.94, and 13.15 ns, respectively. This is because as the load current increases, the

$$t_{\rm ddoff\_opt}=R_gC_{iss}(1+\ln(V_{\rm GG}/(V_{\rm th}+I_{L\max}/g_{fs})))+(2Q_{oss}|_0^{V_O}-R_gC_{iss}V_{\rm th}g_{fs}\ln((V_{\rm th}+I_{L\max}/g_{fs})/V_{\rm th}))/I_{L\max}+t_f-(2(C_{iss}R_g\ln(V_{\rm GG}/(V_{\rm GG}-V_{\rm th})))+t_rV_{\rm th}/V_{\rm GG}). \tag{19}$$

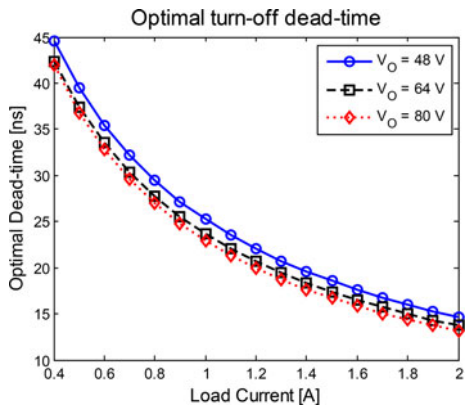

Fig. 5. Optimal turn-off deadtime $t_{\mathrm{ddoff\_opt}}$ as a function of GaN converter output voltage V_{O} and load current I_{Load}.

inductor current also increases, which will charge the output capacitor of devices at a faster rate; thus, shortening the turn-off process of control FET M_1 ($t_{12} - t_{15}$).

As converter output voltage V_{O} increases, $t_{\mathrm{ddoff\_opt}}$ also decreases. However, the dependence of $t_{\mathrm{ddoff\_opt}}$ on V_{O} is very weak. In the case of 2-A load current, $t_{\mathrm{ddoff\_opt}}$ decreases from 14.67 to 13.15 ns when V_{O} increases from 48 to 80 V. This can be explained as follows. As V_{O} increases, inductor current I_{Lmax} increases, which helps to reduce the deadtime needed; however, the output capacitors of devices also need to be charged to a higher voltage, thus counteracting the effect of increased charging current. As a result, weak dependence of $t_{\mathrm{ddoff\_opt}}$ on V_{O} is observed.

III. Verification of Deadtime Model Using Circuit Simulation

A. Simulation Methods

As a first step to verify the modeling results presented in the previous section, circuit simulation is carried out in LTSpice to search for the optimal deadtime values of the GaN synchronous boost converter by parametric study.

The specification of the converter simulated is provided in Table II. The same GaN device as analyzed above (EPC2001) is used as the power switches, whose SPICE model is provided by the manufacturer. Gate driver circuitry is realized by two programmable independent voltage sources, and the voltage rise time of 7 ns and fall time of 1.5 ns are also incorporated. A 1-Ω external gate resistance is used. In addition, equivalent series resistances have been added to each passive component to represent their loss. Note that negative values of t_{ddon} are included to show shoot-through losses and to justify that $t_{\mathrm{ddon-opt}}$ is around 0 ns. Since different deadtimes also have an effect on the output voltage, the duty cycle is adjusted to keep the output voltage at 80 V for each case.

To quantify the impact of deadtimes, the converter efficiencies and losses are recorded for each test case. With the built in analytical function in LTSpice software, the average power supplied by the dc power source P_{in} and the power consumed by load resistor P_{out} can be easily obtained. Converter efficiency η is then calculated by taking ratio of the two

$$\eta = P_{\mathrm{out}}/P_{\mathrm{in}}. \tag{20}$$

Hence, the efficiency value does not take account of the loss in gate drive circuit.

In order to illustrate the loss distribution in the converter for each simulation case, losses on the control FET M_1 and sync FET M_2 are accounted for separately. In addition, the total converter loss is also broken down into different parts: HEMT conduction loss, switching loss, diode conduction loss, shoot-through loss, and passive component loss (such as loss on inductor and capacitors).

The optimal deadtime can be identified as the value that yields the highest converter efficiency (or lowest total loss) for each test case.

TABLE IV
Summarization of Simulation Cases for Deadtime Analysis

Case No.	Load	Deadtimes
1	0.5 A	t_{ddon} is varied from –10 to 20 ns in 5 ns increments, while t_{ddoff} is set to be 35 ns
2		t_{ddoff} is varied from 0 to 50 ns in 5 ns increments, while t_{ddon} is set to be 0 ns
3	1 A	t_{ddon} is varied from –10 to 20 ns in 5 ns increments, while t_{ddoff} is set to be 20 ns
4		t_{ddoff} is varied from 0 to 50 ns in 5 ns increments, while t_{ddon} is set to be 0 ns
5	2 A	t_{ddon} is varied from –10 to 20 ns in 5 ns increments, while t_{ddoff} is set to be 10 ns
6		t_{ddoff} is varied from 0 to 30 ns in 5 ns increments, while t_{ddon} is set to be 0 ns

B. Simulation Results for GaN Deadtime Optimization

The total converter efficiencies at three load conditions (corresponding to simulation cases listed in Table IV) are plotted in Fig. 6 with respect to different deadtimes. In the figures, the markers represent the data points obtained from simulation, and the lines are fitted curves using piecewise cubic hermite interpolating polynomials.

As can be seen from Fig. 6(a), the optimal turn-on deadtime $t_{\mathrm{ddon\_opt}}$ is around 0 ns, regardless of the loading condition of the converter. This is consistent with the prediction made by proposed model in Section II-D. In addition, negative turn-on deadtime t_{ddon} will cause significant efficiency decrease due to the phase leg shoot through phenomena. With -5 and -10 ns t_{ddon}, the converter efficiencies are below 90% and 80%, which are too low to be shown in the figure. Too long t_{ddon} also penalizes the converter performance by diode conduction. For example, 20 ns t_{ddon} will lead to a 0.1–0.2% reduction in converter efficiency.

From Fig. 6(b), the optimal turn-off deadtime $t_{\mathrm{ddoff-opt}}$ is dependent on load current. For 2-, 1-, and 0.5-A load currents, $t_{\mathrm{ddoff-opt}}$ is in the vicinity of 10, 20, and 35 ns, respectively, which again shows good correlation with the modeling results presented earlier. In the 2-A case, shortening t_{ddoff} by 10 ns from the optimal value will cause 0.53% reduction in efficiency,

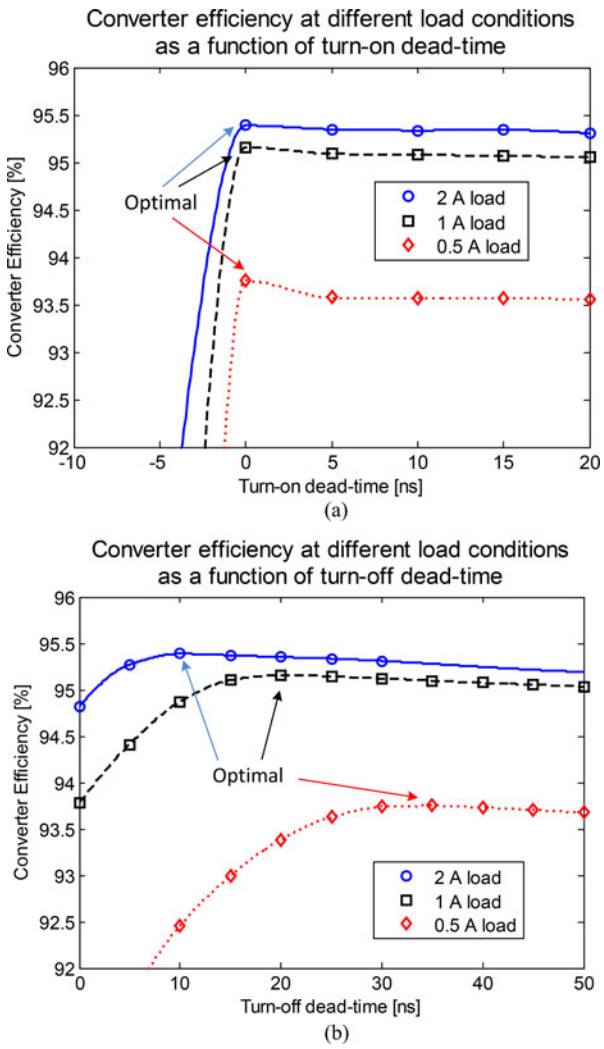

Fig. 6. Simulated GaN converter efficiency at three load conditions as a function of deadtimes. (a) Turn-on deadtime is varied while turn-off deadtime fixed. Blue circle solid line: simulation case 1; black square dashed line: simulation case 3; red diamond dotted line: simulation case 5. (b) Turn-off deadtime is varied while turn-on deadtime fixed. Blue circle solid line: simulation case 2; black square dashed line: simulation case 4; red diamond dotted line: simulation case 6.

due to partial voltage turn-on of M_2, and increasing it by 20 ns will decrease converter efficiency by roughly 0.1%.

To show the effect of the deadtimes on the converter loss distribution, the total loss for each simulation case is broken down into eight parts: switching loss on M_1, switching loss on M_2, conduction on M_1, conduction loss on M_2, diode conduction loss, passive component loss, shoot-through loss on M_1, and shoot-through loss on M_2. The corresponding results for 1-A load condition are plotted in Fig. 7. Similar phenomena exist for the other two load conditions and, hence, are not shown.

In Fig. 7(a), the strong dependence of diode conduction loss and shoot-through losses on turn-on deadtime can be observed. As t_{ddon} increases from 0 to 20 ns, the diode conduction loss increases from 0 to around 6.5×10^{-2} W, which is even higher than the conduction loss on synchronous FET M_2. Shoot-through loss only exists for negative t_{ddon} values, and is mainly generated by the control FET M_1. Except for the losses mentioned above, the other loss components vary little as t_{ddon} increases. Another important observation from Fig. 7(a) is that switching loss on M_1 is around 3 W and is always the most dominant loss component when shoot-through is not present, while the switching loss on M_2 is only 1.36×10^{-2} W due to the zero voltage switching transitions of M_2.

In Fig. 7(b), the variation of both the switching loss on M_2 and the diode conduction loss is observed. As t_{ddoff} is decreased from 20 to 0 ns, the switching loss on M_2 increases from 1.36×10^{-2} to 1.98 W due to the partial voltage turn-on transition of M_2. In addition, as t_{ddoff} is increased from 20 to 50 ns, the diode conduction loss increases from 0 to 0.18 W and becomes the third most dominant loss component among all. Shoot-through is not observed for the chosen t_{ddoff} range, and the rest loss components are almost constant.

IV. Experimental Verification of the Proposed GaN Device Deadtime Optimization Model

A. Experimental GaN Device Circuit

To validate the given simulation and modeling results, a 160-W GaN-based synchronous boost converter has been built and tested. The exact same specifications (see Table II) and switching device (see Table III) described previously are used for the converter hardware. To expedite the prototyping process, an EPC9002 demo board has been utilized. The demo board comes with two EPC2001 in a phase-leg configuration, a gate driver LM5113 to drive the two HEMTs, and a deadtime generating circuit as shown in Fig. 8. Two film capacitors are used as the input and output capacitors of the converter. The choke inductor is directly purchased from Coilcraft. Fig. 9 shows the converter prototype with critical parts labeled.

The deadtime generation scheme shown in Fig. 8 can be explained as follows. A PWM signal is first fed to an AND gate and a NAND gate to generate two complementary signals. Then, each signal is sent to an RDC circuit. At the signal rising edge, the capacitor *C* will be charged through *R*, which introduces a delay for the capacitor voltage to increase to the gate driver threshold. Hence, a delay will also be added to the gate driver output voltage rising edge, generating a deadtime. However, for the falling edge, the capacitor discharges through the diode almost simultaneously, and no delay will be added. The resulted gate driver voltages will follow the timing sequence shown in Fig. 2. The turn-on and turn-off deadtimes can be adjusted separately by adjusting the resistances R_1 and R_2.

As mentioned earlier in Section II, deadtime intervals defined in this paper are based on the output voltages of gate driver rather than the digital gating signals. Hence, the deadtimes measurements in this section are also carried out on the gate driver outputs. As a result, the propagation mismatch between the two driving channels of the gate driver is already accounted for in the measurements. If one tries to generate deadtimes using digital controllers, such as a DSP, and only has access to the timing information at the digital gating outputs, then the propagation mismatch of the gate driver and any conditioning circuits between the gate diver and digital controller needs to be measured

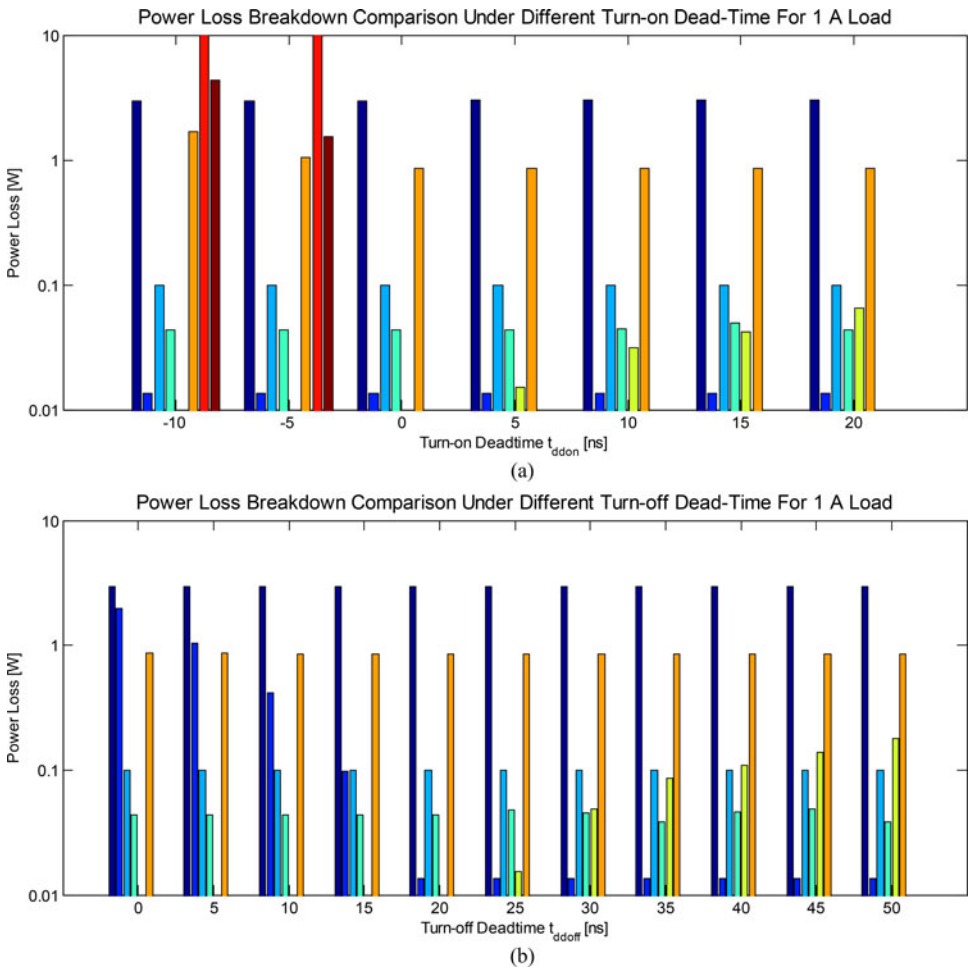

Fig. 7. GaN converter loss breakdown for 1-A load. Loss components are (from left to right): switching loss on M_1 (dark blue), switching loss on M_2 (blue), conduction on M_1 (light blue), conduction loss on M_2 (green), diode conduction loss (yellow), passive component loss (orange), shoot-through loss on M_1 (red), and shoot-through loss on M_2 (brown). (a) t_{ddon} is varied from -10 to 20 ns in 5 ns increments, while t_{ddoff} is set to be 20 ns. (b) t_{ddoff} is varied from 0 to 50 ns in 5 ns increments, while t_{ddon} is set to be 0 ns.

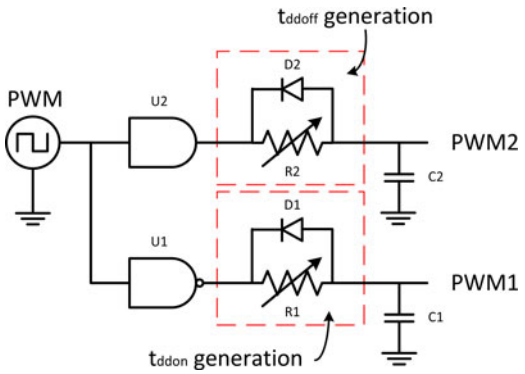

Fig. 8. Deadtime generating circuit.

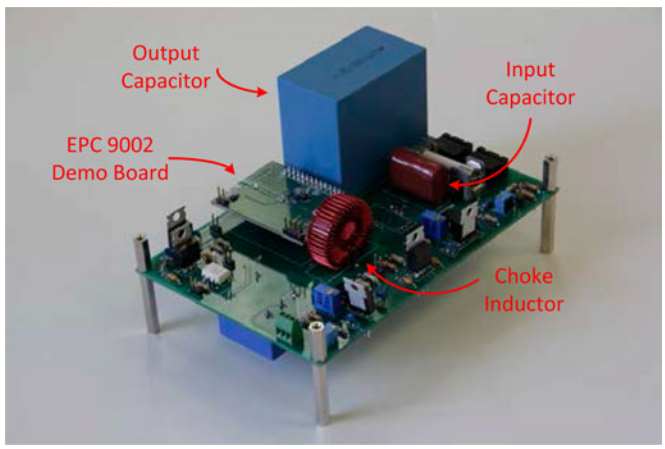

Fig. 9. Prototype GaN device-based synchronous boost converter built and tested for experimental results.

and added to obtain the actual deadtime values at the gate driver outputs.

The converter operating conditions under test are similar to those used in the simulation. A 24-V input voltage is fed from a dc power supply, and 400-kHz PWM signal is sent from a TI MCU. Duty cycles are adjusted during the tests to keep the converter output voltage at 80 V. A 160-, 80-, and 40-Ω load resistors are used to create three loading conditions (0.5, 1, and 2 A). For each load condition, t_{ddon} is varied from 0 to 31 ns

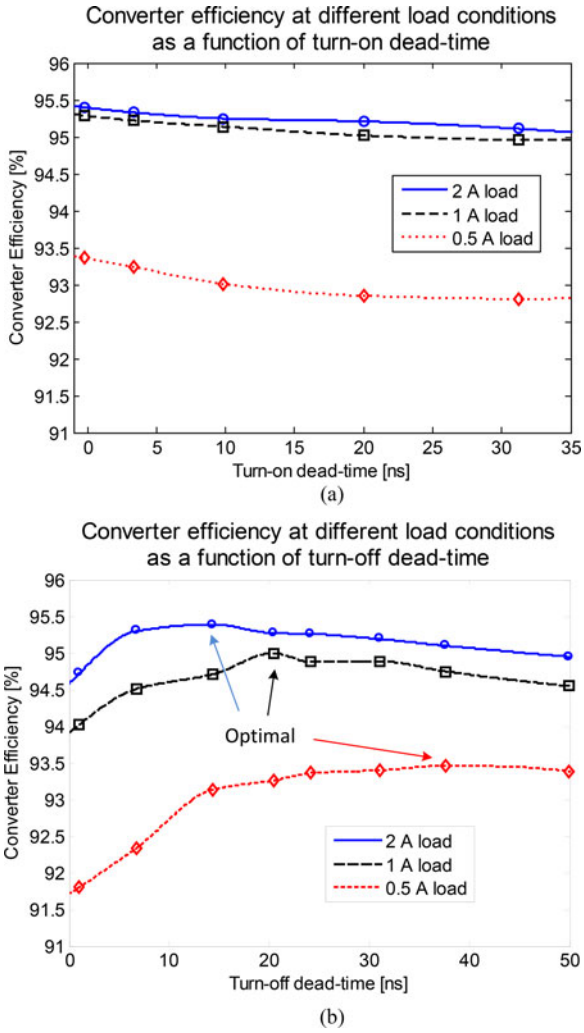

Fig. 10. Tested GaN converter efficiency at three load conditions as a function of deadtimes. (a) Turn-on deadtime is varied, while turn-off deadtime fixed at 20 ns. (b) Turn-off deadtime is varied, while turn-on deadtime fixed at 0 ns.

when t_{ddoff} is kept as 20 ns, and t_{ddoff} is varied from 1 to 50 ns when t_{ddon} is kept as 0 ns. Different from the simulation, negative t_{ddon} is not used for experiments since it would destroy the switching device.

During the experiments, five quantities, i.e., input and output voltages and currents as well as the switch node voltage, are measured and recorded for each case. The corresponding converter efficiency values are also obtained based on the measurements. In order to achieve accurate measurements, high-end scope and probes are used. The scope used is WaveSurfer 104 MXs-B from LeCroy with 1-GHz bandwidth and 5-GS/s sample rate. A 20-MHz differential voltage probes (ADP300) and 100 MHz (CP031) current probes are used to measure the voltages and currents.

B. Test Results for GaN Deadtime Optimization

The measured converter efficiencies at various loads and deadtimes are shown in Fig. 10. Again, the markers represent actual test data, and the lines are fitted curves. From Fig. 10(a), it is seen that the efficiency curve shows a decreasing trend

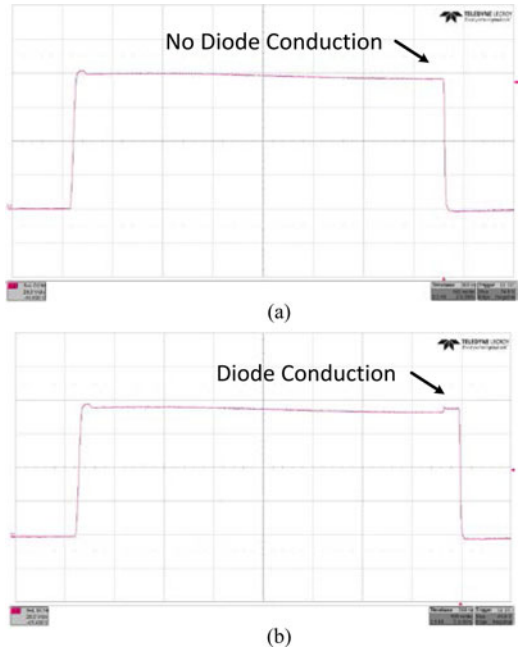

Fig. 11. Measured switch node voltage waveforms for GaN device 2-A load condition and 20 ns t_{ddoff}, (a) t_{ddon} is 0 ns, (b) t_{ddon} is 31 ns.

for increasing positive t_{ddon} values and corresponds well with the simulation results. A 30 ns t_{ddon} leads to 0.3–0.6% efficiency decrease compared to 0 ns t_{ddon} cases for all load conditions. However, since negative t_{ddon} are not tested, it is not clear whether 0 ns is the optimal value by merely referring to the monotonic efficiency curve. This issue will be addressed later.

Fig. 10(b) clearly shows that converter efficiency peaks around 14-, 20-, and 38-ns t_{ddoff} for 2-, 1-, and 0.5-A load conditions, respectively. In the 2-A case, using 1 ns t_{ddoff} will decrease the efficiency by about 0.7%, and using 50-ns t_{ddoff} will decrease the efficiency by 0.44% roughly.

To further validate the optimal $t_{\mathrm{ddon-opt}}$ and $t_{\mathrm{ddoff\text{-}opt}}$ values, the waveforms of switch node voltage V_p are used as a reference. In Fig. 11, V_p waveforms for 0- and 31-ns t_{ddon} are compared at 2-A load. It is seen that during the M_1 turn-on transitions, i.e., V_p falling edge, obvious diode conduction voltage drop can be observed for 31-ns t_{ddon}, but not for 0-ns case. Hence, it is safe to conclude that $t_{\mathrm{ddon\text{-}opt}}$ for 2-A load is around 0 ns, and further reducing t_{ddon} to negative values will induce shoot-through. Same observations can be made for 1- and 0.5-A loading conditions, and 0 ns is identified as the $t_{\mathrm{ddon\text{-}opt}}$ for all load cases.

In Fig. 12, V_p waveforms for different t_{ddoff} are compared at 0.5-A load. In the case of 24-ns t_{ddoff}, an increase in output capacitor charging rate can be observed on the V_p rising edge, which indicates the partial voltage turn-on of M_2. In the case of 50-ns t_{ddoff}, 3 V raised from the output voltage indicates the diode conduction during deadtime. The waveform for 38-ns t_{ddoff} shows no such features and corresponds to the $t_{\mathrm{ddoff\text{-}opt}}$ at 0.5-A load. Similarly, the $t_{\mathrm{ddoff\text{-}opt}}$ values for 2- and 1-A loads can be identified as around 14 and 20 ns, respectively. These values match well with the analytical and simulation results.

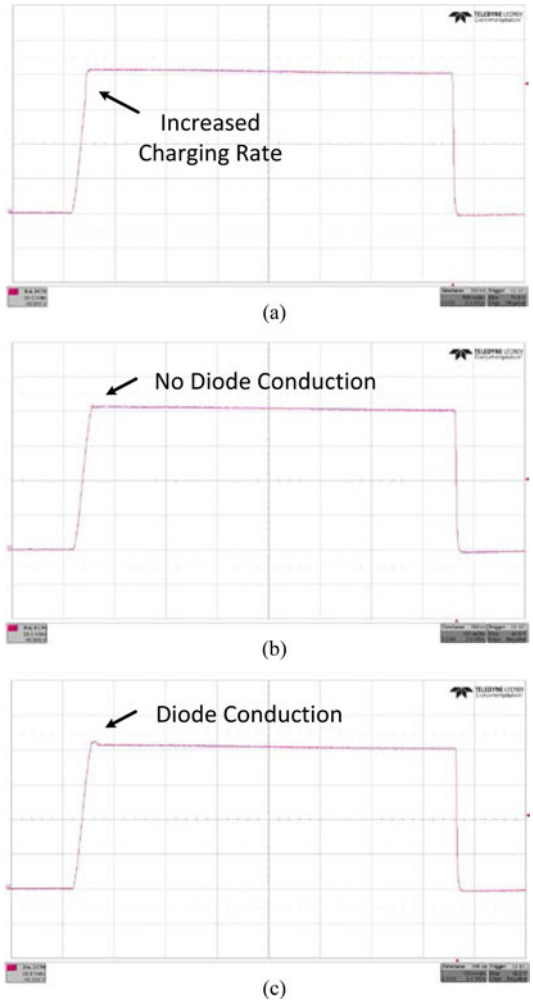

Fig. 12. Measured switch node voltage waveforms for GaN device 0.5-A load condition and 0 ns t_{ddon}, (a) t_{ddoff} is 24 ns, (b) t_{ddoff} is 38 ns, (c) t_{ddoff} is 50 ns.

TABLE V
COMPARISON BETWEEN CALCULATED, SIMULATED, AND TESTED OPTIMAL DEADTIME VALUES OF GAN DEVICES

Load	Optimal Deadtime	Calculated	Simulated	Tested
0.5 A	$t_{\mathrm{ddon\text{-}opt}}$ (ns)	0.427	0	0
	$t_{\mathrm{ddoff\text{-}opt}}$ (ns)	36.82	35	38
1 A	$t_{\mathrm{ddon\text{-}opt}}$ (ns)	0.427	0	0
	$t_{\mathrm{ddoff\text{-}opt}}$ (ns)	22.94	20	20
2 A	$t_{\mathrm{ddon\text{-}opt}}$ (ns)	0.427	0	0
	$t_{\mathrm{ddoff\text{-}opt}}$ (ns)	13.15	10	14

C. Validation of Deadtime Optimization Model With Experimental Results

To show the effectiveness and accuracy of the deadtime optimization model proposed, calculated optimal deadtimes are compared with those obtained from simulation and experiments in Table V.

As can be seen, values listed in the table show good correlation between the analytical model, simulation, and experimentation. In particular, the calculated values deviate from tested values by less than 3 ns. As reported in the literature, the best industrial solution for deadtime optimization on Si converter still generates nonoptimal errors of more than 13 ns [23]. Hence, the optimization model presents significantly improvements with at least four times more accuracy.

V. CONCLUSION

An original modeling method for deadtime optimization on a GaN device-based synchronous boost converter has been proposed in this paper. The optimal deadtime calculation model is based on analyzing the switching transition times given the switching device data, gate drive circuit information, and converter operating conditions. The model is applied to predict the optimal deadtimes of the 160-W GaN converter for different operating conditions. Simulation and experimental results on the given converter are used to validate the accuracy of the proposed model. The experimental data shows very good correlation with analytical and simulation results. The optimal deadtime values predicted by analytical model lie within ± 3 ns range compared to the test results, and this shows significant improvements over the deadtime optimization technique used for Si converters in industry, which generates more than 13-ns errors. Furthermore, while most conventional deadtime optimization methods require either specialized drivers or high fidelity sensors, the proposed model can be easily implemented in a digital controller with a few lines of codes.

As GaN-based switching devices will be used for power converters with very high switching frequencies (up to several megahertz) in the future, the influence of improper deadtimes will become even more prominent, and optimization of deadtimes will be critical. The research results presented in this paper are applicable to a wide range of applications, where phase-leg configurations are utilized, including topologies, such as voltage source inverters and synchronous buck converters. In practice, the proposed optimal deadtime model can be applied either offline by precalculating all the deadtime values needed for different operating conditions, or used online by adjusting the deadtimes in real time based on the current and voltage measurements.

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