Deadbeat Predictive Power Control of Single-Phase Three-Level Neutral-Point-Clamped Converters Using Space-Vector Modulation for Electric Railway Traction

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***Abstract*—This paper presents an alternative approach to address the control and modulation problem of single-phase three-level converters applied in the high-speed railway electrical traction drive system. Following the principle of deadbeat predictive direct torque control of ac motors, this paper discusses an improved direct power control (DPC) method based on a deadbeat active and reactive power prediction technique. Comparing with the conventional PI-based DPC scheme, the proposed deadbeat predictive DPC scheme can provide these advantageous features: lower current harmonics and THD index, lower active and reactive power ripples, and fewer adjusted parameters. Moreover, compared with PI-based DPC with the PI parameters optimization, this approach can also easily obtain fast dynamic response but without the main voltage orientation. A single-phase three-level space vector pulse width modulation (SVPWM) with inherent neutral-point voltage balancing capability is adopted, which can be combined with DPC scheme as an overall control and modulation system. A series of simulation and experimental tests have been conducted to demonstrate an excellent performance of the deadbeat predictive DPC. In addition, the neutral-point-voltage balancing ability of the adopted SVPWM method has been verified.**

***Index Terms*—Deadbeat prediction, direct power control (DPC), neutral-point voltage balancing, single phase, space vector pulse width modulation (SVPWM), three-level converter.**

I. Introduction

A REPRESENTATIVE high-speed railway traction drive system consists of traction transformers, single-phase pulse width modulation (PWM) converters, three-phase PWM inverters, and induction motors [1]. The front-end power converter of electrical traction drive system usually adopts a single-phase PWM converter to achieve high power factor, low current harmonics, constant dc-link voltage, and the bidirectional power-flow capability [2]–[6]. The typical structures of single-phase PWM traction converters can be divided into two categories: two-level [1] and three-level neutral-point-clamped (NPC) topologies [2], [3]. The latter features lower voltage stress on power semiconductors, lower voltage harmonics, and smaller electromagnetic interference, while the former features simpler circuit. From overall system design point of view, the latter is more suitable for high voltage and large power applications. Recently, the three-level NPC converter-inverter propulsion system has been widely applied in Japan and China high-speed electric multiple units [3]–[5].

To achieve high power factor, near-sinusoidal line current, and constant dc-link voltage, various control strategies have been proposed for single-phase PWM converters in the railway traction drive system. These strategies can be classified into current internal loop controllers [6]–[8] and indirect active/reactive power controllers [9], [10]. Current loop controllers commonly use indirect current control [11], instantaneous current prediction control [12], and proportional-integral (PI) [8] or proportional-resonant-based control methods [7]. In particular, indirect active/reactive power control of single-phase converters, based on fictitious-axis emulation to achieve zero steady-state current error, is essentially an active and reactive current decoupling control scheme in direct-quadrature (*d-q*) synchronous reference frames. This method is also called voltage-oriented control (VOC) for current vector orientation with respect to the voltage vector [13].

Nowadays, a direct power control (DPC) technique based on the instantaneous power theory introduced by Akagi *et al.* [14] has emerged in three-phase PWM converters [15]–[34]. This DPC technique originates from the well-known direct torque control (DTC) used in adjustable speed drives system. The DPC algorithm directly selects the instantaneous active and reactive power terms as control variables rather than the current variables that are commonly used in the VOC system [19], which is similar to the application of stator flux and torque terms as control variables in DTC. As a result, the performance of DPC schemes depends on two key factors: one is the accurate evaluation of the instantaneous active and reactive power values; the other is the accurate orientation of power-source voltage vector position [20] or virtual-flux vector position [21]. The basic idea of DPC is to choose the best switching state of the power switches through a lookup table with hysteresis comparisons to maintain constant dc-link voltage and achieve unity power factor [20], [22]. Therefore, one advantage of the conventional

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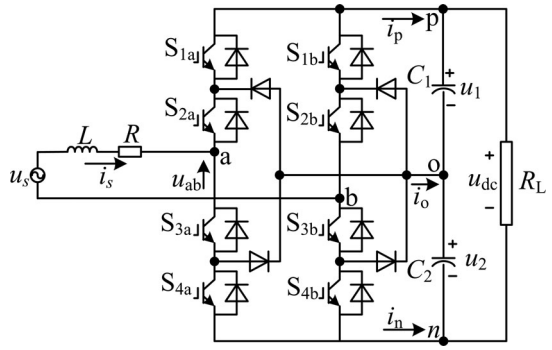

Fig. 1. Single-phase three-level NPC converter.

DPC scheme is the fast dynamic power regulation response. The main drawbacks of this DPC scheme are the needs for a higher sampling frequency to obtain satisfactory performance, and a variable switching frequency. To overcome these drawbacks, various modified DPC schemes with a constant switching frequency, such as model predictive DPC [23]–[25], PI-based DPC [26], [27], slide-mode control DPC [28], and predictive DPC schemes with space-vector PWM (SVPWM) [29]–[31] or vector sequences with duty cycle calculating [32], [33], have been widely proposed and reported for three-phase converters in recent years. However, only several literatures have reported the fuzzy logic table-lookup DPC [35], constrained model predictive DPC [36] and predictive DPC schemes with carrier-based PWM [37] in single-phase converters application. Although performances of the predictive DPC scheme proposed in [37] are better than those of VOC scheme, single-phase instantaneous power calculation still depends on the voltage orientation in VOC by generating two fictitious orthogonal signals of the main voltage and the line current with second-order generalized integrator (SOGI) method. Therefore, the performance of predictive DPC scheme is directly determined by the accuracy of voltage orientation and SOGI method.

In this paper, a digital deadbeat predictive DPC scheme of single-phase three-level converters is proposed to realize a sinusoidal line current drawing, unit power factor, constant dc-link voltage, time delay compensation in the digital control, and fast dynamic performance. Furthermore, a new calculation method of single-phase instantaneous power without the main voltage orientation is discussed. As it is well known, three-level NPC converters have a significant problem related to the fluctuation of the neutral-point voltage [5], [9]. Therefore, a single-phase three-level SVPWM with neutral-point voltage balancing capability [38] is adopted to solve dc-link capacitor voltage unbalance problem, and to generate PWM drive signals. Simulation and experimental tests verified the proposed deadbeat predictive DPC using SVPWM, and demonstrated an advantageous performance compared to a conventional PI-based DPC strategy.

II. DQ Modeling of Single-Phase Three-Level NPC Converters

Fig. 1 shows the topology of a single-phase three-level NPC converter, where *L* and *R* are symbols for the equivalent inductance and resistance of traction transformer in railway locomotive application, respectively; C_1 and C_2 are symbols for the two dc-link capacitors; and R_L is the symbol for the equivalent resistance of inverter-motor side; S_{1a}, S_{2a}, S_{3a}, and S_{4a} are insulated-gate bipolar transistor (IGBT) modules with antiparallel diodes of **a** phase; and S_{1b}, S_{2b}, S_{3b}, and S_{4b} are IGBT modules with antiparallel diodes of **b** phase.

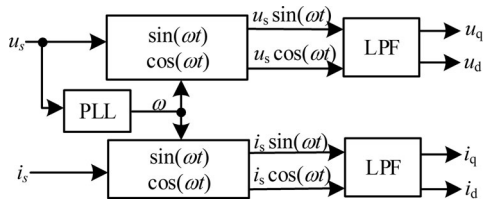

Fig. 2. Block diagram of calculating u_d, u_q and i_d, i_q.

The main voltage u_s, the line current i_s, and the input voltage u_{ab} of the adopted converter in *d-q* synchronous reference frame are defined as follows:

$$u_s = u_d \cos(\omega t) + u_q \sin(\omega t) \tag{1}$$

$$i_s = i_d \cos(\omega t) + i_q \sin(\omega t) \tag{2}$$

$$u_{ab} = u_{abd} \cos(\omega t) + u_{abq} \sin(\omega t) \tag{3}$$

where ω represents angular frequency of the main voltage u_s; u_d, i_d, and u_{abd} are the *d*-axis component of the main voltage u_s, the line current i_s, and input voltage u_{ab} in *d-q* reference frame; u_q, i_q, and u_{abq} are the *q*-axis component of the main voltage u_s, the line current i_s, and input voltage u_{ab}.

The *d*-axis and *q*-axis components can be demodulated from the multiplying cos(*ωt*) and sin(*ωt*), which is realized with a frame transformation similar to the one with *d-q* coordinates in a three-phase system. As an illustration, (4) and (5) depict the demodulation processes of voltages u_d and u_q

$$\begin{aligned} u_s \cos(\omega t) &= u_d \cos^2(\omega t) + u_q \sin(\omega t)\cos(\omega t) \\ &= \frac{u_d}{2} + \frac{u_d \cos(2\omega t) + u_q \sin(2\omega t)}{2} \end{aligned} \tag{4}$$

$$\begin{aligned} u_s \sin(\omega t) &= u_d \cos(\omega t)\sin(\omega t) + u_q \sin^2(\omega t) \\ &= \frac{u_q}{2} + \frac{u_d \sin(2\omega t) - u_q \cos(2\omega t)}{2}. \end{aligned} \tag{5}$$

As dc voltage components, u_d and u_q can be extracted from (4) and (5) by two low-pass filters (LPF) or notch filters. Similar expressions can also be derived for the line current i_s. The block diagram of calculating u_d, u_q, i_d, and i_q is shown in Fig. 2, where LPFs are adopted to filter the twice frequency components, and the other frequency components caused by the harmonics of voltage u_s and current i_s.

As shown in Fig. 1, the Kirchhoff voltage law is used to analyze the voltage across the inductor *L*. The voltage equation is

$$L\frac{di_s}{dt} = u_s - Ri_s - u_{ab}. \tag{6}$$

Substituting (1)–(3) into (6) and expanding it in *d-q* frame yield

$$\begin{cases} u_{abd} = u_d - Ri_d - L\frac{di_d}{dt} - \omega L i_q \\ u_{abq} = u_q - Ri_q - L\frac{di_q}{dt} + \omega L i_d. \end{cases} \tag{7}$$

Applying the first-order discrete approximation to *d-q* frame converter model expressed in (7), a discrete model of the adopted converter in *d-q* frame is expressed as

$$\begin{cases} u_{abd}(k) = u_d(k) - \frac{L}{T_s}[i_d(k+1) - i_d(k)] \\ \qquad\qquad - Ri_d(k) - \omega L i_q(k) \\ u_{abq}(k) = u_q(k) - \frac{L}{T_s}[i_q(k+1) - i_q(k)] \\ \qquad\qquad - Ri_q(k) + \omega L i_d(k) \end{cases} \tag{8}$$

where T_s is the sampling period.

III. DPC of Single-Phase Three-Level NPC Converters

A. Conventional PI-Based DPC

The application of the three-phase instantaneous power theory [14] into the single-phase converter system is shown as follows:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{1}{2}\begin{bmatrix} u_d & u_q \\ u_q & -u_d \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{9}$$

where *P* and *Q* are the instantaneous active and reactive powers in *d-q* rotary reference frame, respectively. Then, the currents can be derived from (9) as

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{u_{dq}^2}\begin{bmatrix} u_d & u_q \\ u_q & -u_d \end{bmatrix}\begin{bmatrix} P \\ Q \end{bmatrix} \tag{10}$$

where

$$u_{dq}^2 = u_d^2 + u_q^2. \tag{11}$$

Substituting (10) into (7) and neglecting the resistor *R* yield

$$\begin{bmatrix} u_{abd} \\ u_{abq} \end{bmatrix} = \begin{bmatrix} u_d \\ u_q \end{bmatrix} - \frac{2L}{u_{dq}^2}\begin{bmatrix} u_d\frac{dP}{dt} + u_q\frac{dQ}{dt} \\ u_q\frac{dP}{dt} - u_d\frac{dQ}{dt} \end{bmatrix} - \frac{2}{u_{dq}^2}\begin{bmatrix} \omega L u_q & -\omega L u_d \\ -\omega L u_d & -\omega L u_q \end{bmatrix}\begin{bmatrix} P \\ Q \end{bmatrix}. \tag{12}$$

If the main voltage u_s is oriented to *d*-axis, then u_q equals zero, and (12) could be simplified as

$$\begin{bmatrix} u_{abd} \\ u_{abq} \end{bmatrix} = \begin{bmatrix} u_d \\ 0 \end{bmatrix} - \frac{2L}{u_d}\begin{bmatrix} \frac{dP}{dt} \\ -\frac{dQ}{dt} \end{bmatrix} + \frac{2}{u_d}\begin{bmatrix} \omega L Q \\ \omega L P \end{bmatrix}. \tag{13}$$

Equation (13) represents the decoupled process of active and reactive powers on the premise of the main voltage oriented to *d*-axis. As *d*-axis and *q*-axis voltage or power components are both dc components, the derivative of active power *P* and reactive power *Q* in (13) can be realized by PI regulators.

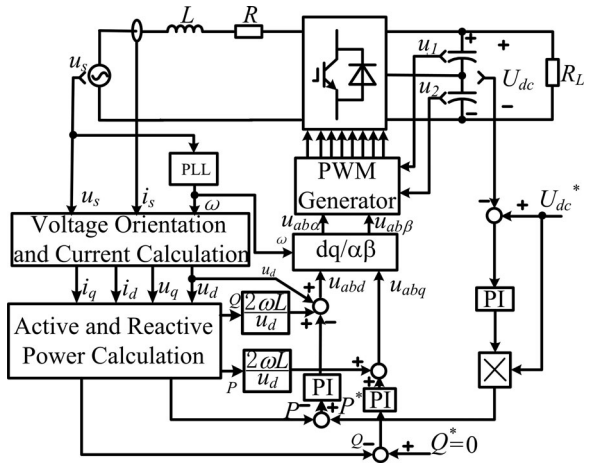

Fig. 3. Block diagram of conventional PI-based DPC with constant switching frequency.

Fig. 3 shows block diagram of the conventional DPC with two PI-based power controllers. In this figure, a PI-based voltage controller is adopted to regulate the dc-link voltage. The output of the PI-based voltage controller multiplied by the dc-link voltage can result in the active reference power P^*. Alternatively, the reactive reference power Q^* is set as zero for achieving unit power factor. The *d-q* axis components (u_d and u_q) of the main voltage can be calculated from (4) and (5). But cos(ωt) and sin(ωt) in the left-hand expressions of (4) and (5) should be replaced by $\cos(\omega t + \varphi)$ and $\sin(\omega t + \varphi)$ in order to realize the main voltage orientation ($u_q = 0$), where φ represents phase angle of the main voltage. Therefore, the performance of the main voltage orientation depends on the phase angle detection accuracy in PLL block. The *d-q* axis components calculation method shown in (4) and (5) is also available for the line current. *P* and *Q* can be calculated through (9), which are decoupled with two PI-based power controllers. A two-axis rotary (*d-q)* to stationary ($\alpha-\beta$) reference frame transformation is adopted to transform the output voltages of power controllers, which can be expressed in $\alpha-\beta$ frame as

$$\begin{bmatrix} u_{ab\alpha} \\ u_{ab\beta} \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ \sin\omega t & -\cos\omega t \end{bmatrix}\begin{bmatrix} u_{abd} \\ u_{abq} \end{bmatrix}. \tag{14}$$

And then, a PWM module is used to generate the gate signals of power switches, and obtain a constant switching frequency. Actually, this DPC scheme is very similar to the voltage-oriented vector control scheme in [10]. The accurate decoupling of the active and reactive powers or currents completely depends on the orientation accuracy of the main voltage in *d*-axis. As a result, any small voltage orientation deviation would deteriorate the performance of power decoupling controller. Another drawback of this conventional PI-based DPC is a need for three PI regulators. The selection of the proportional and integral parameters of three PI regulators is also a complicated task. Two PI-based power controllers will result in a slow dynamic response for power regulation. Therefore, the performances of the PI-based DPC scheme are not only restricted to the accuracy

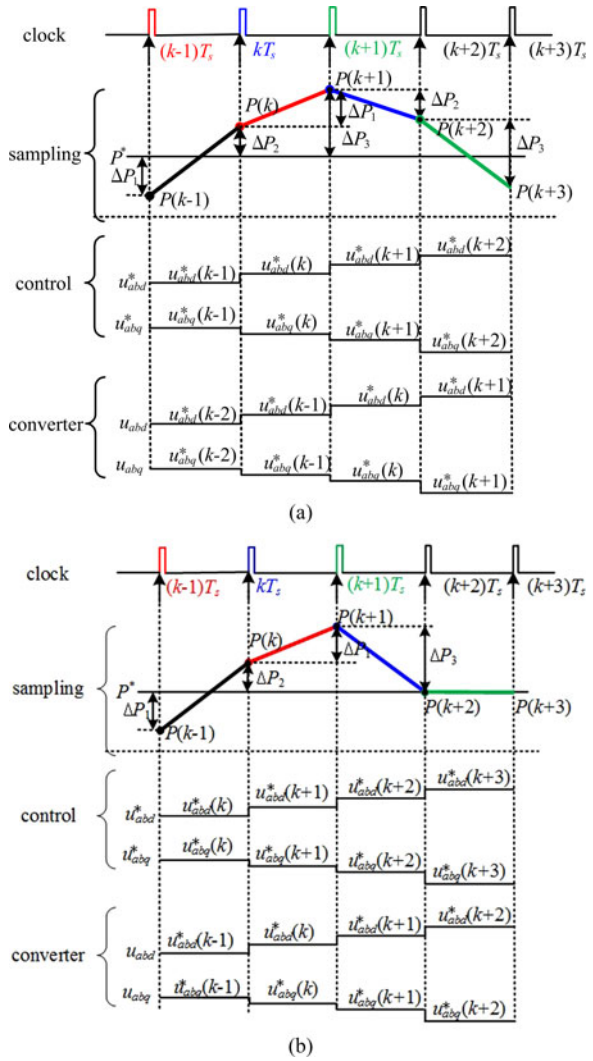

Fig. 4. Digital prediction diagram of active power and the voltages. (a) Conventional predictive control. (b) Deadbeat predictive control.

of voltage orientation in *d-q* rotary reference frame, but also depended on parameters optimization of PI regulators.

B. Deadbeat Predictive DPC

It is assumed that the sampling period T_s equals the control period, and is much smaller than the period of the main voltage, the main voltage can be approximately considered as a constant value in one sampling interval. Thus then

$$\begin{bmatrix} u_d(k+1) \\ u_q(k+1) \end{bmatrix} \approx \begin{bmatrix} u_d(k) \\ u_q(k) \end{bmatrix}. \tag{15}$$

On the basis of (9) and (15), the variation of powers *P* and *Q* during a sampling interval can be shown as

$$\begin{bmatrix} P(k+1)-P(k) \\ Q(k+1)-Q(k) \end{bmatrix} = \frac{1}{2}\mathbf{U}\begin{bmatrix} i_d(k+1)-i_d(k) \\ i_q(k+1)-i_q(k) \end{bmatrix} \tag{16}$$

where

$$\mathbf{U} = \begin{bmatrix} u_d(k) & u_q(k) \\ u_q(k) & -u_d(k) \end{bmatrix}. \tag{17}$$

Equation (16) can be transformed as

$$\begin{bmatrix} i_d(k+1)-i_d(k) \\ i_q(k+1)-i_q(k) \end{bmatrix} = \frac{2}{u_{dq}^2(k)}\mathbf{U}\begin{bmatrix} P(k+1)-P(k) \\ Q(k+1)-Q(k) \end{bmatrix}. \tag{18}$$

Substituting (18) into (8) yields

$$\begin{bmatrix} u_{abd}(k) \\ u_{abq}(k) \end{bmatrix} = \begin{bmatrix} u_d(k) \\ u_q(k) \end{bmatrix} - \begin{bmatrix} R & \omega L \\ -\omega L & R \end{bmatrix}\begin{bmatrix} i_d(k) \\ i_q(k) \end{bmatrix} - \frac{2L\mathbf{U}}{T_s u_{dq}^2(k)}\begin{bmatrix} P(k+1)-P(k) \\ Q(k+1)-Q(k) \end{bmatrix}. \tag{19}$$

Applying a discretized expression of (10) and substituting currents $i_d(k)$ and $i_q(k)$ at *k*th sampling instant into (19), the discrete voltages' expressions of the adopted converter in *d-q* axis frame are rewritten as

$$\begin{bmatrix} u_{abd}(k) \\ u_{abq}(k) \end{bmatrix} = \begin{bmatrix} u_d(k) \\ u_q(k) \end{bmatrix} - \frac{2\mathbf{U}}{u_{dq}^2(k)}\begin{bmatrix} R & \omega L \\ -\omega L & R \end{bmatrix}\begin{bmatrix} P(k) \\ Q(k) \end{bmatrix} - \frac{2L\mathbf{U}}{T_s u_{dq}^2(k)}\begin{bmatrix} P(k+1)-P(k) \\ Q(k+1)-Q(k) \end{bmatrix}. \tag{20}$$

$P(k+1)$ and $Q(k+1)$ at the $(k+1)$th sampling instant are derived from (20) as

$$\begin{bmatrix} P(k+1) \\ Q(k+1) \end{bmatrix} = \frac{T_s\mathbf{U}}{2L}\left(\begin{bmatrix} u_d(k) \\ u_q(k) \end{bmatrix} - \begin{bmatrix} u_{abd}(k) \\ u_{abq}(k) \end{bmatrix}\right) + \mathbf{Z}\begin{bmatrix} P(k) \\ Q(k) \end{bmatrix} \tag{21}$$

where

$$\mathbf{Z} = \begin{bmatrix} 1-\dfrac{T_s R}{L} & -\omega T_s \\ \omega T_s & 1-\dfrac{T_s R}{L} \end{bmatrix}. \tag{22}$$

On the basis of (20), the desired voltages $u_{abd}(k+1)$ and $u_{abq}(k+1)$ are derived as

$$\begin{bmatrix} u_{abd}(k+1) \\ u_{abq}(k+1) \end{bmatrix} = \begin{bmatrix} u_d(k+1) \\ u_q(k+1) \end{bmatrix} - \frac{2\mathbf{U}}{u_{dq}^2(k+1)}\begin{bmatrix} R & \omega L \\ -\omega L & R \end{bmatrix}\begin{bmatrix} P(k+1) \\ Q(k+1) \end{bmatrix} - \frac{2L\mathbf{U}}{T_s u_{dq}^2(k+1)}\begin{bmatrix} P(k+2)-P(k+1) \\ Q(k+2)-Q(k+1) \end{bmatrix}. \tag{23}$$

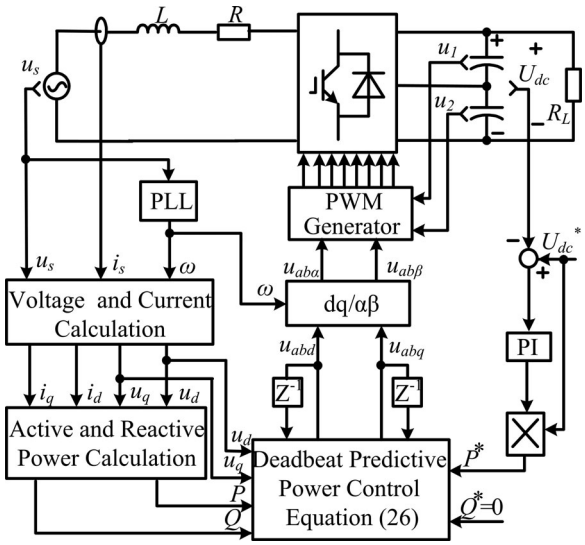

Fig. 5. Block diagram of the deadbeat predictive DPC scheme.

Substituting (15) and (21) into (23) yields

$$\begin{bmatrix} u_{abd}(k+1) \\ u_{abq}(k+1) \end{bmatrix} = (\mathbf{Z}+\mathbf{E}) \begin{bmatrix} u_d(k) \\ u_q(k) \end{bmatrix} - \mathbf{Z} \begin{bmatrix} u_{abd}(k) \\ u_{abq}(k) \end{bmatrix} + \frac{2L\mathbf{U}}{T_s u_{dq}^2(k)} \left(\mathbf{Z}^2 \begin{bmatrix} P(k) \\ Q(k) \end{bmatrix} - \begin{bmatrix} P(k+2) \\ Q(k+2) \end{bmatrix} \right) \tag{24}$$

where $\mathbf{E}$ is an identity matrix.

As it is well known, both of computation time delay and sampling time delay exist surely in digital control system. In a real digital controller (e.g., TI TMS320F2812), the conversion frequency of analog-to-digital (A/D) module can reach several megahertz. And the control frequency is several kilohertz. The sampling time delay caused by A/D module conversion is much smaller than computation time delay (called the control period), and can be neglected. It is significant that the sampling period is greater than or equal to the control period. Therefore, in digital control system, there is one sampling period delay between the reference voltages calculated in the controller and the real sampling voltages of converter. Fig. 4(a) shows the conventional predictive control diagram of active power and voltages. In Fig. 4(a), the reference voltages u_{abd}^* and u_{abq}^* during $[kT_s, (k+1)T_s]$ interval equal and hold on to the values $u_{abd}^*(k)$ and $u_{abq}^*(k)$ at the kth sampling instant, respectively. And $u_{abd}^*(k-1)$ and $u_{abq}^*(k-1)$ are loaded to PWM module in $[kT_s, (k+1)T_s]$ sampling interval. So, the power difference between $P(k+1)$ and $P(k)$ equals ΔP_1, and $\Delta P_1 = P^* - P(k-1)$. In $[(k+1)T_s, (k+2)T_s]$ sampling interval, voltage values $u_{abd}^*(k)$ and $u_{abq}^*(k)$ are both loaded to PWM module to generate PWM drive signals. So that the power difference between $P(k+2)$ and $P(k+1)$ equals $-\Delta P_2$, and $-\Delta P_2 = P^* - P(k)$. Meanwhile, the power difference between $P(k+2)$ and P^* at the $(k+2)$th sampling instant exists, and equals ΔP_1. Therefore, in order to eliminate the active power error caused by control time delay, a deadbeat predictive control scheme is proposed and illustrated in Fig. 4(b). The reference voltages u_{abd}^* and u_{abq}^* in $[kT_s, (k+1)T_s]$ sampling interval are $u_{abd}^*(k+1)$ and $u_{abq}^*(k+1)$ predicted and estimated in (24) to compensate the digital controller delay. Until the $(k+1)$th sampling instant, the reference voltages $u_{abd}^*(k+1)$ and $u_{abq}^*(k+1)$ were loaded and executed in the PWM module of digital controller (such as TI TMS320F2812 chip). Therefore, the input active and reactive powers $P(k+2)$ and $Q(k+2)$ at the $(k+2)$th sampling instant can follow and reach the references $P^*(k)$ and $Q^*(k)$, respectively. In deadbeat predictive control, $P(k+2)$ and $Q(k+2)$ can be expressed as

$$\begin{cases} P(k+2) = P^*(k) \\ Q(k+2) = Q^*(k). \end{cases} \tag{25}$$

Substituting (25) into (24) yields

$$\begin{bmatrix} u_{abd}^*(k+1) \\ u_{abq}^*(k+1) \end{bmatrix} = (\mathbf{Z}+\mathbf{E}) \begin{bmatrix} u_d(k) \\ u_q(k) \end{bmatrix} - \mathbf{Z} \begin{bmatrix} u_{abd}(k) \\ u_{abq}(k) \end{bmatrix} + \frac{2L}{T_s u_{dq}^2} \left(\mathbf{Z}^2 \mathbf{U} \begin{bmatrix} P(k) \\ Q(k) \end{bmatrix} - \mathbf{U} \begin{bmatrix} P^*(k) \\ Q^*(k) \end{bmatrix} \right). \tag{26}$$

Fig. 5 shows the block diagram of the proposed deadbeat predictive DPC scheme for the single-phase three-level NPC converter. After the reference voltages calculated from (26) are transformed to the expressions in the $\alpha-\beta$ synchronous reference frame, the reference values $u_{ab\alpha}^*(k+1)$ and $u_{ab\beta}^*(k+1)$ are uploaded into PWM module to generate PWM drive signals at the $(k+1)$th instant.

Compared to the conventional PI-based DPC shown in Fig. 3, the proposed predictive DPC scheme does not require the main voltage orientation and can compensate digital control delay. Furthermore, the controller design is greatly simplified and free from difficult tuning of multiple PI controller parameters.

IV. Single-Phase Three-Level SVPWM Algorithm With Neutral-Point Voltage Balance

A. Definition of Space Voltage Vectors and Sectors

A single-phase three-level SVPWM with neutral-point voltage balance is adopted to generate PWM drive signals. The SVPWM algorithm is analyzed in the following section [38].

For the convenience of discussion, a switching function S_i is defined for the adopted converter as

$$S_i = \begin{cases} 1 & \text{if } S_{1i} \text{ and } S_{2i} \text{ ON} \\ 0 & \text{if } S_{2i} \text{ and } S_{3i} \text{ ON} \\ -1 & \text{if } S_{3i} \text{ and } S_{4i} \text{ ON} \end{cases} \qquad (i = a, b). \tag{27}$$

Therefore, the adopted converter owns a total of nine switching combinations. Each switching state ($S_a S_b$) is defined as one or two space vectors. The vector of state (1 1) and (-1 -1) is defined as $\boldsymbol{V}_{3+}$ or $\boldsymbol{V}_{3-}$; the vector of state (0 0) is defined as $\boldsymbol{V}_0$; the vector of state (1 -1) is defined as $\boldsymbol{V}_{1+}$; the vector of state (-1 1) is defined as $\boldsymbol{V}_{1-}$. When the neutral point voltage is a half of dc-link voltage ($u_1 = u_2$), states (1 0) and (0 -1) are

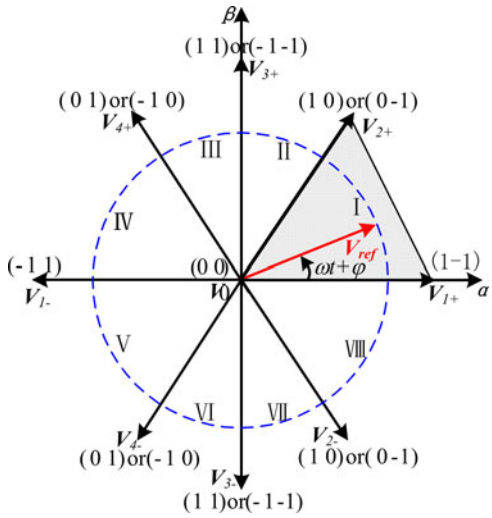

Fig. 6. Sector definition diagram of the SVPWM algorithm.

equivalent to each other, and their corresponding vector is $\boldsymbol{V_{2+}}$ or $\boldsymbol{V_{2-}}$. Similarly, states (0 1) and $(-1\ 0)$ are equivalent to each other, and their corresponding vector is $\boldsymbol{V_{4+}}$ or $\boldsymbol{V_{4-}}$. The difference between $\boldsymbol{V_{i+}}$ and $\boldsymbol{V_{i-}}(i = 2, 3, 4)$ is that directions of their β-axis components are opposite, which is shown in Fig. 6.

Fig. 6 shows sector definition of this SVPWM algorithm. There are eight active vectors and one zero-vector. A rule is defined that α-axis component of each active vector equals the input voltage u_{ab} of the adopted converter. Therefore, the amplitudes of each vector equal the dc-link voltage value $U_{\rm dc}$; and the phase angles with α-axis of vectors $\boldsymbol{V_1}$, $\boldsymbol{V_{2+}}$, $\boldsymbol{V_{3+}}$, $\boldsymbol{V_{4+}}$, $\boldsymbol{V_{1-}}$, $\boldsymbol{V_{4-}}$, $\boldsymbol{V_{3-}}$, and $\boldsymbol{V_{2-}}$ are 0°, 60°, 90°, 120°, 180°, 240°, 270°, and 300°, respectively. The $\alpha-\beta$ stationary frame is divided into eight sectors due to eight active voltage vectors.

B. Calculation of the Duty Cycles by Using Projections

A reference voltage vector $\boldsymbol{V_{\rm ref}}$ in $\alpha - \beta$ stationary frame is defined as

$$\boldsymbol{V_{\rm ref}} = u_{ab\alpha} + ju_{ab\beta}. \tag{28}$$

The reference vector $\boldsymbol{V_{\rm ref}}$ can be generated using the SVPWM technique of the three switching vectors ($\boldsymbol{V_a}$, $\boldsymbol{V_b}$ and zero vector $\boldsymbol{V_0}$) that are nearest to the reference vector at each switching interval. If the reference vector lies on the triangle connecting the tips of vectors $\boldsymbol{V_a}$, $\boldsymbol{V_b}$, and $\boldsymbol{V_0}$ (e.g., $\boldsymbol{V_{1+}}$, $\boldsymbol{V_{2+}}$, and $\boldsymbol{V_0}$ in Fig. 6), the reference vector can be represented as

$$\boldsymbol{V_{\rm ref}}T_{\rm sw} = \boldsymbol{V_a}T_a + \boldsymbol{V_b}T_b + \boldsymbol{V_0}T_0 \tag{29}$$

$$T_{\rm sw} = T_a + T_b + T_0 \tag{30}$$

where $T_{\rm sw}$ is the switching cycle; and T_a, T_b, and T_0 are the corresponding duty cycles of $\boldsymbol{V_a}$, $\boldsymbol{V_b}$, and $\boldsymbol{V_0}$ in each switching interval, respectively. The duty cycle expression of the corresponding vector in each sector is discussed in [38].

TABLE I
SIMULATION AND EXPERIMENTAL SYSTEM PARAMETERS

Parameters	Value
The main voltage (*rms*) $U_s/\rm V$	60
DC-link reference voltage $U_{\rm dc}^*/\rm V$	120
Switching frequency $f_{\rm sw}/\rm kHz$	2.5
The rating load R_L/Ω	30
AC-side inductor $L/\rm mH$	5.0
DC-link capacitors $C_1 = C_2/\rm mF$	4.4
Sampling and control frequency $f_s/\rm kHz$	5.0
The dead time of PWM signals $\tau/\mu s$	2.5

C. Neutral-Point Voltage Balancing

A sign function $S_{\rm NPVB}$ of controlling neutral point voltage is defined as

$$S_{\rm NPVB} = \text{sign}[i_s(u_1 - u_2)]$$

$$= \begin{cases} 1 & i_s(u_1 - u_2) \geq 0 \\ 0 & i_s(u_1 - u_2) < 0\,. \end{cases} \tag{31}$$

Then, the rule for choosing switching states of vectors $\boldsymbol{V_{i+}}$ and $\boldsymbol{V_{i-}}(i = 2, 3, 4)$ are designed to balance neutral point voltage. Take a case in sector II as an example, $\boldsymbol{V_a}$ is defined as $\boldsymbol{V_{2+}}$, which represents states (1 0) and $(0\ -1)$. If $S_{\rm NPVB} = 1$, $i_s > 0$, and $u_1 > u_2$ in sector II, state $(0\ -1)$ is chosen as the state of vector $\boldsymbol{V_a}$ in the overall switching interval $T_{\rm sw}$. Switching state $(0\ -1)$ will ensure that capacitor C_2 is charged by the positive line current i_s ($i_s > 0$), while capacitor C_1 is discharged through the load R_L. In such manner, the voltages difference on capacitor C_1 and C_2 is always adjusted toward zero so as to effectively adjust and balance the neutral point voltage.

D. Vector Sequence Design

In each sector, the reference vector $\boldsymbol{V_{\rm ref}}$ is synthesized by two adjacent voltages vectors $\boldsymbol{V_a}$, $\boldsymbol{V_b}$, and zero vector $\boldsymbol{V_0}$. The synthesized sequences in the switching interval $T_{\rm sw}$ are scheduled as follows:

$$\boldsymbol{V_0} \rightarrow \boldsymbol{V_a} \rightarrow \boldsymbol{V_b} \rightarrow \boldsymbol{V_a} \rightarrow \boldsymbol{V_0}.$$

The corresponding duty cycles of the aforementioned vector sequences during $T_{\rm sw}$ are scheduled as

$$T_0/2 \rightarrow T_a/2 \rightarrow T_b \rightarrow T_a/2 \rightarrow T_0/2.$$

V. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the validation of the proposed deadbeat predictive DPC scheme, a comparison of the proposed predictive DPC and the conventional PI-based DPC is adopted in simulation and experimental tests. Table I shows simulation and experimental system parameters.

A. Simulation Results

Fig. 7 shows simulation waveforms of the main voltage, the line current, and two dc-link capacitor voltages for these two

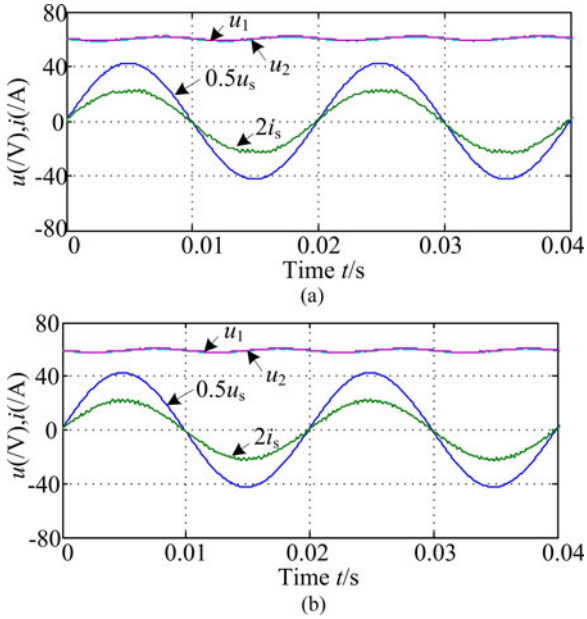

Fig. 7. Simulation waveforms of the main voltage, the line current, and two dc-link capacitor voltages in steady state. (a) PI-based DPC. (b) Deadbeat predictive DPC.

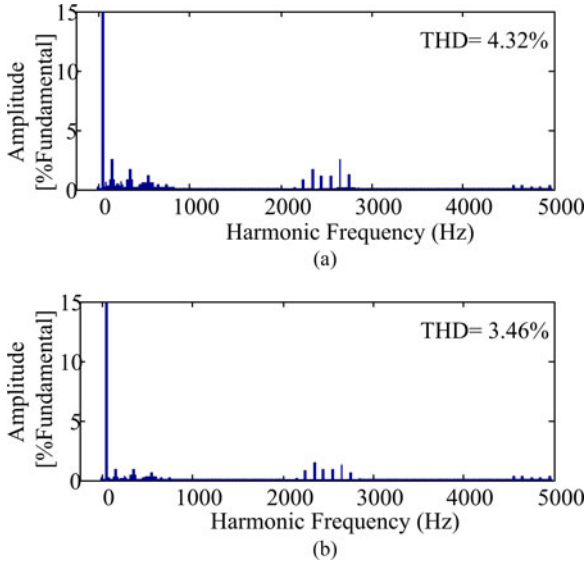

Fig. 8. FFT results of the line currents in simulation. (a) PI-based DPC. (b) Deadbeat predictive DPC.

DPC schemes in steady state, where Fig. 7(a) and (b) shows simulation results of the conventional PI-based DPC and the proposed predictive DPC, respectively. Compared with Fig. 7(a) and (b), the line currents are both drawn to be sinusoidal in phase with the main voltages in these two DPC schemes. And dc-link capacitor voltages u_1 and u_2 are absolutely equal to each other. But the sinusoidal profile of the line current in the proposed predictive DPC is better than that of the line current in the conventional PI-based DPC.

Fig. 8(a) and (b) shows FFT simulation results of the line currents of the conventional PI-based DPC and the proposed

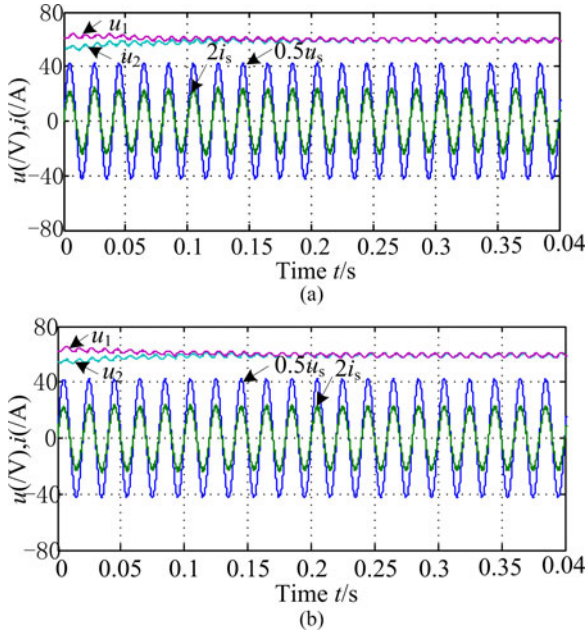

Fig. 9. Simulation waveforms of dc-link capacitor voltages, the main voltage, and the line current with the different initial values of capacitor voltages. (a) PI-based DPC. (b) Deadbeat predictive DPC.

predictive DPC, respectively. In Fig. 8, both of high-order harmonics in the line currents distribute around the switching frequency $f_{\rm sw}$ due to the same SVPWM method adopted in both of control systems. But current THD (3.46%) of the predictive DPC scheme in Fig. 8(b) is lower than that (4.32%) of the PI-based DPC scheme in Fig. 8(a) because of the precise deadbeat prediction of the proposed control system.

Fig. 9 shows simulation waveforms of dc-link capacitor voltages, the main voltage, and the line current with the different initial values of capacitor voltages at $t = 0\,\rm s$. In Fig. 9(a) and (b), it is clear that both of control methods can balance two capacitors' voltages within 0.1 s. Therefore, the inherent neutral-point voltage balancing capability in the single-phase three-level SVPWM method is verified in simulation.

To test dynamic response of active and reactive powers regulation under sudden power change condition, Fig. 10 presents simulation waveforms of active power P and P^*, reactive power Q, and the line current i_s, while active power command P^* steps from 75% to 100% rating value at 0.1 s. From Fig. 10(a) and (b), a comparison of active power P and reactive power Q shows that both control precision and dynamic response of power regulation in the deadbeat predictive DPC are better than those in conventional PI-based DPC. Fig. 11 shows simulation waveforms of dynamic response of dc-link voltages under sudden load change condition. The load is scheduled from 30 to 130 Ω at 0.3 s and vice versa at 1.3 s. Compared with dc-link voltages shown in Fig. 11(a) and (b), dynamic response of dc-link capacitors voltages of the predictive DPC method is faster and better that that of the PI-based DPC method. Therefore, it is clear that the deadbeat predictive DPC scheme can obtain a faster dynamic response than the PI-based DPC method from a comparison of simulation results shown in Figs. 10 and 11.

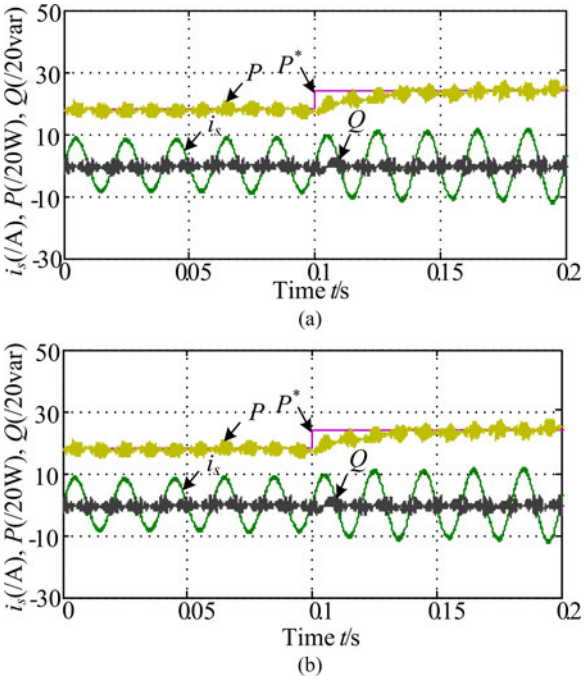

Fig. 10. Simulation waveforms of dynamic response of active and reactive powers regulation under power sudden change from 75% to 100% rating value condition. (a) PI-based DPC. (b) Deadbeat predictive DPC.

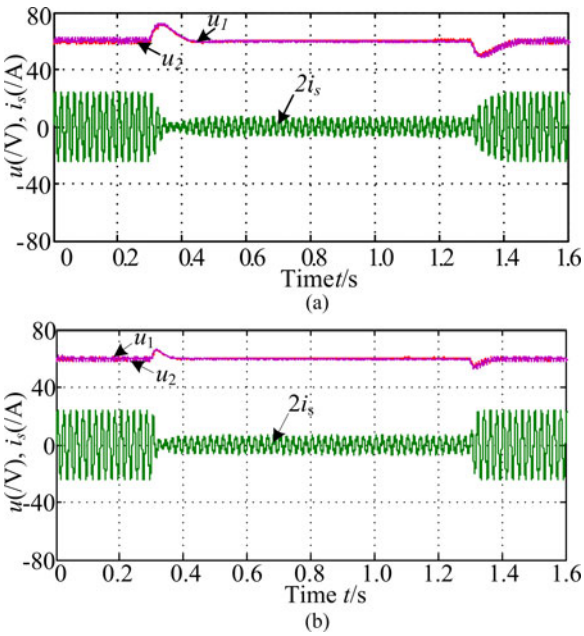

Fig. 11. Simulation waveforms of dynamic response of dc-link voltages under load sudden change condition. (a) PI-based DPC. (b) Deadbeat predictive DPC.

B. Experimental Results

In order to further verify theoretical analysis and simulation results, both of PI-based DPC and the proposed deadbeat predictive DPC schemes are tested in a single-phase three-level NPC converter experimental prototype. The photograph of the experimental hardware prototype platform is shown in Fig. 12.

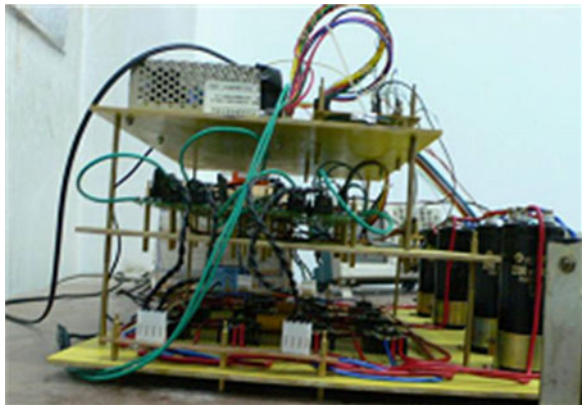

Fig. 12. Photograph of the experimental hardware prototype.

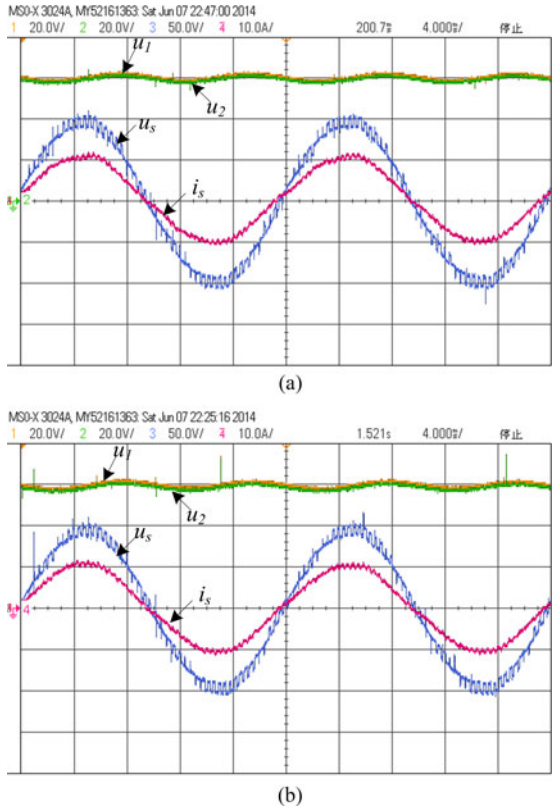

Fig. 13. Experimental waveforms of the main voltage, the line current, and two dc-link capacitor voltages in steady state (u_s : 50 V/div, u_1 and u_2: 20 V/div, i_s : 10 A/div, time: 4 ms/div). (a) PI-based DPC. (b) Deadbeat predictive DPC.

It consists of the main power circuit, the sensor sampling and signal processing circuit, TMS320F2812 controller, gate signal driving and protecting circuit and so on.

Fig. 13 shows experimental waveforms of the main voltage, the line current, and two dc-link capacitor voltages for these two DPC schemes in steady state, where Fig. 13(a) and (b) shows experimental results of the conventional PI-based DPC and the proposed predictive DPC, respectively. There are some harmonic pulse voltages in the waveforms of the main voltages, due to the inductance of an autotransformer as power supply in the experimental prototype. Compared with Fig. 13(a) and (b),

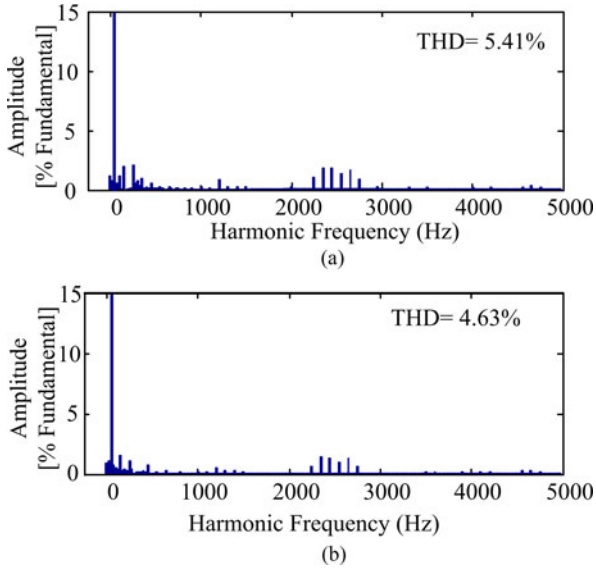

Fig. 14. FFT results of the line currents in experiment. (a) PI-based DPC. (b) Deadbeat predictive DPC.

it is clear that the line current of deadbeat predictive DPC is more sinusoidal with high power factor than that of PI-based DPC scheme. DC-link capacitor voltages u_1 and u_2 are absolutely equal and balanced, too. The experimental results are very similar to the simulation results in Fig. 7(a) and (b).

Fig. 14(a) and (b) shows FFT experimental results of the line currents of the conventional PI-based DPC and the proposed predictive DPC, respectively. Experimental Current THD results in Fig. 14 are close to the simulation current THD results in Fig. 8. And the former THD values are a little higher than the latter THD values due to sensor sampling noise disturbance. Therefore, a comparison of experimental results verifies better performances of the proposed predictive DPC scheme.

Fig. 15 shows experimental waveforms of dc-link capacitor voltages, the main voltage, and the line current with the different initial values of capacitor voltages at $t = 0$ s. Both experimental results of dc-link voltages in Fig. 15(a) and (b) verify the effectiveness of neutral-point voltage balancing capability of the adopted SVPWM method.

Fig. 16 shows experimental waveforms of dynamic response of active and reactive powers regulation under sudden power change from 75% to 100% rating value condition, where experimental waveforms of active power P and P^*, reactive power Q, and the line current of PI-based DPC scheme and deadbeat predictive DPC scheme are shown in Fig. 16(a) and (b), respectively. Compared with Fig. 16(a) and (b), the power dynamic response performance of deadbeat predictive DPC is faster than that of PI-based DPC scheme. Experimental results verify the effectiveness of theory analysis and simulation in further.

Fig. 17 shows experimental waveforms of dynamic response of dc-link voltages under sudden load change condition. The load is scheduled from 30 to 130 Ω and vice versa at the instant after 1.25 s. Compared with dc-link voltages shown in Fig. 17(a) and (b), experimental results also verify that the deadbeat

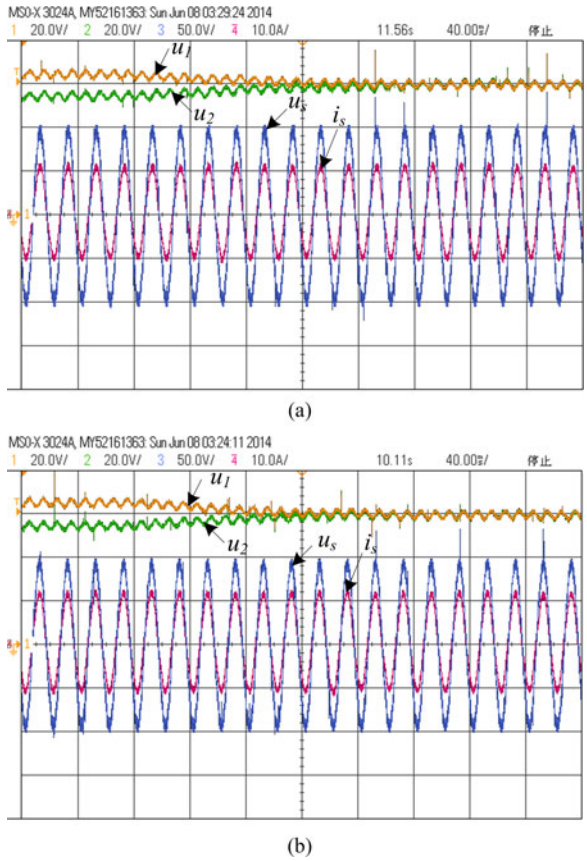

Fig. 15. Experimental waveforms of dc-link capacitor voltages, the main voltage, and the line current with the different initial values of capacitor voltages (u_s : 50 V/div, u_1 and u_2 : 20 V/div, i_s : 10 A/div, time: 40 ms/div). (a) PI-based DPC. (b) Deadbeat predictive DPC.

predictive DPC scheme can obtain a faster dynamic response for dc-link voltage than the PI-based DPC method.

C. Simulation and Experimental Sensitivity Analysis

The deadbeat predictive control loop is particularly sensitive to any model mismatch and to the possibly incorrect identification of the model parameters [39], [40]. From (23), a parameter mismatch between the modeled inductance L or resistance R and their actual values may deteriorate performance of the adopted control system. Because the internal resistance R of the ac-side inductor is very small, the impact of resistance R on system sensitivity can be approximately ignored. Therefore, only parameter mismatch of inductance L should be considered to analysis the system sensitivity [40].

Fig. 18(a) and (b) shows simulation waveforms of dynamic response of active and reactive powers regulation in the adopted deadbeat predictive DPC with $L_m/L = 0.5$ and $L_m/L = 1.5$, respectively, where L_m is the estimation value of inductor used in the control system. Fig. 19(a) and (b) shows the corresponding experimental waveforms of dynamic response with $L_m/L = 0.5$ and $L_m/L = 1.5$, respectively. Comparing with Figs. 18 and 10(b), even if the estimation value of inductor error $(L_m - L)/L$ reaches 50% or −50%, the fast dynamic response of active and reactive powers regulation in the adopted

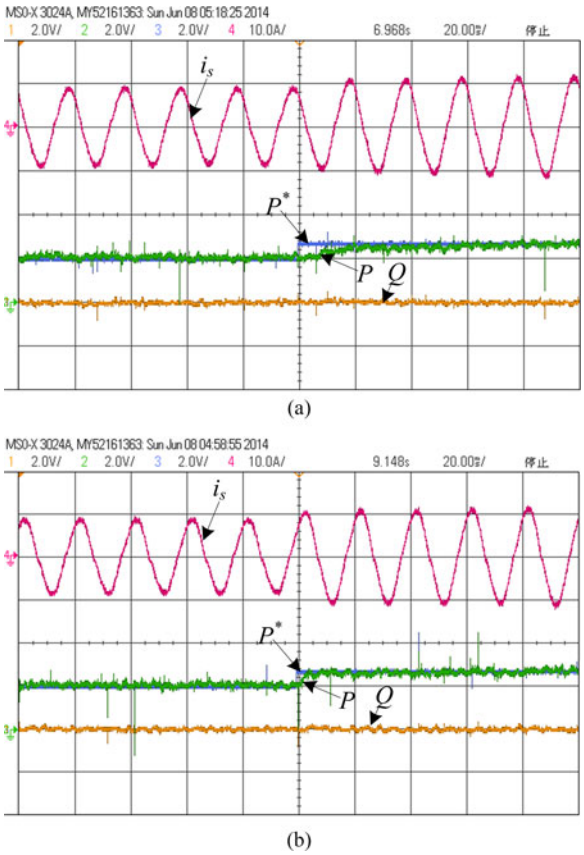

Fig. 16. Experimental waveforms of dynamic response of active and reactive powers regulation under power sudden change from 75% to 100% rating value condition (P and P^*: 360 W/div, Q: 360 var/div, i_s : 10 A/div, time: 20 ms/div). (a) PI-based DPC. (b) Deadbeat predictive DPC.

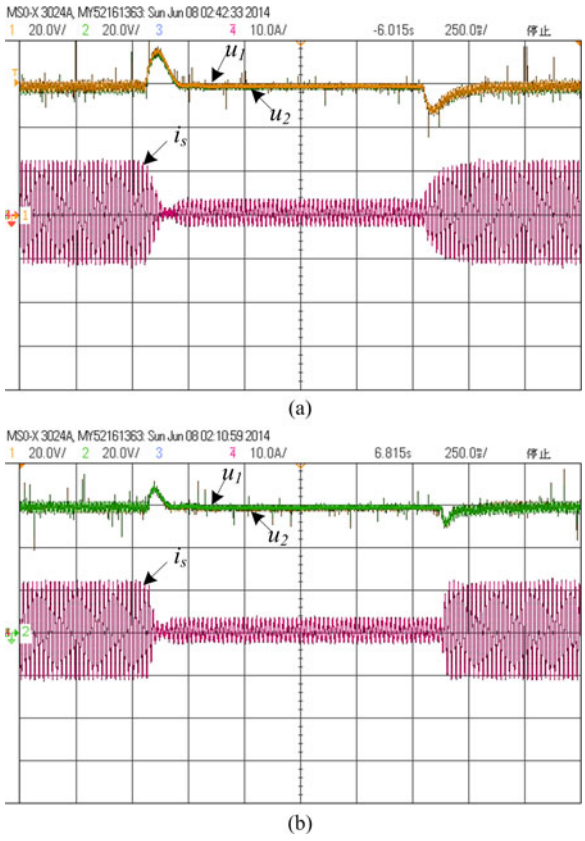

Fig. 17. Experimental waveforms of dynamic response of dc-link voltages under load sudden change condition (u_1 and u_2: 20 V/div, i_s : 10 A/div, time: 250 ms/div). (a) PI-based DPC. (b) Deadbeat predictive DPC.

deadbeat predictive DPC can still be achieved. Experimental results shown in Fig. 19 also illustrate that dynamic response of the adopted deadbeat predictive DPC is not sensitive to the ac-side inductance. Moreover, comparing with Figs. 19 and 16(b), it is clear that there is a little bit fluctuation in reactive power waveform at the sudden power change instant, while the inductor value error $(L_m - L)/L$ is 50% or -50%. Therefore, the reactive power is a little sensitive to the ac-side inductance.

VI. Conclusion

In this paper, a deadbeat predictive DPC scheme for single-phase three-level NPC converters is proposed. And a new single-phase three-level SVPWM with inherent neutral-point voltage balancing capability is adopted to balance dc-link capacitor voltages and generate gate PWM signals of this converter. By comparing the performance of the proposed control scheme with that of conventional PI-based DPC approach in simulation and experiment tests, the conducted studies conclude that the salient features of deadbeat predictive DPC and single-phase three-level SVPWM strategies are as follows:

1) the deadbeat predictive DPC scheme is free of complicated multiple PI controllers design, and does not depend on the main voltage orientation;

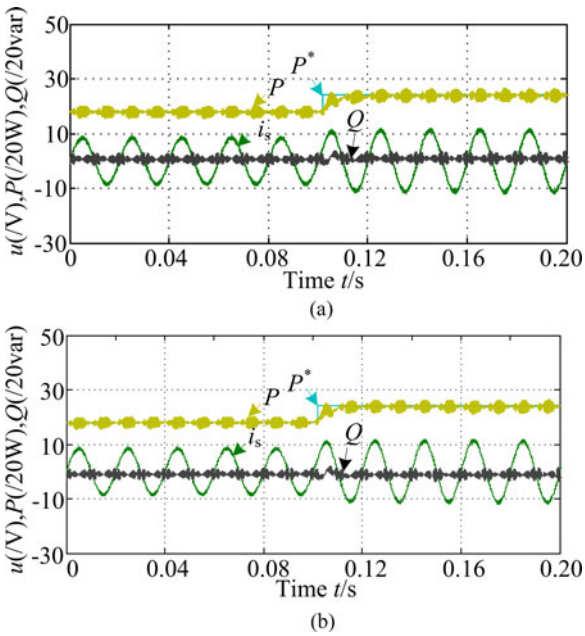

Fig. 18. Simulation waveforms of dynamic response of active and reactive powers regulation under power sudden change from 75% to 100% rating value condition. (a) Deadbeat predictive DPC ($L_m/L = 0.5$, $L_m = 2.5$ mH). (b) Deadbeat predictive DPC ($L_m/L = 1.5$, $L_m = 7.5$ mH).

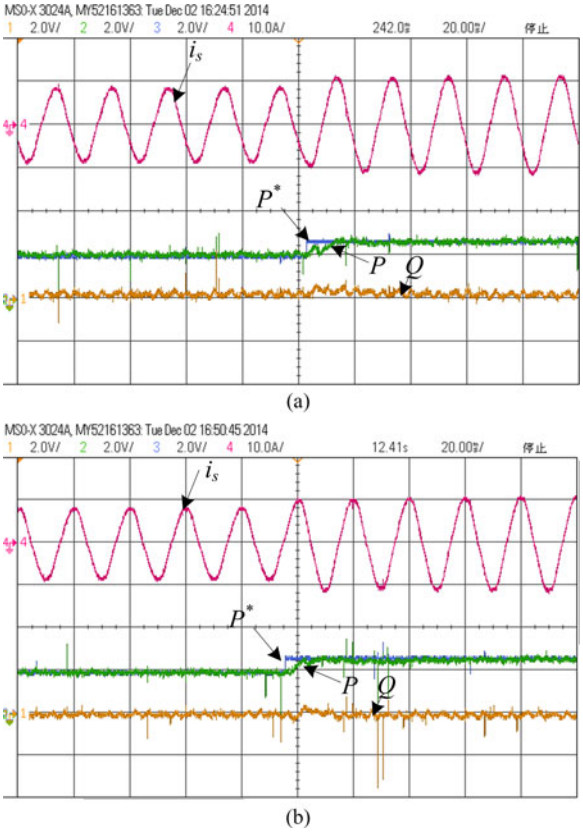

Fig. 19. Experimental waveforms of dynamic response of active and reactive powers regulation under power sudden change from 75% to 100% rating value condition (P and P^* : 360 W/div, Q : 360 var/div, i_s : 10 A/div, time: 20 ms/div). (a) Deadbeat predictive DPC ($L_m/L = 0.5$, $L_{\rm m} = 2.5$ mH). (b) Deadbeat predictive DPC ($L_m/L = 1.5$, $L_m = 7.5$ mH).

2) the deadbeat predictive DPC scheme can reduce current harmonics components and THD, and active and reactive power ripples, significantly;
3) the deadbeat predictive DPC scheme can easily achieve fast dynamic response for power and dc-link voltages;
4) the single-phase three-level SVPWM scheme can achieve neutral-point voltage balancing effectively, and guarantee that the high-order current harmonics concentrates on the multiples of switching frequency, which facilitates the filter design easily.

A performance comparison of conventional PI-based and deadbeat predictive DPC schemes is summarized shown in Table II. It is worthwhile to note that: in this comparison, the parameters of active and reactive power PI controllers in PI-based DPC scheme are not optimized. If the parameters of the conventional PI controllers are optimized, or advanced PI controllers such as slide-mode PI, self-adaptive PI, etc., are adopted, the PI-based DPC scheme could also obtain fast dynamic response like as the deadbeat predictive DPC. Therefore, the proposed deadbeat predictive DPC is an alternative control method for single-phase converters, whose performance could be equivalent to that of PI-based DPC methods with parameters optimization.

Moreover, the proposed deadbeat predictive DPC scheme and SVPWM methods are also desirable for single-phase three-level NPC UPS inverter or solar inverter applications.

TABLE II
PERFORMANCE COMPARISON AND SUMMARY OF TWO DPC SCHEMES

Performances	Control schemes	
	Conventional PI-based DPC	Deadbeat predictive DPC
Dynamic response	slow	fast
Current harmonics (% THD)	high	low
Number of PI controllers	3	1
Parameter design of PI controllers	complicated	easy
Is the main voltage orientation required?	yes	no

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