Avoiding Si MOSFET Avalanche and Achieving Zero-Voltage Switching for Cascode GaN Devices

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***Abstract*—The cascode structure is widely used for high-voltage normally-on wide-bandgap devices. However, the interaction between the high-voltage normally-on device and the low-voltage normally-off Si MOSFET may induce undesired features. This paper analyzes the voltage distribution principle during the turn-off transition as well as the zero-voltage-switching (ZVS) principle during the turn-on transition for cascode GaN devices. The capacitance mismatch between high-voltage normally-on GaN switch and the low-voltage Si MOSFET causes the Si MOSFET to avalanche, and internal high-voltage GaN switch lose the ZVS condition. This issue must be solved in consideration of both power loss and reliability. A simple and effective solution is proposed by adding an extra capacitor to compensate the capacitance mismatch, thereby avoiding Si MOSFET avalanche and achieving true ZVS for cascode GaN devices. The benefits and small penalty of this solution are analyzed in detail. The theoretical analysis is validated by experiments, which are implemented based on a 600-V cascode GaN device. The experiment shows that the proposed method improves the 600-V cascode GaN devices performance significantly in high-frequency applications. The analysis and proposed solution are also applicable to other cascode devices.**

***Index Terms*—Avalanche, wide-bandgap, cascode, zero-voltage switching (ZVS).**

I. Introduction

WITH the ever increasing power demands of modern systems, as well as the desire for smaller size and lower power consumption, high power density, and high efficiency are the key drivers and metrics for the advancement of power conversion technologies. The most straightforward way to increase power density is to increase the switching frequency in order to reduce the passive component volume. However, higher switching frequency is seemingly at the detriment of efficiency when using silicon-based devices. As a result, the switching frequency can barely be pushed to hundreds of kilohertz due to the power loss consideration. In recent years, wide-bandgap devices, especially gallium nitride (GaN) devices, have emerged as a promising way to replace silicon devices due to a better figure of merit [1]–[7]. GaN devices have a much lower gate charge and lower output capacitance, and therefore, are capable of operating at a considerably higher switching frequency than that of the silicon MOSFET while maintaining high efficiency.

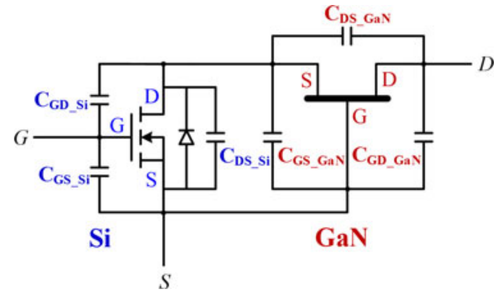

Fig. 1. Cascode structure for a high-voltage deletion mode wide-bandgap device.

The high-voltage GaN devices can be categorized into two types defined by their operation mode: enhancement mode (normally-off) and depletion mode (normally-on). Compared to the enhancement mode GaN devices, the depletion mode GaN devices usually have lower on-resistance and smaller junction capacitance, therefore, are deemed more attractive for applications that require high efficiency. To easily apply a high-voltage depletion mode GaN switch in a circuit design, a low-voltage Si MOSFET is used in series to drive the GaN switch. This configuration is known as cascode structure [8], and is shown in Fig. 1 with all junction capacitors.

In the cascode configuration, the Si MOSFET controls the ON/OFF state of the GaN switch. The interaction between the two devices may result in instability due to the large package parasitic inductance [9]. However, an advanced package method, such as the chip-on-chip technique, can dramatically reduce the package inductance and avoid instability [10]. On the other hand, the junction capacitors of the two devices play an important role to achieve high efficiency, especially under soft-switching conditions. The voltage distribution between the GaN switch and Si MOSFET during the turn-off transition is majorly determined by the junction capacitor charge. In some circumstances, the Si MOSFET may reach avalanche, which would cause additional loss and reliability concerns. The zero-voltage-switching (ZVS) turn-on transition is the reverse procedure of voltage distribution during the turn OFF transition. The GaN switch cannot achieve ZVS when the Si MOSFET reaches avalanche during the turn OFF transition, even when the external waveform of the cascode device looks like ZVS. A detailed analysis of this process is shown in Section II.

This paper aims to analyze the voltage distribution and ZVS turn-on principle of cascode devices. The junction capacitance

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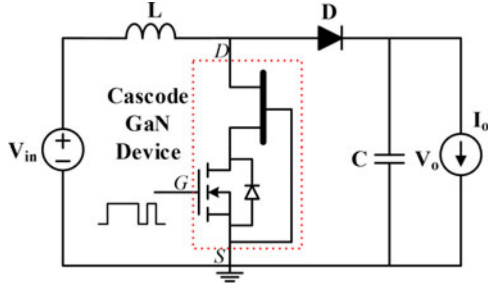


Fig. 2. Boost converter with cascode GaN device.

mismatch causes the Si MOSFET to avalanche and the internal GaN switch to lose ZVS, as shown in Section II. A simple, effective solution is proposed in Section III, where an external capacitor is added in parallel with the drain–source of the Si MOSFET to avoid avalanche and achieve true ZVS for cascode devices. Finally, the theoretical analysis is validated by experimental results in Section IV.

II. Voltage Distribution and ZVS Turn ON Principle of Cascode Device

To analyze the voltage distribution and ZVS turn ON principle of a cascode device, a boost converter is used as an example. The bottom switch is the cascode GaN device shown in Fig. 2.

A. Voltage Distribution Principle of Cascode GaN Devices During Turn-OFF Transition

The voltage distribution process is determined by the turn-off sequence of the cascode GaN device. There are two possible turn-off transitions in the cascode GaN device, which are shown in Fig. 3. The waveforms are derived from simulation models of two different cascode GaN devices. V_{GS} is the gate signal applied on the gate–source terminal of the cascode GaN device. $V_{\mathrm{DS_Si}}$ and $V_{\mathrm{DS_GaN}}$ are the drain–source voltage of the Si MOSFET and GaN switch, accordingly. It is apparent that the gate–source voltage of the GaN switch is the same as the drain–source voltage of the Si MOSFET with reverse polarity. The difference in waveforms between these two cascode devices is determined by whether the Si MOSFET is driven to avalanche. The definition of a well-matched cascode GaN device is that the charge stored in $C_{\mathrm{DS_GaN}}$ is lower than the charge stored in $\mathrm{C_{OSS\text{-}Si}}$ and $C_{\mathrm{GS_GaN}}$, where $C_{\mathrm{oss_Si}}$ is the sum of $C_{\mathrm{DS_Si}}$ and $C_{\mathrm{GD_Si}}$. Similarly, a mismatched cascode GaN device means the charge of $C_{\mathrm{DS_GaN}}$ is larger than the charge of $C_{\mathrm{oss_Si}}$ and $C_{\mathrm{GS_GaN}}$. To better illustrate the voltage distribution process, the equivalent circuits during t_1–t_4 are shown in Fig. 4. The stage III equivalent circuit only exists in the mismatched cascode GaN device. The inductor current is treated as a current source during the turn-off transition period.

The turn-off signal is applied to the gate terminal of the Si MOSFET at t_0, and the MOSFET channel is turned OFF at t_1. Then, $C_{\mathrm{oss_Si}}$ and $C_{\mathrm{GS_GaN}}$ are charged in parallel through the channel of the GaN switch until the source–gate voltage of the GaN switch rises to its threshold voltage $V_{\mathrm{TH_GaN}}$ at t_2. Then, the GaN switch is turned OFF, and $C_{\mathrm{DS_GaN}}$ is charged in series with $C_{\mathrm{oss_Si}}$ and $C_{\mathrm{GS_GaN}}$. The charging path through $C_{\mathrm{GD_GaN}}$ has no impact on the voltage distribution between the GaN switch and the Si MOSFET. For a well-matched cascode device, the terminal current charges these capacitors until the voltage reaches steady state. $V_{\mathrm{DS_Si}}$ reaches V_1, which is lower than avalanche value V_{av}, and $V_{\mathrm{DS_GaN}}$ rises to $V_O - V_1$. The turn-off transition is completed at t_3.

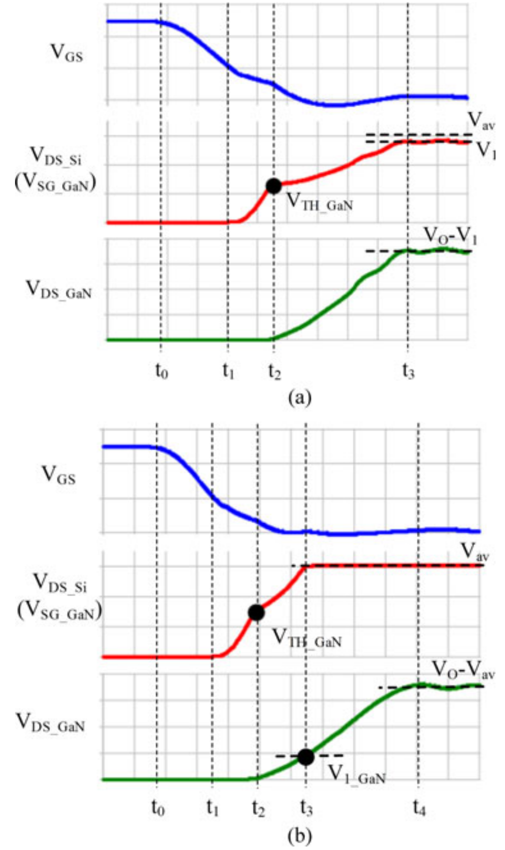


Fig. 3. Two possible turn-off transition of cascode GaN devices. (a) Turn-off transition of well-matched cascode device. (b) Turn-off transition of mismatched cascode device.

For a mismatched cascode GaN device, $V_{\mathrm{DS_Si}}$ is driven to avalanche at t_3, while $V_{\mathrm{DS_GaN}}$ only rises to $V_{1_{\mathrm{GaN}}}$, which is quite a bit lower than the steady-state value. During Stage II, the total amount of charge stored in $C_{\mathrm{oss_Si}}$ and $C_{\mathrm{GS_GaN}}$ is defined as Q_{II}. There is the same amount of charge stored in $C_{\mathrm{DS_GaN}}$, since they are in series on the current path. During Stage III, the Si MOSFET stays in the avalanche region. $C_{\mathrm{DS_GaN}}$ is charged independently through the avalanche path as shown in Fig. 4(c), and the $V_{\mathrm{DS_GaN}}$ rises from V_{1_GaN} to the steady-state value. The total amount of charge stored in $C_{\mathrm{DS_GaN}}$ during Stage III is defined as Q_{III}. The same charge flows through the avalanche path, which causes additional loss in every switching cycle. This part of the loss is defined as P_{av} and can be quantified as follows, where f_s is the switching frequency:

$$P_{\mathrm{av}} = V_{\mathrm{av}} \times Q_{III} \times f_s. \quad (1)$$

According to the aforementioned equation, P_{av} is proportional to the switching frequency. This is undesirable, especially in the high-frequency application.

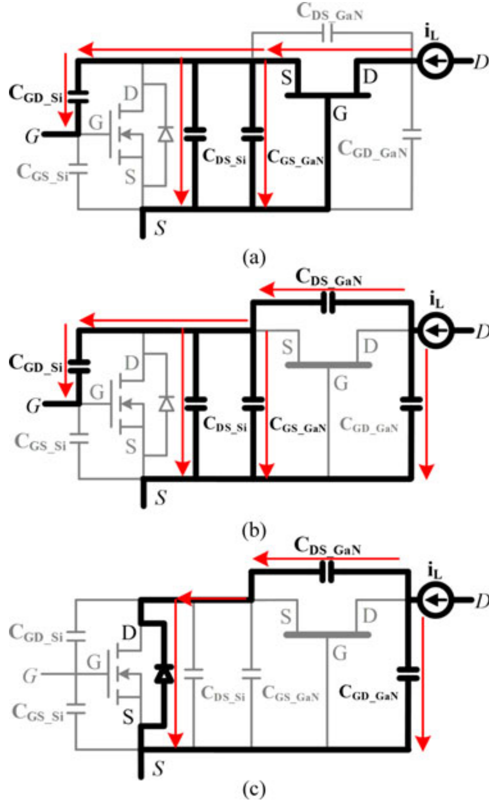


Fig. 4. Voltage distribution of cascode device during turn OFF period (a) Stage I: t_1–t_2 (b) Stage II: t_2–t_3 (c) Stage III: t_3–t_4 (only in mismatched cascode device).

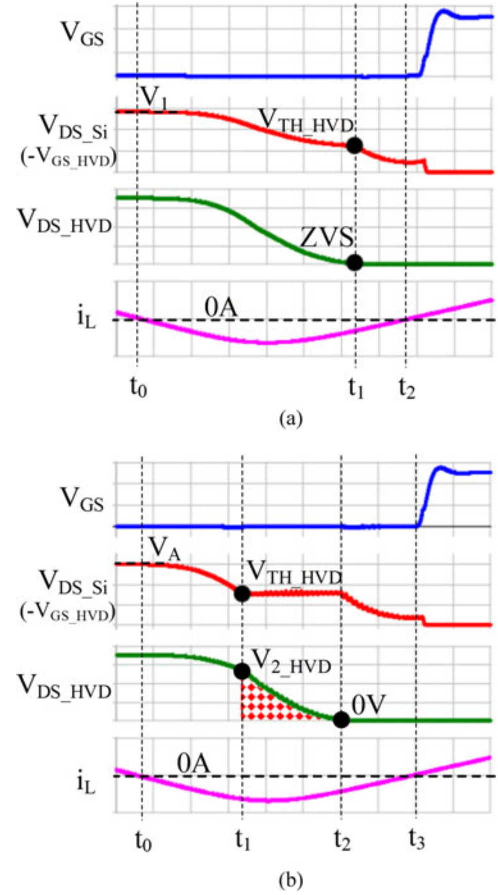


Fig. 5. Two possible ZVS turn ON transition of cascode GaN device. (a) ZVS Turn ON transition of well-matched cascode device (b) ZVS turn ON transition of mismatched cascode device.

B. ZVS Turn-On Principle of Cascode GaN Devices

Similar to the turn-off transition, there are two possible ZVS turn-on transitions in a cascode GaN device, which are shown in Fig. 5. The negative inductor current is used to discharge the junction capacitors to achieve ZVS. The waveform difference between these two cascode devices is whether the $V_{\mathrm{DS_GaN}}$ drops to zero when $V_{\mathrm{DS_Si}}$ drops to $V_{\mathrm{TH_GaN}}$. The equivalent circuits are shown in Fig. 6. The mismatched cascode GaN device has one more stage than the well-matched case.

At t_0, the negative inductor current begins to discharge the junction capacitors. $C_{\mathrm{DS_GaN}}$ is discharged in series with $C_{\mathrm{oss_Si}}$ and $C_{\mathrm{GS_GaN}}$ from the initial condition. For the well-matched cascode device, $V_{\mathrm{DS_Si}}$ decreases from initial value V_1 to $V_{\mathrm{TH_GaN}}$ at t_1. Meanwhile, $V_{\mathrm{DS_GaN}}$ drops from initial value $V_O - V_1$ to zero due to the charge balance. This stage is the reverse process of voltage distribution during the turn-off transition. The total amount of charge stored in $C_{\mathrm{DS_GaN}}$ as well as $C_{\mathrm{oss_Si}}$ and $C_{\mathrm{GS_GaN}}$ is completely recycled to the input source. After $V_{\mathrm{DS_Si}}$ reaches $V_{\mathrm{TH_GaN}}$, GaN switch is turned ON and the remaining charge stored in $C_{\mathrm{oss_Si}}$ and $C_{\mathrm{GS_GaN}}$ is continuously discharged by the inductor current as shown in Fig. 6(c).

For a mismatched cascode device, since the charge stored in the GaN switch is much larger than the charge stored in the Si MOSFET, $V_{\mathrm{DS_GaN}}$ only decreases to V_{2_GaN} when $V_{\mathrm{DS_Si}}$ decreases to $V_{\mathrm{TH_GaN}}$ at t_1. The total charge being discharged during Stage I is Q_{II}, which is exactly the charge stored during the turn-off in Stage II.

After $V_{\mathrm{DS_Si}}$ decreases to $V_{\mathrm{TH_GaN}}$, the channel of the GaN switch begins to conduct during Stage II, as shown in Fig. 6(b). The remaining charge of $C_{\mathrm{DS_GaN}}$, which is Q_{III}, is dissipated through the channel directly, and this induces additional turn-on loss that is proportional to the switching frequency. During Stage II, the voltage decrease slopes of $C_{\mathrm{DS_GaN}}$ and $C_{\mathrm{GD_GaN}}$ are consistent. The majority of the inductor current flows through $C_{\mathrm{GD_GaN}}$, and the circuit satisfies the following equations:

$$\begin{cases} v_{\mathrm{DS_GaN}} + v_{\mathrm{DS_Si}} = v_{\mathrm{GD_GaN}} \\ C_{\mathrm{GD_GaN}} \dfrac{dv_{\mathrm{GD_GaN}}}{dt} = i_L \\ C_{\mathrm{DS_GaN}} \dfrac{dv_{\mathrm{DS_GaN}}}{dt} = g_{f_\mathrm{GaN}}(-v_{\mathrm{DS_Si}} - V_{\mathrm{TH_GaN}}) \end{cases} \quad (2)$$

where g_{f_GaN} is the transconductance of GaN switch. A small decrease in $V_{\mathrm{DS_Si}}$ results in a large increase of the GaN switch displace current, which leads to a fast voltage decrease slope. Therefore, $V_{\mathrm{DS_Si}}$ stays almost constant during this stage to maintain a consistent voltage slope, which is shown in Fig. 5(b). The waveform of $V_{\mathrm{DS_GaN}}$ makes the terminal waveform of the cascode GaN device appear to have ZVS turn-on. However, part

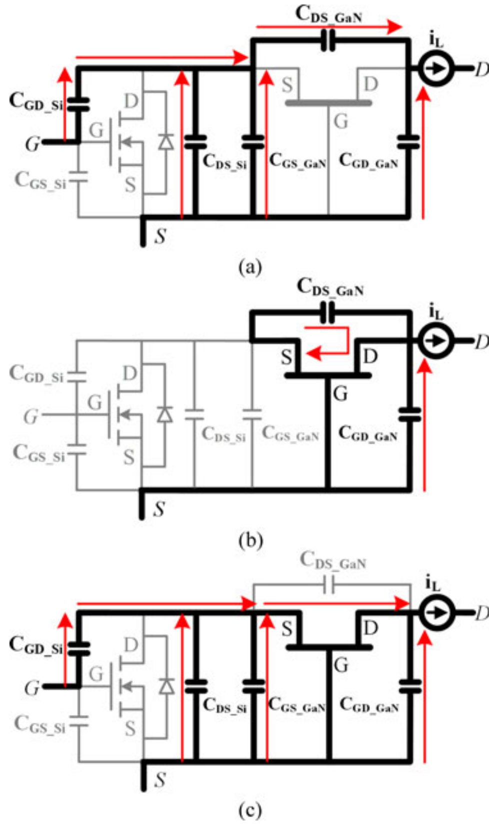


Fig. 6. Voltage distribution of cascode device during turn ON period. (a) Stage I: $t_0 \sim t_1$. (b) Stage II: $t_1 \sim t_2$ (only in mismatched cascode device). (c) Stage III: $t_1 \sim t_2$ (in well-matched cascode device), or $t_2 \sim t_3$ (in mismatched cascode device).

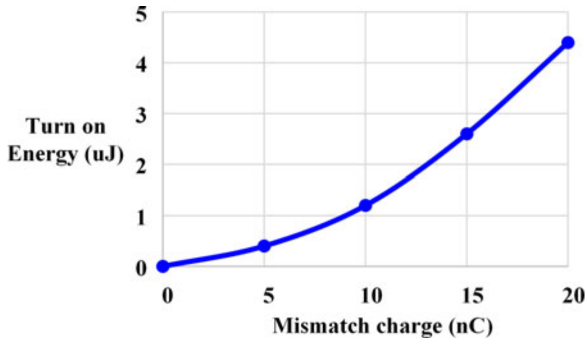


Fig. 7. Relationship of internal turn-on switching loss and mismatch charge.

of the energy stored in $C_{\mathrm{DS_GaN}}$ is actually dissipated internally due to a mismatch in charge. This phenomenon always occurs, no matter what kind of ZVS techniques are applied. The internal switching loss is related to the mismatch charge, and Fig. 7 shows the relationship, which is derived from simulation. For the cascode GaN device used in experiments shown in Section IV, the GaN device rating is 600 V/12 A and the Si MOSFET rating is 30 V/11 A. The mismatch charge is around 10.5 nC.

Overall, the junction capacitance mismatch of the Si MOSFET and the GaN switch in a cascode structure will cause the Si

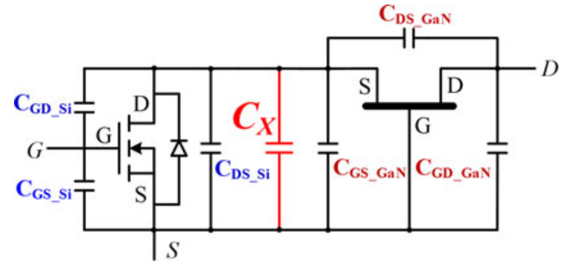


Fig. 8. Adding extra capacitor in cascode device.

MOSFET to reach avalanche and lose ZVS of the GaN switch even when a ZVS technique is applied. The avalanche loss and internal GaN switch turn-on loss are proportional to the switching frequency and related to mismatched charge. These prevent the cascode GaN device from being applicable to megahertz frequency applications, and the additional power loss may impact the thermal condition of the device. Therefore, this issue must be solved for reasons of both efficiency and reliability.

III. Proposed Solution to Avoid Si MOSFET Avalanche and Achieve True ZVS for Cascode GaN Devices

The most straightforward method to prevent the Si MOSFET from reaching avalanche is to select an appropriate Si MOSFET with a larger junction capacitance according to the junction capacitance of the GaN switch. However, the total gate charge of the Si MOSFET will also increase, which will increase the driving loss significantly at high frequency. Moreover, the increase of $C_{\mathrm{GD_Si}}$ will elongate the Si MOSFET turn-off transition and increase switching loss due to a strong miller effect. Therefore, selecting a Si MOSFET with proper capacitance is not the most effective solution.

This paper proposes a convenient method to compensate the mismatch charge of the junction capacitance of a Si MOSFET and GaN switch in a cascode structure. Based on the analysis in Section II, the total mismatch charge in the cascode device is Q_{III}. Therefore, an additional capacitance C_X is added in parallel with the drain–source terminals of the Si MOSFET to compensate the charge mismatch, as shown in Fig. 8. The required minimum value of C_X should guarantee that $C_{\mathrm{DS_GaN}}$ achieves its steady-state voltage before the Si MOSFET reaches avalanche. Therefore, the expression of C_X is as follows:

$$C_X \geq \frac{Q_{III}}{V_{\mathrm{av}} - V_{\mathrm{TH_GaN}}}. \quad (3)$$

Paralleling C_X between the drain–source terminals of the Si MOSFET will not increase its driving loss, and the turn OFF loss is still very small due to the merit of the cascode structure, as mentioned in [11]. The impact of an extra capacitor on the turn-off loss is shown in Fig. 9, which is derived from simulation. The cascode GaN used in the simulation is same with the one used in the experiment shown in Section IV. The GaN device rating is 600 V/12 A and the Si MOSFET rating is 30 V/11 A. The mismatch charge is around 10.5 nC. The turn OFF current is

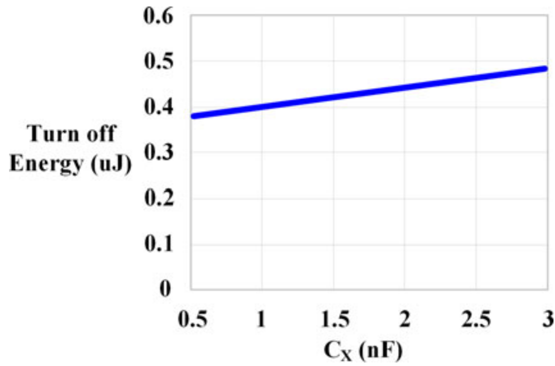


Fig. 9. Impact of an extra capacitor on turn-off switching loss.

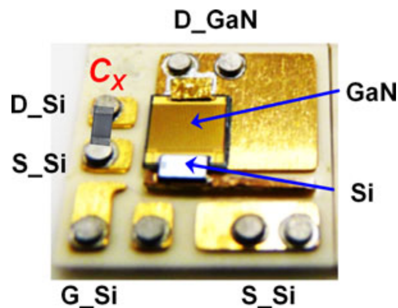
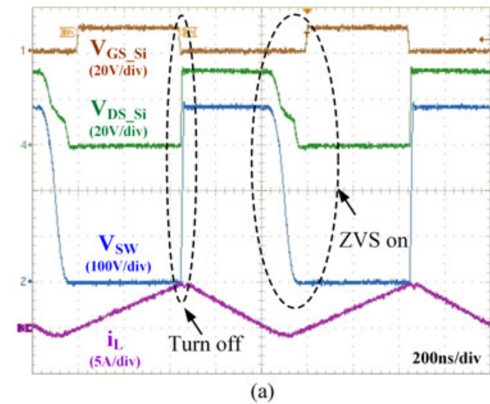


Fig. 10. Chip-on-chip package for cascode GaN device with an extra capacitor.

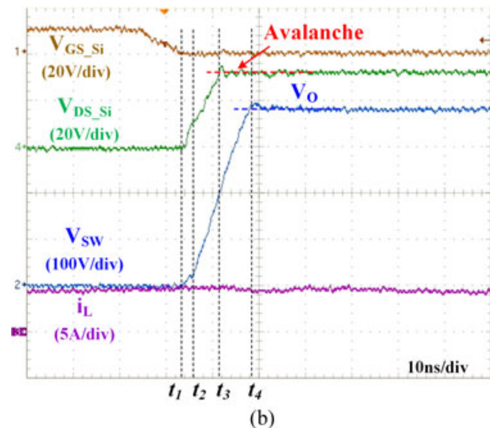
10 A and turn OFF steady-state voltage is 380 V in the simulation. The data indicate a little increase in turn OFF loss due to this extra capacitor.

The proposed solution is a simple and effective way to compensate the mismatch charge of the Si MOSFET and the GaN switch, and it is convenient for mass production. Moreover, the proposed method improves the device performance and can be used in any topology with any ZVS technique.

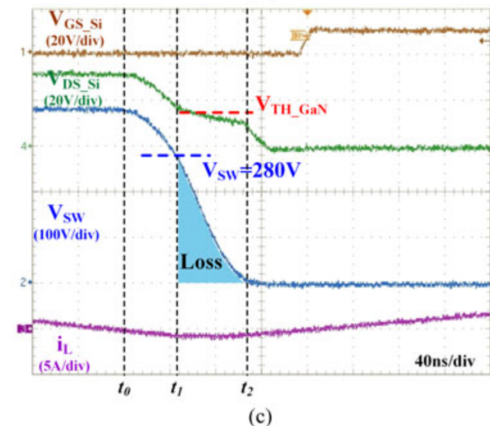
It is noticed that the aforementioned issues may not occur at low-voltage condition, such as below 200-V application. The proposed solution may slow down the device switching speed, but with very limited increase of turn OFF switching loss. Generally speaking, the proposed solution is targeting to solve the issues for the 600–1200 V rating cascode devices, which are generally used in 400–800 V application.



(a)



(b)



(c)

Fig. 11. Experimental waveforms without adding extra capacitor. (a) Steady-state waveform. (b) Detailed turn OFF transition. (c) Detailed ZVS turn ON transition.

IV. Experimental Verification and Discussion

A 600-V cascode GaN device is used in a 1-MHz 180-V /380-V critical current mode (CRM) boost converter to verify the analysis of the mismatch charge impact on the voltage distribution and ZVS turn-on performance. To easily integrate an extra capacitor into the cascode device, a chip-on-chip package is fabricated, as shown in Fig. 10. The 600-V normally-on GaN chip is provided by Transphorm Inc. The threshold voltage is around −15 V and the maximum source–gate voltage is around −35 V. Therefore, a 30-V Si MOSFET is selected to control the ON/OFF state of the GaN as well as to protect the GaN gate by clamping the source–gate voltage of the GaN to the avalanche value of the Si MOSFET, which is 30 V. Another criterion for choosing the Si MOSFET is to minimize the driving loss at high frequency. Therefore, the junction capacitance of this 30-V Si MOSFET is usually small, and the charge of the GaN and the Si MOSFET are mismatched. The estimated mismatch charge is about 10 nC, and therefore, an 800-pF capacitor is added according to (3). The comparisons of the behavior of cascode GaN device with and without an extra capacitor during the turn-on and turn-off transition are shown in Figs. 11 and 12.

Fig. 11 shows the experimental waveform without adding the extra capacitor. Fig. 11(b) and (c) show the detailed turn OFF and ZVS turn ON transition, respectively. $V_{\rm SW}$ is the terminal

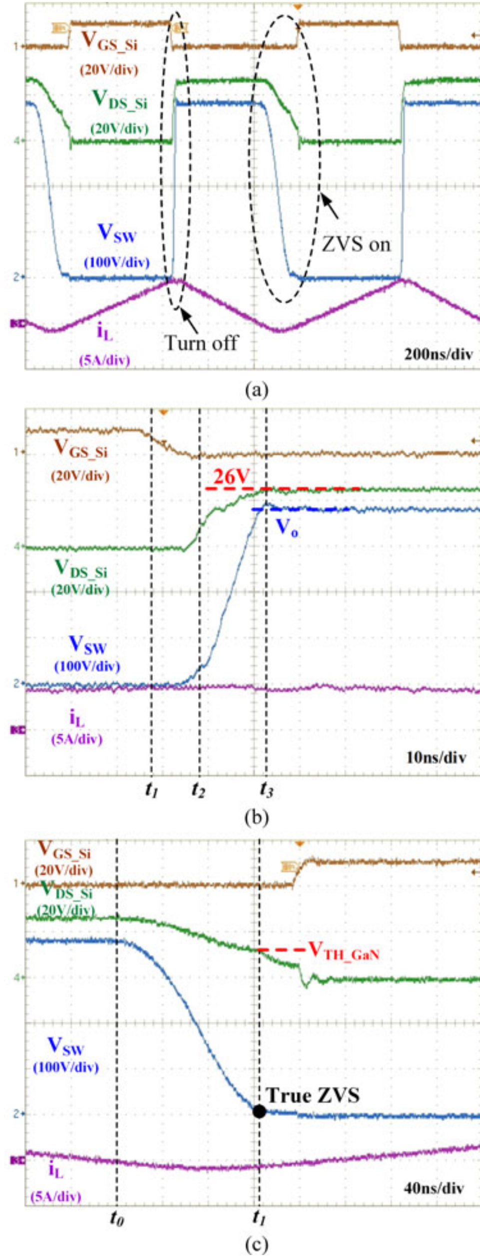


Fig. 12. Experimental waveforms with extra capacitor. (a) Steady-state waveform. (b) Detailed turn OFF transition. (c) Detailed ZVS turn ON transition.

voltage across the cascode GaN device. During the turn-off transition, $V_{\mathrm{DS_Si}}$ reaches avalanche at t_3, while the terminal voltage V_{SW} only rises to 170 V. After t_3, $C_{\mathrm{DS_GaN}}$ is continuously charged through the avalanched path until V_{SW} reaches V_{O} at time t_4. The mismatch charge is about 10.5 nC in this cascode GaN device. According to (1), the avalanche loss P_{av} is 0.315 W at 1 MHz. This part of the loss is considerable at high frequency.

During the ZVS turn-on transition, $V_{\mathrm{DS_Si}}$ decreases to $V_{\mathrm{TH_GaN}}$ at t_1, while the terminal voltage only drops to around 280 V. The remaining energy stored in $C_{\mathrm{DS_GaN}}$ is dissipated through the GaN channel. The internal non-ZVS loss is estimated to be about 1.2 W at 1 MHZ. Therefore, the total power

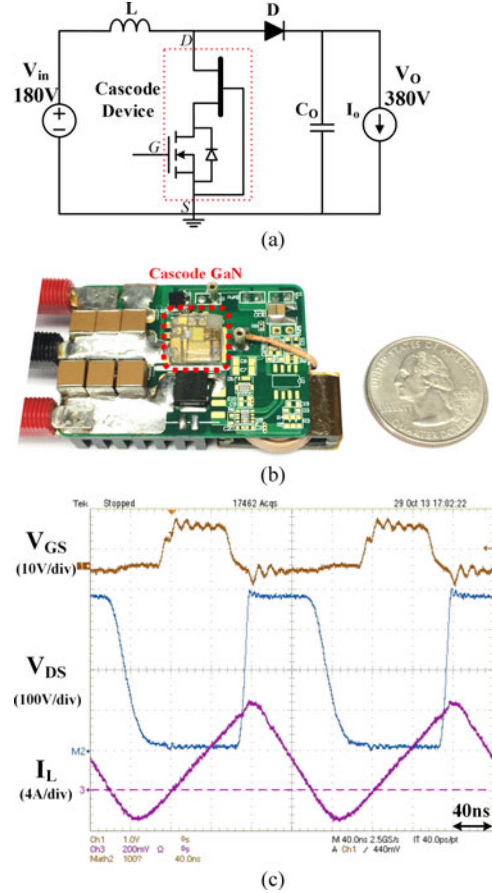


Fig. 13. Demonstration of 5-MHz boost converter with cascode GaN device. (a) Boost Converter cascode GaN device. (b) Prototype of 5-MHz boost converter with cascode GaN device. (c) Experimental waveforms of 5-MHz boost converter.

loss caused by junction capacitor mismatch in this cascode GaN device is about 1.5 W at 1 MHz.

Fig. 12 shows the experimental waveform with the extra capacitor. Fig. 12(b) and (c) show the detailed turn-off and ZVS turn-on transition, respectively. Fig. 11(b) shows that $V_{\mathrm{DS_Si}}$ rises to 26 V when the terminal voltage reaches steady-state condition. Therefore, adding this capacitor can effectively avoid Si MOSFET reaching avalanche. Fig. 11(c) shows that the terminal voltage drops to nearly zero when $V_{\mathrm{DS_Si}}$ drops to $V_{\mathrm{TH_GaN}}$. Therefore, real ZVS can be achieved for the cascode GaN device by adding this capacitor.

It is worthwhile to point out that the extra capacitor does not impact the driving loss based on the loss measured from the driving circuit. Moreover, the total loss reduction of the prototype with the extra capacitor is about 1.5 W at 1 MHz, which can match with the estimated loss induced by avalanche and internal non-ZVS issues. The loss reduction also indicates that the increase in turn OFF loss due to the extra capacitor is negligible.

With proposed solution, the cascode GaN device could achieve very high efficiency with soft-switching technique, and therefore, allow much higher operation frequency. Fig. 13 demonstrates a 5-MHz CRM boost converter prototype and

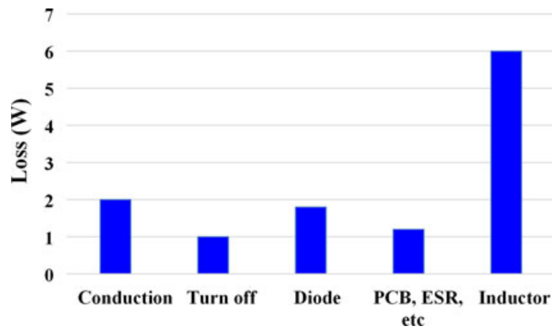


Fig. 14. Loss breakdown of 5-MHz boost converter with cascode GaN device.

experimental waveforms with cascode GaN device integrated the extra capacitor. The converter can achieve 98% efficiency and 1000 W/in^3 power density at 600-W output conditions. The loss breakdown at 600-W output condition is shown in Fig. 14. The largest share of the loss part is the inductor winding loss, which occurs due to the skin effect and fringe effect, and can be measured using Dr. Mu's method described in [12]. The measured cascode GaN switch temperature is about 45 °C, which indicates the total loss of this device is below 3 W.

V. Conclusion

The cascode structure is widely used in high-voltage normally-on GaN devices to make circuit design easy and to make them compatible with commercial gate drives. However, the charge mismatch of the junction capacitor in the cascode device will force a low-voltage Si MOSFET to reach avalanche at the turn-off transition, and internally lose ZVS for GaN switch at the soft switching turn-on transition. The avalanche and internal switching loss is considerable at high frequency for cascode GaN device, which should be solved for high-frequency operation.

This paper proposes a simple and effective solution to avoid Si MOSFET avalanche and achieve true ZVS for cascode GaN devices. An external capacitor is added in parallel with the drain–source of the Si MOSFET to compensate the capacitance mismatch between the GaN switch and the Si MOSFET. The proposed method can effectively solve the issue with a minor penalty of a small increase in turn-off loss. The theoretical analysis is validated by experiments, which are implemented based on the 600-V cascode GaN device. The experiments show that the proposed method improves the 600-V cascode GaN devices performance dramatically in 1-MHz applications. The benefits of the proposed method will be more significant at higher frequency.

It should be pointed out that the mismatch phenomenon may not occur at lower voltage condition. The proposed method may slow down the switching speed but with very limited increase of the turn off loss. Overall, the proposed method could solve the issues of the cascode device at high-voltage condition, but do not increase the switching loss much at low-voltage condition.

It is worthwhile to point out that the theoretical analysis and proposed solution are applicable to all kind of cascode devices.

Acknowledgment

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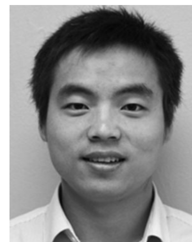

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