An Analytical Switching Process Model of Low-Voltage eGaN HEMTs for Loss Calculation

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***Abstract*—This paper proposes an improved analytical switching process model to calculate the switching loss of low-voltage enhancement-mode Gallium Nitride high-electron mobility transistors (eGaN HEMTs). The presented eGaN HEMTs models are more or less derived from silicon MOSFETs models, whereas eGaN HEMTs are different from three aspects: higher switching speed, much more reduced parasitic inductance in switching loop, and absence of reverse recovery. Applying the traditional model to eGaN HEMTs results in inaccurate prediction of switching waveforms and losses. The proposed model considers the effect of low-parasitic inductances, nonlinearity of junction capacitances, and nonlinearity of transconductance. The turn-on and turn-off switching processes are described in detail and the resulting equations can be easily solved. The accuracy of the proposed model is validated by comparing the predicted switching waveforms and converter's efficiency with the experimental results, respectively. Based on the analytical model, the effects of gate resistance, gate supply voltage, and parasitic inductances on switching losses are investigated. Meanwhile, a novel current measuring method based on magnetic coupling is proposed to measure the switching current waveform with improved accuracy.**

***Index Terms*—Analytical model, current measurement, gallium nitride (GaN), switching loss.**

I. Introduction

In recent years, Gallium Nitride high-electron-mobility transistors (GaN HEMTs) have emerged as a kind of promising devices for high efficiency and high density power conversion [1]–[6]. They have a higher switching speed and lower switching loss, comparing with the state-of-the-art silicon MOSFETs. Therefore, the switching frequency has been continuously pushed up to several megahertz to reduce the size of passive components and, therefore, increase power density [7]–[12].

On the other hand, the switching loss increases as the switching frequency increases. When the switching frequency is very high, the switching loss dominates the total power loss and limits the ability to further increase the switching frequency. We need an accurate switching process model to have a deep insight into the switching process, and therefore, the circuit parameters can be optimized to reduce the switching loss. What's more, an accurate switching process model that estimates switching loss is highly desirable for predicting maximum junction temperatures and overall power converter's efficiency.

To have a good understanding of the switching process, various types of models have been reported within these years. One of the most popular analytical loss models is the piecewise linear model presented in [13] and [14]. The model enables simple and rapid estimation of switching loss. However, the parasitic inductances and the nonlinearity of the junction capacitances of the device are not taken into account. Therefore, the results generally do not match very well with the experimental results, especially for high-frequency applications. More comprehensive analytical loss models based on silicon MOSFETs are presented in [15]–[21]. These models consider the nonlinearity of the junction capacitance and the parasitic inductance. The experimental results prove that these models are more accurate than the piecewise linear model. Nevertheless, these models are still not suitable for enhancement-mode Gallium Nitride (eGaN) HEMTs. First, the reverse recovery of silicon MOSFETs has a great effect on switching transition and switching loss. However, eGaN HEMTs have no such reverse recovery characteristics. Second, when an eGaN HEMT is turned ON/OFF, the drain–source voltage changes very fast (about 20 V/ns according to [22]), resulting in a large current flowing through the parasitic capacitances of the GaN HEMT. The current cannot be neglected because it is comparable with the load current. Unfortunately, the models based on silicon MOSFETs neglect this current for simplicity. Third, parasitic inductance in a well-layout GaN HEMTs circuit is typically less than 1 nH [9], [23], which is far smaller than that in silicon MOSFET circuit. So, some assumptions and simplifications in silicon models are not suitable for GaN HEMTs model. Reusch applies the silicon model presented in [17] to GaN HEMTs with some modifications in his dissertation [24]. The model assumes a constant transconductance and does not distinguish the channel current from the drain current for simplification, which results in some inaccuracy prediction of the switching waveforms and losses. Recently, an analytical loss model is proposed for GaN HEMTs [25], [26]. But the model is fit for a high-voltage depth-mode GaN HEMT with a low-voltage silicon MOSFET in series to drive the GaN HEMT, which in turn makes the switching transition different from that of low-voltage eGaN HEMTs. Therefore, an accurate analytical model of low-voltage eGaN HEMTs is required.

As for the demonstration method, there are two effective methods to validate the accuracy of the proposed analytical model. One is to measure a converter's efficiency, and the other

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is to compare the switching waveforms (the drain current and drain–source voltage) between the analytical model and experiment. However, there is a lack of papers that could accurately match the analytical switching waveforms with experimental waveforms for a low-voltage silicon MOSFET or GaN HEMT. The reported models are inaccurate because of excessive simplification. Meanwhile, it is very difficult to accurately measure the switching current. In [22] and [25], a resistor is employed to measure the drain current. However, the result is not accurate because of the effect of the series parasitic inductance at a very high ringing frequency (about 200 MHz). Even worse, the resistance changes with frequency, which has been analyzed in [22].

Based upon that consideration, this paper aims to propose an accurate analytical switching process model of low-voltage eGaN HEMTs for loss calculation. The proposed model considers the low-parasitic inductance, as well as the nonlinearity of junction capacitances and nonlinearity of transconductance. The turn-on and turn-off switching processes are described in detail. The methods to solve the waveforms and losses are discussed. The switching waveforms for a low-voltage switching device between analytical model and experiment are compared for the first time in this paper. Moreover, the effects of gate resistance, gate supply voltage, and parasitic inductances on switching losses are investigated based on the proposed model.

Another main contribution of this paper is a novel current measuring method based on magnetic coupling is proposed. This method is suitable for measuring the switching current and does not consume additional energy. Besides, the current measuring structure can be easily integrated in a multilayer PCB substrate.

The rest of this paper is organized as follows. First, the basis of the circuit model is described. Then, the switching process is discussed in detail during turn-on and turn-off transitions. Finally, the proposed model is verified by simulation and experimental results.

II. Basis of the Circuit Model

In order to improve the accuracy of the analytical model, three important parameters should be taken into consideration: the parasitic inductances, the nonlinear capacitances, and the nonlinear transconductance. The parasitic inductances are extracted from Maxwell 3-D simulation. Curve fitting is applied to accurately model the nonlinear capacitances, such as input capacitance C_{iss}, output capacitance C_{oss} and reverse capacitance C_{rss}. The nonlinear capacitances can be expressed as

$$C = f(V_{ds}) \tag{1}$$

where C represents C_{iss},C_{oss} or C_{rss}, and f is a polynomial obtained by curve fitting. The nonlinear transconductance curve is obtained in the same way. Fig. 1 shows the nonlinear transconductance curves obtained from the datasheet and curve fitting. We should notice that the curves are measured when the drain–source voltage keeps constant. So the channel current equals the drain current because no current flow through the output capacitance.

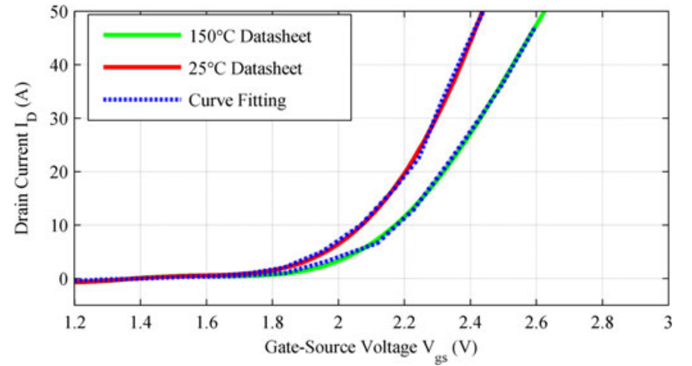

Fig. 1. Nonlinear transconductance comparison between the curves obtained from datasheet (solid lines) and curve fitting (dash lines).

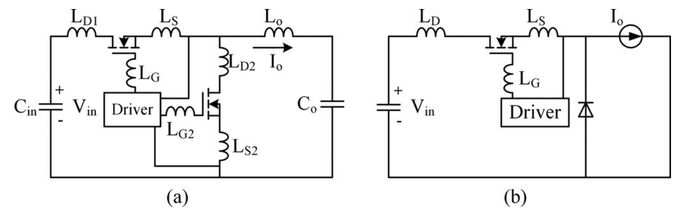

Fig. 2. (a) Synchronous buck converter. (b) Simplified equivalent circuit for buck converter during the transition period.

To analyze the switching loss, a simple synchronous buck converter is taken as an example [see Fig. 2(a)]. During the dead time, the "body diode" of bottom GaN HEMT conducts reverse current. It is reasonable to use a freewheeling diode instead of an eGaN HEMT as the bottom switch (BS) for the switching loss analysis. The inductor current I_L is treated as a constant current source during the transition period because the commutation time is sufficiently short so that the inductor current does not apparently change during switching period. Based on these assumptions, the buck converter in Fig. 2(a) is redrawn in Fig. 2(b). The common source inductance L_S is the inductance shared by the driver loop and the power loop. The drain inductance L_D includes L_{D1}, L_{D2}, and L_{S2}, resulting from the series inductance of the input capacitor C_{in}, the PCB trace parasitic inductance, and the package inductances of the switching devices. The high-frequency power loop inductance L_{Loop} is a sum of the common source inductance L_S and the drain inductance L_D. Actually, the simplified equivalent circuit is also suitable for analyzing the device behaviors during the transition period for other topologies, such as boost, buck–boost, etc.

III. Turn-On Transition

Before the top switch (TS) is turned ON, the inductor current I_L flows through the BS and the input voltage V_{in} is applied to the TS. Fig. 3 shows typical waveforms of a buck converter during turn-on transition. The turn-on transition can be divided into four stages, which are analyzed in the following sections. At each stage, the equations are obtained from an equivalent circuit (see Fig. 4). By solving the equations, we can obtain

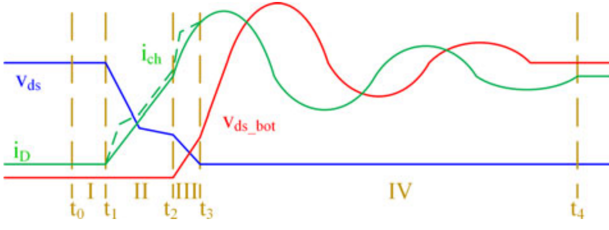

Fig. 3. Typical waveforms of a buck converter during turn-on transition.

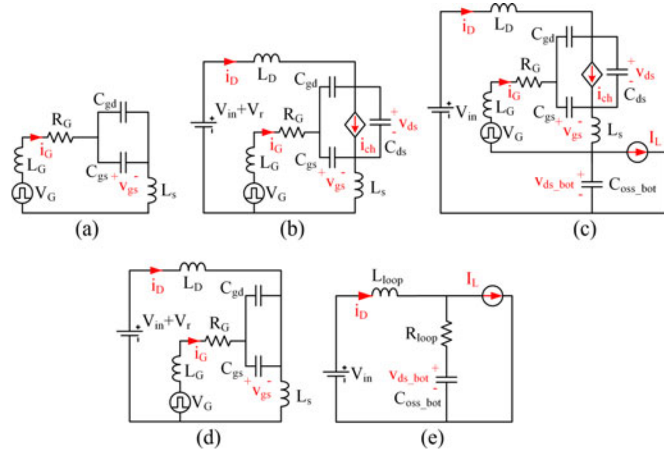

Fig. 4. Simplified equivalent circuits for different stages during turn-on transition. (a) Stage I. (b) Stage II. (c) Stage III: Case I. (d) Stage III: Case II. (e) Stage IV.

five variables, namely, the drain current i_D, the drain–source voltage $v_{\rm ds}$, the drain–source voltage of BS $v_{\rm ds_bot}$, the gate–source voltage $v_{\rm gs}$, and the gate current i_G. For easy calculation with a math tool, the equations are written in a matrix form given in the appendix.

A. Stage I: Delay Period

When the gate voltage V_G is applied, the gate current charges the input capacitance C_{iss}, which is the combination of $C_{\rm gs}$ and $C_{\rm gd}$. From the equivalent circuit in Fig. 4(a), the following equations are obtained:

$$i_G = (C_{\rm gs} + C_{\rm gd})\frac{dv_{\rm gs}}{dt} \tag{2}$$

$$V_G = (L_G + L_S)\frac{di_G}{dt} + R_G i_G + v_{\rm gs}. \tag{3}$$

This period ends when the gate–source voltage $v_{\rm gs}$ reaches the threshold voltage $V_{\rm th}$.

B. Stage II: Main Transition Period

During this stage, the equivalent circuit is shown in Fig. 4(b). When $v_{\rm gs}$ reaches $V_{\rm th}$, the channel of TS starts conducting and the channel current $i_{\rm ch}$ is controlled by $v_{\rm gs}$

$$i_{\rm ch} = g_{fs}(v_{\rm gs} - V_{\rm th}). \tag{4}$$

Meanwhile, the capacitances $C_{\rm gd}$ and $C_{\rm ds}$ are discharged by the channel, resulting in the decrease of drain–source voltage $v_{\rm ds}$. The drain current i_D is the sum of the channel current $i_{\rm ch}$ and the current charging the capacitance $C_{\rm gd}$ and $C_{\rm ds}$

$$i_D = i_{\rm ch} + (C_{\rm ds} + C_{\rm gd})\frac{dv_{\rm ds}}{dt}. \tag{5}$$

The voltage difference between $v_{\rm ds}$ and its initial voltage $V_{\rm in} + V_r$ is applied to the parasitic inductances L_D and L_S, which forces the drain current i_D to increase

$$V_{\rm in} + V_r = v_{\rm ds} + (L_D + L_S)\frac{di_D}{dt} \tag{6}$$

where V_r is the reverse conduction voltage of BS.

The power loop has a great effect on the driver loop through the common source inductance L_S and the drain–gate capacitance $C_{\rm gd}$. The increase of the drain current i_D induce a positive voltage drop in L_S, which tends to prevent the gate–source voltage $v_{\rm gs}$ from increasing

$$V_G = v_{\rm gs} + R_G i_G + L_G\frac{di_G}{dt} + L_S\frac{di_D}{dt}. \tag{7}$$

The current discharging $C_{\rm gd}$ shares a part of gate current i_G, which slows down the increase of gate–source voltage $v_{\rm gs}$

$$i_G = C_{\rm gs}\frac{dv_{\rm gs}}{dt} + C_{\rm gd}\left(\frac{dv_{\rm gs}}{dt} - \frac{dv_{\rm ds}}{dt}\right). \tag{8}$$

This period ends when either the drain–source voltage $v_{\rm ds}$ drops to zero or the drain current i_D reaches the load current. Which event is completed first depends on the switching speed capability of TS, circuit parameters, and load current. As the TS, GaN HEMTs have a very fast switching speed capability. If smaller gate resistance R_g and common source inductance L_S are achieved, $i_{\rm ch}$ will increase faster due to a faster increase of $v_{\rm gs}$. As the change rate of i_D is limited by $L_{\rm Loop}$, the current discharging C_{oss} (namely $i_{\rm ch} - i_D$) is larger, which results in a faster drop of $v_{\rm ds}$. If the loop inductance $L_{\rm Loop}$ is larger, i_D will increase slowly, while $v_{\rm ds}$ will drop faster. The larger the I_L, the longer time is needed when i_D reaches the load current I_L. In short, $v_{\rm ds}$ tends to drop to zero first when small R_g, small L_S, large $L_{\rm Loop}$, or large I_L is achieved. Conversely, i_D tends to reach I_L first.

C. Stage III: Remaining Transition Period

1) Case I: The drain current reaches the load current before the drain–source voltage drops to zero. After the drain current reaches the load current, the current flowing thought BS (namely $i_D - I_L$) reverses. The channel of BS stops conducting. The current difference between i_D and I_L charges $C_{oss_{\rm bot}}$, resulting in the increase of $v_{\rm ds_bot}$. The channel current of TS $i_{\rm ch}$ is still controlled by the gate–source voltage $v_{\rm gs}$. The case is similar to stage II. From the equivalent circuit in Fig. 4(c), the following key equations are obtained:

$$i_{\rm ch} = g_{fs}(v_{\rm gs} - v_{\rm th}) \tag{9}$$

$$i_D = i_{\rm ch} + (C_{\rm ds} + C_{\rm gd})\frac{dv_{\rm ds}}{dt} \tag{10}$$

$$V_{\rm in} = (L_D + L_S)\frac{di_D}{dt} + v_{\rm ds} + v_{\rm ds_bot} \tag{11}$$

$$V_G = v_{\rm gs} + R_G i_G + L_G\frac{di_G}{dt} + L_S\frac{di_D}{dt} \tag{12}$$

$$i_G = C_{\rm gs}\frac{dv_{\rm gs}}{dt} + C_{\rm gd}\left(\frac{dv_{\rm gs}}{dt} - \frac{dv_{\rm ds}}{dt}\right) \tag{13}$$

$$i_D = I_L + C_{oss_{\rm bot}}\frac{dv_{\rm ds_bot}}{dt}. \tag{14}$$

This period ends when the drain–source voltage $v_{\rm ds}$ decreases to zero.

2) Case II: The drain–source voltage drops to zero before the drain current reaches the load current. Once $v_{\rm ds}$ drops to zero, it will not change any more. The channel current $i_{\rm ch}$ is no longer controlled by the gate–source voltage and the change rate of the drain current is limited by the power loop inductance $L_{\rm Loop}$. The equivalent circuit is shown in Fig. 4(d) and the following key equations are obtained:

$$V_{\rm in} + V_r = (L_D + L_S)\frac{di_D}{dt} \tag{15}$$

$$V_G = v_{\rm gs} + i_G R_G + L_G\frac{di_G}{dt} + L_S\frac{di_D}{dt} \tag{16}$$

$$i_G = (C_{\rm gs} + C_{\rm gd})\frac{dv_{\rm gs}}{dt}. \tag{17}$$

This period ends when the drain current reaches the load current.

D. Stage IV: Ringing Period

During this stage, the TS is turned ON and the BS is turned OFF. The power loop inductance $L_{\rm Loop}$ resonates with the output capacitance of the BS $C_{oss_{\rm bot}}$. The resistance $R_{\rm Loop}$ represents the high-frequency damping resistance. From equivalent circuit in Fig. 4(e), the following key equations are obtained:

$$i_D = C_{oss_{\rm bot}}\frac{dv_{\rm ds_bot}}{dt} + I_L \tag{18}$$

$$V_{\rm in} = R_{\rm Loop}(i_D - I_L) + L_{\rm loop}\frac{di_D}{dt} + v_{\rm ds_bot}. \tag{19}$$

This period ends when the ringing is fully damped.

IV. Turn-Off Transition

Before the TS is turned OFF, the inductor current I_L flows through the TS, and the input voltage $V_{\rm in}$ is applied to the BS. The turn-off transition can be divided into four stages (as shown in Fig. 5). For each stage, the equivalent circuit is shown in Fig. 6. Similar to turn-on transition, we can obtain five variables by solving the equations, namely, the drain current i_D, the drain–source voltage $v_{\rm ds}$, the drain–source voltage of BS $v_{\rm ds_bot}$, the gate–source voltage $v_{\rm gs}$, and the gate current i_G.The equations at different stages are written in a matrix form are given in the appendix.

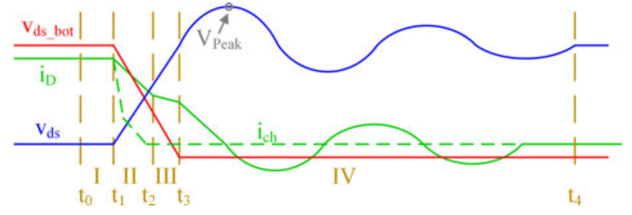

Fig. 5. Typical waveforms of a buck converter during turn-off transition.

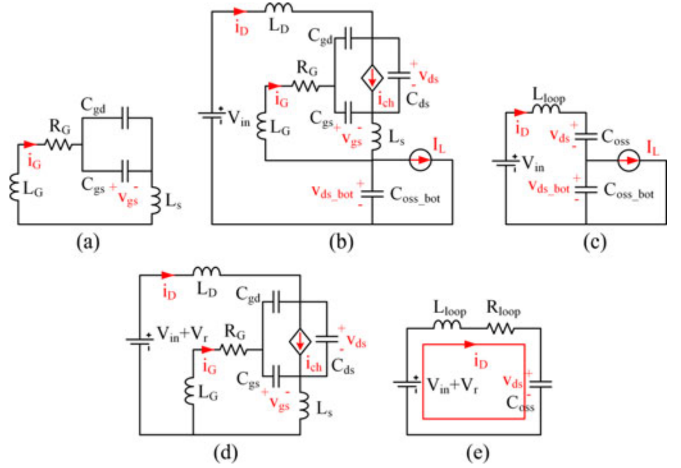

Fig. 6. Simplified equivalent circuits for different stages during turn-off transition. (a) Stage I. (b) Stage II. (c) Stage III: Case I. (d) Stage III: Case II. (e) Stage IV.

A. Stage I: Delay Period

When the gate drive voltage is pulled down to 0 V, the input capacitance C_{iss} is discharged. The equivalent circuit is shown in Fig. 6(a), and key equations are as follow:

$$i_G = (C_{\rm gs} + C_{\rm gd})\frac{dv_{\rm gs}}{dt} \tag{20}$$

$$0 = v_{\rm gs} + R_G i_G + (L_G + L_S)\frac{di_G}{dt}. \tag{21}$$

This stage ends when the gate–source voltage satisfies the following relationship:

$$v_{\rm gs} = V_{\rm th} + \frac{I_L}{g_{fs}}. \tag{22}$$

B. Stage II: Main Transition Period

The equivalent circuit is shown in Fig. 6(b). During this stage, the channel current decreases under the control of the gate voltage $v_{\rm gs}$. As the change rate of i_D is limited by $L_{\rm Loop}$, the decrease rate of i_D is smaller than that of $i_{\rm ch}$. The current difference between i_D and $i_{\rm ch}$ charges C_{oss}, resulting in the increase of $v_{\rm ds}$. The current difference between I_L and i_D discharges $C_{oss_{\rm bot}}$, resulting in the decrease of $v_{\rm ds_bot}$. The equations are the same as the equations in Section III-C1, and the only difference is $V_G = 0$.

This stage ends when the channel current $i_{\rm ch}$ drops to zero or the drain–source voltage of BS $v_{\rm ds_bot}$ drops to $-V_r$. Which

event is completed first depends on the switching speed capability of TS, circuit parameters, and the load current. If smaller gate resistance R_g and common source inductance L_S are achieved, $i_{\rm ch}$ can decrease faster due to a faster drop of $v_{\rm gs}$. If the loop inductance $L_{\rm Loop}$ is larger, i_D will decrease more slowly. So the current discharging $C_{oss_{\rm bot}}$ (namely$I_L - i_D$) is smaller, which results in a slower drop of $v_{\rm ds_bot}$. If I_L is smaller, the shorter time is needed when $i_{\rm ch}$ drops to zero, while $v_{\rm ds_bot}$ drops slower due to a smaller discharging current. In short, $i_{\rm ch}$ tends to drop to zero first when small R_g, small L_S, large $L_{\rm Loop}$, or small I_L is achieved. Conversely, $v_{\rm ds_bot}$ tends to drops to $-V_r$ first.

C. Stage III: Remaining Transition Period

1) Case I: The channel current drops to zero before $v_{\rm ds_bot}$ drops to $-V_r$. Once the channel current drops to zero, the channel of TS stops conducting current. The load current I_L flows through the capacitance C_{oss} and $C_{oss_{\rm bot}}$ [see Fig. 6(c)]

$$V_{\rm in} = L_{\rm loop}\frac{di_D}{dt} + v_{\rm ds} + v_{\rm ds_bot} \tag{23}$$

$$i_D = C_{oss}\frac{dv_{\rm ds}}{dt} \tag{24}$$

$$i_D = C_{oss_{\rm bot}}\frac{dv_{\rm ds_bot}}{dt} + I_L. \tag{25}$$

This period ends when the drain voltage reaches the input voltage $V_{\rm in}$.

2) Case II: $v_{\rm ds_bot}$ drops to $-V_r$ before the channel current decreases to zero. During this stage, the channel current is still controlled by gate–source voltage and the BS starts conducting reverse current. Fig. 6(d) is the equivalent circuit. The analysis is similar to that in Section III-B and the voltage V_G need to be set to zero. This period ends when the channel current decreases to zero.

D. Stage IV: Ringing Period

During this stage, the TS is turned OFF and the BS conducts reverse current. The power loop inductance $L_{\rm Loop}$ resonates with the output capacitance of TS C_{oss}. The resistance $R_{\rm Loop}$ represents the high-frequency damping resistance. Fig. 6(e) shows the equivalent circuit and the key equations can be expressed as follows:

$$i_D = C_{oss}\frac{dv_{\rm ds}}{dt} \tag{26}$$

$$V_{\rm in} + V_r = R_{\rm loop} i_D + L_{\rm loop}\frac{di_D}{dt} + v_{\rm ds}. \tag{27}$$

This period ends when the ringing is fully damped.

V. Loss Calculation

During the turn-on/turn-off transition, there are two components consuming energy. One is the equivalent voltage-controlled current source located in the channel of switching device. The other one is the equivalent high-frequency damping resistance distributed in the high-frequency power loop.

The accurate method to calculate the loss dissipated in the channel is to calculate the overlap loss between the channel current and the drain–source voltage. However, the traditional method is to calculate the overlap loss between the drain current and the drain–source voltage. The accurate overlap loss $P_{\rm Overlap}$ and the traditional overlap loss $P_{\rm Overlap1}$ are expressed as

$$P_{\rm Overlap} = f_s \cdot \int i_{\rm ch} v_{\rm ds} dt \tag{28}$$

$$P_{\rm Overlap1} = f_s \cdot \int i_D v_{\rm ds} dt \tag{29}$$

where f_s is the switching frequency.

When the TS is turned ON, the drain–source voltage starts decreasing. The energy stored in the output capacitance is dissipated in the channel. So the turn-on overlap loss $P_{\rm Overlap_ON}$ is the sum of energy stored in output capacitance $P_{Coss\,{\rm at}\,(V_{\rm in}+V_r)}$ and the traditional turn-on overlap loss $P_{\rm Overlap1_ON}$. Thus, the relationship can be expressed as

$$\begin{aligned} P_{\rm Overlap_ON} &= f_s \cdot \int_{t1}^{t_{(v_{\rm ds}=0)}} i_{\rm ch} v_{\rm ds} dt \\ &= f_s \cdot \int_{t1}^{t_{(v_{\rm ds}=0)}} (i_D + i_{Coss}) v_{\rm ds} dt \\ &= P_{\rm Overlap1_ON} + P_{Coss\,{\rm at}\,(V_{\rm in}+V_r)} \end{aligned} \tag{30}$$

where i_{Coss} is the current discharging the output capacitance of TS and $P_{Coss\,@\,(V_{\rm in}+V_r)}$ is the energy stored in the output capacitance when the applied voltage is $V_{\rm in} + V_r$.

When the TS is turned OFF, the drain–source voltage starts increasing and the energy is stored in the output capacitance. The energy stored in the output capacitance is usually quite large because of the high peak drain–source voltage. The turn-off overlap loss $P_{\rm Overlap_OFF}$ is the difference between the traditional overlap loss $P_{\rm Overlap1_OFF}$ and the energy stored in output capacitance $P_{Coss\,@\,V_{\rm Peak}}$. Thus, the relationship can be expressed as

$$\begin{aligned} P_{\rm Overlap_OFF} &= f_s \cdot \int_{t1}^{t_{(i_D=0)}} i_{\rm ch} v_{\rm ds} dt \\ &= f_s \cdot \int_{t1}^{t_{(i_D=0)}} (i_D - i_{Coss}) v_{\rm ds} dt \\ &= P_{\rm Overlap1_OFF} - P_{Coss\,@\,V_{\rm Peak}} \end{aligned} \tag{31}$$

where $P_{Coss\,@\,V_{\rm Peak}}$ is the energy stored in the output capacitance when the applied voltage is $V_{\rm Peak}$.

The high-frequency damping resistance $R_{\rm Loop}$ represents the loss related with the high-frequency ringing current, such as high-frequency power loop resistance, radiation loss, etc. It damps the ringing current. The ringing frequency is usually above 100 MHz, and even up to 500 MHz. So, the power loop ac resistance is much larger than dc resistance because of the skin effect. Besides, the radiation energy cannot be ignored in such high ringing frequency. The turn-on ringing loss $P_{\rm Ring_ON}$ and the turn-off ringing loss $P_{\rm Ring_OFF}$ are expressed as follows:

$$P_{\rm Ring_ON} = f_s \cdot \int_{t3}^{t4} (i_D(t) - I_L) R_{\rm Loop} dt \tag{32}$$

$$P_{\text{Ring_OFF}} = f_s \cdot \int_{t3}^{t4} i_D(t) R_{\text{Loop}} dt. \quad (33)$$

When v_{ds} drops from V_{Peak} to the steady-state voltage V_{in}, a part of $P_{Coss\,@\,V_{\text{Peak}}}$ is recycled by the input voltage source and part is dissipated at R_{Loop}. The remaining power is dissipated at the channel when TS is turned ON. Here we should notice that v_{ds} reaches V_{Peak} when i_D drops to zero. The drain current can be written as

$$i_D = -I_D e^{-\alpha(t - t_{(i_D=0)})} \sin(\omega(t - t_{(i_D=0)})) \quad (34)$$

where $\alpha = R_{\text{Loop}}/(2L_{\text{Loop}})$ and $\omega \approx 1/\sqrt{L_{\text{Loop}} C_{oss}}$. The power supplied by input voltage source is

$$\begin{aligned} P_{V_{\text{in}}} &= \int_{t_{(i_D=0)}}^{t_4} V_{\text{in}} i_D \, dt \\ &= -V_{\text{in}} I_D \int_{t_{(i_D=0)}}^{t_4} e^{-\alpha(t - t_{(i_D=0)})} \sin(\omega(t - t_{(i_D=0)})) dt \\ &= -\frac{\omega}{\alpha^2 + \omega^2} V_{\text{in}} I_D < 0. \end{aligned} \quad (35)$$

As $P_{V_{\text{in}}}$ is negative, a part of the energy is recycled by the input voltage source.

VI. Verifications and Discussions of the Analytical Model

A. Simulation Verification

For verification purposes, a synchronous buck converter is built with LTSpice software tool. The converter operates at an input voltage of 12 V, an output voltage of 3.6 V, and an output current of 9 A. The switching frequency is 2 MHz. The switching device is EPC2015 using the manufacturer's device model [27]. The analytical results are calculated by the equations attached in the appendix step by step. The nonlinear capacitance and the nonlinear transconductance are considered. A good matching between simulation and analytical waveforms is observed for the turn-on and turn-off transitions, as shown in Fig. 7.

B. Experimental Configuration

A synchronous buck converter is designed to verify the analytical model. The GaN HEMTs are EPC2015, the driver is LM5113, and the output inductance is SLC1175-271MEB. Fig. 8 shows an experiment prototype. The converter operates at an input voltage of 12 V, an output voltage of 3.3 V, and an output current of 7.9 A. The switching frequency is 2 MHz. Fig. 9 is the layout of the buck converter. The copper thickness is 2 oz and the thickness of the PCB board is 1 mm. The input capacitors, TS, and BS are located on top layer and connected in turn. The bottom layer connects to the top layer through via holes so that the high-frequency power loop is closed. The high-frequency power loop inductance is about 0.85 nH, which is extracted from Maxwell 3- D simulation.

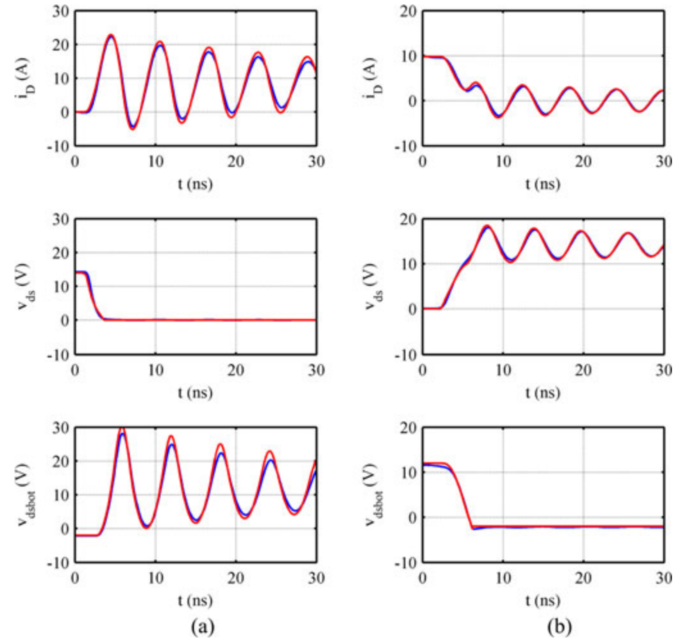

Fig. 7. Turn-on/off waveforms comparisons (Blue line: simulation, red line: analytical model). (a) Turn-on transition. (b) Turn-off transition.

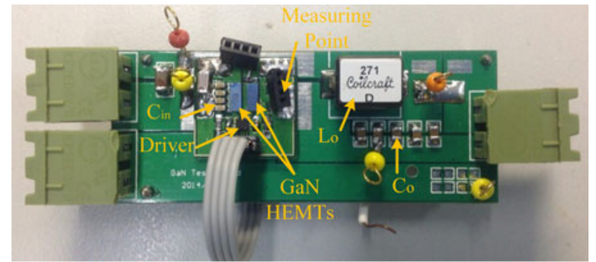

Fig. 8. Experiment prototype of a synchronous buck converter.

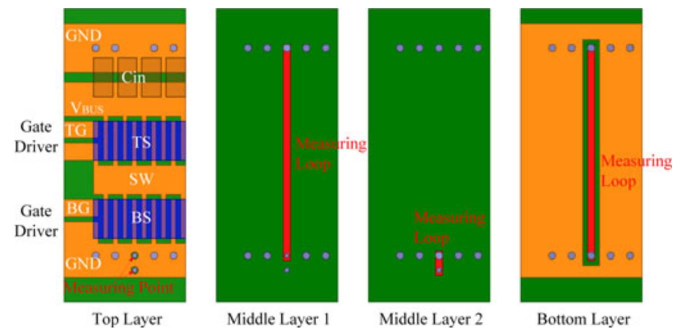

Fig. 9. Layout of a synchronous buck converter with integrated current measuring loop using four-layer PCB substrate.

C. Current Measuring Method

In order to measure the switching waveform of the drain current, a measuring loop is integrated in the four-layers PCB substrate (see Fig. 9). The measuring loop locates in the middle of the high-frequency power loop in order to improve the mutual inductance between the high-frequency power loop and

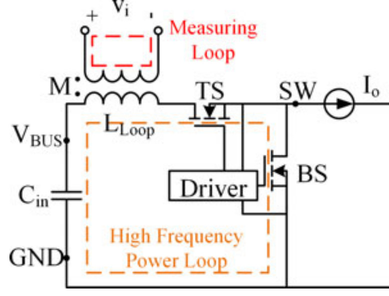

Fig. 10. Equivalent circuit based on the layout in Fig. 8.

TABLE I
MUTUAL INDUCTANCE AT DIFFERENT FREQUENCIES

f(Hz)	1 M	10 M	100 M	1000 M
M(nH)	0.6696	0.7019	0.7020	0.7020

the measuring loop. The measuring loop is not a closed loop and its terminals are used as two measuring points in top layer. Fig. 10 shows the equivalent circuit. When the drain current i_D changes, the induced voltage v_i can be observed between the two measuring points, which can be expressed as

$$M\frac{di_D}{dt} = v_i \tag{36}$$

where M is the mutual inductance between the high-frequency power loop and the measuring loop. From (36), the drain current i_D can be derived as

$$i_D = \int \frac{v_i}{M} dt. \tag{37}$$

The mutual inductance is extracted from Maxwell 3-D simulation based on the layout in Fig. 9. The result is shown in Table I. When the frequency changes from 1 MHz to 1GHz, the relative change of mutual inductance is 4.8%. So we can conclude that the mutual inductance can be regarded as a constant in a wide frequency range.

Fig. 11 shows the measured waveform of the induced voltage v_i during turn-on and turn-off transition. The induced voltage v_i can be as high as 3 V, which can be accurately measured by an oscilloscope probe without an amplifier. The ringing frequency is about 170 MHz; therefore, we need a high-bandwidth oscilloscope to ensure that the measured waveform has no distortion.

The voltage probe is P6158 and the oscilloscope is DPO7254. Fig. 12 shows the equivalent circuit of the probe's load effect on the current measured waveform. v_i is the induced voltage and v_o is the measured voltage. The values of L_2 and $L_{\rm Probe}$ are extracted from the Maxwell 3-D simulation. The values of C and R are obtained from the probe's datasheet [28]. The magnitude and phase of voltage gain v_o/v_i are shown in Fig. 13. The maximum errors of magnitude and phase are 0.08 and 1.47° when the frequency varies from 1 to 300 MHz. The errors will be smaller if L_2 and $L_{\rm Probe}$ are further reduced. As the ringing

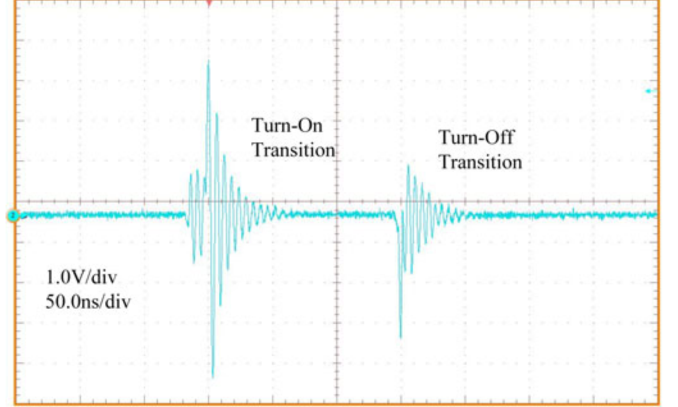

Fig. 11. Measured waveform of the voltage v_i during turn-on and turn-off transition.

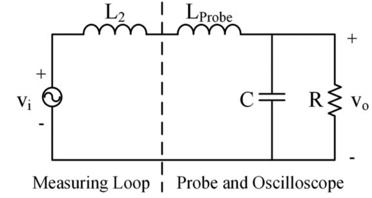

Fig. 12. Equivalent circuit of the probe's load effect on the current measured waveform.

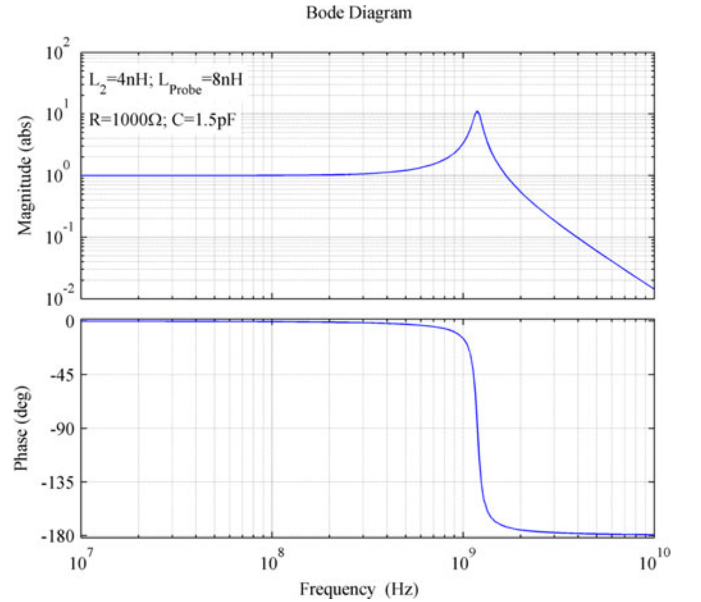

Fig. 13. Magnitude and phase of voltage gain v_o/v_i.

frequency is about 170 MHz, we can conclude that the probe has quite small load effect on the measured waveform.

D. Experimental Results and Discussions

The drain current i_D is calculated by (37) after the induced voltage v_i is measured. The drain–source voltage of the BS

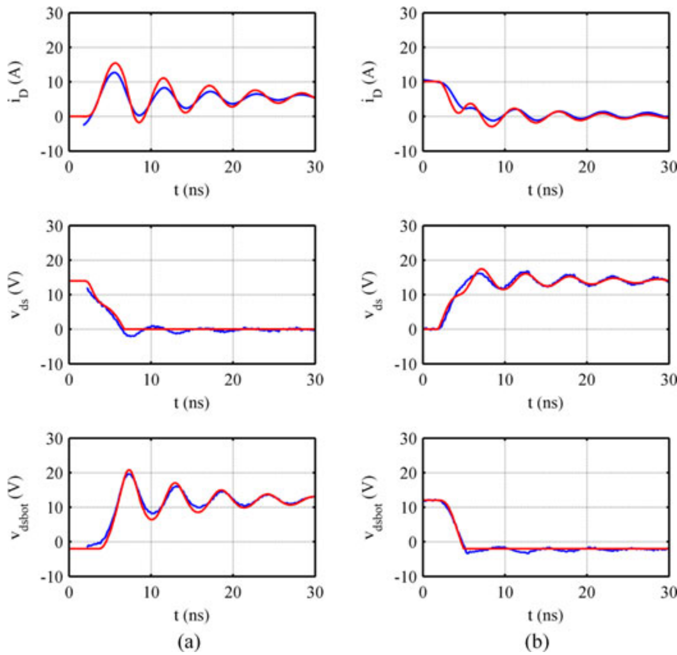

Fig. 14. Comparison of switching waveforms (Blue line: experiment, red line: analytical model). (a) Turn-on transition. (b) Turn-off transition.

$v_{\mathrm{ds_bot}}$ and the drain voltage of the TS v_D are measured directly by an oscilloscope. The drain–source voltage v_{ds} is the difference between the voltage v_D and $v_{\mathrm{ds_bot}}$. The analytical results are calculated by the equations attached in the appendix step by step. The nonlinear capacitance and the nonlinear transconductance are considered. The turn-on and turn-off transition waveforms of the analytical model are compared with the measured waveforms in Fig. 14 and they show a good agreement.

The switching speed in spice simulation is always larger than that in experiment. One of the reasons is that the transconductance decreases as the junction temperature increases (see Fig. 1). In experiment, the junction temperature of switching device is higher than the surrounding environment due to the consumed energy. As a result, the transconductance decreases. With the same gate–source voltage increment, the channel current changes more slowly, resulting in a lower switching speed. The spice model does not consider the effect of junction temperature.

The ringing in experiment damps faster than that in spice simulation, due to a larger high-frequency damping resistance. However, it is difficult to place the high-frequency damping resistance R_{Loop} in a suitable location in spice simulation circuit.

The loss breakdown of the buck converter is shown in Fig. 15. The dead time is about 15 ns. To accurately estimate the reverse conduction loss, the reverse conduction voltage and reverse conduction time are obtained from the experiment waveforms. The reverse conduction loss of the BS dominates the total power loss because of the large reverse conduction voltage of the eGaN HEMTs. So the reverse conduction time need to be carefully optimized. Besides, the turn-on overlap loss is significant for three reasons.

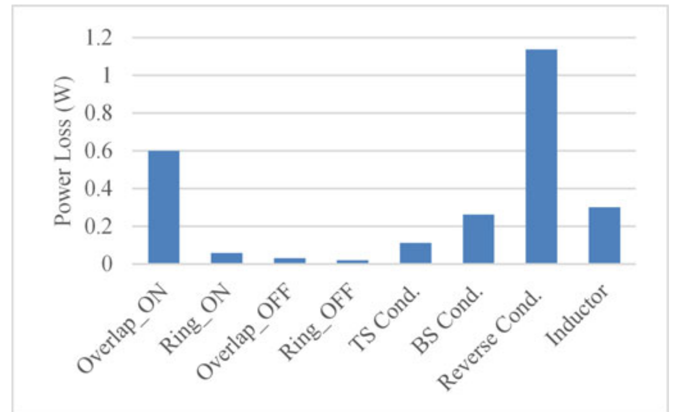

Fig. 15. Switching loss breakdown.

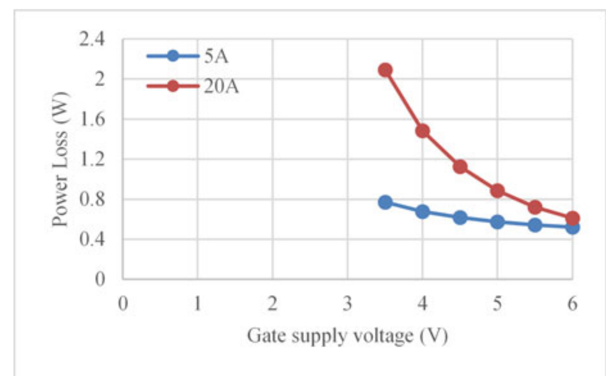

Fig. 16. Relationship between the turn-on switching loss and gate supply voltage.

1) *Low gate supply voltage*: The supply voltage of the driver is 5 V. Actually, the top gate supply voltage is only about 4.3 V because the boost diode voltage drop is about 0.7 V [29]. When the channel current of eGaN HEMTs is controlled by the gate supply voltage, the gate–source voltage is around 2 V. The smaller voltage difference between the gate–source voltage and the gate supply voltage drives the eGaN HEMT more slowly, resulting in a larger turn-on overlap loss. Fig. 16 shows the relationships between gate supply voltage and turn-on switching loss when the turn-on currents are 5 and 20 A. The results show that turn-on switching loss increases as the gate supply voltage decreases, especially in large turn-on current conditions.
2) *Large turn-on gate resistor*: The gate's breakdown voltage of eGaN HEMTs is 6 V. However, the device is designed to achieve optimal performance with a gate drive voltage about 5 V. This leaves a very small margin for driver overshoot to ensure safe operation. The turn-on and turn-off gate resistances are about 2.6 and 1.1 Ω, respectively, which include the internal gate resistance of the GaN HEMT and internal resistance of the driver. In fact, the ac resistance of the driver loop should not be neglected. A large turn-on gate resistor damps the voltage spike caused by the resonance between parasitic

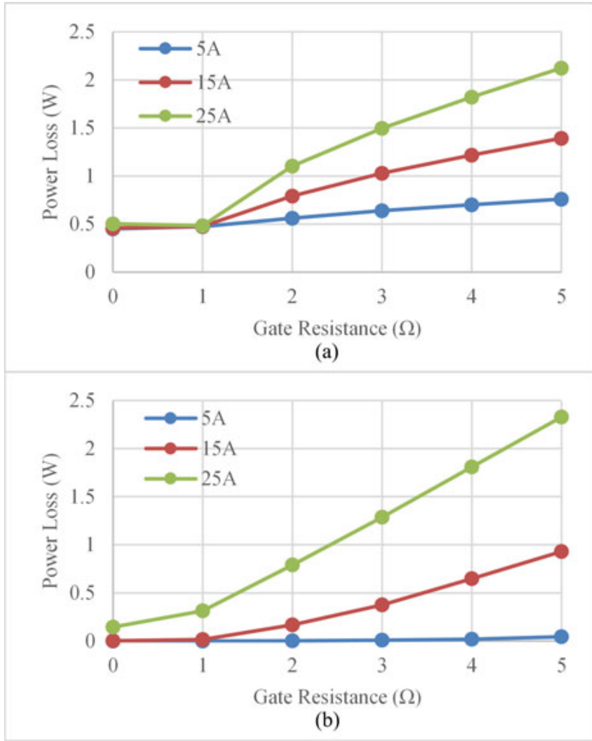

Fig. 17. Relationship between switching losses and gate resistance. (a) Turn-on switching loss. (b) Turn-off switching loss.

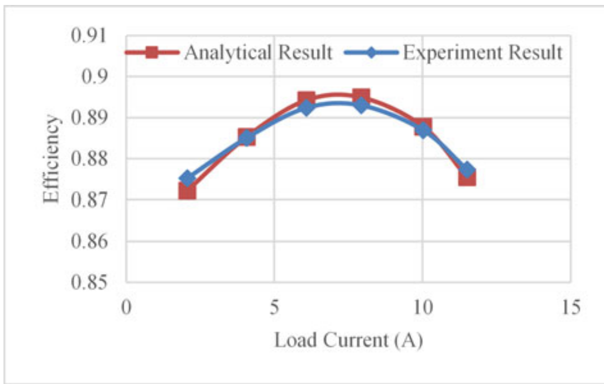

Fig. 18. Efficiency comparison between experiment result and analytical result over a wide load current.

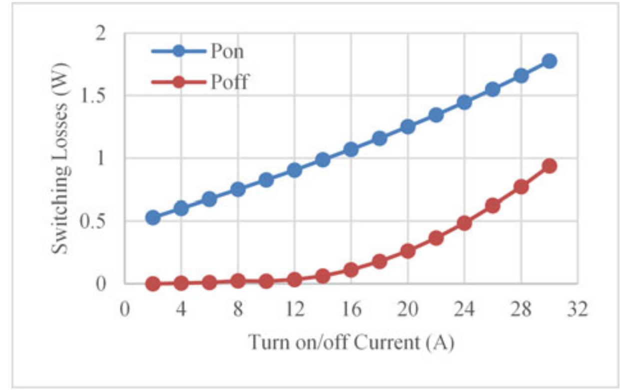

Fig. 19. Relationship between switching losses and turn-on/off current.

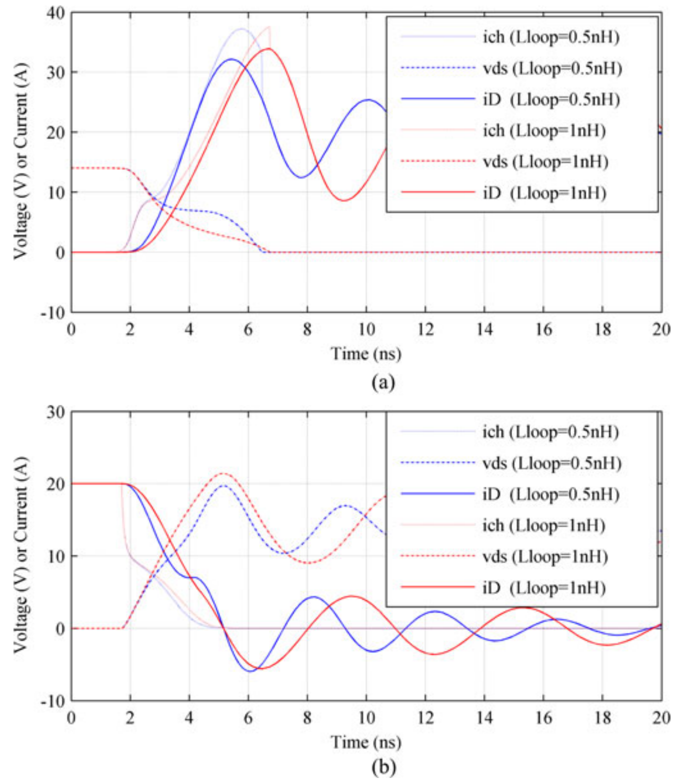

Fig. 20. Switching waveforms obtained by the proposed model (turn-on/off current: 20 A; f_s: 2 MHz; Blue lines: $L_{\rm Loop} = 0.5\,{\rm nH}$; Red lines: $L_{\rm Loop} = 1\,{\rm nH}$). (a) Turn-on transition waveforms. (b) Turn-off transition waveforms.

inductance and capacitance, which prevents the eGaN HEMTs from broken. However, large gate resistor limits the turn-on switching speed and, therefore, increases the turn-on overlap loss. As shown in Fig. 17, smaller gate resistance results in smaller switching loss. Both the total turn-on and turn-off gate resistance should be less than 1 Ω.

3) *Energy stored in output capacitance*: The energy stored in output capacitance dissipated in the channel during turn-on transition.

Except for the reverse conduction loss, effort should be taken to improve the turn-on switching speed to reduce the turn-on overlap loss.

To further validate the accuracy of the analytical model, the converter's efficiency is measured over a wide load range. The analytical result is in good agreement with the experiment result when the load current is from 2 to 12 A, as shown in Fig. 18.

The turn-on/off switching losses are plotted in Fig. 19 when the turn-on/off current varies from 2 to 30 A, which are obtained from the proposed model. The results show that the turn-on/off switching loss increases as the turn-on /off current increases. As turn-on switching loss is much larger than turn-off switching loss, zero-voltage switching technology (ZVS) is recommended to eliminate the turn-on switching loss.

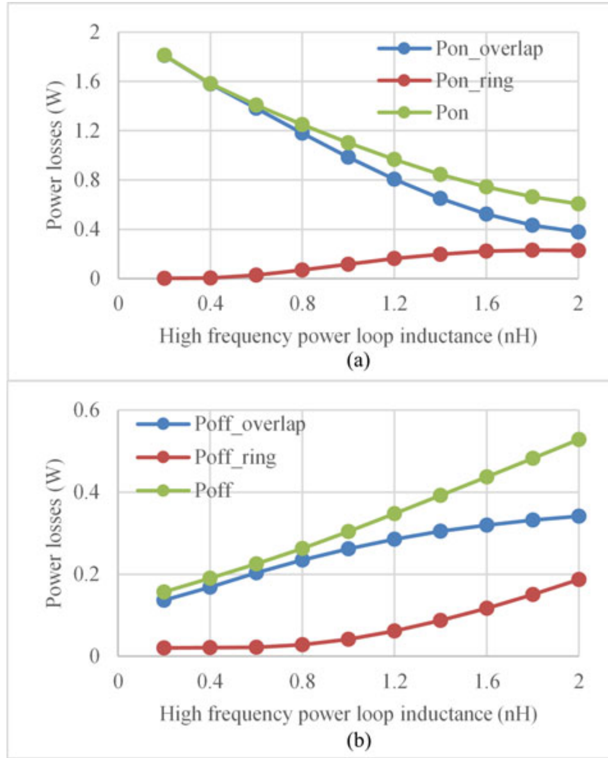

Fig. 21. Relationship between switching losses and high-frequency power loop inductance (turn-on/off current: 20 A; f_s: 2 MHz). (a) Turn-on switching loss. (b) Turn-off switching loss.

Besides, the proposed model is applied to analyze how the parasitic inductance influences the turn-on/off switching loss. The layouts based on eGaN HEMTs have been discussed in [9] and L_{Loop} in the reported layouts varies from 0.4 to 1.8 nH. The turn-on and turn-off switching waveforms are plotted in Fig. 20, when L_{Loop} are 0.5 and 1 nH, respectively. The relationship between turn-on/off switching loss and L_{Loop} is shown in Fig. 21. With the increase of L_{Loop}, the turn-on overlap loss decreases mainly because of faster drop of v_{ds} and slower increase of i_{ch}. With the increase of L_{Loop}, the turn-off overlap loss decreases mainly because of larger overshoot of v_{ds}. Both the turn-on and turn-off ringing losses increase as L_{Loop} increases. The final results show that turn-on switching loss decreases with the increase of L_{Loop}, while turn-off switching loss increases with the increase of L_{Loop}.

VII. Conclusion

Based on the analytical model and experimental results presented in this paper, the following conclusions can be drawn:

1) The analytical models for silicon MOSFETs are not suitable for eGaN HEMTs, since eGaN HEMTs are different from three aspects: higher switching speed, much more reduced parasitic inductance in switching loop, and absence of reverse recovery.
2) The turn-on switching loss is significant because of a limited turn-on switching speed. We can reduce the turn-on switching loss by reducing gate resistance and increasing gate supply voltage. As eGaN HEMTs have a much larger reverse conduction voltage than silicon MOSFETs, the reverse conduction loss could be dominate in the total power loss if dead time is large. Therefore, we need to put much efforts to improve the turn-on switching speed and reduce the dead time.
3) Additionally, a current measuring method based on magnetic coupling is proposed to measure the switching current waveform with improved accuracy. This method is suitable for measuring the high-frequency ringing current, and the current measuring structure can be easily integrated in a multilayer PCB substrate.

Appendix

The equations at different stages can be written in a unified form

$$\begin{cases} \frac{d\boldsymbol{x}(t)}{dt} = \boldsymbol{A}x(t) + \boldsymbol{B} \\ \boldsymbol{x}(t_0) = \boldsymbol{x}_0 \end{cases} \tag{38}$$

where $\boldsymbol{x} = [\,i_D\ v_{\text{ds}}\ v_{\text{ds_bot}}\ v_{\text{gs}}\ i_G\,]^T$ and x_0 is the initial conditions. The end conditions for one stage become the starting conditions for the next. The analytical results are calculated from the equations step by step. If the nonlinearity of the junction capacitances (including C_{iss}, C_{rss}, C_{oss}, and C_{oss_bot}) and transconductance are considered, the junction capacitances and transconductance in matrixes A and B should be replaced by the polynomial obtained by curve fitting. The matrixes A and B become functions of the state variable x and (38) turns to a nonlinear differential equation. The solutions of the nonlinear differential equations can be obtained by numerical methods, such as Runge–Kutta formula. In this paper, the function ODE45 in MATLAB software [30], which is based on Runge–Kutta formula, is applied to solve the equations. For simplification, we define $C_{iss} = C_{\text{gs}} + C_{\text{gd}}$, $C_{oss} = C_{\text{ds}} + C_{\text{gd}}$, $C_{oss_\text{bot}} = C_{\text{ds_bot}} + C_{\text{gd_bot}}$, and $L_{\text{Loop}} = L_S + L_D$.

Turn-on transition

$$\mathbf{x}_0 = [0 \quad V_{\text{in}} + V_r \quad -V_r \quad 0 \quad 0]^T.$$

Stage I:

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{iss}} \\ 0 & 0 & 0 & \frac{-1}{L_G+L_S} & \frac{-R_G}{L_G+L_S} \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{V_G}{L_G+L_S} \end{bmatrix}.$$

Stage II:

$$A = \begin{bmatrix} 0 & \frac{-1}{L_{\text{Loop}}} & 0 & 0 & 0 \\ \frac{1}{C_{oss}} & 0 & 0 & -\frac{g_{fs}}{C_{oss}} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{C_{\text{gd}}}{C_{iss}C_{oss}} & 0 & 0 & \frac{-g_{fs}C_{gd}}{C_{iss}C_{oss}} & \frac{1}{C_{iss}} \\ 0 & \frac{L_s}{L_G L_{\text{Loop}}} & 0 & \frac{-1}{L_G} & \frac{-R_G}{L_G} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{V_{\rm in}+V_r}{L_{\rm Loop}} \\ \frac{g_{fs}V_{\rm th}}{C_{oss}} \\ 0 \\ \frac{g_{fs}V_{\rm th}C_{\rm gd}}{C_{iss}C_{oss}} \\ \frac{V_G}{L_G} - \frac{L_s(V_{\rm in}+V_r)}{L_G L_{\rm Loop}} \end{bmatrix}.$$

Stage III:
Case 1:

$$A = \begin{bmatrix} 0 & \frac{-1}{L_{\rm Loop}} & \frac{-1}{L_{\rm Loop}} & 0 & 0 \\ \frac{1}{C_{oss}} & 0 & 0 & -\frac{g_{fs}}{C_{oss}} & 0 \\ \frac{1}{C_{oss_\rm bot}} & 0 & 0 & 0 & 0 \\ \frac{C_{\rm gd}}{C_{iss}C_{oss}} & 0 & 0 & \frac{-g_{fs}C_{gd}}{C_{iss}C_{oss}} & \frac{1}{C_{iss}} \\ 0 & \frac{L_s}{L_G L_{\rm Loop}} & \frac{L_s}{L_G L_{\rm Loop}} & \frac{-1}{L_G} & \frac{-R_G}{L_G} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{V_{\rm in}}{L_{\rm Loop}} \\ \frac{g_{fs}V_{\rm th}}{C_{oss}} \\ -\frac{I_L}{C_{oss_\rm bot}} \\ \frac{g_{fs}V_{\rm th}C_{\rm gd}}{C_{iss}C_{oss}} \\ \frac{V_G}{L_G} - \frac{L_s V_{\rm in}}{L_G L_{\rm Loop}} \end{bmatrix}.$$

Case 2:

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{iss}} \\ 0 & 0 & 0 & \frac{-1}{L_G} & \frac{-R_G}{L_G} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{V_{\rm in}+V_r}{L_{\rm Loop}} \\ 0 \\ 0 \\ 0 \\ \frac{V_G}{L_G} \end{bmatrix}.$$

Stage IV:

$$A = \begin{bmatrix} -\frac{R_{\rm Loop}}{L_{\rm Loop}} & 0 & -\frac{1}{L_{\rm Loop}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_{oss_\rm bot}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{iss}} \\ 0 & 0 & 0 & \frac{-1}{L_G} & \frac{-R_G}{L_G} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{V_{\rm in}+R_{\rm Loop}I_L}{L_{\rm Loop}} \\ 0 \\ -\frac{I_L}{C_{oss_\rm bot}} \\ 0 \\ \frac{V_G}{L_G} \end{bmatrix}.$$

Turn-off transition

$$x_0 = [I_L \quad 0 \quad V_{\rm in} \quad V_G \quad 0]^T.$$

Stage I:

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{iss}} \\ 0 & 0 & 0 & \frac{-1}{L_G+L_S} & \frac{-R_G}{L_G+L_S} \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}.$$

Stage II:

$$A = \begin{bmatrix} 0 & \frac{-1}{L_{\rm Loop}} & \frac{-1}{L_{\rm Loop}} & 0 & 0 \\ \frac{1}{C_{oss}} & 0 & 0 & -\frac{g_{fs}}{C_{oss}} & 0 \\ \frac{1}{C_{oss_\rm bot}} & 0 & 0 & 0 & 0 \\ \frac{C_{\rm gd}}{C_{iss}C_{oss}} & 0 & 0 & \frac{-g_{fs}C_{\rm gd}}{C_{iss}C_{oss}} & \frac{1}{C_{iss}} \\ 0 & \frac{L_s}{L_G L_{\rm Loop}} & \frac{L_s}{L_G L_{\rm Loop}} & \frac{-1}{L_G} & \frac{-R_G}{L_G} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{V_{\rm in}}{L_{\rm Loop}} \\ \frac{g_{fs}V_{\rm th}}{C_{oss}} \\ -\frac{I_L}{C_{oss_\rm bot}} \\ \frac{g_{fs}V_{\rm th}C_{\rm gd}}{C_{iss}C_{oss}} \\ -\frac{L_s V_{\rm in}}{L_G L_{\rm Loop}} \end{bmatrix}.$$

Stage III:
Case 1:

$$A = \begin{bmatrix} 0 & \frac{-1}{L_{\rm Loop}} & \frac{-1}{L_{\rm Loop}} & 0 & 0 \\ \frac{1}{C_{oss}} & 0 & 0 & 0 & 0 \\ \frac{1}{C_{oss_\rm bot}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{iss}} \\ 0 & 0 & 0 & \frac{-1}{L_G} & \frac{-R_G}{L_G} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{V_{\rm in}}{L_{\rm Loop}} \\ 0 \\ -\frac{I_L}{C_{oss_\rm bot}} \\ 0 \\ 0 \end{bmatrix}.$$

Case 2:

$$A = \begin{bmatrix} 0 & \frac{-1}{L_{\rm Loop}} & 0 & 0 & 0 \\ \frac{1}{C_{oss}} & 0 & 0 & -\frac{g_{fs}}{C_{oss}} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{C_{\rm gd}}{C_{iss}C_{oss}} & 0 & 0 & \frac{-g_{fs}C_{\rm gd}}{C_{iss}C_{oss}} & \frac{1}{C_{iss}} \\ 0 & \frac{L_s}{L_G L_{\rm Loop}} & 0 & \frac{-1}{L_G} & \frac{-R_G}{L_G} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{V_{\rm in}+V_r}{L_{\rm Loop}} \\ \frac{g_{fs}V_{\rm th}}{C_{oss}} \\ 0 \\ \frac{g_{fs}V_{\rm th}C_{\rm gd}}{C_{iss}C_{oss}} \\ -\frac{L_s(V_{\rm in}+V_r)}{L_G L_{\rm Loop}} \end{bmatrix}.$$

Stage IV:

$$A = \begin{bmatrix} -\frac{R_{\rm Loop}}{L_{\rm Loop}} & -\frac{1}{L_{\rm Loop}} & 0 & 0 & 0 \\ \frac{1}{C_{oss}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{iss}} \\ 0 & 0 & 0 & \frac{-1}{L_G} & \frac{-R_G}{L_G} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{V_{\rm in}+V_r}{L_{\rm Loop}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}.$$

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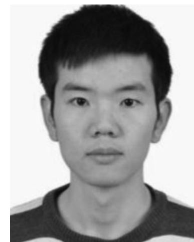

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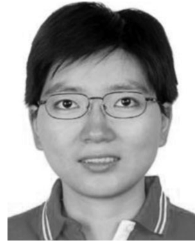

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