A Digital Predictive Peak Current Control for Power Factor Correction With Low-Input Current Distortion

Han-Shin Youn, *Student Member, IEEE*, Jin-Sik Park, *Student Member, IEEE*, Ki-Bum Park, *Member, IEEE*, Jae-Il Baek, *Student Member, IEEE*, and Gun-Woo Moon, *Member, IEEE*

***Abstract*—A digital predictive peak current control (PPCC) employing the adaptive slope compensation is proposed in this paper. The PPCC precisely predicts the peak current reference with the adaptive slope compensation according to operation regions and load conditions. Thereby, the PPCC can control the peak inductor current, and it significantly reduces the total harmonic distortion compared to that of the conventional digital average current control with duty ratio feed-forward which is widely used. In addition, parts of the PPCC are implemented by utilizing the internal high-resolution ramp generator and comparator of a digital signal processor without external components. The principle and analysis of the PPCC are presented, and the performance and feasibility are verified by experimental results with universal input (90 V_{rms} ∼ 260 V_{rms}) and 750 W − 400 V output laboratory prototype.**

***Index Terms*—Digital control, duty ratio feed-forward-control (DFF), power factor correction (PFC), predictive control.**

I. Introduction

THE importance of complying with the harmonics regulation limit of international standards such as IEC6100-3-2, 80 Plus, and internal specifications of the power supply system manufacturers is growing up to minimize the power loss, noise, and line current distortion resulting from the reactive power [1], [2]. To alleviate these problems, a continuous conduction mode (CCM) boost power factor correction (PFC) circuit is popular in medium- to high-power applications because of its small conduction loss and high power density [4].

Nowadays, due to the performance improvement and reduced cost of digital signal processors (DSPs), the digital control is gradually applied to the high switching frequency switching mode power supply instead of analog control ICs. In addition, since the digital control has many advantages such as design flexibility, management convenience, low part counts, and possibility of integration with other ICs [5], a lot of digital control algorithms and implementations have been explored [8]–[21].

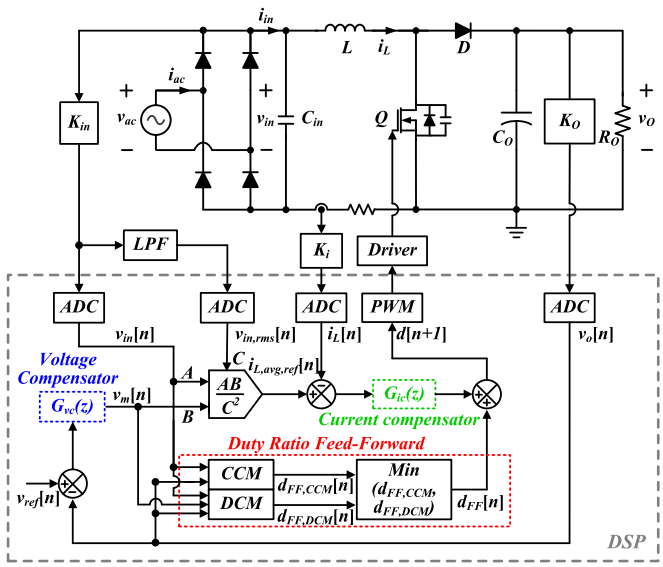


Fig. 1. Control block diagram of DFF ACC.

Most digital control schemes for the CCM boost PFC converter adopt the average current control (ACC) which needs high-current control bandwidth and gain, normally above 10 kHz, to achieve the sufficient disturbance rejection [6], [7]. However, due to the sample and hold effect and time delay of the digital control, the current control bandwidth is limited to one-tenth of the sampling frequency (f_{samp}) which is only half of that of the analog ACC. Consequently, the conventional digital ACC method encounters the large input current distortion [7]. In order to enhance the performance of the current control, the duty ratio feed-forward (DFF) technique in Fig. 1 has been widely adopted [8]–[14]. This DFF technique can cancel input and output voltage disturbances by calculating the ideal duty ratio and adding this duty ratio to the current control output. Moreover, the DFF can compensate the dynamics difference between CCM and discontinuous conduction mode (DCM), so the CCM compensator can be applied in DCM as well as CCM [11], [14]. As a result, the input current distortion can be reduced without increasing the current control loop bandwidth and gain. However, in DCM–CCM transition called the mixed conduction mode (MCM), the inductor and input current can be distorted due to the inaccurate DFF resulting from the inductance tolerance and unpredictable inductor current oscillations

Manuscript received September 19, 2014; revised January 19, 2015; accepted March 11, 2015. Date of publication March 30, 2015; date of current version September 21, 2015. This work was supported by the National Research Foundation of Korea grant funded by the Korea Government (MSIP) (No. 2010-0028680). Recommended for publication by Associate Editor D. Maksimovic.

H.-S. Youn, J.-Il Baek, and G.-W. Moon are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: poweryhs@kaist.ac.kr; dpi1067@kaist.ac.kr; gwmoon@kaist.ac.kr).

J.-S. Park is with Samsung Electro-Mechanics, Daejeon 305-701, Korea (e-mail: jinsik.park@samsung.com).

K.-B. Park is with the Power Electronic Converters Group, ABB Corporate Research, Baden Dättwil 5405, Switzerland (e-mail: ki-bum.park@ch.abb.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2417194

in DCM [14]. Moreover, inductor current oscillations also induce irregular high-frequency disturbance in the current control loop, thus, the input current distortion in DCM is inevitable.

To relieve the current distortion caused by the inductance tolerance, the inductance estimation method was proposed maintaining the DFF technique in [15]. However, this method still causes the input current distortion, when the boost converter is designed with low switching frequency to achieve a maximum efficiency. This is because the current control loop bandwidth and gain limited by the low switching and sampling frequencies are insufficient to cancel disturbances resulting from inductor current oscillations in DCM. In [16] and [17], the MCM control methods with separate CCM and DCM current compensators were proposed to enhance the performance of the current control in DCM. However, since the DFF technique cannot be applied to MCM control methods, they still require a high-current control bandwidth above 10 kHz and gain which is not suitable for low switching frequency applications. In addition, they also require the added bulk space and complex implementations, because these methods utilize the auxiliary winding or other digital techniques for the zero-crossing detection.

Meanwhile, the predictive current control for PFC which obviates the current loop compensator and achieves a fast response in the current control, i.e., single-cycle response, has been also applied to the PFC control [18]–[21]. Most of the predictive current control algorithms for PFC eliminate the input current distortion resulting from the low control bandwidth and gain, so these can generate a precise sinusoidal input current waveform in CCM. However, the input and inductor currents could not adequately chase the input voltage in DCM, because the inductor current oscillations in DCM are unpredictable and they deteriorate the input current distortion in DCM.

To alleviate aforementioned problems, a digital predictive peak current control (PPCC) with the adaptive slope compensation for the CCM boost PFC converter is proposed in this paper. The PPCC adopts the concept of the DFF which estimates the ideal duty ratio of the boost converter. Through this estimated duty ratio, the PPCC predicts the precise peak current reference and adaptive slope corresponding to operation regions and load conditions. As a result, the PPCC obviates the current loop compensator which requires a high sampling frequency to increase the current control bandwidth and gain. In addition, by using internal high-speed comparators and high-resolution slope ramp generators in the modern DSP, the PPCC controls the peak inductor current precisely without additional components. Therefore, the PPCC can provide the sinusoidal input current minimizing the current distortion.

This paper is organized as follows. In Section II, the principle of the proposed PPCC is presented including the prediction of the duty ratio, peak current reference, and adaptive slope compensation. Section III presents the analysis of the current distortion resulting from the current oscillations in DCM and inductance tolerance of a boost inductor. The experimental results of a universal input ($90 \sim 260\ \mathrm{V_{rms}}$) and $750\ \mathrm{W} - 400\ \mathrm{V}$ output laboratory prototype are presented in Section VI compared to the conventional DFF ACC, followed by a conclusion in Section V.

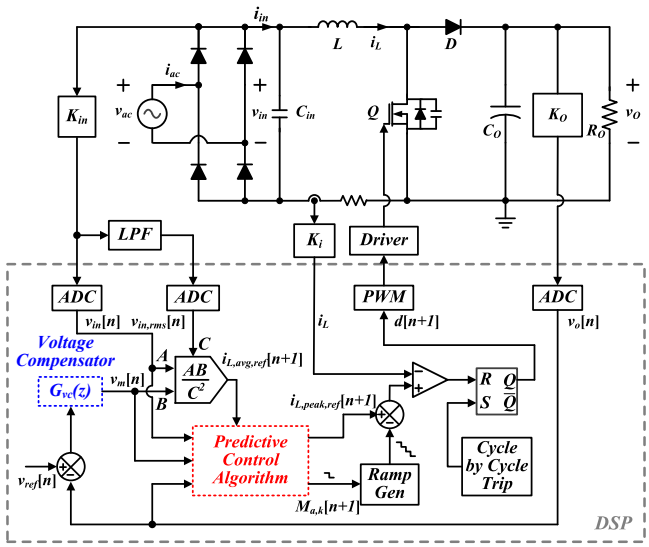


Fig. 2. Control block diagram of proposed PPCC.

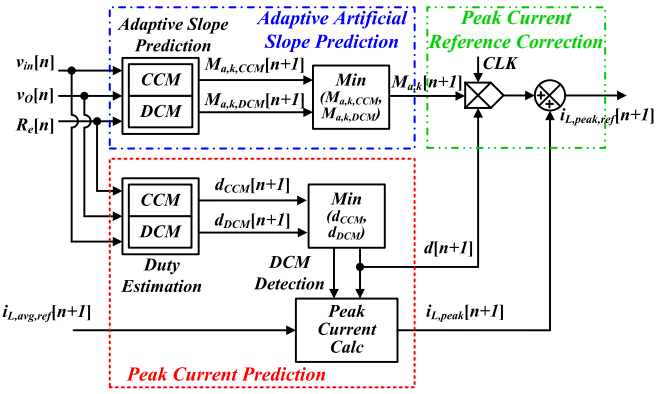


Fig. 3. Detail block diagram of the proposed predictive control algorithm.

II. Proposed PPCC

Fig. 2 shows the control block diagram of the PPCC, and Fig. 3 depicts the detailed block diagram of the predictive control algorithm in the PPCC.

The main characteristics of the PPCC are presented as follows.

1) The output voltage controller is the same as that of the conventional ACC.
2) The proposed PPCC provides the peak inductor current and adaptive artificial slope for the slope compensation by using the estimated duty ratio.
3) The proposed PPCC predicts the corrected peak current reference considering the adaptive slope compensation.
4) The adaptive slope compensation is implemented by the internal high-resolution slope ramp generator in the DSP, and the cycle-by-cycle current restriction is also carried out through the internal comparator.

To implement the proposed PPCC, the TMS320F28069PZT from Texas Instruments is chosen as a digital controller due to its integrated comparators and high-resolution slope ramp

generators. Moreover, since the predicted control variables of the proposed PPCC cannot be applied in the current switching cycle, most variables are determined for the next switching cycle based on sampled values.

A. Output Voltage Control

The output voltage control of the PPCC utilizes that of the conventional ACC, and basic control laws are presented in [3]. From [3], the output voltage controller can provide the average inductor current reference ($i_{L,\mathrm{avg,ref}}[n]$) as in (1), where $v_m[n]$ is the output of the output voltage loop compensator which means input power (W), $v_{\mathrm{in}}[n]$ is the rectified input voltage, and $v_{\mathrm{in,rms}}[n]$ is the input voltage rms value

$$i_{L,\mathrm{avg,ref}}[n] = i_{L,\mathrm{avg}}[n] = \frac{v_m[n]v_{\mathrm{in}}[n]}{v^2_{\mathrm{in,rms}}[n]}. \tag{1}$$

Assuming the unity power factor, where the shape of $i_{L,\mathrm{avg,ref}}[n]$ follows that of $v_{\mathrm{in}}[n]$, the emulated resistance ($R_e[n]$) which presents the load conditions can be expressed as

$$R_e[n] = \frac{v_{\mathrm{in}}[n]}{i_{L,\mathrm{avg,ref}}[n]} = \frac{v_{\mathrm{in}}[n]}{\frac{v_m[n]v_{\mathrm{in}}[n]}{v^2_{\mathrm{in,rms}}[n]}} = \frac{v^2_{\mathrm{in,rms}}[n]}{v_m[n]}. \tag{2}$$

Since the magnitude of $R_e[n]$ is almost constant, the estimated average current reference for the next switching cycle ($i_{L,\mathrm{avg,ref}}[n+1]$) is only affected by the input voltage variation and can be expressed as

$$i_{L,\mathrm{avg,ref}}[n+1] = \frac{v_{\mathrm{in}}[n+1]}{R_e[n]} \approx \frac{2v_{\mathrm{in}}[n] - v_{\mathrm{in}}[n-1]}{R_e[n]}, \tag{3}$$

where the estimated input voltage ($v_{\mathrm{in}}[n+1]$) is $2v_{\mathrm{in}}[n] - v_{\mathrm{in}}[n-1]$, and it can be obtained by assuming that $v_{\mathrm{in}}[n]$ is a linear term, because the switching frequency (f_s) is far higher than the line frequency.

B. Peak Inductor Current Prediction

The peak inductor currents in CCM and DCM are different. In order to predict the peak inductor current according to operation regions, the duty ratio in CCM and DCM, i.e., $d_{\mathrm{CCM}}[n+1]$ and $d_{\mathrm{DCM}}[n+1]$, and the operational region for the next switching cycle should be estimated in advance. Based on the DFF in [11] and the input–output equation of the boost converter in [3], $d_{\mathrm{CCM}}[n+1]$ and $d_{\mathrm{DCM}}[n+1]$ can be derived as

$$d_{\mathrm{CCM}}[n+1] = 1 - \frac{v_{\mathrm{in}}[n+1]}{v_O[n+1]} \approx 1 - \frac{2v_{\mathrm{in}}[n] - v_{\mathrm{in}}[n-1]}{v_O[n]},$$

$$d_{\mathrm{DCM}}[n+1] = \sqrt{\frac{2L}{R_e[n]T_s} \cdot d_{\mathrm{CCM}}[n+1]}, \tag{4}$$

where L is the inductance of a boost inductor, T_S is one switching period, and estimated output voltage ($v_O[n+1]$) is approximated as the sampled output voltage ($v_O[n]$) due to its negligible output voltage ripple.

Fig. 4 depicts $d_{\mathrm{CCM}}[n+1]$ and $d_{\mathrm{DCM}}[n+1]$ during the half-line cycle in several load conditions. As looking at Fig. 4,

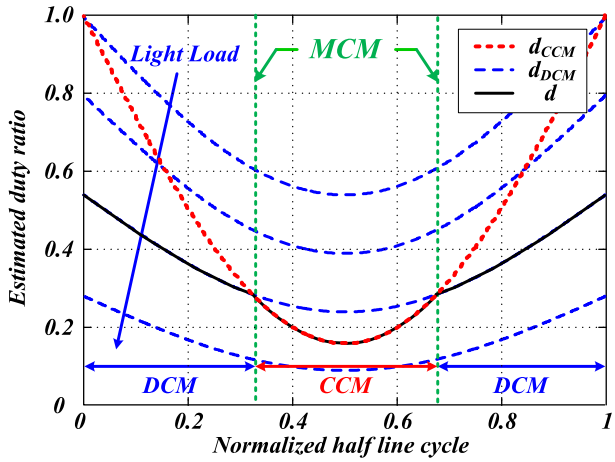


Fig. 4. Estimated duty ratio.

$d_{\mathrm{CCM}}[n+1]$ is independent of load variations during the half cycle of the ac input voltage. On the other hand, as the output load decreases, $d_{\mathrm{DCM}}[n+1]$ is lower and lower, so intersection points between $d_{\mathrm{DCM}}[n+1]$ and $d_{\mathrm{CCM}}[n+1]$ occur. Provided that estimated duty ratios are exactly equal to ideal duty ratio, these intersection points express CCM and DCM boundary points, and a lower value between $d_{\mathrm{CCM}}[n+1]$ and $d_{\mathrm{DCM}}[n+1]$ is matched to its operation region. Thus, the estimated duty ratio ($d[n+1]$) and operational region can be determined.

Based on duty ratios and operation regions, predicted CCM and DCM peak inductor currents, i.e., $i_{L,\mathrm{peak,CCM}}[n+1]$ and $i_{L,\mathrm{peak,DCM}}[n+1]$, are presented as in (5) and (6), and they are shown in Fig. 5, where $\Delta i_L[n+1]$ means the predicted boost inductor current ripple

$$\begin{aligned} i_{L,\mathrm{peak,CCM}}[n+1] &= i_{L,\mathrm{avg,ref}}[n+1] + \Delta i_L[n+1] \\ &= i_{L,\mathrm{avg,ref}}[n+1] + \frac{v_{\mathrm{in}}[n+1]}{2L} d_{\mathrm{CCM}}[n+1]T_S, \end{aligned} \tag{5}$$

$$\begin{aligned} i_{L,\mathrm{peak,DCM}}[n+1] &= 2\Delta i_L[n+1] \\ &= \frac{v_{\mathrm{in}}[n+1]}{L} d_{\mathrm{DCM}}[n+1]T_S. \end{aligned} \tag{6}$$

Fig. 6 presents waveforms of predicted peak inductor currents in the PPCC. As shown in Fig. 6, it is possible to make the ideal sinusoidal average inductor current by controlling the peak inductor current. Besides, since the current transition from DCM to CCM softly occurs, the current distortion in MCM can be minimized.

C. Adaptive Artificial Slope Prediction

The subharmonic oscillation of the peak current control occurs when the duty ratio is above 50%. In order to solve this problem, the slope compensation which adds a constant artificial slope ramp to the control output or the inductor current is commonly used [3], [22]. However, the slope compensation with the constant artificial slope ramp is inadequate for the PFC PCC due to its wide input voltage range [22]. Consequently,

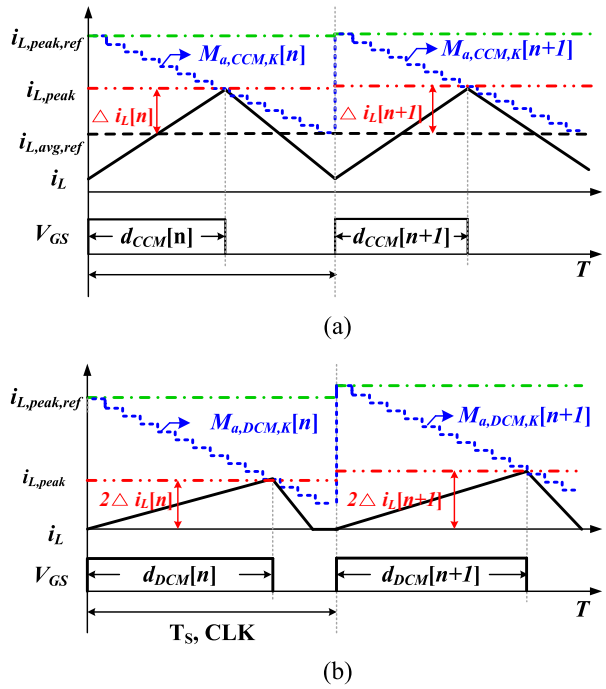


Fig. 5. Predicted peak inductor current waveforms. (a) CCM. (b) DCM.

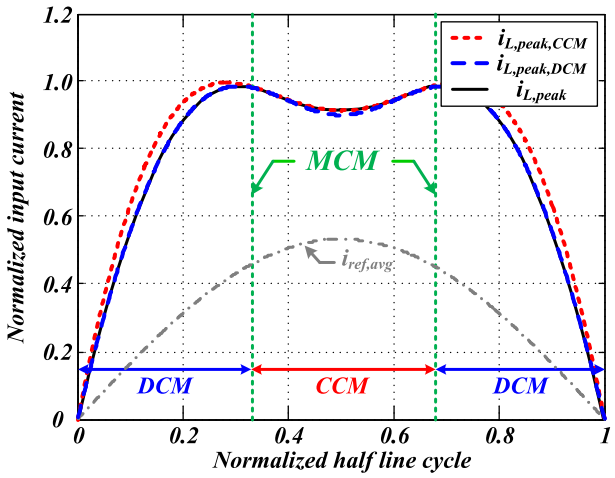


Fig. 6. Peak inductor current waveforms.

the adaptive artificial slope ramp should be required to reject undesirable disturbances.

Generally, the artificial slope ramp for the PCC should be more than a half falling slope of the inductor current and less than a falling slope of the inductor current for stability over the entire duty ratio [3]. To generate this artificial slope ramp, the PPCC utilizes a 16-bit high-resolution ramp generator which is integrated in DSP as depicted in Fig. 7. This high-resolution ramp generator makes the adaptive artificial slope ramp by accumulating $M_{a.K}[n+1]$ on every counter clock, i.e., $M_{a.K}[n+1]$ means an adaptive artificial slope corresponding to one counter clock of the integrated high-ramp generator. Considering the high-resolution ramp generator and falling slope of

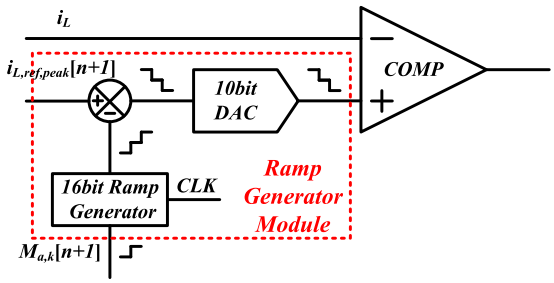


Fig. 7. Block diagram of the internal high-resolution ramp generator and comparator.

the boost inductor current, the CCM minimum and maximum adaptive artificial slope corresponding to one counter clock, i.e., $M_{a.\mathrm{CCM},K,\min}[n+1]$, $M_{a.\mathrm{CCM},K,\max}[n+1]$, are presented as

$$\begin{aligned} M_{a,\mathrm{CCM},K,\min}[n+1] &= \frac{T_S\left(v_O[n]-v_{\mathrm{in}}[n+1]\right)}{2L\cdot\mathrm{CLK}} \\ &= \frac{T_S d[n+1]v_O[n]}{2L\cdot\mathrm{CLK}}, \\ M_{a,\mathrm{CCM},K,\max}[n+1] &= \frac{T_S d[n+1]v_O[n]}{L\cdot\mathrm{CLK}}, \end{aligned} \tag{7}$$

where CLK means a total ramp generator counter clock during one switching period.

To maximize stability in the current control and obviate the subharmonic oscillation resulting from the inductance tolerance, the CCM adaptive artificial slope ($M_{a.\mathrm{CCM},K}[n+1]$) should be determined at the midpoint between $M_{a.\mathrm{CCM},K,\max}[n+1]$and $M_{a.\mathrm{CCM},K,\min}[n+1]$, and $M_{a.\mathrm{CCM},K}[n+1]$ can be expressed as

$$\begin{aligned} M_{a,\mathrm{CCM},K}[n] &= \frac{3T_S\left(v_O[n]-v_{\mathrm{in}}[n+1]\right)}{4L\cdot\mathrm{CLK}} \\ &= \frac{3T_S d[n+1]v_O[n]}{4L\cdot\mathrm{CLK}}. \end{aligned} \tag{8}$$

Considering $M_{a.\mathrm{CCM},K}[n+1]$, the proposed PPCC can effectively suppress the subharmonic oscillation and instability up to $\pm 33.33\%$ inductance discrepancy.

On the other hand, the boost converter in DCM is stable without the slope compensation. However, if DCM and CCM operation regions are mistakenly detected, the subharmonic oscillation occurs in MCM, and the boost PFC converter is no longer stable. In order to avoid instability in MCM, the slope compensation can also be included in DCM. For the imperceptible transition in MCM, the MCM adaptive slope can be selected for DCM. As a result, the DCM adaptive artificial slope ($M_{a,\mathrm{DCM},K}[n+1]$) which copes with *CLK* can be expressed as in (8) and illustrated in Fig. 5(b), where $d_{\mathrm{MCM}}[n+1]$ means $2L/(T_s R_e[n])$

$$\begin{aligned} M_{a,\mathrm{DCM},K}[n+1] &= M_{a,\mathrm{MCM},K}[n+1] \\ &= \frac{3T_S d_{\mathrm{MCM}}[n+1]v_O[n]}{4L\cdot\mathrm{CLK}} \\ &\approx \frac{3v_O[n]}{2R_e[n]\mathrm{CLK}}. \end{aligned} \tag{9}$$

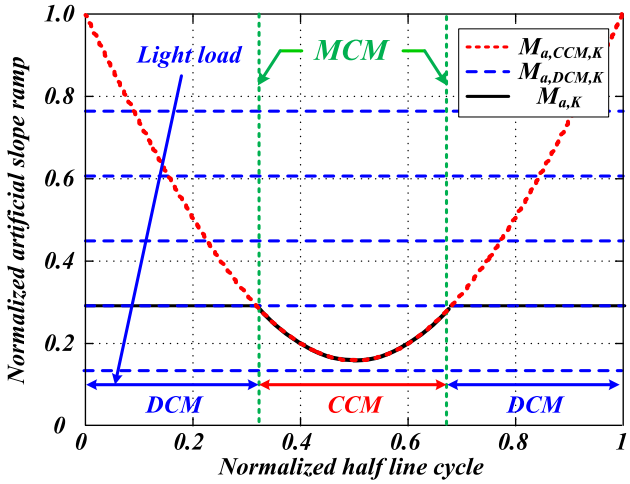


Fig. 8. Normalized artificial slope ramp.

Fig. 8 shows the normalized adaptive artificial slope during the half-line cycle. Since $M_{a.\mathrm{DCM},K}[n+1]$ is inversely proportional to $R_e[n]$, $M_{a.\mathrm{DCM},K}[n+1]$ is decreased as the load is decreased. As a result, a lower value between $M_{a.\mathrm{CCM},K}[n+1]$ and $M_{a.\mathrm{DCM},K}[n+1]$ should be chosen as $M_{a,K}[n+1]$ to reduce the effect of the excessive slope compensation in DCM. In addition, in light-load conditions, because of small $M_{a.K}[n+1]$, the effect of $M_{a.K}[n+1]$ can be ignored, and the PPCC can efficiently suppress the current distortion caused by unpredictable current oscillations in DCM.

D. Peak Current Reference Correction and Adaptive Slope Compensation

To eliminate the current distortion near the zero crossing of the input voltage resulting from the slope compensation [22], $i_{L,\mathrm{peak}}[n+1]$ should be corrected considering the adaptive slope compensation. From the peak inductor current, adaptive artificial slope, and duty ratio, the predicted peak current reference ($i_{L,\mathrm{peak,ref}}[n+1]$) can be corrected and determined as in (10), and it is also shown in Fig. 5

$$i_{L,\mathrm{peak,ref}}[n+1] = i_{L,\mathrm{peak}}[n+1] + M_{a,K}[n+1]d[n+1]\mathrm{CLK}. \quad (10)$$

The ramp generator module in the DSP shown in Fig. 7 subtracts the predicted adaptive artificial slope from this revised peak current reference on every counter clock of the integrated ramp generator, so the carrier signal including the slope compensation is generated. By using the integrated comparator, the proposed PPCC turns OFF the switch providing the cycle-by-cycle current restriction, when the carrier signal intersects with the inductor current. Therefore, the proposed PPCC controls the peak inductor current, and it reduces the input current distortion which is unavoidable in the conventional DFF ACC. In addition, $i_{L,\mathrm{peak,ref}}[n+1]$ is independent of input and output voltage disturbances, so a high sampling frequency to enlarge the current control loop bandwidth and gain is not required, and the burden of the DSP can also be reduced.

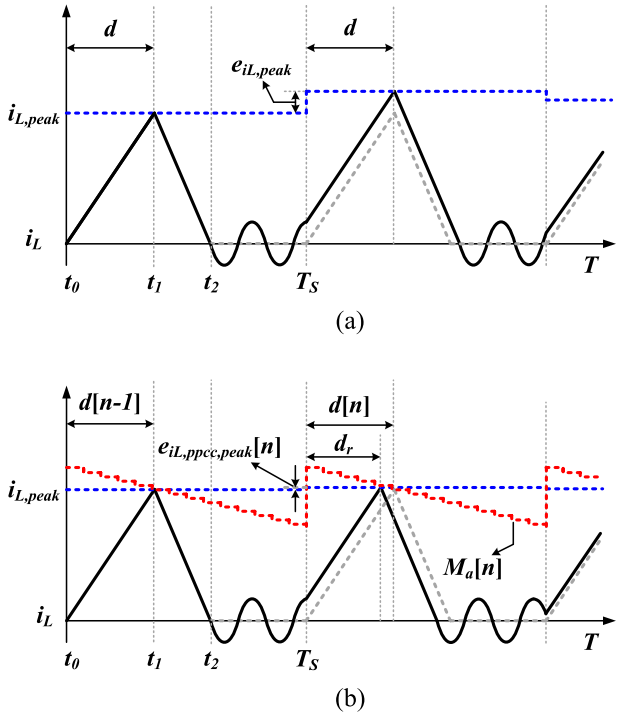


Fig. 9. Inductor current waveforms in DCM. (a) DFF ACC. (b) PPCC.

III. Analysis of Current Distortion

The proposed PPCC can considerably curtail the current distortion not only in DCM but also in MCM, and it can achieve a low total harmonic distortion (THD) especially in DCM by suppressing unpredictable inductor current oscillations in DCM. However, a little current distortion in light-load conditions can occur owing to the effect of the small slope ramp compensation. Moreover, iron powder cores utilized in the PFC converter have up to 10% inductance tolerance in manufacturing. This inductance tolerance brings about the inductance discrepancy and inaccurate prediction of the PPCC resulting in the input current distortion. Therefore, the effects of the slope compensation in DCM and inductance tolerance are analyzed in this section.

A. Current Distortion in DCM

The resonance in DCM caused by the boost inductance (L) and output capacitance of the switch (C_{oss}) brings about inductor current oscillations in DCM which vary depending on the continuously changing input voltage as expressed below and shown in Fig. 9(a)

$$i_{L,r}(t) = -i_{L,r}\sin(\omega_r(t-t_2)) = \begin{cases} -\dfrac{v_O - v_{\mathrm{in}}}{Z_r}\sin(\omega_r(t-t_2)), & v_{\mathrm{in}} \geq \dfrac{v_O}{2} \\ -\dfrac{v_{\mathrm{in}}}{Z_r}\sin(\omega_r(t-t_2)), & v_{\mathrm{in}} < \dfrac{v_O}{2} \end{cases} \quad (11)$$

where $\omega_r = 1/\sqrt{LC_{oss}}$ and $z_r = \sqrt{L/C_{oss}}$.

In addition, these current oscillations in DCM have influences on the irregular current peak of the boost inductor ($e_{iL,\mathrm{peak}}$).

As a result, the effects of current oscillations in DCM are unpredictable, and high-frequency disturbances in current control loop occur resulting in the current distortion. Meanwhile, the proposed PPCC enables the peak inductor current to follow the predicted peak inductor current value as illustrated in Fig. 9(b). Although the small peak current error ($e_{iL,\mathrm{ppcc,peak}}[n]$) in DCM can be generated by the slope compensation as expressed in (12), the effect of the slope compensation is reduced as load is decreased due to the small adaptive artificial slope

$$e_{iL,\mathrm{ppcc,peak}}[n] = e_{iL,\mathrm{peak}}[n]\left(1 - \frac{v_{\mathrm{in}}[n]T_S/L}{v_{\mathrm{in}}[n]T_S/L + M_a[n]}\right). \tag{12}$$

Because of this reason, the PPCC has almost no effect on the input and inductor currents in light-load conditions, and it can mostly get rid of the input current distortion. Therefore, the PPCC can increase the power quality in light-load conditions.

B. Average Inductor Current Error in One Switching Cycle With Inductance Discrepancy

The inductance discrepancy resulting from the tolerance as well as current oscillations in DCM affects the performance of the PPCC as shown in Fig. 10. Thus, the average inductor current error ($e_{iL,\mathrm{avg}}[n]$) in one switching cycle according to each operation region, i.e., CCM, DCM, and MCM, is analyzed in the following.

1) CCM: The average inductor current error in CCM ($e_{iL,\mathrm{avg,CCM}}[n]$) is determined by the inductance difference as shown in Fig. 10(a). Considering this, the average inductor current with the inductance discrepancy ($i_{L,\mathrm{avg,dis}}[n]$) and $e_{iL,\mathrm{avg,CCM}}[n]$ can be obtained as follows:

$$\begin{aligned} i_{L,\mathrm{avg,dis}}[n] =\ & i_{L,\mathrm{avg,ideal}}[n] + \frac{v_{\mathrm{in}}[n]}{2L_{\mathrm{ideal}}}d[n]T_S \\ & - \frac{v_{\mathrm{in}}[n]}{2L_{\mathrm{dis}}}d[n]T_S, \end{aligned} \tag{13}$$

$$\begin{aligned} e_{i_{L,\mathrm{avg,CCM}}}[n] =\ & i_{L,\mathrm{avg,ideal}}[n] - i_{L,\mathrm{avg,dis}}[n] \\ =\ & \frac{v_{\mathrm{in}}[n]d[n]T_S}{2}\left(\frac{L_{\mathrm{ideal}} - L_{\mathrm{dis}}}{L_{\mathrm{ideal}}L_{\mathrm{dis}}}\right), \end{aligned} \tag{14}$$

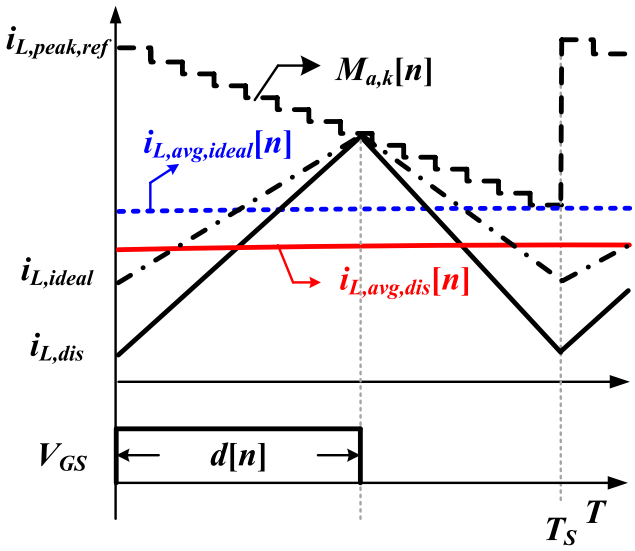
where L_{dis} means the inductance influenced by the tolerance.

2) DCM: As can be seen in Fig. 10(b), the DCM current error ($e_{iL,\mathrm{avg,DCM}}[n]$) is influenced by the inductance discrepancy as well as the adaptive slope compensation. Thereby, the peak inductor current changes, and the polarity of $e_{iL,\mathrm{avg,DCM}}[n]$ is opposite compared with that of $e_{iL,\mathrm{avg,CCM}}[n]$. The peak inductor current with L_{dis} ($i_{L,\mathrm{peak,dis}}[n]$) can be achieved as in (15), where $M_a[n]$ is $M_{a.K}[n] \times \mathrm{CLK}$

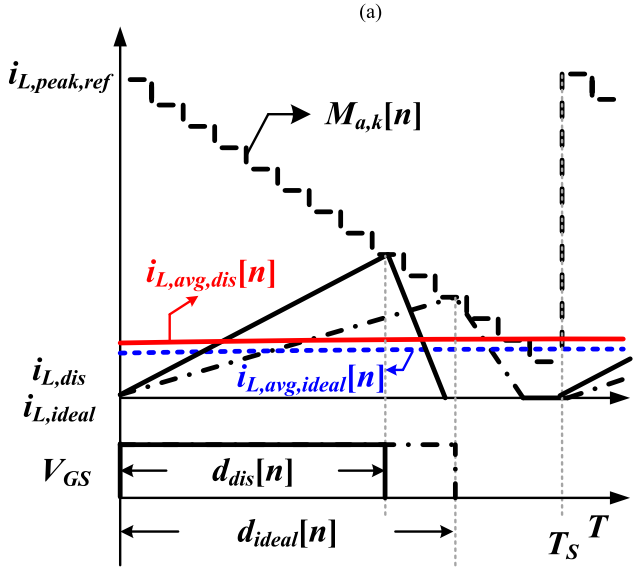
$$\begin{aligned} i_{L,\mathrm{peak,dis}}[n] =\ & i_{L,\mathrm{peak,ideal}}[n] + M_a[n]\left(d_{\mathrm{ideal}}[n] - d_{\mathrm{dis}}[n]\right) \\ =\ & \frac{v_{\mathrm{in}}[n]}{L_{\mathrm{dis}}}d_{\mathrm{dis}}[n]T_S. \end{aligned} \tag{15}$$

By rearranging (15), the duty ratio affected by L_{dis} ($d_{\mathrm{dis}}[n]$) can be derived as in (16)

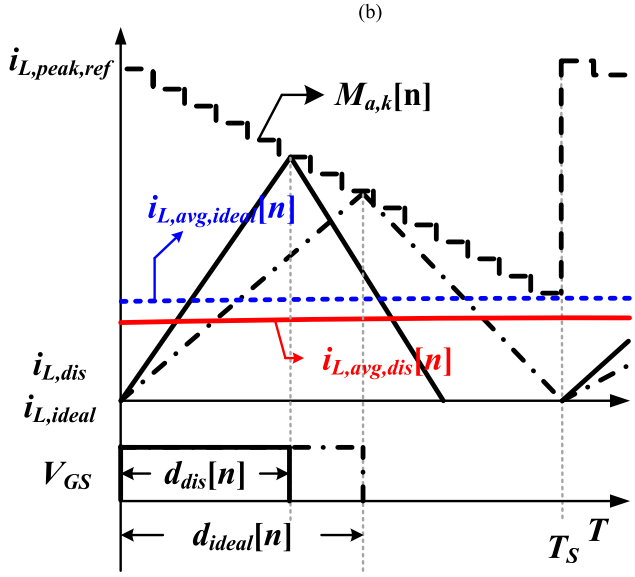
$$d_{\mathrm{dis}}[n] = \left(\frac{K_{\mathrm{ideal}}[n]}{K_{\mathrm{dis}}[n]}\right)d_{\mathrm{ideal}}[n], \tag{16}$$



(a)



(b)



(c)

Fig. 10. Average inductor current error. (a) CCM. (b) DCM. (c) MCM.

where $K_{\text{ideal}}[n]$ is $v_{\text{in}}[n]T_S/L_{\text{ideal}} + M_a[n]$ and $K_{\text{dis}}[n]$ is $v_{\text{in}}[n]T_S/L_{\text{dis}} + M_a[n]$.

From (16), the average inductor current with L_{dis} ($i_{L,\text{avg,dis}}[n]$) and $e_{iL,\text{avg,DCM}}[n]$ can be expressed as

$$i_{L,\text{avg,dis}}[n] = \frac{i_{L,\text{peak}}[n]d_{\text{dis}}[n]}{2d_{\text{CCM}}[n]} = \frac{v_{\text{in}}[n]}{2L_{\text{dis}}}\frac{d_{\text{dis}}^2[n]}{d_{\text{CCM}}}$$

$$T_S = i_{L,\text{avg,ideal}}[n]\left(\frac{K_{\text{ideal}}}{K_{\text{dis}}}\right)^2, \tag{17}$$

$$e_{i_{L,\text{avg}},\text{DCM}}[n] = i_{L,\text{avg,ideal}}[n] - i_{L,\text{avg,dis}}[n]$$

$$= i_{L,\text{avg,ideal}}[n]\left(1 - \left(\frac{K_{\text{ideal}}[n]}{K_{\text{dis}}[n]}\right)^2\right). \tag{18}$$

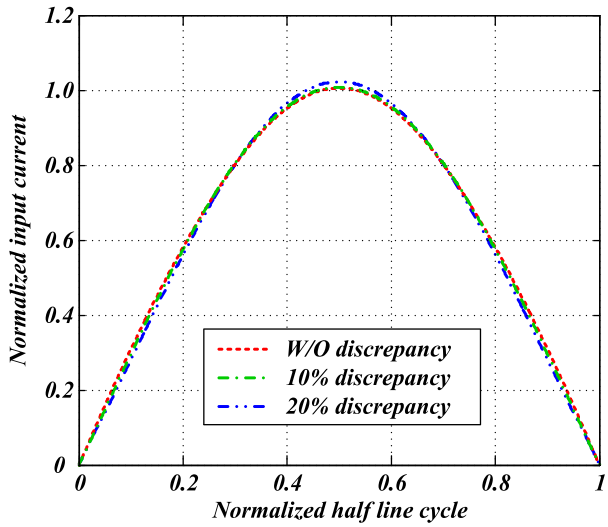
3) MCM: As aforementioned, $e_{iL,\text{avg,CCM}}[n]$ and $e_{iL,\text{avg,DCM}}[n]$ have the opposite signed value at the same inductance discrepancy. Because of this reason, the average inductor current changes significantly in MCM, and it leads to the relatively large current distortion as shown in Fig. 10(c). Based on the same procedure of the DCM analysis, the average inductor current error in MCM ($e_{iL,\text{avg,MCM}}[n]$) can be achieved as

$$e_{i_{L,\text{avg}},\text{MCM}}[n] = i_{L,\text{avg,ideal}}[n] - i_{L,\text{avg,dis}}[n] = i_{L,\text{avg,ideal}}[n]$$
$$\left(1 - \left(\frac{i_{L,\text{avg,ideal}}[n]/d_{\text{ideal}} + (K_{\text{ideal}} + v_{\text{in}}[n]T_S/2L_{\text{ideal}})}{K_{\text{dis}}}\right)^2\right). \tag{19}$$

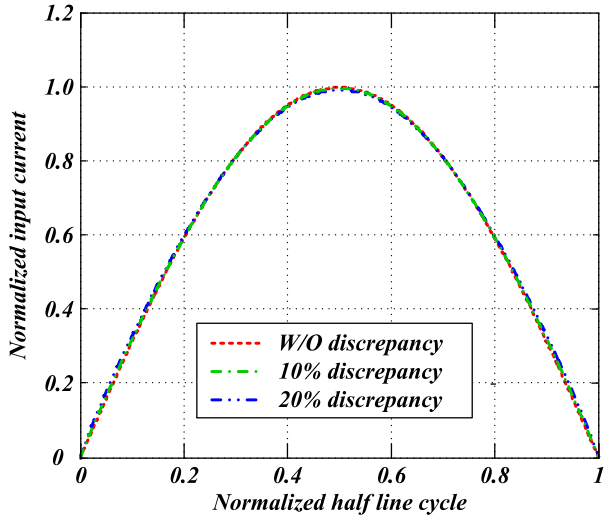
C. Input Current Distortion in One-Line Cycle With Inductance Discrepancy

Fig. 11 presents theoretical input current waveforms with up to 20% inductance discrepancy. This theoretical analysis is implemented at 230 V_{rms} input, 750 W- 400 V output, and 1 mH inductance with 0%, 10%, and 20% tolerance. Assume that the converter fully operates in CCM and DCM as shown in Fig. 11(a) and (b), the effect of the average inductor current errors is much small, because the PF and THD are not influenced by the fundamental component but harmonic components of $e_{iL,\text{avg}}[n]$. Therefore, these errors can be neglected in light- and heavy-load conditions. However, when the boost converter operates in MCM and intermediate-load conditions as shown in Fig. 11(c), the current distortion occurs due to opposite-signed current errors between DCM and CCM. Thus, the larger inductance discrepancy occurs, the more current distortion arises in MCM.

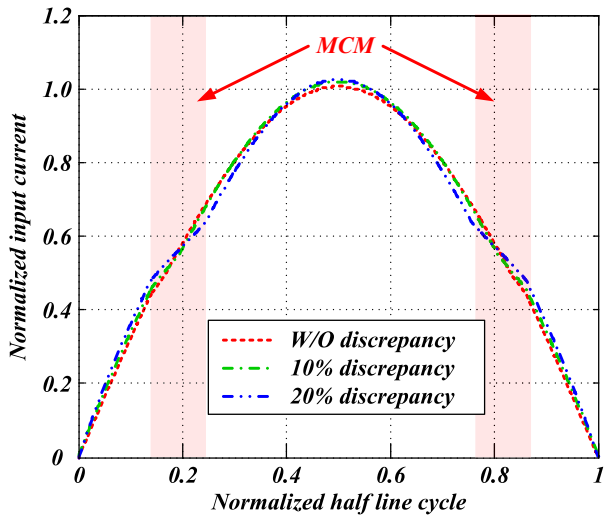
Fig. 12 shows the theoretical harmonic current in intermediate-load conditions which is the worst case of the PPCC. The IEC61000-3-2 Class D harmonics standard is also illustrated in Fig. 12. Despite the most deficient performance of the PPCC in this load conditions, all harmonic components are far smaller than the harmonic standards, and its effect is negligible.



(a)



(b)



(c)

Fig. 11. Normalized input current of PPCC with inductance discrepancy. (a) Heavy-load conditions in CCM. (b) Light-load conditions in DCM. (c) Intermediate-load conditions in MCM.

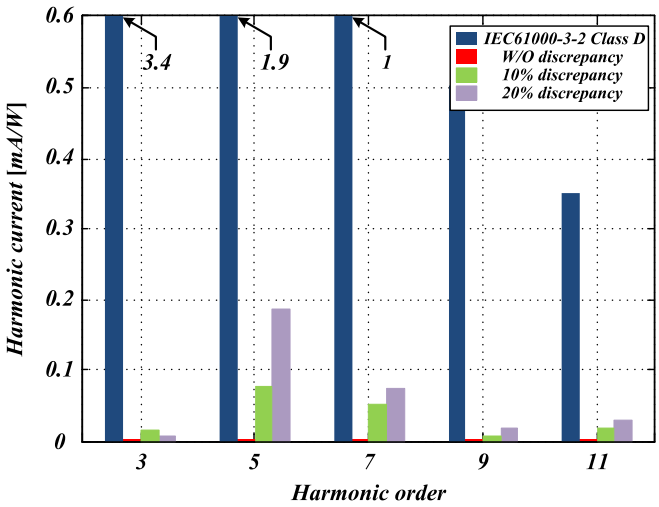


Fig. 12. Theoretical harmonic currents of PPCC with inductance discrepancy in intermediate-load conditions compared to IEC61000-3-2.

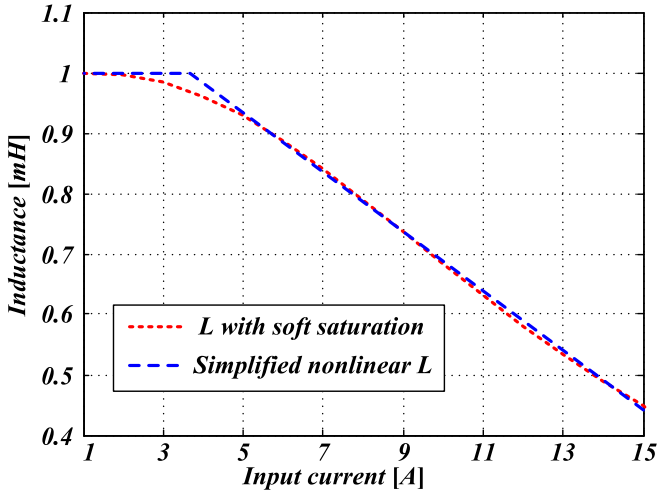


Fig. 13. Nonlinear boost inductance.

TABLE I
DESIGNED PARAMETERS

Input voltage	50 Hz, 230 V_{rms}
Output voltage and power	400 V, 750 W
Switch (Q)	IPP6R099CP6
Diode (D)	D08G60C
Inductor (L)	1 mH
Output capacitor (C_O)	560 μF
Switching Frequency (f_{sw})	45 kHz
Sampling Frequency (f_{samp})	45 kHz

IV. Implementation and Experimental Results

In order to verify the effectiveness of the PPCC, the PPCC is applied to a prototype of the CCM boost PFC converter which is designed for 750-W and 80 Plus titanium server power supply. Table I shows design parameters of the prototype. To maximize efficiency, the boost PFC converter adopts the silicon carbide Schottky diode which solves reverse recovery problems, and the switching frequency is selected as 45 kHz to reduce the switching loss. The boost inductor is designed to be about 1 mH using the high-flux OD270-1.5 T core with 43 μ permeability for over 0.95 PF in 20% load conditions at 230 $\mathrm{V_{rms}}$. The 450 V $-$ 560 μF capacitor is used as an output capacitor (C_O) to meet the hold-up regulations.

A. Implementation of Proposed PPCC and Conventional DFF ACC

The DSP chosen for the implementation of control algorithms is TMS320F28069PZT from Texas Instrument. With internal comparators and slope ramp generators, the proposed PPCC can be conducted without any additional components. In addition, since the switching frequency is 45 kHz, the sampling and interrupt frequency are also chosen as 45 kHz.

To verify the effectiveness of the proposed PPCC, the DFF ACC is chosen as a conventional control algorithm because of its low input current distortion compared with the other ACC algorithms. Besides, a single-current compensator designed for CCM is used regardless of the conduction modes. This is because the DFF rejects the input and output disturbances and dynamics change. For the conventional DFF ACC, the discrete PID controller is used as a current compensator, and it gave 4kHz cutoff frequency and 45° phase margin. The design procedure of the current compensator is not included in this paper,

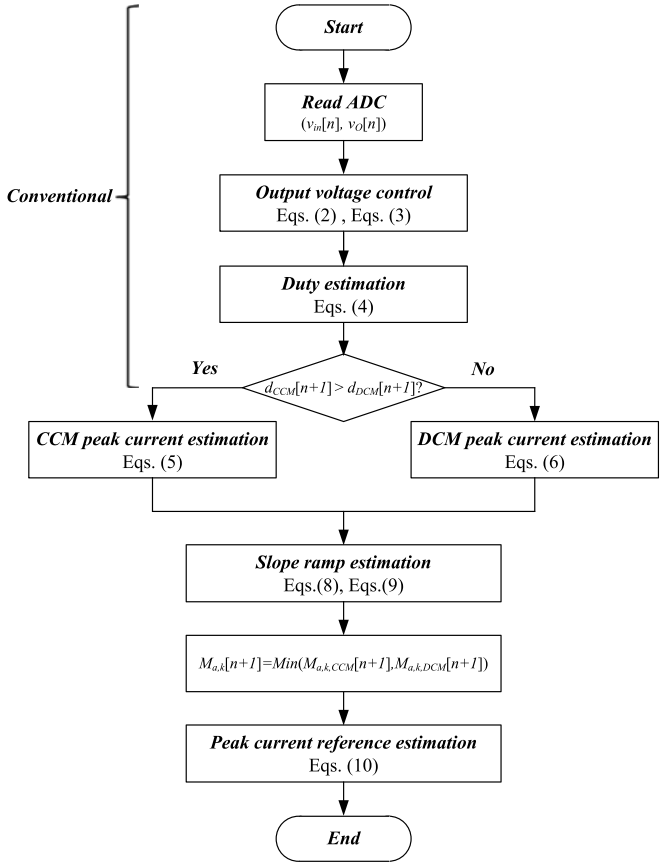


Fig. 14. Flowchart of PPCC.

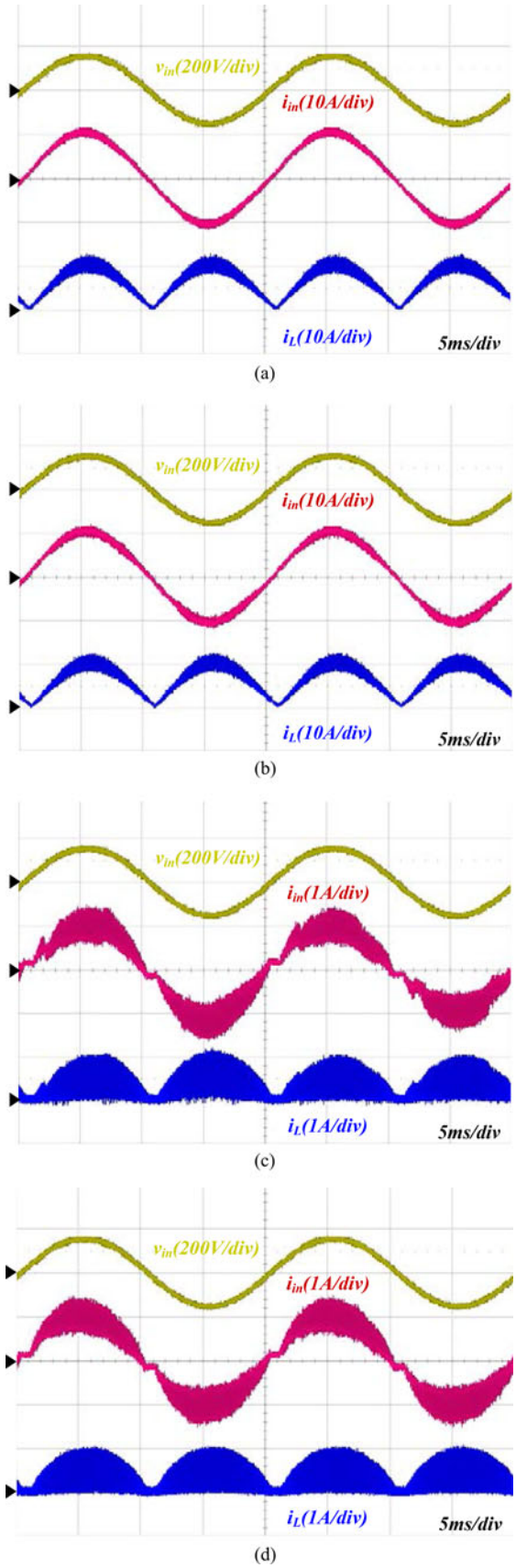


Fig. 15. Experimental waveforms at $110\,\mathrm{V_{rms}}$ and $1\,\mathrm{mH}$. (a) DFF ACC in 100% load conditions. (b) PPCC in 100% load conditions. (c) DFF ACC in 10% load conditions. (d) PPCC in 10% load conditions.

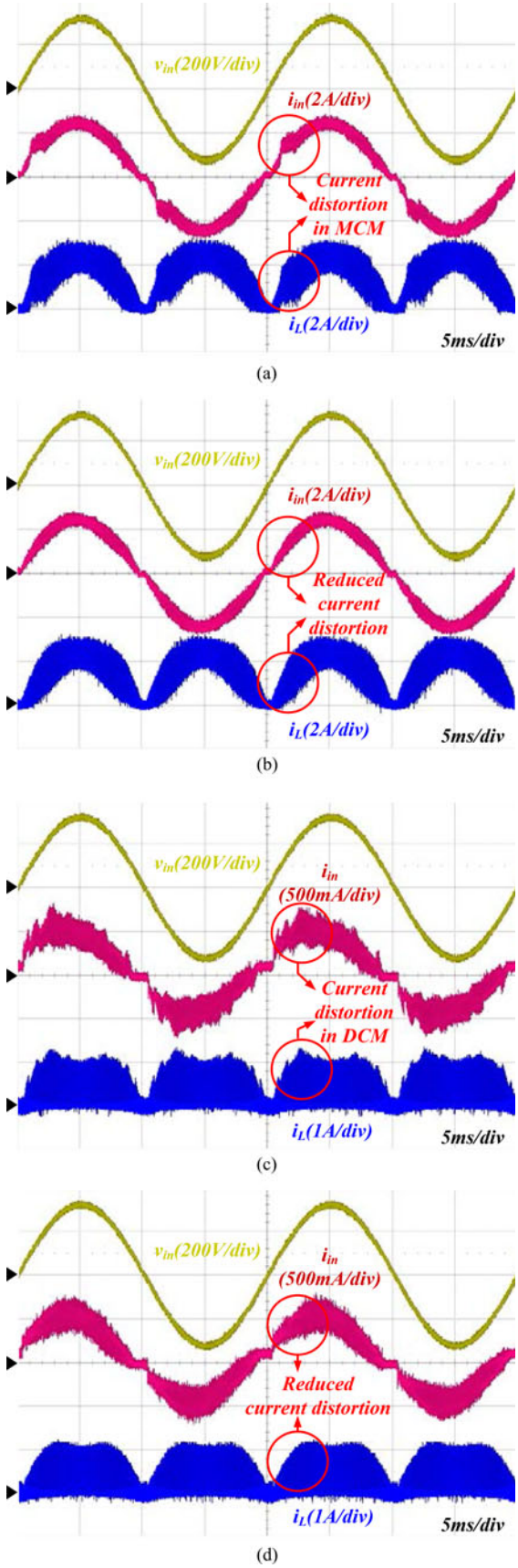


Fig. 16. Experimental waveforms at $230\,\mathrm{V_{rms}}$ and $1\,\mathrm{mH}$. (a) DFF ACC in 50% load conditions. (b) PPCC in 50% load conditions. (c) DFF ACC in 10% load conditions. (d) PPCC in 10% load conditions.

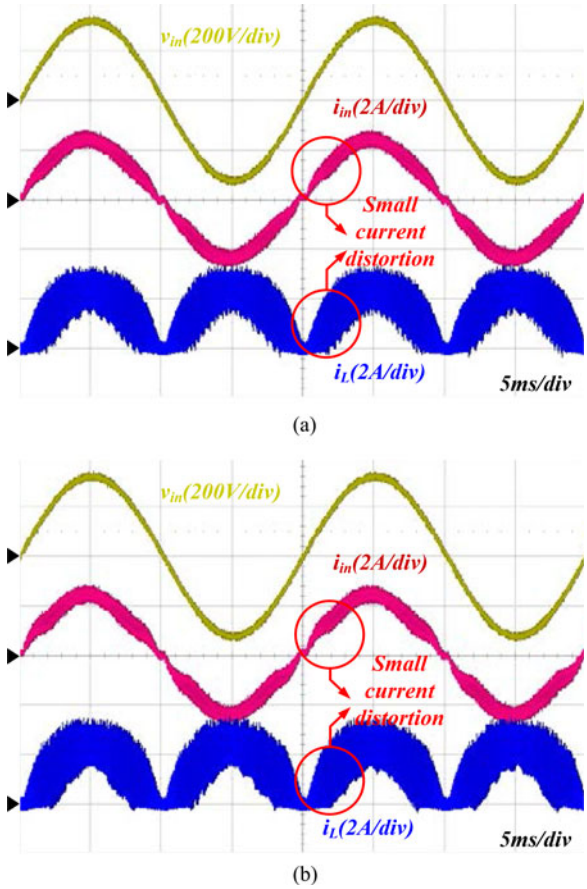


Fig. 17. Experimental waveforms of PPCC with inductance discrepancy in 50% load condition at 230 $\mathrm{V_{rms}}$. (a) 10% inductance discrepancy. (b) 20% inductance discrepancy.

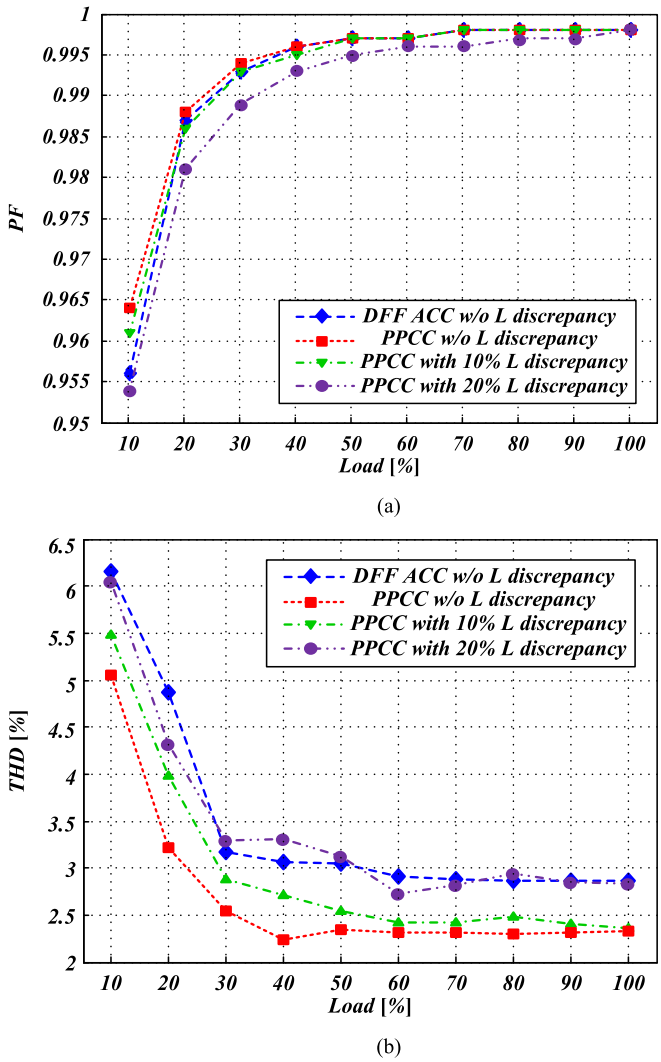


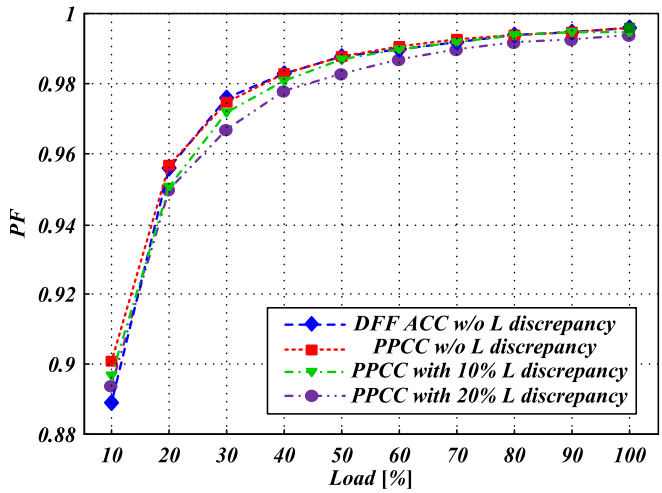
Fig. 18. Measured PF and THD at 110 $\mathrm{V_{rms}}$. (a) PF. (b) THD.

because it is the same as other conventional ACC methods [10], [11], [14], [17].

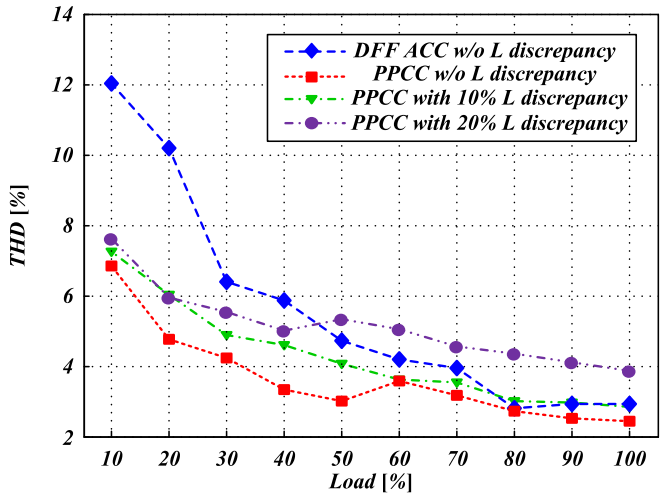
Meanwhile, the proposed PPCC predicts all control variables, and conducts the current control without the current compensator. As a result, it can achieve a fast response in current control and a high-power quality by suppressing the current distortion caused by the low-current loop bandwidth and gain. However, the PPCC is affected by not only the inductance tolerance but also the soft saturation characteristics of the boost inductor as depicted in Fig. 13, and the PPCC cannot guarantee stability with this reduced inductance. To compensate this soft saturation characteristic of the boost inductor, a simple nonlinear inductance as shown in Fig. 13 is adopted in the proposed PPCC. Fig. 14 represents the flowchart of the proposed PPCC during every sampling period. The interrupt starts at every sampling period and the PPCC is conducted by updating $M_{a,k}[k+1]$ and $i_{L,\mathrm{peak,ref}}[n+1]$. At the beginning, $v_{\mathrm{in}}[n]$ and $v_O[n]$ are sensed and sampled by two ADC modules. On the other hand, i_L is directly connected to a negative input of the internal comparator to turn OFF the switch. The output voltage controller provides $i_{L,\mathrm{avg,ref}}[n+1]$ and $R_e[n]$ to regulate $v_O[n]$. $d_{\mathrm{CCM}}[n+1]$ and $d_{\mathrm{DCM}}[n+1]$ are obtained through the duty estimation. Then, the duty and the operation region can be defined by comparing these two estimated duty ratio. After the detection of the operation region, the conventional DFF ACC fulfills ACC through the current compensator. On the other hand, the PPCC carries out the prediction of $i_{L,\mathrm{peak}}[n+1]$ and $M_{a,k}[n+1]$, and determines and updates $i_{L,\mathrm{peak,ref}}[n+1]$ as (10) in Section II.

The output voltage controller designs for both DFF ACC and PPCC are exactly equal [7], [14], [17], because the output voltage controller generates the same average current reference. Thereby, the output voltage compensators of the DFF ACC and PPCC are also designed to reject the disturbance of the output voltage ripple with about 10 Hz control loop bandwidth. Because of this reason, the design procedure of the output voltage controller is omitted in this paper.

The resolution of the high-resolution slope ramp generator is 16-bit as can be seen in Fig. 7. This 16-bit resolution is sufficiently high to precisely generate the artificial slope ramp, so the quantization error of the $M_{a,k}[n+1]$ is small enough and negligible. Moreover, by adjusting the clock of the high-resolution ramp generator, the quantization error of the ramp generator can be minimized. Thus, the quantization error of the $M_{a,k}[n+1]$ is small enough and negligible. On the other hand,

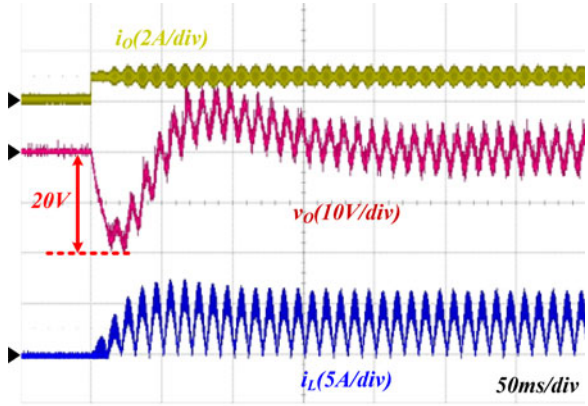


(a)

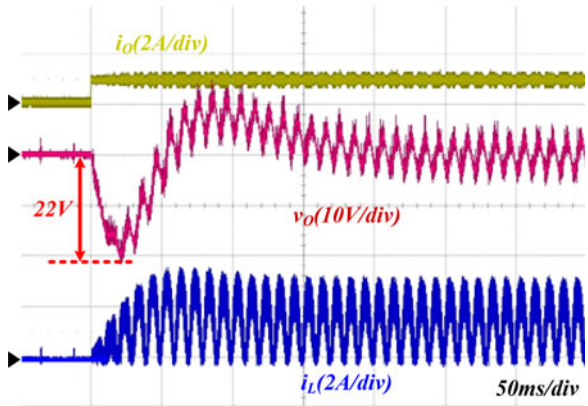


(b)

Fig. 19. Measured PF and THD at 230 V_{rms}. (a) PF. (b) THD.



(a)



(b)

Fig. 20. Experimental waveforms of PPCC with load change. (a) Load change from 0% to 50% at 110 V_{rms}. (b) Load change from 0% to 50% at 230 V_{rms}.

the DAC which is used as a positive input of the comparator has a 10-bit resolution. Despite a relatively lower resolution, the performance of the PPCC is hardly affected by the quantization error of the DAC, because the DAC operates as a low-pass filter, and the 3 mV voltage level is also sufficient to conduct the PPCC. Thus, in this paper, the effect of the quantization error is ignored due to the negligible quantization error.

B. Experimental Result

The experimental waveforms of the DFF ACC and PPCC are shown in Figs. 15 and 16. Both the DFF ACC and PPCC show a low-current distortion, where the boost PFC converter fully operates in CCM as shown in Fig. 15(a) and (b). On the other hand, the input and inductor current waveforms of the DFF ACC show the current distortion in DCM and MCM due to the low control bandwidth, gain, and inaccurate DFF. Meanwhile, the reduced input current distortion is shown in the PPCC waveforms, because the PPCC controls the peak inductor current precisely. Therefore, the drastically low THD can be achieved with the proposed PPCC especially in DCM and MCM.

Fig. 17 shows the waveforms according to the discrepancy of the inductance in half-load conditions at 230 V_{rms}. As previously mentioned, the small inductance discrepancy can be negligible. However, as the inductance discrepancy arises more, the current distortion of PPCC in half-load conditions can be increased as aforementioned in Section III.

The detailed performance comparisons between the conventional DFF ACC and PPCC in various load conditions are presented in Figs. 18 and 19. As shown in Fig. 18, in low input voltage conditions, the power quality of the PPCC is slightly enhanced or almost the same as the conventional method, since the PFC converter mostly operates in CCM and it causes the ignorable current distortion as mentioned in Section III. In high input voltage conditions, assume that there is no inductance discrepancy, the THD is significantly reduced as shown in Fig. 19(b). However, when the inductance discrepancy arises up to 20%, the THD of the proposed PPCC over half-load conditions is increased, since the DCM and MCM operations are expanded near the zero crossing of the input voltage. Despite the THD increment in heavy-load conditions, THD in light-load conditions is significantly reduced regardless of the inductance discrepancy. In addition, the inductor generally has 10% tolerance, so

the 20% inductance discrepancy can be considered as abnormal conditions.

The load regulations and transient characteristics of the PPCC are represented in Fig. 20. Likewise the conventional method, the output voltages are well regulated and vary within 25 V while the load is changed from 0% to 50%.

These experimental results are well matched with the previous analysis in Section III. Therefore, the proposed PPCC has the strength in reducing the current distortion in MCM and DCM.

V. Conclusion

This paper proposes a PPCC employing the adaptive slope compensation for the CCM boost PFC converter, and the validity of this study is confirmed by experimental results. The PPCC is suitable for the digital PFC control due to following reasons.

1) The PPCC reduces the input current distortion without increasing the sampling frequency, since it predicts the precise peak current reference and constraints the peak inductor current.
2) The PPCC is realized by utilizing the internal comparators and slope ramp generator founded in the DSP without external components.
3) There is no need for designing the complex and time-consuming optimization procedure for the current loop compensator, because the current loop control is accomplished in nature.

Therefore, the PPCC is very promising for the CCM boost PFC converter which requires high performance.

References

[1] *Limits for Harmonic Current Emissions (Equipment Input Current $<16A$ per Phase)*, IEC International Standard 1000–3–2, 2001.

[2] 80 PLUS. (2014). [Online]: Available: http://www.plugloadsolutions.com

[3] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Secaucus, NJ, USA: Kluwer, 2001.

[4] Y. S. Kim, W. Y. Sung, and B. K. Lee, "Comparative performance analysis of high density and efficiency PFC topologies," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2666–2679, Jun. 2014.

[5] D. Maksimovic, R. Zane, and R. Erickson, "Impact of digital control in power electronics," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, May 2004, pp. 13–22.

[6] J. B. Williams, "Design of feedback loop in unity power factor AC to DC converter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1989, vol. 2, pp. 959–967.

[7] F. A. Huliehel, F. C. Lee, and B. H. Cho, "Small-signal modeling of the single-phase boost high power factor correction techniques," in *Proc. VPEC Semin.*, Sep. 1992, pp. 93–100.

[8] K. De Gussemé, D. M. Van de Sype, and J. A. Melkebeek, "Design issues for digital control of boost power factor correction converters," in *Proc. IEEE Symp. Ind. Electron.*, Jul. 2002, vol. 3, pp. 731–736.

[9] K. De Gusseme, D. M. Van de Sype, A. P. M. Van den Bossche, and J. A. Melkebeek, "Input-current distortion of CCM boost PFC converters operated in DCM," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 858–865, Apr. 2007.

[10] D. M. Van de Sype, K. De Gusseme, A. P. M. Van den Bossche, and J. A. Melkebeek, " Duty-ratio feedforward for digitally controlled boost PFC converters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 108–115, Feb. 2005.

[11] K. De Gussemé, D. M. Van de Sype, A. P. M. Van den Bossche, and J. A. Melkebeek, "Digitally controlled boost power-factor-correction converters operating in both continuous and discontinuous conduction mode," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 88–97, Feb. 2005.

[12] L. Roggia, F. Beltrame, J. E. Baggio, and J. R. Pinheiro, "Digital control system applied to a PFC boost converter operating in mixed conduction mode," in *Proc. Brazilian Power Electron. Conf.*, Sep. 2009, pp. 698–704.

[13] H. S. Kim, J. K. Kim, K. B. Park, H. W. Seong, G. W. Moon, and M. J. Youn, "On/off control of boost PFC converters to improve light load efficiency in paralleled power supply units for servers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1235–1242, Mar. 2014.

[14] S. F. Lim and A. M. Khambadkone, "A simple digital DCM control scheme for boost PFC operating in both CCM and DCM," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1802–1812, Jul./Aug. 2011.

[15] S. Moon, L. Corradini, and D. Maksimovic, "Autotuning of digitally controlled boost power factor correction rectifiers," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 3006–3018, Oct. 2011.

[16] C. Liou, H. Chieh, and W. Liou, "Design and implementation of a boost power factor correction stage operated in mixed-conduction mode," in *Proc. Int. Conf. Elect. Inf. Control Eng.*, Apr. 2011, pp. 2069–2072.

[17] C. W. Clark, F. Musavi, and W. Eberle, "Digital DCM detection and mixed conduction mode control for boost PFC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 347–355, Jan. 2014.

[18] J. Chen, A. Prodíc, R. Erickson, and D. Maksimovíc, "Predictive digital current programmed control," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 411–419, Jan. 2003.

[19] P. Athalye, D. Maksimovíc, and R. Erickson, "Variable-frequency predictive digital current-mode control," *IEEE Power Electron. Lett.*, vol. 2, no. 4, pp. 113–116, Dec. 2004.

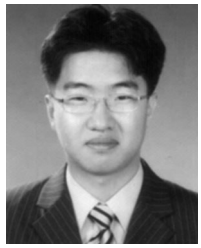
[20] M. Ferdowsi, "An estimative current mode controller for dc-dc converters operating in continuous conduction mode," in *Proc. Appl. Power Electron. Conf.*, Mar. 2006, pp. 19–23.

[21] B. Mather, B. Ramachandran, and D. Maksimovíc, "A digital PFC controller without input voltage sensing," in *Proc. IEEE 22nd Appl. Power Electron. Conf.*, 2007, pp. 198–204.

[22] C. Zhou and M. Jovanovic, "Design trade-offs in continuous current-mode controlled boost power-factor correction circuits," in *Proc. High Freq. Power Convers. Conf.*, May 1992, pp. 209–220.

Han-Shin Youn (S'14) was born in Korea, in 1983. He received the B.S. degree in electrical engineering from Hanyang University, Seoul, Korea, in 2009, and the M.S. degree in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2011, where he is currently working toward the Ph.D. degree.

His main research interests include ac/dc converters, dc/dc converters, drive systems, and digital control method.



Jin-Sik Park (S'08) was born in Korea, in 1981. He received B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2003, 2005, and 2012, respectively.

Since 2012, he has been a Senior Engineer at Samsung Electro-Mechanics, Suwon, Korea. His current research interests include the design of motor drive systems, sensorless drive of ac motor, and dc/dc power converter topology.

Ki-Bum Park (S'07–M'10) was born in Korea, in 1981. He received B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2003, 2005, and 2010, respectively.

He is currently with the ABB Corporate Research Center, Baden-Dättwil, Switzerland, as a Senior Scientist. His current research interests include power electronic converters for renewable energy sources, future energy collection/distribution network, and drive systems. He has published more than 70 papers in technical journals and conferences.

Dr. Park received the second Prize Paper Award at the International Telecommunications Energy Conference 2009 and the third Prize Paper award at Energy Conversion Congress and Exposition-Asia 2011.

Jae-Il Baek (S'14) was born in Korea, in 1988. He received the B.S. degree in electronics and electrical engineering from Sungkyunkwan University, Suwon, Korea, and the M.S. degree in the electrical engineering and computer science from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2015, where he is currently working toward the Ph.D. degree.

His research interests are in the areas of power electronics: DC/DC converters, AC-DC converters, LED driver, battery charger, and digital control approach of converters.

Gun-Woo Moon (S'92–M'00) received the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1992 and 1996, respectively.

He is currently a Professor in the Department of Electrical Engineering, KAIST. His research interests include modeling, design, and control of power converters, soft-switching power converters, resonant inverters, distributed power systems, power-factor correction, electric drive systems, driver circuits of plasma display panels, and flexible ac transmission systems.

Dr. Moon is a member of the Korean Institute of Power Electronics, Korean Institute of Electrical Engineers, Korea Institute of Telematics and Electronics, Korea Institute of Illumination Electronics and Industrial Equipment, and the Society for Information Display.