A Cascade Point of Load DC–DC Converter With a Novel Phase Shifted Switched Capacitor Converter Output Stage

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***Abstract*—This paper presents the analysis, design, modeling and control of a cascaded two-stage step-down dc–dc converter with a conventional synchronous buck converter in the first stage and a new phase shifted switched capacitor (PSSC) buck converter in the second stage. Higher efficiency and higher power density compared to the conventional multiphase buck converter are the prominent features of the proposed architecture which make it suitable as a point of load converter, widely used in powering computing, communication and networking equipment. The first stage buck converter is operated at high switching frequency with extended duty ratio and is designed for high efficiency. The second stage PSSC converter with low input voltage attains high efficiency when operated at a fixed conversion ratio with low switching frequency and a simple constant current charging technique. A laboratory prototype converter achieved a peak efficiency of 86.8% at 30-A load current while operating at 12-V input voltage and 1.3-V output voltage. The capacitor-based output power stage drastically reduces the number of inductors compared to the multiphase buck converter. A low frequency small signal model of the converter and a state feedback controller for the output voltage are developed analytically. The closed-loop transient performance of the converter using this state feedback controller is also verified experimentally.**

***Index Terms*—DC–DC power conversion, dynamic modeling, point of load, state feedback two-stage, switched capacitor.**

I. Introduction

RAPID growth in the capabilities of telecommunications, networking, high-end computing and data processing equipment over the past decade has significantly raised their power consumption. Increasing need for higher currents at multiple low voltages has forced the power supply design engineers to come up with new power supply architectures. Intermediate bus architecture (IBA), offering significant cost savings and size reduction potential (see [1], [2]) has emerged as a popular choice. The intermediate bus converter generates loosely regulated intermediate bus voltages in the range of 6 to 12 V which, in turn, supplies the point of load (PoL) converters strategically placed near the load. These PoL converters must be highly efficient to achieve high overall power delivery efficiency. Proximity to the load and stringent transient specifications also require the PoL converters to be compact and be able to provide fast response.

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Multiphase-interleaved synchronous buck converter [3] has conventionally been adopted as the preferred single-stage PoL converter topology as it offers several benefits such as reduced input and output current ripples, reduced filter capacitance requirement and even heat distribution. However, this topology also suffers from some major drawbacks (see [3], [4]) when operated with large load currents and wide voltage conversion range. The drawbacks are poor ripple current cancelation due to narrow duty cycle operation, increased phase current ripple, increased conduction and switching losses in the MOSFETs, increased conduction loss in the inductor, etc. Moreover, this converter exhibits conflicting requirement (see [4]–[6]) of the phase inductance for satisfactory steady state and transient performance.

To extend the duty ratio of single stage topologies, the coupled-inductor/transformer has been employed. Tapped inductor buck [7], winding-coupled buck [8], phase-shift buck [9], nonisolated double ended topologies (see [10], [11]), nonisolated half bridge [12] and other coupled converters as in [13], [14] are some of the duty ratio extended topologies reported in the literature. The addition of clamp components to recover the leakage energy makes these converter topologies complex and inefficient (see [15], [16]). Also, converters employing magnetics suffer from low power density and control bandwidth unless operated at high switching frequency (see [17]–[19]), at the cost of reduced efficiency.

Soft switching increases the efficiency of high frequency operated converters by eliminating the switching losses. A zero-voltage-switched nonisolated full-bridge converter [10] and an asymmetrical buck converter [20], both operating at 1 MHz, have reported higher efficiencies compared to the conventional two-phase buck converter in the complete load range. However, these converters suffer from low power density due to the additional magnetic components and low light load efficiency. Therefore, it has become imperative to investigate alternate dc–dc converter architectures for PoL application.

The two-stage architecture proposed in [21], [22] uses a low frequency, highly efficient single phase synchronous buck converter in the first stage to step down the high input voltage to an intermediate level. The second stage multiphase buck converter operates at high switching frequency to achieve high control bandwidth. Reduced input voltage of the second stage allows the use of low voltage lateral MOSFETs with low figure of merit (FoM) to minimize the switching and conduction losses. High efficiencies of both the first and the second stages address the efficiency challenge. Also, the efficiency of the two-stage

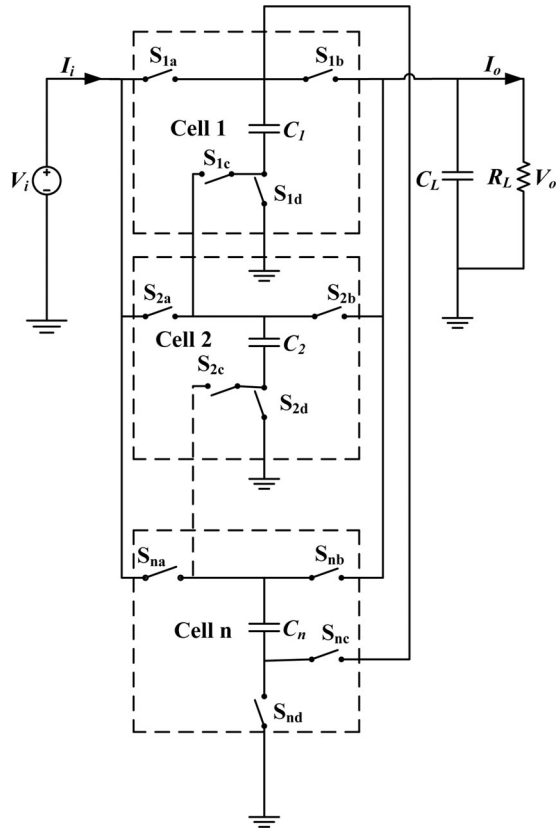


Fig. 1. n-cell PSSC converter.

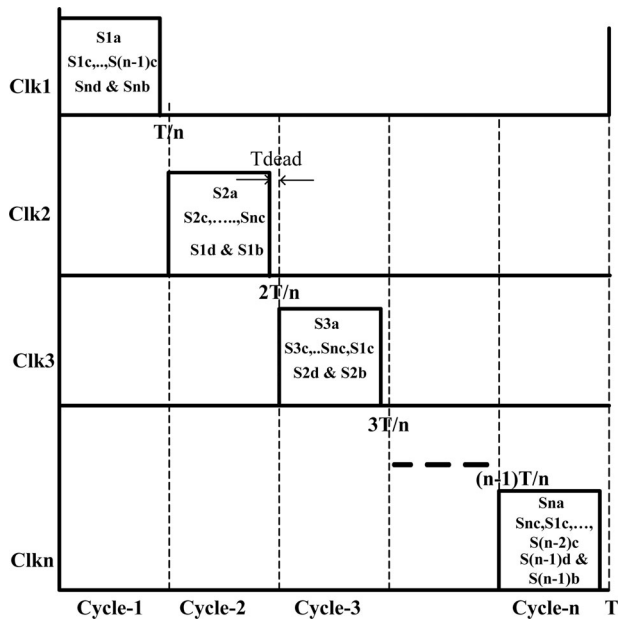


Fig. 2. Timing diagram.

converter is less sensitive to the variations in the input voltage [22]. However, the bulky inductor in the first stage, increases the solution size. To solve this problem, a switched capacitor (SC) voltage divider with fixed conversion ratio has been proposed in [23], [24] to replace the synchronous buck converter in the first stage of [21], [22]. The SC converter [23] achieved high power density of 2500 W/in^3 and a full load efficiency of 97.2%. Efficiency of SC converters drops rapidly as the conversion ratio moves away from the nominal value (see [25]–[27]). Therefore, the two-stage architectures reported in [28]–[30] also use a conventional buck converter in the second stage for regulation.

Another two-stage converter proposed for low power on-chip applications in [31] uses a similar approach but additionally introduces a soft charging technique to enhance the power density and efficiency of the first stage SC converter. The absence of magnetic storage elements in the SC converters and availability of high density capacitors in the standard CMOS technology have resulted in SC converters being increasingly used in low-power on-chip applications (see [32], [33]).

This paper presents a two-stage architecture for dc–dc PoL converters in which the first stage is a high frequency single phase synchronous buck converter designed for high efficiency. The second stage is a newly proposed PSSC buck converter. The PSSC converter is operated at low switching frequency and fixed conversion ratio to attain high efficiency. The line and load regulations of the converter are achieved by adjusting the duty ratio of the first stage. Since the PSSC converter uses only one small output inductor, it is well suited for monolithic integration [34]. Placing this converter at the output stage of the two-stage architecture drastically reduces the number of inductors compared to [23], [24] and increases the power density. The rest of the paper is organized as follows. Section II introduces the PSSC buck converter architecture and constant current charging technique. Section III discusses the design and steady-state performance of the two-stage converter. Section IV presents the dynamic modeling and control of the proposed converter. Implementation details along with experimental results from a laboratory prototype converter are given in Section V-A. Section VI concludes the paper.

II. Phase Shifted SC Buck Converter

The PSSC buck converter comprises basic SC cells connected in series and back to back as shown in Fig. 1. Each SC cell is made of one charge-transfer (CT) capacitor and four switches. The operation of the PSSC converter with n cells is divided into n cycles. If the switching frequency of the converter is $1/T$, the time period of each cycle is T/n. The n phase shifted clocks along with their corresponding ON switches are shown in Fig. 2. Fig. 3 shows the effective circuits of the converter in three consecutive cycles of operation of a three-cell PSSC buck converter. It was shown in [34] that from the analysis point of view, PSSC converter can be considered as the dual of the conventional phase shifted multiphase buck converter. The ideal conversion ratio of the converter was derived in [34] as

$$V_o = V_i/n \tag{1}$$

$$I_i = I_o/n. \tag{2}$$

In an n-cell PSSC converter, the maximum voltage across a switch in any cell is nV_c, and it appears across the switch "c." V_c is the steady-state voltage, assuming negligible voltage

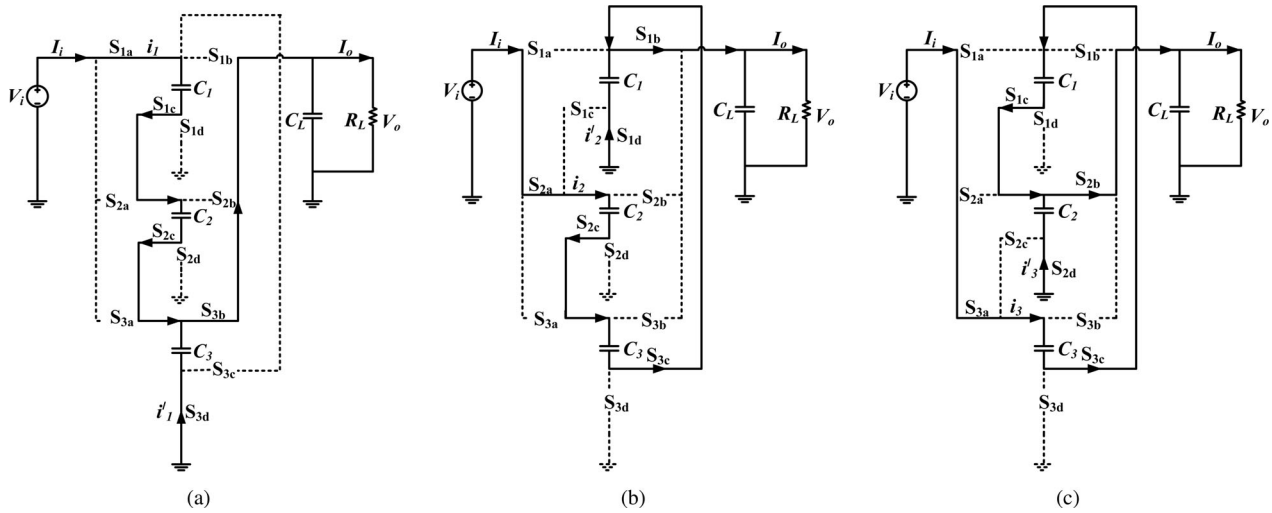


Fig. 3. Effective circuits of operation of a three-cell PSSC converter. (a) Cycle-1. (b) Cycle-2. (c) Cycle-3.

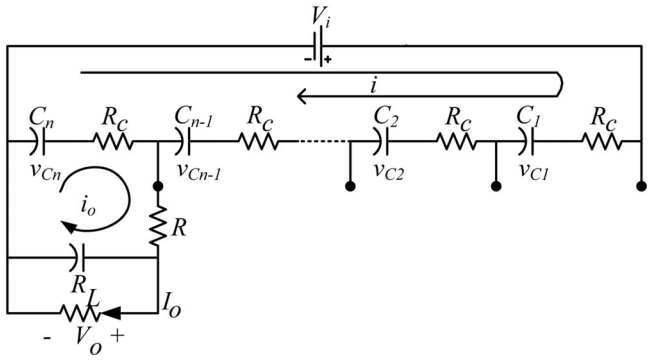


Fig. 4. Equivalent representation of an n-cell PSSC converter over one cycle.

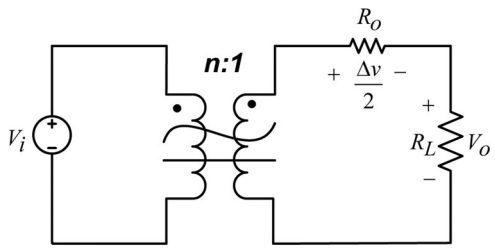


Fig. 5. Dc model of an n-cell PSSC buck converter.

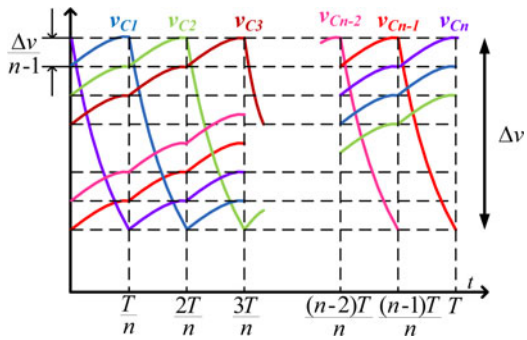


Fig. 6. Steady-state voltage waveforms across the CT capacitors.

ripple, across a CT capacitor. In an ideal n-cell PSSC converter, supplying an output current I_o, "b" switch carries the total output current I_o for one cycle while "d" and "a" switches carry currents $((n-1)/n)I_o$ and I_o/n, respectively, for one cycle. "c" switch carries a current of I_o/n for $n-1$ cycles.

A. Steady-State Equivalent Circuit of the Nonideal PSSC Buck Converter

Fig. 4 shows the equivalent representation of an n-cell PSSC buck converter. The resistor R_C represents the sum of the resistances of the conducting switches in series with the CT capacitor and the ESR of the CT capacitor. The resistor R represents the on-resistance of the switch "b" (see Fig. 1). The conversion losses in the converter can be modeled as the loss in the output resistance R_O of the converter [26] as shown in the dc model of an n-cell PSSC buck converter in Fig. 5. Nonetheless, other losses such as switching and gate drive losses can also be included as in [35].

Fig. 6 shows the voltage waveforms across the CT capacitors. In the case of slow switching limit (SSL), where the charge and discharge time constants are much lower than the switching period, the voltages across the CT capacitors change exponentially and attain their equilibrium in each switching cycle. Output resistance R_O in this case, as shown in the Appendix, follows the SSL given by

$$R_{SSL} = \frac{(n-1)T}{2n^2C}. \tag{3}$$

From (3), it is clear that, in the SSL region, the output resistance is independent of the resistances appearing in the current paths. In the fast switching limit (FSL) case, where the charge and discharge time constants are much higher than the switching period, voltage ripple across the CT capacitors is very low and varies almost linearly. Output resistance R_O in this case, as shown in the Appendix, reaches the FSL given by

$$R_{FSL} = \frac{(n-1)R_C}{n} + R. \tag{4}$$

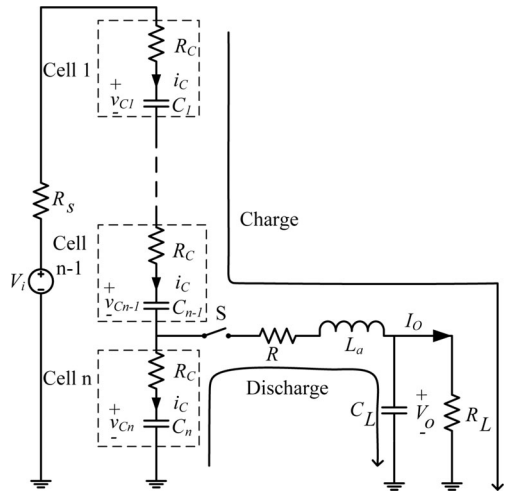


Fig. 7. PSSC converter with auxiliary inductor.

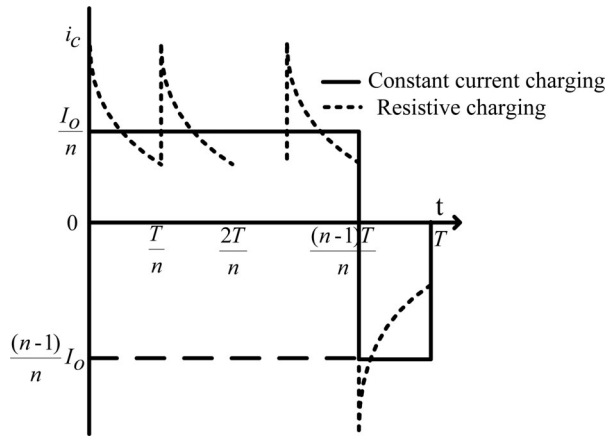


Fig. 8. Current waveforms through the CT capacitors.

From (4), it can be inferred that, the output resistance in the FSL region depends only on the resistances appearing in the charge and discharge paths, and it can be minimized by reducing the on-resistance of the switches. However, in the FSL region, switching and gate drive losses, which are not accounted for in calculating the R_O, become dominant at high switching frequencies.

B. Constant Current Charging

Output resistance in the SSL region can be reduced by either using a large value of the CT capacitance or increasing the switching frequency. Large value of the CT capacitance reduces the power density of the converter, while high switching frequency increases the switching loss. Neither of these approaches is optimal from the design viewpoint of a PoL converter. A simple solution proposed here, to reduce the SSL output resistance, is to place an auxiliary inductor L_a in the path common to both charging and discharging paths of the CT capacitors as shown in Fig. 7. By properly choosing the auxiliary inductor value, exponential currents associated with the resistive charging and discharging are replaced with constant currents as derived in the Appendix and shown in Fig. 8. The output resistance of the PSSC converter in the SSL region with constant current charging, as shown in the Appendix, is the same as the output resistance with resistive charging in the FSL region. Therefore, with the constant current charging technique, it is possible to obtain the low output resistance corresponding to the FSL region, while the converter is still operating in the SSL region. Hence, the auxiliary inductor helps to improve the efficiency of the PSSC converter. Selection of the auxiliary inductor value is described in Section III.

III. Design, Simulation and Loss Analysis of the Two-Stage Buck Converter

A. Design of the Two-Stage Buck Converter

In contrast to [24], in the proposed converter, a synchronous buck converter is used in the first stage to step-down the input

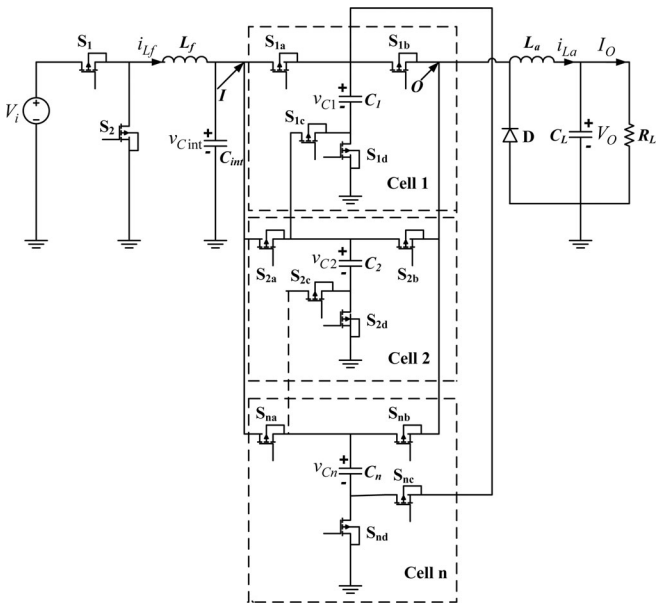


Fig. 9. Cascade two-stage buck converter with an n-cell PSSC converter in the second stage.

voltage to an intermediate level. The second stage is a fixed conversion ratio PSSC converter described in Section II. The placement of the PSSC converter in the second stage serves two purposes: 1) It reduces the required number of discrete inductors. 2) It allows the monolithic integration of the second stage switches in a low voltage, low FoM CMOS process. The two-stage cascade buck converter, with an n-cell PSSC converter in the second stage, is shown in Fig. 9. Let V_O and I_O be the average output voltage and current of the converter. Assuming the PSSC buck converter to be lossless, the average voltage across the CT capacitors is $V_C = V_O$ and the average output voltage of the first stage $V_{\rm cint} = nV_C$. The average current through first stage filter inductor is I_o/n. The effective switching frequency at the input node (I) and the output node (O), shown in Fig. 9, of the PSSC converter is nF, where F is the switching frequency of the second stage PSSC converter. Increased switching frequency at the input and output nodes reduces the input and output filter capacitor

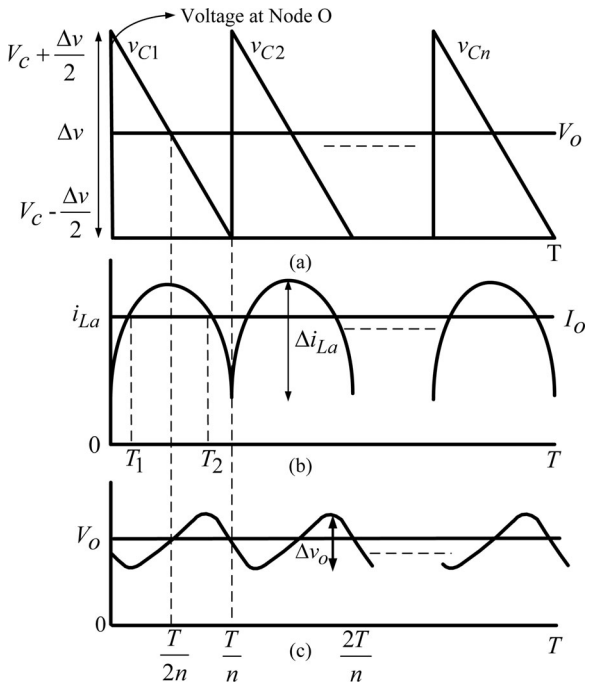


Fig. 10. Output node voltage, auxiliary inductor current and output voltage waveforms.

requirement of the second stage. The intermediate capacitor $C_{\rm int}$ serves both as an output filter of the first stage and an input filter of the second stage. The first stage of the two-stage converter can be designed easily, following any standard method of designing a single phase buck converter with input voltage V_{in}, output voltage nV_o and output current I_o/n. The second stage design, which involves selection of appropriate values of the CT capacitor, the auxiliary inductor and the output capacitor is described next.

1) Voltage Ripple Across the CT Capacitors (Δv): The ideal current waveform through the CT capacitor, with constant current charging technique, is shown in Fig. 8. As per this figure, the peak to peak voltage ripple across the CT capacitor is given by

$$\Delta v = \frac{1}{C}\int_0^{\frac{n-1}{n}T} i_C(t)dt = \frac{1}{C}\times\frac{(n-1)T}{n}\times\frac{I_O}{n}. \quad (5)$$

A higher value of CT capacitance reduces the ripple and increases the efficiency, but will also reduce the power density. Therefore, there will be an inevitable tradeoff between efficiency and power density, while choosing the CT capacitor.

2) Current Ripple in the Auxiliary Inductor (Δi_{La}): Fig. 10(a) shows the instantaneous voltage waveform at node O (refer to Fig. 9), where v_{C1}, v_{C2}....,v_{Cn} are the instantaneous voltages across the CT capacitors C_1, C_2...,C_n. Assuming the PSSC converter to be loss less, the average output voltage V_O is equal to the average voltage across the CT capacitors V_C. Neglecting the output voltage ripple, the instantaneous voltage v_{La} across the auxiliary inductor is given by

$$v_{La} = \left(\frac{\Delta v}{2}\right) - \frac{n\Delta v}{T}\times t, \qquad 0 \le t \le T/n. \quad (6)$$

The peak-to-peak current ripple Δi_{La} in the auxiliary inductor is given by

$$\Delta i_{La} = \frac{1}{L_a}\int_0^{T/2n} v_{La}(t)\,dt \quad (7)$$

$$\Delta i_{La} = \frac{1}{L_a}\left(\frac{1}{2}\times\frac{T}{2n}\times\frac{\Delta v}{2}\right). \quad (8)$$

From (8), it can be observed that the volt-sec, $\frac{\Delta v}{4}\times\frac{T}{2n}$, across the auxiliary inductor is very small. Therefore, the value of the auxiliary inductance required to maintain the given ripple Δi_{La} will be very low. Fig. 10(b) shows the auxiliary inductor current i_{La} along with the average load current I_O.

3) Voltage Ripple Across the Output Capacitor (Δv_o): The average voltage V_O across the output capacitor C_L and its ripple Δv_o are shown in Fig. 10(c). The peak to peak output voltage ripple Δv_o is given by

$$\Delta v_o = \frac{1}{C_L}\int_{T_1}^{T_2} i_{La} - I_O\,dt \quad (9)$$

$$i_{La} = \frac{1}{L_a}\left(\frac{\Delta v}{2}\times t - \frac{n\Delta v}{T}\times\frac{t^2}{2}\right) + I_O - \frac{2}{3}\Delta i_{La} \quad (10)$$

$$\Delta v_o = \frac{1}{C_L La}\left[\frac{\Delta v}{4}(T_2^2 - T_1^2) - \frac{n\Delta v}{6T}(T_2^3 - T_1^3)\right] - \frac{2}{3C_L}\Delta i_{La}(T_2 - T_1) \quad (11)$$

$$T_{1,2} = \frac{T}{2n}\left(1 \mp \frac{1}{\sqrt{3}}\right). \quad (12)$$

A two-stage converter, which can deliver a maximum load current of 60 A at 1.3-V output voltage with 12-V input voltage is designed for a PoL application. The selection of the optimum number of SC cells of the PSSC converter, to maximize the overall efficiency, depends on the input and output voltage specifications of the converter. Less number of second stage SC cells results in high conversion ratio and high output current of the first stage. This leads to a reduction in the first stage efficiency, and thus the overall efficiency. More number of SC cells, on the other hand, also reduces the overall efficiency because of the increased switching and gate drive losses of the second stage. For the input and output voltage specifications chosen previously, it is found that the number of SC cells required for optimal two-stage efficiency is three. A high switching frequency of 1 MHz is chosen for the first stage to reduce the size of the passives and to increase the control bandwidth. Second stage switching frequency is chosen as 170 kHz, much less than that of the first stage, to minimize the switching and gate drive losses. The first stage inductor L_f (220 nH) is chosen for 60% current ripple. Intermediate capacitor $C_{\rm int}$ (50 μF) is chosen for 3% voltage ripple. CT capacitors C_1, C_2 and C_3 (each 196 μF) are designed for 30% voltage ripple. Auxiliary inductor L_a (22 nH) is designed for 10% current ripple. Output capacitor C_L (347 μF) is chosen to maintain a steady-state output voltage

TABLE I
SPECIFICATIONS AND COMPONENT VALUES OF THE TWO-STAGE BUCK CONVERTER

Parameter	Value
Input voltage	12 V
Output voltage	1.3 V
Output voltage ripple	1% V
Maximum output current	60 A
Synchronous buck Switching frequency	1 MHz
PSSC buck Switching frequency	170 kHz
PSSC cells	3
L_f	220 nH, DCR = 2 mΩ
L_a	22 nH, DCR = 0.15 mΩ
C_{int}	50 μF, ESR = 0.1 mΩ
C_1, C_2, C_3	196 μF, ESR = 0.3 mΩ
C_L	347 μF, ESR = 0.1 mΩ

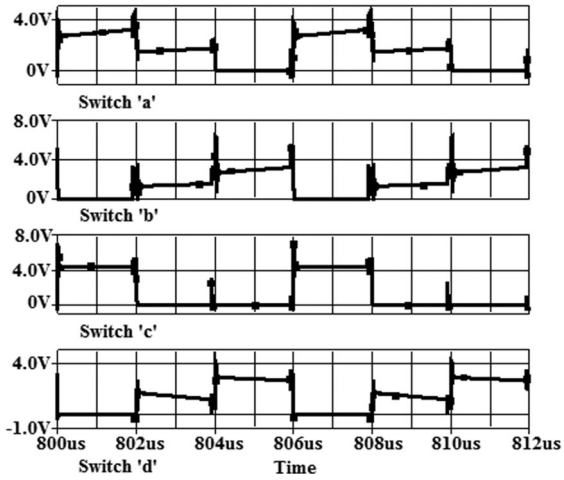


Fig. 11. Voltage waveforms across the switches in an SC cell.

ripple of 0.5%. The specifications and the designed component values of the two-stage converter are summarized in Table I.

B. Loss Analysis of the Proposed Two-Stage Buck Converter

To analyze the losses in the proposed two-stage buck converter, a detailed transient SPICE simulation with accurate device models is carried out for the specifications given in Table I. Fig. 11 shows the voltage waveforms across the switches in an SC cell. Fig. 12 shows the phase shifted voltages across the CT capacitors, auxiliary inductor current and output voltage waveforms. The frequency of the current ripple in the auxiliary inductor and the voltage ripple across the output capacitor is 510 kHz, which is three times the second stage switching frequency of 170 kHz. Ringing observed in the switch voltage and CT capacitor voltage waveforms is due to the output capacitance of the MOSFETs and the parasitic inductance (ESL) of the CT capacitors. In a practical circuit, parasitic inductance also includes the trace inductance and the MOSFET package inductance.

The first stage buck gives greater than 90% efficiency over almost the entire load range because of the widened duty ratio

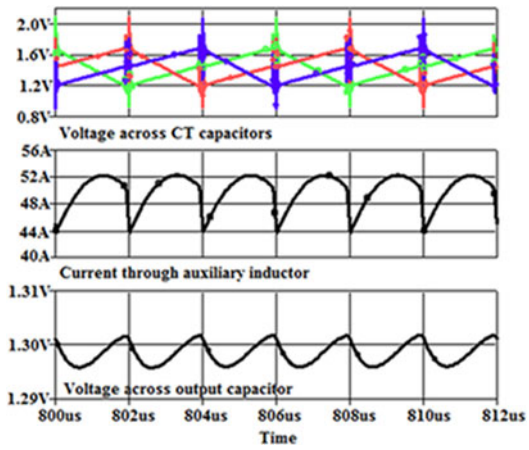


Fig. 12. CT capacitor voltage, auxiliary inductor current and output voltage waveforms.

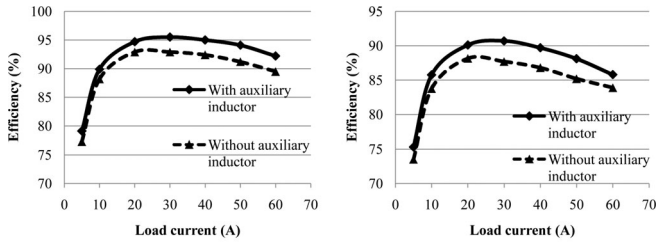


Fig. 13. Estimated efficiency plots. (a) Estimated efficiency of PSSC converter. (b) Estimated efficiency of two-stage buck.

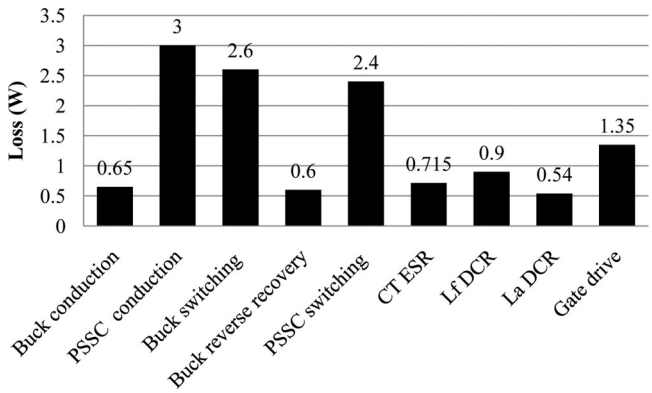


Fig. 14. Loss breakdown at full load.

[36]. Fig. 13 shows the simulated efficiencies of the PSSC converter and the two-stage converter. The efficiency of the PSSC converter is greater than 90% from 10 to 60 A load current. It can also be observed that, the efficiency of the PSSC converter is increased by employing constant current charging using the auxiliary inductor. Fig. 14 shows the loss breakdown of the two-stage converter at 60-A load current.

From Fig. 14, it can be observed that, out of a total MOSFET conduction loss of 3.65 W, the loss in the second stage is 3 W. High RMS currents in the second stage MOSFETs account for higher conduction loss. On the other hand, the switching losses in the first and second stages are nearly equal. Switching

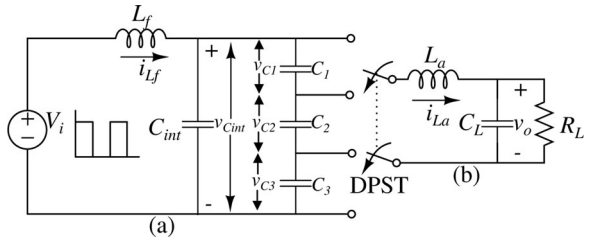


Fig. 15. Schematic representation of the two-stage converter.

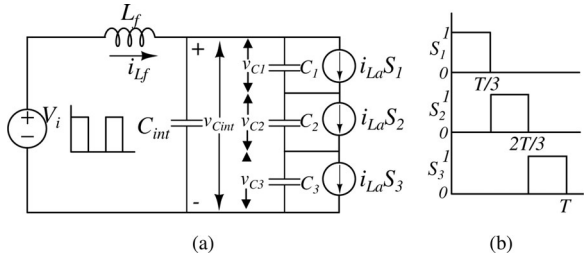


Fig. 16. (a) Equivalent circuit of Fig. 15(a). (b) Switching functions.

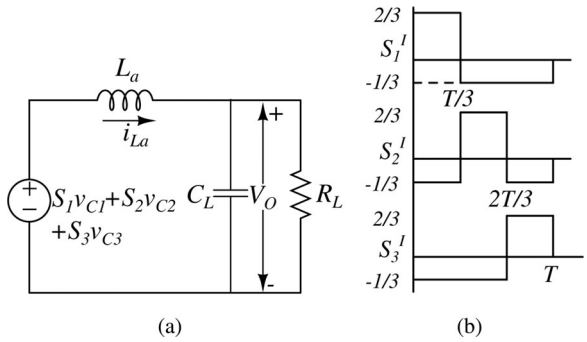


Fig. 17. (a) Equivalent circuit of Fig. 15(b). (b) Modified switching functions.

loss of 2.6 W in the first stage buck converter occurs only in the top MOSFET. High switching frequency (1 MHz), at full input voltage of 12 V, is the reason for this high switching loss. Reduced input voltage and low switching frequency reduces the switching losses in the second stage, in spite of its large number of switches. The gate drive loss of 1.35 W is dependent only on the MOSFET gate voltage, total gate charge and the switching frequency, but is independent of the load current. At light loads, the fixed gate drive loss dominates over the load dependent conduction and switching losses. Therefore, the efficiency of the two-stage converter [see Fig. 13(b)] drops sharply when the load current falls below a certain limit.

IV. Dynamic Modeling and Control of the Two-Stage Converter

An approximate small-signal model of the converter is derived in this section to find out various transfer functions of the converter. The accuracy of the derived model is verified by comparing the frequency response of the model with the Cadence periodic steady state-periodic ac (PSS-PAC) analysis. The following approximations were made in deriving the small-signal model:

1) switching ripples in the inductor currents and the capacitor voltages in both the stages are neglected and only the average values over a switching period are considered;
2) all components (i.e., CT capacitors, switches and inductors) are assumed to be ideal;
3) the dead time between the cycle transitions in the second stage PSSC converter is neglected.

A. Dynamic Modeling

Fig. 15 shows the schematic representation of an ideal two-stage converter with three cells in the second stage. The switching action of the first stage buck is represented by the pulsed voltage source connected to the input of this circuit. i_{Lf} and i_{La} are the first stage and second stage average inductor currents and v_{C1}, v_{C2} and v_{C3} are the average voltages across the PSSC CT capacitors. $v_{C\mathrm{int}}$ is the average voltage across the first stage capacitor. To simplify the modeling exercise the output section of the PSSC converter consisting *LC* filter (L_a, C_L) and the load is separated from the rest of the converter through a double pole single throw switch. This output section gets connected sequentially to each of the PSSC CT capacitors within one second stage switching period which results in the same circuit topologies in different second stage switching cycles as in the actual converter.

Fig. 16(a) shows the equivalent circuit of Fig. 15(a). The second stage switching operation can be represented by the switching functions S_1, S_2 and S_3, shown in Fig. 16(b), for one second stage switching period. Therefore, the switching currents across each of the PSSC CT capacitors will be $i_{La}S_1$, $i_{La}S_2$ and $i_{La}S_3$.

Fig. 17(a) shows the equivalent circuit of Fig. 15(b) in which the switching voltage across the output section is represented by the function $S_1v_{C1} + S_2v_{C2} + S_3v_{C3}$

$$\begin{aligned} S_1v_{C1} + S_2v_{C2} + S_3v_{C3} &= S_1v_{C1} + S_2v_{C2} + S_3v_{C3} \\ &+ \frac{(v_{C1} + v_{C2} + v_{C3})(S_1 + S_2 + S_3)}{3} \\ &- \frac{(v_{C1} + v_{C2} + v_{C3})(S_1 + S_2 + S_3)}{3}. \end{aligned} \tag{13}$$

Since $S_1 + S_2 + S_3 = 1$ and $v_{C1} + v_{C2} + v_{C3} = v_{C\mathrm{int}}$

$$\begin{aligned} &S_1v_{C1} + S_2v_{C2} + S_3v_{C3} \\ &= \frac{v_{C\mathrm{int}}}{3} + S_1'v_{C1} + S_2'v_{C2} + S_3'v_{C3} \end{aligned} \tag{14}$$

where the modified switching functions S_1', S_2' and S_3' are given by

$$S_1' = \frac{(2S_1 - S_2 - S_3)}{3} \tag{15}$$

$$S_2' = \frac{(2S_2 - S_1 - S_3)}{3} \tag{16}$$

$$S_3' = \frac{(2S_3 - S_1 - S_2)}{3}. \tag{17}$$

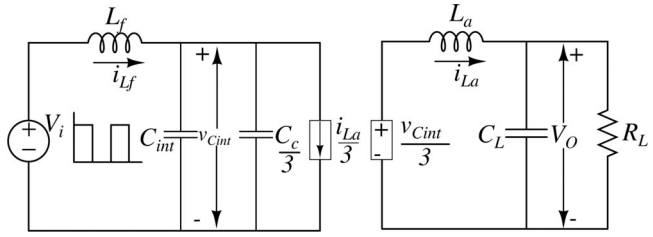


Fig. 18. Equivalent circuit of the two-stage converter.

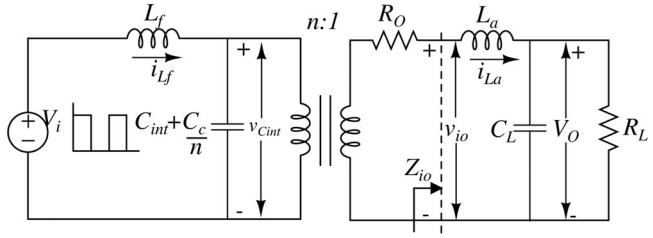


Fig. 19. Generalized equivalent circuit of nonideal two-stage converter.

The switching waveforms $S_1^{'}$, $S_2^{'}$ and $S_3^{'}$ are shown in Fig. 17(b). From Figs. 16(a) and 17(a) the dynamic equivalent circuit of the two-stage converter shown in Fig. 15 is drawn as shown in Fig. 18. The left-hand side of Fig. 18 is obtained by assuming $C_1 = C_2 = C_3 = C_c$ in Fig. 16(a) and taking the Norton equivalent circuit across the $C_{\rm int}$. In order to obtain the right-hand side of this figure it is noted that the lowest frequency component in the Fourier series representation of the modified switching functions $S_1^{'}$, $S_2^{'}$ and $S_3^{'}$ shown in Fig. 17(b) is the second stage switching frequency. If the maximum frequency component present in the perturbation of v_{C1}, $v_{C2}$and v_{C3} is assumed to be low compared to the second stage switching frequency, the terms $S_1^{'}v_{C1}$, $S_2^{'}v_{C2}$ and $S_3^{'}v_{C3}$ will contain only those frequency terms which are close to the second stage switching frequency and its multiples. Neglecting these high frequency components for low frequency modeling, the equivalent circuit of Fig. 17(a) reduces to the right-hand side of Fig. 18. Fig. 18 can be easily generalized, for an ideal two-stage converter with n cells in the second stage, by replacing $'3'$ in Fig. 18 with $'n'$ and the dependent current source voltage source pair by a $n:1$ ideal transformer. In an ideal two-stage converter the output impedance of the PSSC converter is zero. In the case of a nonideal converter, the output resistance R_O of the PSSC converter with constant current charging is given by (4). Fig. 19 shows the equivalent circuit of a nonideal two-stage converter with n second stage cells incorporating the output resistance R_O of the PSSC converter. The audio susceptibility transfer function of the PSSC converter is given by

$$G_{\rm vint}(s) \triangleq \frac{\hat{v}_{io}(s)}{\hat{v}_{Cint}(s)} = \left(\frac{1}{n} \times \frac{Z_{io}(s)}{Z_{io}(s)+R_O}\right) \quad (18)$$

$$\text{where } Z_{io}(s) = sL_a + (R_L/(1+sR_LC_L)). \quad (19)$$

For $R_O << Z_{io}(s)$, $G_{\rm vint}(s) \approx 1/n$. Hence, PSSC converter can be considered as an ideal transformer over the range of frequencies where $R_O << Z_{io}(s)$. Replacing the first stage buck converter in the primary of Fig. 19 with its small signal averaged model and referring the secondary of the $(n:1)$ transformer to the primary, the small-signal average model of the two-stage converter can be obtained and is shown in Fig. 20.

1) Control-to-Output Transfer Function: Output voltage regulation in the proposed two-stage converter is achieved by controlling the duty ratio of the first stage buck converter. The control-to-output transfer function $G_{vd}(s)$ is determined by setting $\hat{v_i} = 0$ and $\hat{i}_{\rm load} = 0$ in the small-signal model shown in Fig. 20

$$G_{vd}(s) = \frac{V_i n R_L (sR_iC_{ie}+1)(sR_{cl}C_L+1)}{s^4d_4 + s^3d_3 + s^2d_2 + sd_1 + d_0} \quad (20)$$

where $C_{ie} = C_{\rm int} + C_c/n$. R_i and R_{cl} are the ESRs of the effective intermediate (C_{ie}) and output (C_L/n^2) capacitors. R_{lf}, R_{la} are the dc resistances of L_f and L_a. The coefficients d_4–d_0 are given in the Appendix. Fig. 21 shows the plots of the frequency response of the control-to-output transfer function using the specifications given in Table I. All the component values, except the load capcitance (C_L), provided in Table I are used in (20). The value of C_L is increased to 1.5 mF to meet the transient overshoot and undershoot specification of 10% of the nominal output voltage. The same frequency response obtained from the PSS-PAC analysis is also superimposed in this figure for the purpose of comparison. The close match between the model prediction and the results obtained from PSS-PAC analysis seen in Fig. 21 validates the model given in Fig. 20. From the frequency response plots it can be observed that the control-to-output transfer function consists of two pairs of complex poles and two real zeroes. One pair of complex poles $(\omega 1)$ are contributed by the auxiliary inductor (L_a) and the output capacitor (C_L) and the other pair $(\omega 2)$ by the first stage filter inductor (L_f) and the equivalent intermediate capacitance (C_{ie}). The two real zeroes are attributed to the output capacitor ESR and the equivalent intermediate capacitor ESR.

B. Control of the Two-Stage Converter

The output voltage of the two-stage converter can be changed by varying the conversion ratio of either the first stage or the second stage or both. The conversion ratio of the first stage buck converter is varied by changing its duty ratio. The conversion ratio of the second stage PSSC converter can be varied by changing its switching frequency. However, the efficiency of SC converters drops rapidly as the conversion ratio moves away from the designed value (see [26], [27]). Therefore, it is desirable to operate the PSSC converter at a fixed conversion ratio and use the duty ratio of the first stage buck converter to control the output voltage.

One approach to control the output voltage is to use a PID compensator with the output voltage feedback. The PID compensator in this case (see Fig. 21) requires one integrator and four lead-lag compensators to achieve adequate stability margins at the desired crossover frequency. For good stability margins the poles of the lead lag compensators must be placed far beyond the loop gain crossover frequency. If the crossover frequency is increased these poles will come too close to the second stage effective switching frequency. The resulting compensator will

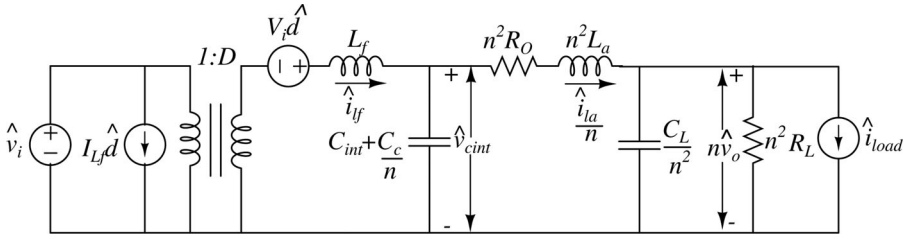


Fig. 20. Small-signal average model of the two-stage converter.

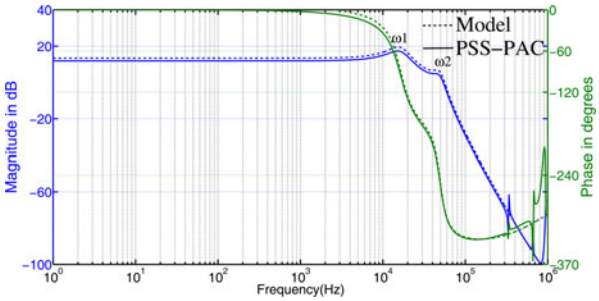


Fig. 21. Control-to-output frequency response plots obtained from small-signal model and PSS-PAC analysis.

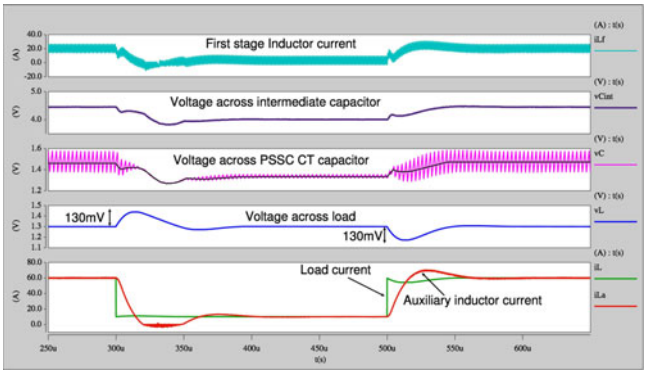


Fig. 22. Simulated load-transient response of two-stage converter with full state feedback controller.

have a large high frequency gain which will amplify the output voltage ripple and interfere with proper operation of the converter. Hence, using a simple PID compensator, it is difficult to simultaneously achieve wide control bandwidth and a low high frequency gain. Another effective approach to control the output voltage is to use a full state feedback controller which gives complete control over the placement of all the closed loop poles provided the system is fully controllable. The small-signal averaged model of the generalized ideal two-stage converter can be written in the state space form as

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} \tag{21}$$

$$y = C\hat{x} + D\hat{u} \tag{22}$$

where $\hat{x} = \begin{bmatrix} \hat{i}_{lf} & \hat{i}_{la} & \hat{v}_{\rm cint} & \hat{v}_o \end{bmatrix}^T$ is the state vector and $\hat{u} = [\hat{d}]$ is the control vector.

The state space matrices A, B, C and D are given by

$$A = \begin{bmatrix} 0 & 0 & -1/L_f & 0 \\ 0 & 0 & 1/nL_a & -1/L_a \\ 1/C_{ie} & -1/nC_{ie} & 0 & 0 \\ 0 & 1/C_L & 0 & -1/R_LC_L \end{bmatrix}$$

$$B = \begin{bmatrix} V_i/L_F \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad C = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \quad D = 0.$$

The closed-loop state space description of (21) and (22) with state feedback and integral control action are given by

$$\begin{bmatrix} \dot{\hat{x}} \\ \dot{\delta} \end{bmatrix} = \begin{bmatrix} A - BK & BK_i \\ -C & 0 \end{bmatrix} \begin{bmatrix} \hat{x} \\ \delta \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} \hat{v}_{\rm ref} \tag{23}$$

$$y = \begin{bmatrix} C & 0 \end{bmatrix} \begin{bmatrix} \hat{x} \\ \delta \end{bmatrix} + [0]\hat{v}_{\rm ref} \tag{24}$$

where δ is the output voltage error integrator output, $K = [k_1\ k_2\ k_3\ k_4]$ is the state feedback gain vector and K_i is the integral gain. For the purpose of output voltage regulation, $\hat{v}_{\rm ref} = 0$. Fig. 22 shows the simulated closed-loop transient performance of the converter with the specifications given in Table I and using full state feedback controller with a dominant closed loop real pole at 80 kHz. For a load step of 50 A, with an output capacitance (C_L) of 1.5 mF, output voltage deviation of 130 mV and settling time of 50 μs is observed during both step-up and step-down transients. During transient it can be observed that the average voltage across the second stage CT capacitors closely follows the dynamics of the voltage across the intermediate capacitor. This further justifies Fig. 18 where the effective CT capacitance ($C_c/3$) is connected in parallel to the $C_{\rm int}$. Therefore, the inclusion of the second stage PSSC converter increases the steady-state efficiency of the two-stage converter without introducing any new small-signal frequency dynamics. The dynamic behavior of the two-stage converter is determined only by the first stage $L_fC_{\rm int}$ filter and the output L_aC_L filter.

TABLE II
COMPONENTS USED IN THE PROTOTYPE TWO-STAGE BUCK CONVERTER

Item	Value	Part No
L_f	220 nH	IHLP5050FDERR22M01
L_a	60 nH	FP0805R1-R06-R
C_1, C_2, C_3	$22\,\mu\text{F} \times 8$	GRM21BC81C106KA73L
	$10\,\mu\text{F} \times 2$	GRM32ER61E226KE15K
C_L	$680\,\mu\text{F} \times 2$	RHA0G681MCN1GS
	$10\,\mu\text{F} \times 10$	GRM21BC81C106KA73L
	$4.7\,\mu\text{F} \times 10$	GRM188R60J475ME19D
C_{int}	$10\,\mu\text{F} \times 5$	GRM21BC81C106KA73L
First stage Buck MOSFETs	25 V, 40 A 1 MHz	CSD97370Q5M
Sa, Sc, Sd	30 V, 38 A	CSD17312Q5
Sb	25 V, 100A	PSMN0R9-25YLC
Schottky Diode	15 V, 25 A	MBRB2515LT4G

V. HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. Steady-State Performance

An experimental prototype of the proposed two-stage converter is built to validate the theoretical analysis. The specifications of the prototype are same as those in the Table I. The description of the components used in the prototype is given in Table II. To achieve high efficiency for the first stage, the Texas Instruments power stage IC CSD97370Q5M with integrated gate drivers is used. A low FoM 25-V MOSFET CSD17312Q5 is used in the second stage. It is possible to increase the efficiency of the second stage by using even lower FoM 10-V lateral power MOSFETs [37]. But such low voltage discrete power MOSFETs are still not fully commercially available. Since the RMS current ratings of the switches "b" and "d" in the second stage SC cells are higher, each switch is realized with two MOSFETs in parallel to reduce the conduction losses. CT capacitors are realized with eight 22 μF and two 10 μF ceramic capacitors all in parallel to reduce the RMS currents through each CT capacitor. Due to the unavailability of low inductance (22 nH) and high current (upto 60 A) rating off-the-shelf discrete inductors, auxiliary inductance of 30 nH is realized using two 60-nH discrete inductors in parallel. PWM signals for the first stage buck converter and phase shifted clock signals for the PSSC converter are generated externally from a Xilinx Virtex5 FPGA (XC5VLX50). Fig. 24 shows the photograph of the prototype converter. The prototype is made of a ten-layer, two-ounce PCB. The top layer and four inner layers are used for routing. The bottom layer and the remaining four inner layers are used as ground layers.

Experimental waveforms of the two-stage prototype converter operating with 12-V input voltage and delivering 50-A load current at 1.3-V output voltage are shown in Figs. 23 and 25. Fig. 23(a) shows the first stage synchronous buck converter switch node voltage and inductor current. The average current in the first stage inductor is nearly 17 A with a peak-to-peak ripple of 11 A. Fig. 23(b) shows the first stage output voltage

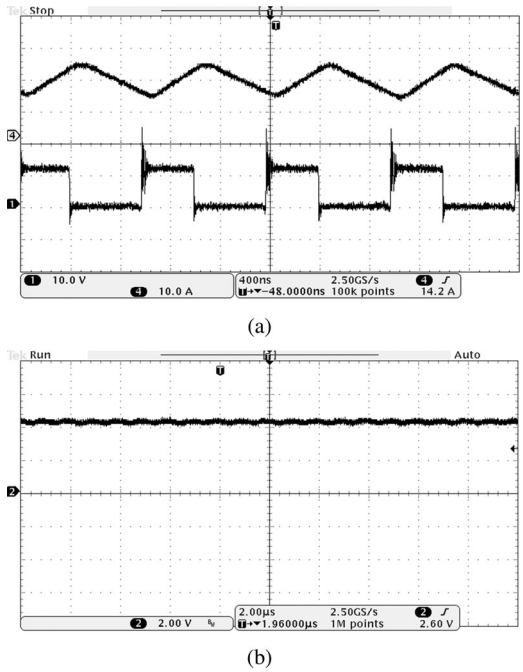
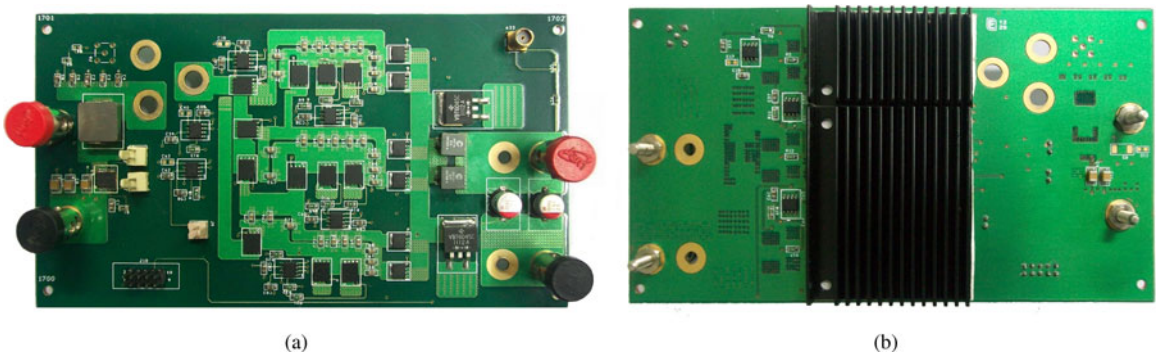


Fig. 23. First stage converter experimental waveforms. (a) CH1: switch node voltage. CH4: inductor current. (b) Intermediate capacitor voltage waveform.

across the intermediate capacitor. The average output voltage of the first stage converter is 4.4 V.

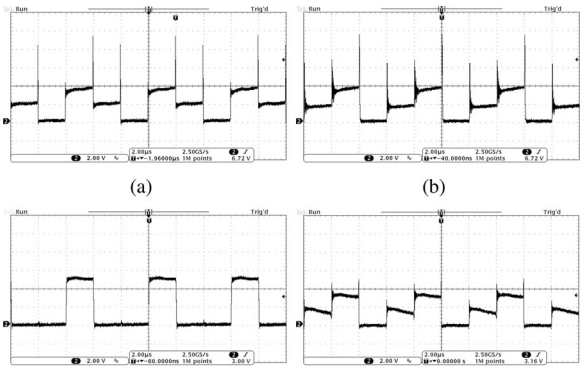
Fig. 25 shows the experimental voltage waveforms across the switches in an SC cell of the second stage PSSC buck converter. The peak value of the observed voltage spike across any switch is 9 V. Fig. 26 shows the phase shifted voltage waveforms across the CT capacitors in all three cells in the ac-coupled mode. The frequency of the voltage waveforms is 170 kHz, which is the same as the second stage switching frequency and the observed peak to peak voltage ripple of 0.5 V closely matches with that of the simulated value of 0.46 V. Linear charge and discharge voltage waveforms across the CT capacitors confirm constant current charging due to output auxiliary inductor.

Fig. 27 shows the voltage waveform at the output node (O) (refer to Fig. 9) of the PSSC converter. The sudden dip in the voltage at the end of each cycle is due to the conduction of an auxiliary diode "D" (refer to Fig. 9) during the dead time between cycle transitions. The dead time used in this design is 50 ns. As observed in the simulation, the spikes in the voltage waveforms across the switches and CT capacitors are due to the ringing between the output capacitance of the MOSFETs and the parasitic inductance (trace inductance and ESL of CT capacitors). Fig. 28 shows the output voltage (inverted) and the auxiliary inductor current ripple waveforms in ac-coupled mode. The magnitudes of the measured voltage and current ripple in Fig. 28 closely match with those in the simulation results shown in Fig. 12. Fig. 29(a) shows the measured efficiency of the first stage synchronous buck at an output voltage of 4.5 V. Fig. 29(b) and (c) shows the measured efficiencies of the second stage PSSC buck converter and the two-stage converter, respectively.



(a) (b)

Fig. 24. Two-stage converter prototype. (a) Top view. (b) Bottom view.



(a) (b) (c) (d)

Fig. 25. Experimental voltage waveforms across switches in an SC cell. (a) Switch "a." (b) Switch "b." (c) Switch "c." (d) Switch "d."

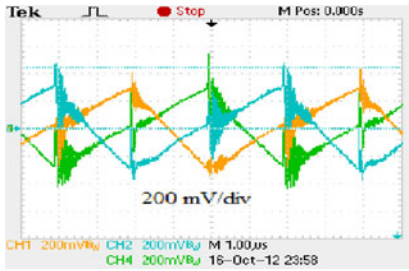


Fig. 26. Experimental voltage waveforms across CT capacitors.

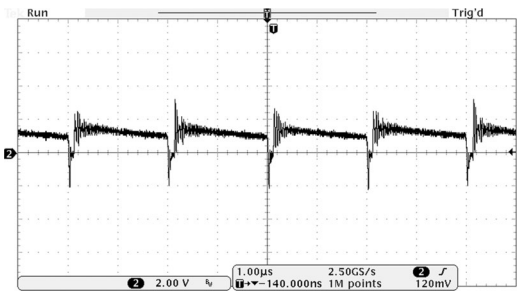


Fig. 27. Voltage waveform at output node of the PSSC converter.

The difference between the measured and simulated efficiency is mainly due to the additional conduction losses in the PCB trace resistance and in the resonant ringing occurring at different nodes in the PSSC converter. To clearly understand

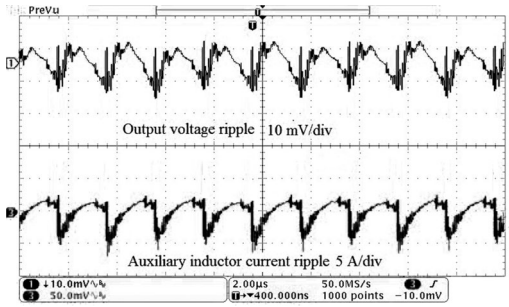


Fig. 28. Output voltage and auxiliary inductor current ripple waveforms.

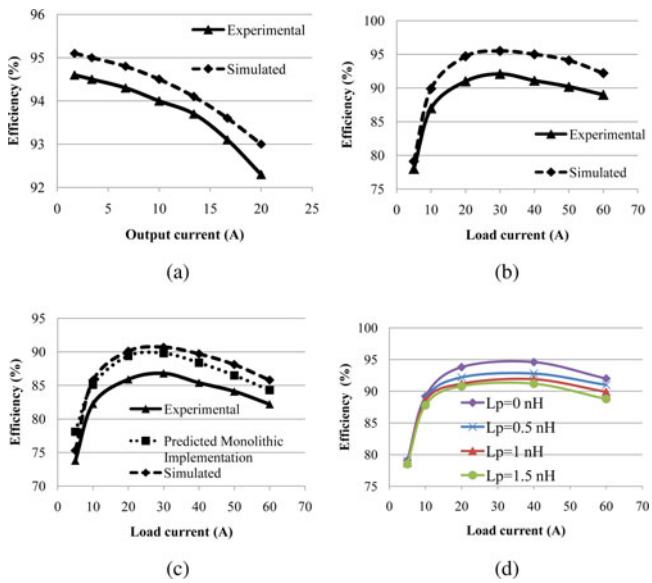


Fig. 29. Efficiency plots. (a) Measured efficiency of first stage buck. (b) Measured efficiency of PSSC buck. (c) Measured efficiency of two-stage buck. (d) Simulated efficiency of PSSC converter with parasitic inductance.

the cause for this additional loss, a SPICE simulation of the PSSC converter is carried out with the parasitic inductance. The parasitic inductance (L_p) which represents the distributed trace inductance is used in series with each MOSFET. During cycle transitions the current in the conducting MOSFET's abruptly goes to zero. The energy stored in the parasitic inductor in the conducting path starts resonating with the device (diode or MOSFET) parasitic capacitors appearing in the same path.

As a result the stored energy in the parasitic inductor is lost in the form of conduction losses. The amount of this extra power loss depends on the magnitude of the current in the conducting MOSFET's at the time of cycle transition, the value of the parasitic inductance and the switching frequency. The simulated efficiency of the PSSC converter with different values of parasitic inductance is shown in Fig. 29(d). Although inclusion of these parasitics in simulations gives better understanding of the loss mechanism, it is is not possible to predict the efficiency accurately as it requires the precise value of the parasitic inductor. The measured efficiency of the proposed converter is greater than that of the conventional two-phase buck converter of [11], [10], [20] for the complete load range. The prototype converter achieves a maximum efficiency of 86.8% at 30 A, which is 3% greater than that of the conventional two-phase buck converter.

The proposed converter attained an efficiency of 82.2% at 60 A compared to the 80.5% efficiency attained by the ZVS nonisolated full-bridge converter proposed in [10]. While the efficiencies of the proposed converter and the full-bridge converter are very close in the load range of 30–50 A, the efficiency of the proposed converter is higher at light loads. The measured efficiency of the first stage in the proposed two-stage converter is less than that of the first stage in [21] because the first stage in the proposed converter is operated at 1 MHz whereas the first stage in [21] is operated at 500 kHz. The measured efficiency of the second stage PSSC converter is greater than that of second stage multiphase buck in [21]. This is also expected since the PSSC converter is operated at a low switching frequency of 170 kHz compared to the 2-MHz switching frequency of the multiphase buck. Furthermore, constant current charging technique improves the efficiency of the PSSC converter. However, the measured two-stage efficiency of the proposed converter is less than that of the two-stage converter in [21]. The lower measured efficiency of the proposed converter is due to the additional losses introduced by the parasitic inductance in the second stage PSSC converter as is evident from Fig. 29(d).

The two-stage converter presented in [24] attained a peak efficiency of 89% at 30 A. The highly efficient first stage SC voltage divider makes it possible, for this converter, to attain high two-stage efficiency compared to that of the proposed converter. Nonetheless, this two-stage converter in [24] contains three discrete inductors in the second stage multiphase buck. Therefore, in a two-stage converter, to attain high efficiency it is desirable to place the SC converter in the first stage but for less inductor count and high overall power density it is advantageous to put the SC converter in the second stage.

One possible solution to improve the efficiency while still retaining the SC converter in the second stage is monolithic integration of the SC stage [34]. The proposed two-stage converter has only two magnetic components, a filter inductor in the first stage buck and an auxiliary inductor in the second stage PSSC converter. As the value of the auxiliary inductance is very low, it can be easily implemented on a PCB with the proper choice of trace width and length. With fewer discrete passive components, which include the first stage filter inductor and capacitor, CT capacitors in the second stage and the output capacitor, the proposed converter is very well-suited for monolithic integration. The synchronous buck converter power stage with integrated gate drivers is already available. Similar monolithic integration of the second stage SC cells, without CT capacitors, is very much feasible. These integrated modular SC cells help in reducing the parasitic inductance and thus improving the efficiency [see Fig. 29(d)]. Another important advantage of monolithic integration of the SC cells is the availability of low voltage lateral power MOSFETs in standard CMOS processes. Lower FoM of low voltage devices increases the efficiency of second stage PSSC buck converter. A predicted efficiency plot of the proposed two-stage converter with monolithic integration of SC cells is shown in Fig. 29(c). For the calculation of the efficiency prediction it is assumed that the value of the L_p is 0.1 nH and the FoM of the integrated low voltage MOSFET [37] is 25% less than that of the discrete high voltage MOSFET.

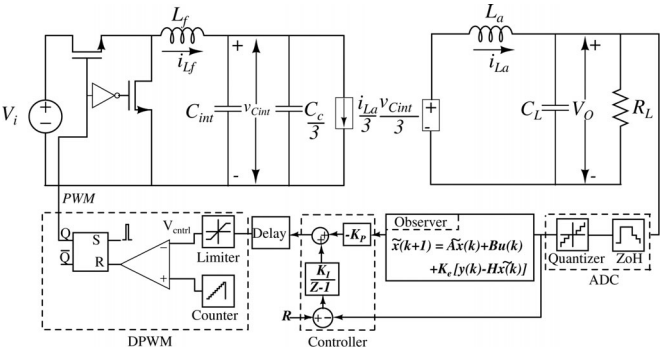
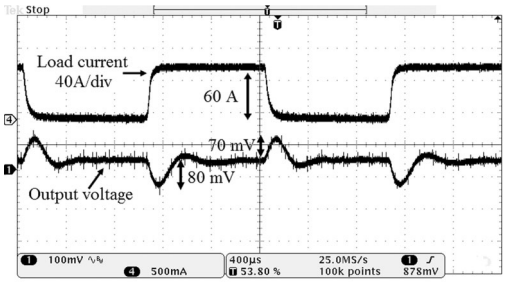


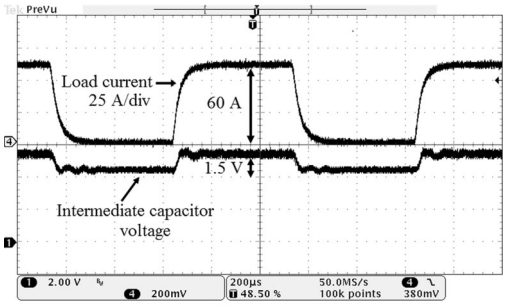
Fig. 30. Schematic of full state feedback digital control scheme.

B. Transient Performance

To verify the transient performance of the two-stage converter, a full state feedback digital controller with an observer is implemented on FPGA. Fig. 30 shows the block level schematic of the implemented closed loop digital control scheme. The output voltage is sensed and fed back to the observer and controller. The observer estimates the other three states. The observer gain matrix K_e is determined using Ackerman's pole placement technique. The observer poles are designed to be four times faster than the controller poles. This ensures that the system response is dominated by the controller poles. The output voltage is sampled at the rate of 25 Msps using LTC2255 A/D converter. The A/D quantization bin size is $\Delta_{V_{A/D}} = 15.6$ mV. The DPWM is implemented using a nine bit counter. The counter uses a 500-MHz internal clock synthesized by digital clock manager of the FPGA. This corresponds to a DPWM time resolution of 2 ns. For a two stage converter with 12-V input voltage and a second stage conversion ratio of $1/3$, the DPWM quantization bin size is $\Delta_{V_{DPWM}} = 4/2^9 = 7.8$ mV. Fig. 31 shows the experimental transient performance for 60-A loading and unloading transients. Fig. 31(a) shows the transient output voltage in ac-coupled mode along with the load current. Fig. 31(b) shows the voltage across the intermediate capacitor during the load transient.



(a)



(b)

Fig. 31. Experimental transient performance with 60-A load transient. (a) Output voltage. (b) Intermediate capacitor voltage.

VI. Conclusion

PoL converters designed for IBA applications require high efficiency and high power density. Conventionally used inductor-based topologies cannot simultaneously meet these two requirements due to the presence of large number of inductors. This paper proposed a hybrid, a combination of inductor-based and capacitor-based, two-stage converter with reduced inductor count. The proposed converter comprises a high frequency, high efficiency synchronous buck converter in the first stage and a high efficiency, high power density, newly proposed PSSC converter in the second stage. The PSSC converter is modular in architecture and is capable of achieving high efficiencies in the complete load range. Efficiency of the PSSC converter is improved by implementing the constant current charging technique. Putting the PSSC buck converter in the output stage reduces the inductor count and makes the topology suitable for monolithic integration.

A laboratory prototype of the proposed converter is built and the performance is verified experimentally. Efficiency of the proposed two-stage converter is greater than that of the conventional two-phase buck converter in the complete load range but less than a similar two-stage converter with the SC voltage divider in the first stage. Efficiency of the PSSC converter can be further increased by integrating the low voltage PSSC cells in a low FoM CMOS process. Monolithic integration will reduce not only the conduction losses but also the losses associated with the parasitic inductance. The small-signal model of the proposed converter is derived and it is shown that the second stage PSSC converter does not introduce any small-signal dynamics. This helps in obtaining a good transient response. A closed-loop controller for the converter with a full state observer and state feedback control scheme is designed and verified experimentally.

Appendix

A. Equivalent Output Resistance With Resistive Charging

From Fig. 4 for $0 \le t \le T/n$

$$V_i = nR_c i - R_c i_o + \sum_{i=1}^{n} v_{Ci} \tag{25}$$

$$v_{Cn} + R_c i = V_o + (R + R_c) i_o \tag{26}$$

$$\frac{d}{dt} v_{Ci} = \frac{d}{dt} v_{Ci+1}, \qquad 1 \le i \le n-2. \tag{27}$$

Assuming $C_1 = C_2 = ... = C_n = C$

$$i_o = C \frac{d}{dt} [v_{Cn-1} - v_{Cn}]. \tag{28}$$

From (27) and Fig. 6

$$\begin{aligned} v_{Ci} &= v_{Ci+1} + \frac{\Delta v}{n-1} \\ &= v_{Cn-1} + \frac{n-1-i}{n-1} \Delta v 1 \le i \le n-2 \end{aligned} \tag{29}$$

$$\begin{aligned} \sum_{i=1}^{n} v_{Ci} &= v_{Cn} + \sum_{i=1}^{n-1} V_{Ci} \\ &= v_{Cn} + (n-1) v_{Cn-1} + \frac{n-2}{2} \Delta v. \end{aligned} \tag{30}$$

Substituting (30) in (25)

$$V_i = nR_c i - R_c i_o + v_{Cn} + (n-1) v_{Cn-1} + \frac{n-2}{2} \Delta v \tag{31}$$

$$R_{ci} = \frac{V_i}{n} - \frac{n-2}{2n} \Delta v - \frac{v_{Cn}}{n} - \frac{n-1}{n} v_{Cn-1} + \frac{R_c}{n} i_o. \tag{32}$$

Substituting (32) in (26)

$$\begin{aligned} V_o + \left[R + \frac{n-1}{n} R_c \right] i_o = \frac{V_i}{n} - \frac{n-2}{2n} \Delta v \\ + \frac{n-1}{n} [v_{Cn-1} - v_{Cn}]. \end{aligned} \tag{33}$$

From (28) and Fig. 6

$$\frac{1}{C} \int_0^t i_o d\tau = v_{Cn-1} - vCn + v_{Cn}(0) - v_{Cn-1}(0) \tag{34}$$

$$v_{Cn} - v_{Cn-1} = \Delta v - \frac{1}{C} \int_0^t i_o d\tau. \tag{35}$$

Substituting (35) in (33)

$$V_o + \left[R + \frac{n-1}{n}R_c\right] i_o = \frac{V_i}{n} - \frac{n-2}{2n}\Delta v + \frac{n-1}{n}\Delta v - \frac{n-1}{nC}\int_0^t i_o d\tau \quad (36)$$

$$\frac{V_i}{n} + \frac{\Delta v}{2} = \left[R + \frac{n-1}{n}R_c\right] i_o + \frac{1}{\frac{nc}{n-1}}\int_0^t i_o d\tau + V_o. \quad (37)$$

(37) suggests the following equivalent circuit where $R_c^{'} = \frac{n-1}{n}R_c$ and $C^{'} = \frac{n}{n-1}C$

$$\therefore\ i_o(t) = \frac{\frac{V_i}{n} - V_o + \frac{\Delta v}{2}}{R + R_c^{'}} e^{-t/\tau'} \quad (38)$$

$$\text{where} \qquad \tau^{'} = C^{'}(R + R_C^{'}). \quad (39)$$

$i_o(t)$ is periodic over T/n

$$\therefore\ I_o = \frac{n}{T}\int_0^{T/n} i_o(\tau)d\tau = \frac{n\tau^{'}}{T}\frac{\frac{V_i}{n} - V_o + \frac{\Delta v}{2}}{R + R_c^{'}}[1 - e^{-T/n\tau'}]. \quad (40)$$

Also from (28)

$$I_o = \frac{n}{T}\int_0^{T/n} i_o(\tau)d\tau = \frac{nC}{T}\left[\frac{\Delta v}{n-1} + \Delta v\right]\frac{n^2}{n-1}\frac{C}{T}\Delta v \quad (41)$$

$$I_o = \frac{n\tau^{'}}{T}\frac{\Delta v}{R + R_c^{'}}. \quad (42)$$

From (40)

$$\frac{I_o}{1 - e^{-T/n\tau^{'}}} = \frac{n\tau^{'}}{T}\frac{\frac{V_{in}}{n} - V_o}{R + R_c^{'}} + \frac{n\tau^{'}}{T}\frac{\Delta v}{2(R + R_c^{'})}. \quad (43)$$

Substituting (42) in (43)

$$\frac{1 + e^{-T/n\tau^{'}}}{1 - e^{-T/n\tau^{'}}}\frac{I_o}{2} = \frac{n\tau^{'}}{T}\frac{\frac{V_i}{n} - V_o}{R + R_c^{'}} \quad (44)$$

$$\frac{V_i}{n} = V_o + \frac{T}{n\tau^{'}}\frac{1 + e^{-T/n\tau^{'}}}{1 - e^{-T/n\tau^{'}}}\frac{R + R_c^{'}}{2}I_o. \quad (45)$$

(45) suggests the dc equivalent model of n-cell PSSC converter shown in Fig. 5

$$\therefore\ R_O = \frac{T}{n\tau^{'}}\frac{1 + e^{-T/n\tau^{'}}}{1 - e^{-T/n\tau^{'}}}\frac{R + R_c^{'}}{2}. \quad (46)$$

For $T/n >> \tau'$

$$R_O = R_{SSL} = \frac{T}{n\tau^{'}}\frac{R + R_c^{'}}{2} = \frac{(n-1)T}{2n^2C}. \quad (47)$$

From (42) $\Delta v = \frac{T}{n\tau^{'}}(R + R_c^{'})I_o.$ (48)

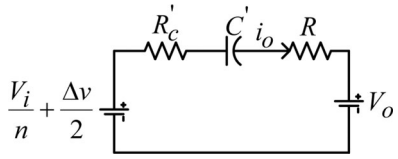


Fig. 32. Resistive charging equivalent circuit.

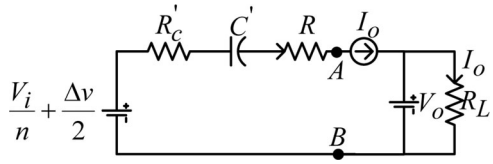


Fig. 33. Constant current charging equivalent circuit.

From (45) $V_o = \frac{V_i}{n} - \frac{\Delta v}{2}$. (49)

For $T/n << \tau'$

$$R_O = R_{FSL} = R + R_c^{'} = R + \frac{(n-1)R_c}{n}. \quad (50)$$

B. Equivalent Output Resistance With Constant Current Charging

With constant current charging, equivalent circuit shown in Fig. 32 is modified as shown in Fig. 33.

Assuming a smaller current ripple in the auxiliary inductor it can be replaced with a constant current source of dc value I_o.

For $0 \le t \le T/n$

$$V_{ab} = \frac{V_i}{2} + \frac{\Delta v}{2} - (R + R_c^{'})I_o - \frac{1}{C'}\int_0^t i_o d\tau \quad (51)$$

$$V_{AB} = \frac{n}{T}\int_0^{T/n} V_{AB}\,dt = \frac{V_i}{2} + \frac{\Delta v}{2} - (R + R_c^{'})I_o - \frac{I_o T}{2C'n}. \quad (52)$$

From (48) $\frac{\Delta v}{2} = \frac{T}{2n\tau^{'}}(R + R_c^{'})I_o = \frac{I_o T}{2C'n}$. (53)

$$\therefore\ V_{AB} = \frac{V_i}{n} - (R + R_c^{'})I_o. \quad (54)$$

Average voltage across the auxiliary inductor is zero

$$\therefore\ V_{AB} = V_o = \frac{V_i}{n} - (R + R_c^{'})I_o. \quad (55)$$

$$\text{Hence} \quad R_O = R + R_c^{'}. \quad (56)$$

The coefficients d_4–d_0 in the (20) are given by

$$\begin{aligned}
d_4 &= n^2 L_f C_{ie} L_a (R_L C_L + R_{cl} C_L) \\
d_3 &= L_f R_i C_{ie} (R_L C_L + R_{cl} C_L) + n^2 L_a (R_L C_L \\
&\quad + R_{cl} C_L) R_i C_{ie} + n^2 L_f C_{ie} (R_L R_{cl} C_L + L_a \\
&\quad + (R_l a + R_{FSL})(R_L C_L + R_{cl} C_L)) \\
d_2 &= n^2 (R_L R_{cl} C_L + L_a + (R_l a + R_{FSL})(R_L C_L \\
&\quad + R_{cl} C_L)) R_i C_{ie} + n^2 L_a (R_L C_L + R_{cl} C_L) \\
&\quad + n^2 L_f C_{ie} (R_L + R_{la} + R_{FSL}) \\
&\quad + L_f (R_i C_{ie} + R_L C_L \\
&\quad + R_{cl} C_L) + n^2 (R_L R_{cl} C_L + L_a \\
&\quad + (R_l a + R_{FSL})(R_L C_L + R_{cl} C_L)) R_{lf} C_{ie} \\
&\quad + R_i C_{ie} (R_L C_L + R_{cl} C_L) R_{lf} \\
d_1 &= n^2 (R_l a + R_{FSL})(R_L C_L + R_{cl} C_L)) + n^2 R_i C_{ie} (R_L \\
&\quad + R_{la} + R_{FSL}) \\
&\quad + L_f + n^2 C_{ie} (R_L + R_{la} + R_{FSL}) R_{lf} \\
&\quad + (R_i C_{ie} + R_L C_L + R_{cl} C_L) R_{lf} \\
d_0 &= R_{lf} + n^2 (R_L + R_{la} + R_{FSL}).
\end{aligned}$$

REFERENCES

[1] R. White, "Emerging on-board power architectures," in *Proc. IEEE App. Power Electron. Conf.*, Feb. 2003, pp. 799–804.

[2] L. Brush, "Distributed power architecture demand characteristics," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, pp. 342–345.

[3] Y. Panov and M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 776–783, Nov. 2001.

[4] X. Zhou, P.-L. Wong, P. Xu, F. Lee, and A. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1172–1182, Nov. 2000.

[5] W. Yuan, G. X. Zhang, X. Xie, J. Zhang, and Z. Qian, "Linear-non-linear AVP control with larger inductance for VRM," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2009, pp. 77–82.

[6] P.-L. Wong, F. Lee, P. Xu, and K. Yao, "Critical inductance in voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 485–492, Jul. 2002.

[7] J.-H. Park and B.-H. Cho, "Nonisolation soft-switching buck converter with tapped-inductor for wide-input extreme step-down applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 8, pp. 1809–1818, Aug. 2007.

[8] K. Yao, Y. Qiu, M. Xu, and F. Lee, "A novel winding-coupled buck converter for high-frequency, high-step-down dc-dc conversion," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1017–1024, Sep. 2005.

[9] J. Wei and F. Lee, "Two novel soft-switched, high frequency, high-efficiency, non-isolated voltage regulators-the phase-shift buck converter and the matrix-transformer phase-buck converter," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 292–299, Mar. 2005.

[10] Z. Zhang, E. Meyer, Y.-F. Liu, and P. Sen, "A 1-MHz, 12-V ZVS non-isolated full-bridge VRM with gate energy recovery," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 624–636, Mar. 2010.

[11] S. Ye, E. Meyer, Y.-F. Liu, and X. Liu, "A novel two phase nonisolated full bridge with shared primary switches," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2363–2376, Sep. 2008.

[12] Z. Yang, S. Ye, and Y.-F. Liu, "A new transformer-based non-isolated topology optimized for VRM application," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2005, pp. 447–453.

[13] H. N. Nagaraja, D. Kastha, and A. Patra, "Design principles of a symmetrically coupled inductor structure for multiphase synchronous buck converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 988–997, Mar. 2011.

[14] Y. Yugang, Y. Dong, and F. Lee, "A new coupled inductors design in 2-phase interleaving VRM," in *Proc. IEEE Power Electron. Motion Contr. Conf.*, May. 2009, pp. 344–350.

[15] Y. Ren, "High frequency, high efficiency two-stage approach for future microprocessors," Ph.D. dissertation, Dept. Elect. Eng., Virginia Polytechnic Inst. State Univ., Blacksburg, VA, USA, Apr. 2005.

[16] J. Wei, "High frequency high-efficiency voltage regulators for future microprocessors," Ph.D. dissertation, Dept. Elect. Eng., Virginia Polytechnic Inst. State Univ., Blacksburg, VA, USA, Sep. 2004.

[17] P. Hazucha, G. Schrom, J. Hahn, B. Bloechel, P. Hack, G. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233-mhz 80 four-phase dc-dc converter utilizing air-core inductors on package," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, Apr. 2005.

[18] G. Schrom, P. Hazucha, F. Paillet, D. Rennie, S. Moon, D. S. Gardner, T. Kamik, P. Sun, T. Nguyen, M. Hill, K. Radhakrishnan, and T. Memioglu, "A 100 MHz eight-phase buck converter delivering 12 A in 25 mm 2 using air-core inductors," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2007, pp. 727–730.

[19] J. Sun, J.-Q. Lu, D. Giuliano, T. Chow, and R. Gutmann, "3d power delivery for microprocessors and high-performance asics," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2007, pp. 127–133.

[20] Z. Zhang, W. Eberle, Y.-F. Liu, and P. Sen, "A nonisolated zvs asymmetrical buck voltage regulator module with direct energy transfer," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3096–3105, Aug. 2009.

[21] Y. Ren, M. Xu, K. Yao, Y. Meng, and F. Lee, "Two-stage approach for 12-v vr," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1498–1506, Nov. 2004.

[22] J. Wei and F. Lee, "Two-stage voltage regulator for laptop computer cpus and the corresponding advanced control schemes to improve light-load performance," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, pp. 1294–1300.

[23] J. Sun, M. Xu, F. Lee, and Y. Ying, "High power density voltage divider and its application in two-stage server vr," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 1872–1877.

[24] J. Sun, M. Xu, Y. Ying, and F. Lee, "High power density, high efficiency system two-stage power architecture for laptop computers," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–7.

[25] K. D. T. Ngo and R. Webster, "Steady-state analysis and design of a switched-capacitor dc-dc converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 30, no. 1, pp. 92–101, Jan. 1994.

[26] M. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1995, pp. 1215–1221.

[27] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[28] S. Ahsanuzzaman, J. Blackman, T. McRae, and A. Prodic, "A low-volume power management module for portable applications based on a multi-output switched-capacitor circuit," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2013, pp. 1473–1479.

[29] A. Radic and A. prodic, "Buck converter with merged active charge-controlled capacitive attenuation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1049–1054, Mar. 2012.

[30] A. Radic, S. Ahssanuzzaman, B. Mahdavikhah, and A. Prodic, "High-power density hybrid converter topologies for low-power dc-dc smps," in *Proc. IEEE Int. Power Electron. Conf.*, May. 2014, pp. 3582–3586.

[31] R. Pilawa-Podgurski and D. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, Jul. 2012.

[32] T. Andersen, F. Krismer, J. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Brandli, P. Buchmann, and P. Francese, "A 4.6 w/mm 2 power density 86 soi cmos," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2013, pp. 692–699.

[33] H. Meyvaert, T. Van Breussegem, and M. Steyaert, "A 1.65 w fully integrated 90 nm bulk cmos capacitive dc-dc converter with intrinsic charge recycling," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4327–4334, Sep. 2013.

[34] S. R. Challa, D. Maksimovic, D. Kastha, and A. Patra, "Monolithic implementation of phase shifted switched capacitor step-down dc-dc converter for portable power applications," in *Proc. IEEE 15th Workshop Control Model. Power Electron.*, Jun. 2014, pp. 1–7.

[35] B. Arntzen and D. Maksimovic, "Switched-capacitor dc/dc converter with resonant gate drive," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1996, pp. 414–420.
[36] *CSD97370Q5M Synchronous Buck NexFET Power Stage*, Texas Instruments., Rev. C, May. 2012.
[37] Z. Shen, D. Okada, F. Lin, S. Anderson, and X. Cheng, "Lateral power mosfet for megahertz-frequency, high-density dc/dc converters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 11–17, Jan. 2006.

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