Variable Modulation Offset SPWM Control to Balance the Neutral-Point Voltage for Three-Level Inverters

Jianguo Lyu, *Student Member, IEEE*, Wenbin Hu, Fuyun Wu, Kai Yao, *Member, IEEE*, and Junji Wu

***Abstract*—In order to solve the neutral-point voltage unbalancing problem for three-level inverters, this paper proposes a method to balance the neutral-point voltage for three-level inverters with variable modulation wave offset sinusoidal pulse-width modulation (SPWM) control. Based on the mathematical expressions of neutral-point voltage unbalancing, the factors are studied, which affect the fluctuation of neutral-point voltage. Theoretically the mathematical expressions of the neutral-point voltage with the proposed method are derived, and the mathematical relationship between the fluctuation of neutral-point voltage and the adjusting offset of modulation wave is studied. This proposed method realizes controlling the neutral-point voltage balance by dynamically calculating the offset superimposed to the modulation wave based on SPWM (DCOSPWM). This DCOSPWM method is very simple, which has good steady-state performance and is easy for digital implementation. The simulation results verify the correctness of the theoretical analysis in this paper, and the feasibility and effectiveness of this method is verified by the experiments in the experimental platform of neutral point clamped three-level inverters based on digital signal processor (DSP)-complex programmable logic device (CPLD).**

***Index Terms*—Neutral-point voltage balance, sinusoidal pulse-width modulation (SPWM), three-level inverters, variable modulation wave offset.**

I. Introduction

MULTILEVEL inverter has been widely used in medium- or high-voltage and high-power conversions, and its control strategies and topologies of power circuits become the main research focuses. Compared with two-level inverter, multilevel inverter has such advantages [1]–[8], [12], [15] for example, low voltage stress on power switching devices [13], low electromagnetic noise and low total harmonic distortion (THD). The more levels multilevel inverter outputs, the more steps of stair waveform, and closer to standard line frequency sinusoidal wave the output waveform is. The three-level inverter is preferred in multilevel inverters [16], and one of the typical circuit topologies for the three-level inverter is the neutral-point-clamped (NPC) inverter, as shown in Fig. 1.

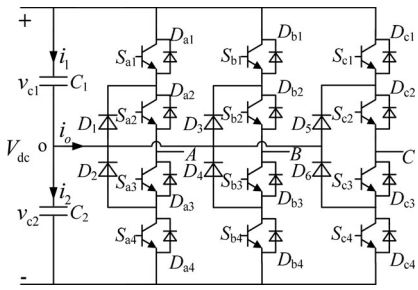

Fig. 1. Main circuit of NPC three-level inverter.

The dc bus of the NPC inverter must use two dc bus capacitors connected in series, so the inverter can output phase voltage with three levels and line voltage with five levels. Ideally, each capacitor voltage is half of the dc bus voltage. But due to the capacitance error of capacitors, the inconsistent characteristics of switching devices or unbalancing of three-phase operation, the voltage difference between the two dc bus capacitors appears in the practical system. So the neutral-point voltage unbalancing is a typical problem in the NPC inverter [16]. The neutral-point voltage unbalancing problem will affect the quality of output waveforms, which makes the output voltage containing low-frequency harmonics. It will also increase the voltage stress on individual switching devices [2], or even worse, it can cause serious damage to the switching devices and disturbs the normal operation of the system. So the neutral-point voltage balance has been the research emphasis of the three-level inverters.

Recently, many scholars and experts have put forward various new methods to solve the neutral-point voltage unbalancing problem. In [1], the method to reduce the leakage current and balance the neutral-point voltage in the three-level inverter is proposed. This method reduces the common-mode voltage that causes the leakage current by using large, medium, and zero vectors, and uses large, medium, and small vectors to balance the neutral-point voltage with reduced common mode voltage. An optimized modulation strategy (OMS) that balances the neutral-point voltage is proposed in [2], and the strategy replaces the P-type or N-type small switching states with other switching states that do not affect the neutral-point voltage. This strategy sacrifices a little bit efficiency and output THD to obtain the strong balancing ability of the neutral-point voltage. Wang and Li [9] proposed a control method based on space vector pulse-width modulation (SVPWM) by injecting zero-sequence voltage components, which is calculated by using optimal search

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and interpolation method to achieve the neutral-point voltage balancing, its algorithm is complex and not easy to implement. In [10], a novel controller with full power-factor range and low distortion is proposed by purposely reinjected third-harmonic NP current pattern with a gain modification, but its control algorithms is high complex. The authors in [20], [22], and [23] proposed control methods based on Proportional and integral (PI) controller, in which usually the PI parameters are selected for the maximum output power condition [22], and the PI parameter is constant, so it cannot show the consistent strong ability for controlling the neutral-point voltage balance when the output varies. In [20], the method uses a PI controller based on SVPWM (PISVPWM) for modifying the angle of the reference vectors to balance the neutral-point voltage.

The objective of this paper is to propose a new simple method to control the neutral-point voltage balance. This proposed method dynamically calculates the offset superimposed to the modulation waves based on SPWM (DCOSPWM) according to the amplitude of the output current, output power factor, and the modulation ratio, so the control method is effective at different load conditions. Section II studies the factors, which influence the neutral-point voltage unbalancing based on analyzing the mathematical expressions of the neutral-point voltage. In Section III, the DCOSPWM method to balance the neutral-point voltage is proposed for NPC inverters, and theoretically, the mathematical expressions of the neutral-point voltage with the proposed method are derived. The mathematical relationship between the fluctuation of neutral-point voltage and adjusting the offset of the modulation wave is studied, and the implementation of the proposed DCOSPWM method is presented. Section IV presents the comparison among the three control methods for neutral-point voltage balance, in terms of switching loss, system efficiency, and the output current harmonics, which has not been presented in [2], [9]–[11], [14], [17]–[20], and [22]–[27]. The analysis results show that, besides strong ability of controlling the neutral-point voltage balance, the output current harmonics has been decreased, and the efficiency is not sacrificed using the proposed DCOSPWM method in this paper. The simulated and experimental results are presented in Section V.

II. Mathematical Expressions of Neutral-Point Voltage Unbalancing for Three-Level Inverters

As shown in Fig. 1, dV_c is defined as the voltage difference between the dc bus capacitors C_1 and C_2. Therefore, the neutral-point voltage balance can be expressed as $v_{c1} = v_{c2} = V_{\rm dc}/2$, so $dV_c = 0$. Where v_{c1} is the voltage of capacitor C_1, v_{c2} is the voltage of capacitor C_2, $V_{\rm dc}$ is dc bus voltage. When $v_{c1} = v_{c2}$, each phase leg of the three-level inverter can output three different levels $(V_{\rm dc}/2, -V_{\rm dc}/2, 0)$. "P", "0", "N" represent three working conditions corresponding to the three output levels, respectively. The relationship between the output levels and the operating state of the switches is shown in Table I. "$\surd$" and "$\times$" of $\rm S_{xn}(x = a, b, c, n = 1, 2, 3, 4)$ represent the turn-on and the turn-off states of the switches, respectively.

Single polar SPWM method is preferred in the conventional three-level SPWM control strategy because of its less switching loss than double polar SPWM control. The control signals for switches are generated by sinusoidal modulation wave comparing with triangular carrier wave. Fig. 2 shows the control signals for the four switches of phase *a*.

TABLE I
Output Levels and Switching Status

Working condition	Switching status				Output leg level
	$\rm S_{X1}$	$\rm S_{X2}$	$\rm S_{X3}$	$\rm S_{X4}$	
P	$\surd$	$\surd$	$\times$	$\times$	$V_{\rm dc}/2$
0	$\times$	$\surd$	$\surd$	$\times$	0
N	$\times$	$\times$	$\surd$	$\surd$	$-V_{\rm dc}/2$

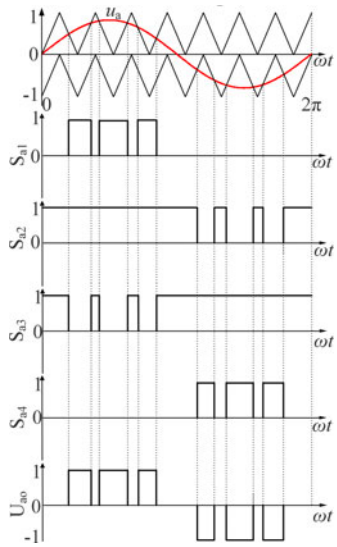

Fig. 2. Single polar SPWM modulation method for NPC three-level inverter.

Ideally, when the carrier amplitude is unity, the three-phase sinusoidal modulation waves can be expressed as

$$\begin{cases} u_a = m\sin(\omega t) \\ u_b = m\sin(\omega t - 2\pi/3) \\ u_c = m\sin(\omega t + 2\pi/3) \end{cases} \tag{1}$$

where m is modulation ratio, $0 < m < 1$; ω is the angular frequency of the modulation waves.

As shown in Fig. 2, when the control signal for switches is high level, the switches turn ON. In the opposite way, the switches turn OFF. For the modulation wave of phase *a*, when the sinusoidal modulation wave is higher than carrier wave on the positive axis, the control signal for $\rm S_{a1}$ is high level, oppositely, the control signal must be low level. In positive half line cycle, the control signals of $\rm S_{a1}$ and $\rm S_{a3}$ are complementary and so as to $\rm S_{a2}$ and $\rm S_{a4}$ in negative half-line cycle.

In a switching cycle $T_{\rm s}$, when the switches operate at "0" state, the duty cycle can be derived as

$$\begin{cases} D_{ao} = 1 - m|\sin(\omega t)| \\ D_{bo} = 1 - m|\sin(\omega t - 2\pi/3)| \\ D_{co} = 1 - m|\sin(\omega t + 2\pi/3)|. \end{cases} \tag{2}$$

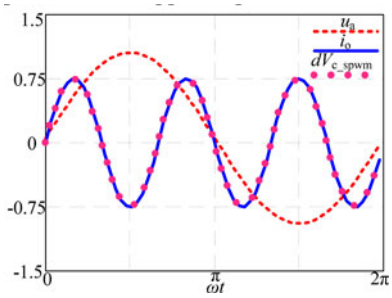

Fig. 3. Waveforms of u_a, i_o, and dV_{c_spwm} in a line cycle.

The three-phase load currents are defined as

$$\begin{cases} i_a = I_m \sin(\omega t - \varphi) \\ i_b = I_m \sin(\omega t - 2\pi/3 - \varphi) \\ i_c = I_m \sin(\omega t + 2\pi/3 - \varphi) \end{cases} \tag{3}$$

where I_m is the amplitude of the phase load current and φ is the load power factor angle.

The neutral-point current i_o can be defined as the average current in a switching cycle T_s, which flows out from the neutral-point O is

$$i_o = D_{ao} i_a + D_{bo} i_b + D_{co} i_c. \tag{4}$$

From Fig. 1, it can be seen that the relationship among i_o, i_1, and i_2 can be defined as

$$\begin{cases} i_1 = C_1 dv_{c1}/dt \\ i_2 = C_2 dv_{c2}/dt \\ i_o = i_1 - i_2 \end{cases} \tag{5}$$

where v_{c1} and v_{c2} are the instantaneous voltage of capacitor C_1 and C_2 separately, and i_1 and i_2 are the instantaneous current of capacitor C_1 and C_2.

In the traditional SPWM control method, if the capacitance of C_1 and C_2 is equal, from (4) and (5), the capacitor voltage difference dV_{c_spwm} between v_{c1} and v_{c2} can be derived as

$$dV_{c\_spwm} = v_{c1} - v_{c2} \tag{6}$$

$$dV_{c\_spwm} = \frac{i_o}{C} T_s \tag{7}$$

$$dV_{c\_spwm} = \frac{T_s}{C}(D_{ao} i_a + D_{bo} i_b + D_{co} i_c) \tag{8}$$

where T_s is the switching cycle, C is the capacitance of C_1 and C_2.

When m, I_m, T_s, and C are normalized, the waveforms of u_a, i_o, and dV_{c_spwm} are shown in Fig. 3, where u_a is the modulation wave of phase a. From Fig. 3, it can be seen that i_o and dV_{c_spwm} both fluctuate at three times the line frequency in a line cycle. The fluctuation of neutral-point voltage is caused by the fluctuation of the neutral-point current. Thus, the neutral-point voltage balance can be achieved by decreasing the neutral-point current ripple amplitude.

III. Variable Modulation Wave Offset Control

Define kdV_{c_spwm} as the adjustment value for three-phase modulation waves in a switching cycle T_s, so the three-phase modulation waves can be expressed as

$$\begin{cases} u_a = m \sin(\omega t) + kdV_{c\_spwm} \\ u_b = m \sin(\omega t - 2\pi/3) + kdV_{c\_spwm} \\ u_c = m \sin(\omega t + 2\pi/3) + kdV_{c\_spwm} \end{cases} \tag{9}$$

where k is the adjustment coefficient and m is the modulation ratio.

Accordingly, after the adjustment, the duty cycle of "0" state can be derived as

$$\begin{cases} D_{ao} = 1 - |m \sin(\omega t) + kdV_{c\_spwm}| \\ D_{bo} = 1 - |m \sin(\omega t - 2\pi/3) + kdV_{c\_spwm}| \\ D_{co} = 1 - |m \sin(\omega t + 2\pi/3) + kdV_{c\_spwm}|. \end{cases} \tag{10}$$

By substituting (10) into (8), in a switching cycle, the capacitor voltage difference between capacitor C_1 and C_2 can be derived as

$$\begin{aligned} dV_c = -\frac{T_s}{C} \{ & i_a |m \sin(\omega t) + kdV_{c\_spwm}| \\ & + i_b |m \sin(\omega t - 2\pi/3) + kdV_{c\_spwm}| \\ & + i_c |m \sin(\omega t + 2\pi/3) + kdV_{c\_spwm}| \}. \end{aligned} \tag{11}$$

When m and φ are given, the ripple amplitude of dV_c depends on k. In order to ensure the "0" state duty cycle being in the range of [0,1]. Thus, the following constraints should be met

$$\begin{cases} |m \sin(\omega t) + kdV_{c\_spwm}| \le 1 \\ |m \sin(\omega t - 2\pi/3) + kdV_{c\_spwm}| \le 1 \\ |m \sin(\omega t + 2\pi/3) + kdV_{c\_spwm}| \le 1. \end{cases} \tag{12}$$

From (3), (8), and (12), when the power factor angle is in the range of $[-\pi, \pi]$, the value range of k can be obtained as

$$0 \le k \le k_{max} \tag{13}$$

where k_{max} is equation (14) as shown on the bottom of the next page

After normalizing the variables I_m, T_s and C, the surface of k_{max} as the function of m and φ is plotted as shown in Fig. 4(a), k should be chosen within the space between axis bottom and the surface.

The variational trend of dV_c is plotted as shown in Fig. 4(b), it can be seen that the amplitude of dV_c varies with k. For example, when $\varphi = 0$ and $m = 0.8$, the range of k must meet the following condition:

$$0 \le k \le 1.5. \tag{15}$$

Fig. 4(b) shows that if k varies, the ripple frequency of dV_c remains the same, but its peak-to-peak value varies. It can be seen that when $k = 0.3$, the peak-to-peak value of dV_c is the lowest and the control effect is most effective.

In details, when $\varphi = 0$ and $m = 0.8$, the amplitude of dV_c, which varies with k using the proposed DCOSPWM method,

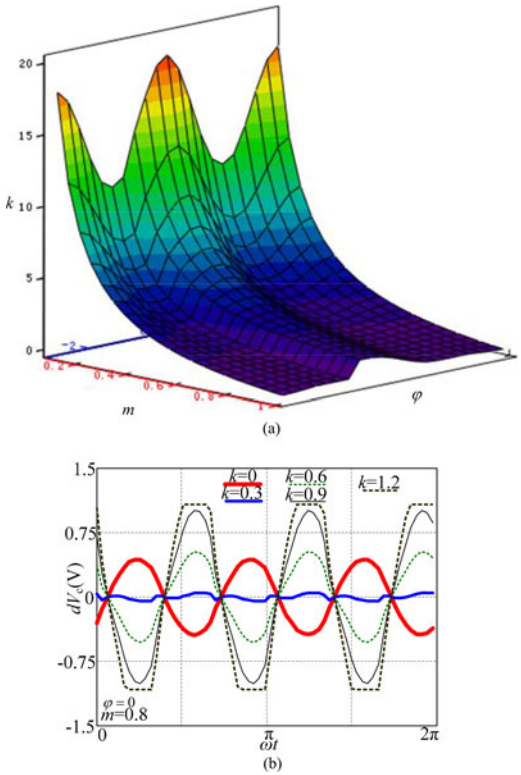

Fig. 4. Range of k and the curves of dV_c with k. (a) Curved surface of k. (b) Relationship between dV_c and k.

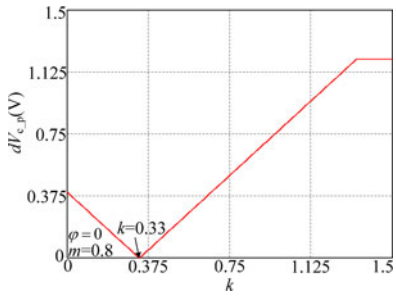

Fig. 5. Relationship between the amplitude value of dV_c and k.

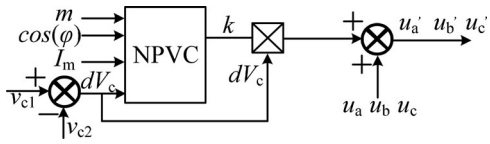

Fig. 6. Simplified control principle diagram of the proposed DCOSPWM method.

which is shown in Fig. 5, it can be seen that when k varies from 0 to 1.5, the dV_{c_p} decreases first, then it increases. So when $k = 0.33$, the lowest value of dV_{c_p} can be obtained. Where dV_{c_p} represents the amplitude value of dV_c with proposed DCOSPWM method.

Fig. 6 shows the simplified control principle diagram of the DCOSPWM method proposed in this paper. Neutral-point voltage control (NPVC) is the controller for the neutral-point voltage balance control. u_a, u_b, and u_c are the modulation waves before adjusting the modulation waves offset, u_a', u_b', u_c' are the modulation waves after the proposed DCOSPWM control, the input parameters of the NPVC unit are m, $\cos(\varphi)$, I_m, and dV_c. The main function of this NPVC unit is that according to the system current parameters, it calculates the range of k, obtains the optimum value of k using a search method, which corresponds to the lowest value of dV_{c_p}. And $k\ dV_c$ is used as the offset superimposed to the modulation waves, so u_a', u_b', u_c' are the final modulation waves, which compare with the carrier waves to generate driving signals for the switches. The main working flowchart of the DCOSPWM method is shown in Fig. 7, and the NPVC unit is shown in the dashed frame. In Fig. 7, to obtain the optimum value of k, which corresponds to the lowest amplitude of dV_c, the fix-step search method is available in this NPVC unit. Where $dV_{c\_av(m)}$ represents the average value of $|dV_c|$, $k_{\max(n)}$ represents the calculated value of $k_{\max}$, and M represents the iterations of the control method, and normally its range is [0, 10]. $k_{\min}$ corresponds to the lowest $dV_{c\_av(m)}$, when the k varies from 0 to $k_{\max}$.

From (11), when $\varphi = \pi/2$, $m = 0.8$, and $k = 0.3$, the curves of the duty cycle of "0" state with the proposed DCOSPWM method are as shown in Fig. 8.

$$k_{\max} = \begin{cases} \dfrac{[2+2m\sin(\varphi/2)]\,C}{mI_mT_s(2+\cos\varphi)}, & -\pi \le \varphi < -2\pi/3 \\ \dfrac{\left(2-\sqrt{3}m\right)C}{-\sqrt{3}mI_mT_s\sin\varphi}, & -2\pi/3 \le \varphi < -\pi/3 \\ \dfrac{\left[2-m\cos(\varphi/2)+\sqrt{3}m\sin(\varphi/2)\right]C}{mI_mT_s(2-\cos\varphi)}, & -\pi/3 \le \varphi < 0 \\ \dfrac{\left[2-m\cos(\varphi/2)-\sqrt{3}m\sin(\varphi/2)\right]C}{mI_mT_s(2-\cos\varphi)}, & 0 \le \varphi < \pi/3 \\ \dfrac{\left(2-\sqrt{3}m\right)C}{\sqrt{3}mI_mT_s\sin\varphi}, & \pi/3 \le \varphi < 2\pi/3 \\ \dfrac{[2-2m\sin(\varphi/2)]\,C}{mI_mT_s(2+\cos\varphi)}, & 2\pi/3 \le \varphi < \pi \end{cases} \tag{14}$$

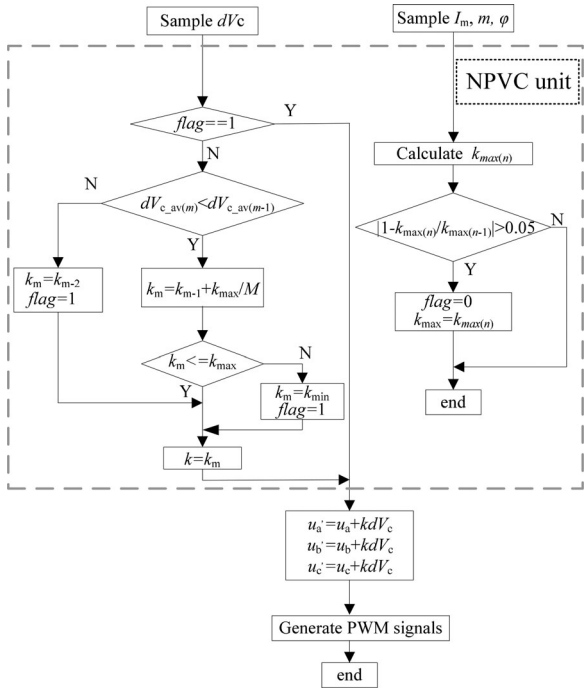

Fig. 7. Flowchart of the proposed DCOSPWM method.

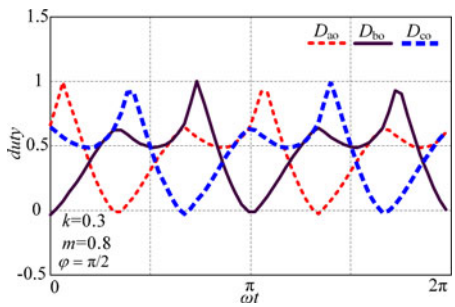

Fig. 8. Three-phase duty cycle of "0" state at $k = 0.3$, $\varphi = \pi/2$, $m = 0.8$.

IV. Performance Comparison

A. Analysis of Switching Loss

The switching loss is the key parameter to compare various control methods. For three-level voltage source inverters, the switching loss is linearly related to the load currents. So in a line cycle, the switching loss $\mathrm{P_{loss}}$ can be expressed as [21]

$$\mathrm{P_{loss}}=\frac{V_e}{2\pi}\int_0^{2\pi}|i(\omega t)|\,d\omega t \tag{16}$$

where V_e is an equivalent dc voltage for dc bus voltage, $i(\omega t)$ is the instantaneous value of the phase load current, and its amplitude is I_m.

For analyzing simply, V_e and I_m are normalized, and the curves of the inverter switching loss with three control methods are as shown in Fig. 9, where $\mathrm{Ploss_1}(I_m)$, $\mathrm{Ploss_2}\ (I_m)$, $\mathrm{Ploss_3}(I_m)$ represents the phase switching loss with the proposed DCOSPWM method in this paper, the OMS method in [2], and the PISVPWM method in [20] respectively.

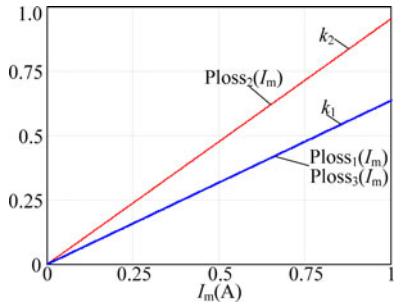

Fig. 9. Curves of $\mathrm{P_{loss}}$ with three control methods.

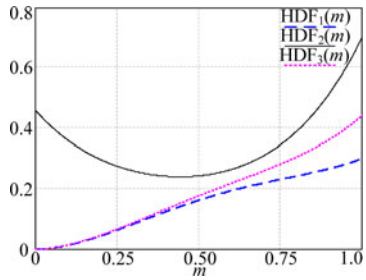

Fig. 10. Curves of HDF with three control methods.

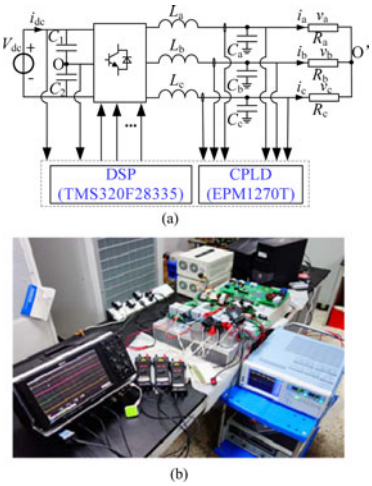

Fig. 11. Schematic diagram and experimental photograph of the system. (a) Schematic diagram of the system. (b) Experimental photograph of the system.

Define k_1 and k_2 as the slope of curves in Fig. 9, so it can be seen that

$$k_2 > k_1. \tag{17}$$

On the equal conditions, only the switching loss is considered, so from the relation between input and output power of the inverter, it can be obtained as

$$\eta = \frac{1}{(2/V_m)k+1} \tag{18}$$

where η is the output efficiency of the inverter, V_m is the amplitude value of the output phase voltage, k is the slope of the curves, which shows the variation of $\mathrm{P_{loss}}$ when I_m is varied.

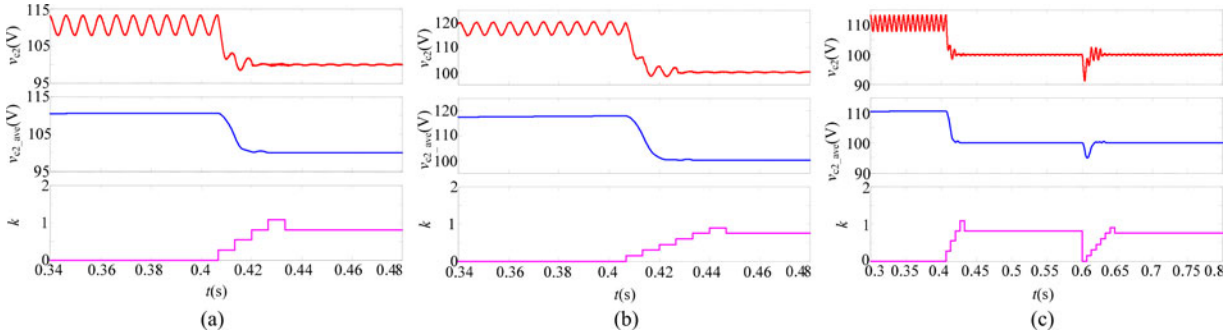

Fig. 12. Simulated waveforms of the proposed DCOSPWM method in this paper. (a) At resistive load. (b) At resistive and inductive load. (c) At varied load.

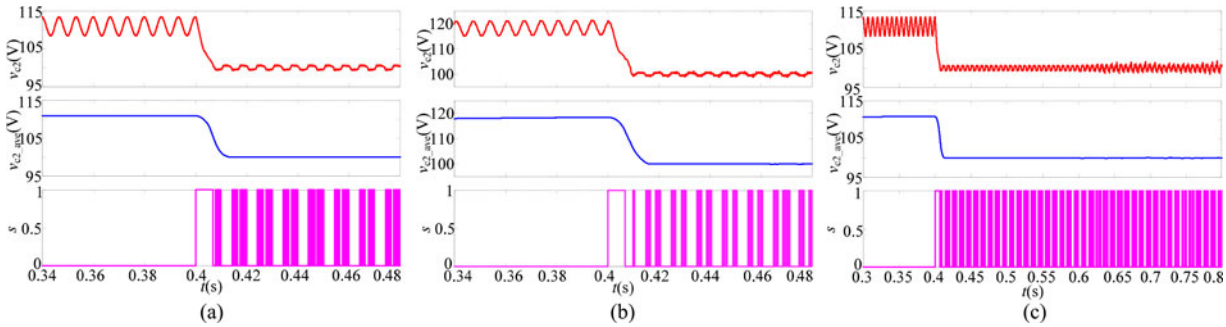

Fig. 13. Simulated waveforms of the OMS method in [2]. (a) At resistive load. (b) At resistive and inductive load. (c) At varied load.

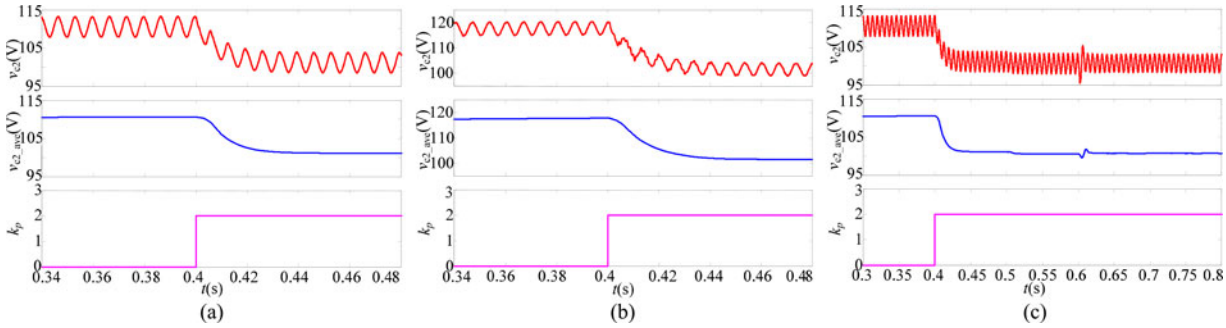

Fig. 14. Simulated waveforms of the PISVPWM method in [20]. (a) At resistive load. (b) At resistive and inductive load. (c) At varied load.

When V_{m} is given, from (17) and (18), the relationship of output efficiency among the three control methods can be expressed as

$$\eta_2 < \eta_1 = \eta_3 \tag{19}$$

where η_1, η_2, and η_3 represents the output efficiency with the proposed DCOSPWM method in this paper, the OMS method in [2], and the PISVPWM method in [20], respectively.

From Fig. 9 and (19), it can be seen that with the OMS method in [2], the output efficiency of the inverter is lower than other two control methods. As with the proposed DCOSPWM method, the PISVPWM method in [20] also obtains high efficiency, but it is at the cost of weaker control ability for balancing the neutral-point voltage and higher output harmonics, which is shown in Figs. 22 and 23.

B. Analysis of the Output Current Harmonics

In order to analyze the harmonic performance of the aforementioned three control methods, the output current should be calculated analytically, so the common expression can be derived as

$$f(m) = \frac{1}{\pi}\int_0^{\pi} \left[(u_2-u_1)^2 + (u_2-u_1)^3 + (u_2-u_1)\left(u_2^3-u_1^3\right)\right] d\omega t \tag{20}$$

where u_1 and u_2 represents the modulation waves of phase *a* and *b* for the three-level inverter, respectively. *f*(*m*) is harmonic distortion factor (HDF) [21], which shows the output current harmonics performance of various PWM control methods for three-level inverters. Define f_{c} as the carrier wave frequency and f_{line} as the fundamental wave frequency, when $f_{\mathrm{c}}/f_{\mathrm{line}}$

TABLE II
SIMULATED RESULTS ANALYSIS

Load condition	The average voltage difference of v_{c1} and v_{c2} / The ripple of v_{c1} or v_{c2}				Controlling process time of three methods		
	Traditional SPWM	Proposed DCOSPWM	OMS	PISVPWM	Proposed DCOSPWM	OMS	PISVPWM
Resistive load ($\cos(\varphi) = 1$)	22 V/6 V	0 V/0.5 V	0 V/2 V	0 V/6 V	34 ms	10 ms	36 ms
Resistive and inductive load ($\cos(\varphi) = 0.866$)	36 V/6 V	0 V/0.5 V	0V/2.5V	0V/6V	47 ms	12 ms	50 ms

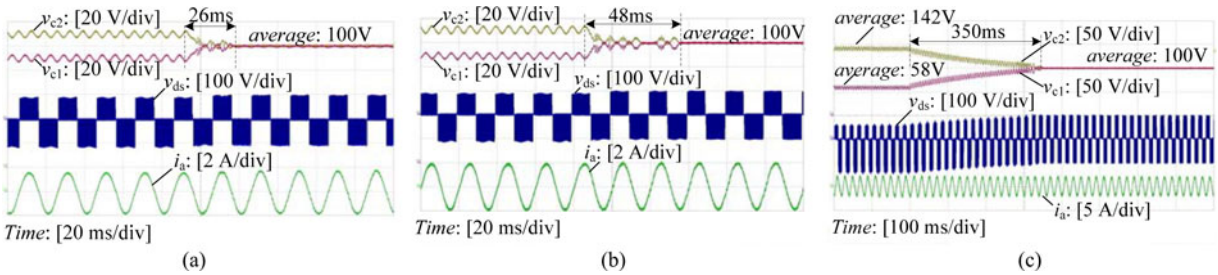

Fig. 15. Experimental waveforms of the proposed DCOSPWM method in this paper. (a) Cos(φ) =1. (b) (a) Cos(φ) =0.866. (c) Cos(φ) =0.

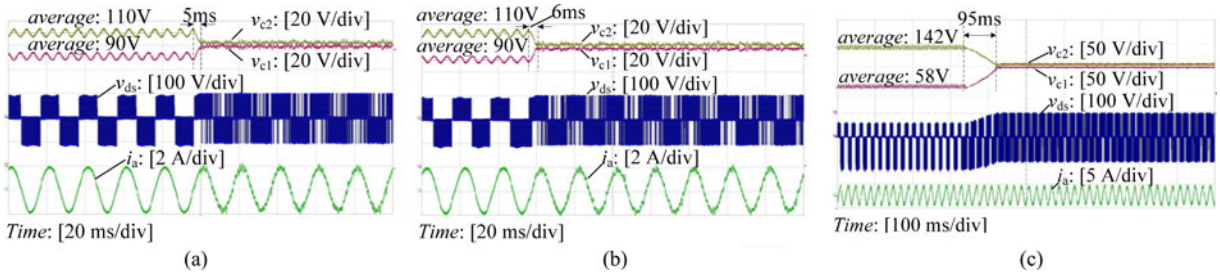

Fig. 16. Experimental waveforms of the OMS method in [2]. (a) Cos(φ) =1 (b) (a) Cos(φ) =0.866 (c) Cos(φ) =0.

is given, the variation trend of THD accords with that of the HDF. So commonly the HDF is used for analyzing THD of the output current for three-level inverters. The variation trend of the HDF with the aforementioned three control methods can be obtained from (20), which is shown in Fig. 10. Where $\mathrm{HDF}_1(m)$, $\mathrm{HDF}_2(m)$, and $\mathrm{HDF}_3(m)$ represent the HDF curves with the proposed DCOSPWM method in this paper, the OMS method in [2], and the PISVPWM method in [20], respectively. *m* is the modulation ratio.

From Fig. 10, it can be seen that when *m* varies from [0, 1], with the DCOSPWM method proposed in this paper, the output current has the lowest HDF value. When using the OMS method in [2], the HDF value increases much higher than other two methods.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the validity of the proposed control method, a simulation model of the NPC three-level inverter has been built using MATLAB tools.

The specifications of the simulation are as follows:

dc bus voltage: $V_{\mathrm{dc}} = 200$ V;

dc bus capacitors: $\mathrm{C}_1 = \mathrm{C}_2 = 150$ μF;

modulation ratio: $m = 0.8$;

switching frequency: $f_{\mathrm{s}} = 20$ kHz;

output power: $\mathrm{P}_{\mathrm{o}} = 200$ W.

Fig. 11 shows the schematic diagram of the simulation module and the photograph of the main experimental system. As shown in Fig. 11(b), the input waveforms, output waveforms, and the driving signals are measured or recorded by oscilloscope Lecroy 604 Zi. The output power, output current THD value, and power factor angle, i.e., are measured or recorded by the power analyzer YokogawaWT1800.

A. Simulation Analysis

To verify the effectiveness of the proposed method when the amplitude of dV_{c} is high, a resistor is connected in parallel with the dc bus capacitor C_1 for the NPC three-level inverter shown in Fig. 1, resulting in the difference between the equivalent impedance of dc bus capacitor C_1 and C_2, so the neutral-point unbalancing appears. Figs. 12–14 show the simulated waveforms of v_{c2} and $v_{\mathrm{c2\_ave}}$ (the average value of v_{c2}), the search process of *k*, the control signal *s*, and the PI parameter k_{p}, respectively. Where in Fig. 13, "*s*" represents control signal of the OMS method in [2], "$s = 1$" represents the system is

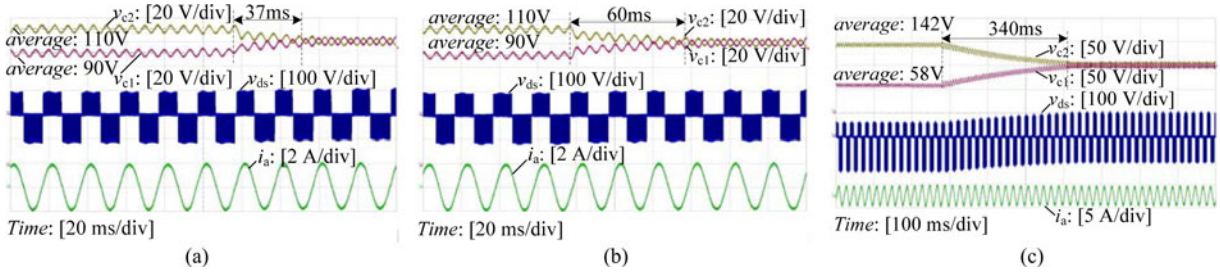

Fig. 17. Experimental waveforms of the PISVPWM method in [20] (a) Cos(φ) =1. (b) Cos(φ) =0.866. (c) Cos(φ) =0.

TABLE III
EXPERIMENTAL WAVEFORMS ANALYSIS

Load condition	The average voltage difference of v_{c1} and v_{c2} / The ripple of v_{c1} or v_{c2}				Controlling process time of three methods		
	Traditional SPWM	Proposed DCOSPWM	OMS	PISVPWM	Proposed DCOSPWM	OMS	PISVPWM
Resistive load ($\cos(\varphi) = 1$)	20 V/6 V	0 V/1V	4 V/3 V	0 V/6V	26 ms	5 ms	37 ms
Resistive and inductive load ($\cos(\varphi) = 0.866$)	20 V/6V	0V/1V	4 V/2 V	1 V/6 V	48 ms	6 ms	60 ms
inductive load ($\cos(\varphi) = 0$)	84 V/10 V	0 V/2 V	6 V/3 V	0V/9V	350 ms	95 ms	340 ms

under the neutral-point voltage balance controlling, "$s = 0$" means that the system is working without neutral-point voltage balance controlling. In Fig. 14, where "k_p" represents the proportional parameter of the proportional controller for balancing the neutral-point voltage using the PISVPWM method in [20].

In Figs. 12–14, before 0.4 s, the system works with the traditional SPWM modulation control. At 0.4 s, the system switches to the different control methods for the neutral-point balance. From Fig. 12(a), it can be seen with the proposed DCOSPWM method in this paper, the system searches the optimal value of *k* at about 0.434 s, and *k* is 0.81, v_{c2_ave} is 100 V, the ripple of v_{c2} is 0.5 V. The whole search time is 34 ms.

And the details of the proposed DCOSPWM method in this paper, the OMS method in [2] and the PISVPWM method in [20], which are shown in Table II.

Compared with the OMS and PISVPWM methods, the proposed DCOSPWM method has strong ability for the neutral-point voltage balancing from the simulated results. When the neutral-point voltage is unbalancing, the proposed DCOSPWM method in this paper can control the neutral-point voltage to be balancing fast, meanwhile, the steady-state error and the ripple of the neural-point voltage is the lowest, which is the shown in Table II, so the system has very good steady-state effects with the DCOSPWM method proposed in this paper.

B. Experimental Verification

Also the proposed DCOSPWM method has been tested in the experimental platform of the NPC three-level inverter based on DSP-CPLD, as shown in Fig. 11(b).

The specifications of the prototype are as follows:
dc bus voltage: $V_{dc} = 200$ V;
dc bus capacitors: $C_1 = C_2 = 150$ μF;
modulation ratio: $m = 0.8$;
switching frequency: $f_s = 20$ kHz;
output power: $P_o = 200$ W;
Digital Process Unit: TMS320F28335 DSP;
Power switches module: IGBT FZ06NPA070FP;
Output phase filter: L: 1.5 mH, C: 10 μF.

When connecting a parallel resistor to the dc bus capacitor C_1 for the NPC three-level inverter shown in Fig. 1, The waveforms of v_{c1}, v_{c2}, v_{ds}, and i_a with the traditional SPWM control, the proposed DCOSPWM method, the OMS method in [2], and the PISVPWM method in [20] are as shown in Figs. 15–17, where v_{ds} is the leg voltage of phase *a* and i_a is the load current of phase *a*.

From Fig. 15(a), Fig. 15(b) and (c), it can be seen that before using the proposed DCOSPWM method, the neutral-point voltage is unbalancing, and the average voltage of the capacitor C_2 is higher than that of C_1 with a big ripple. In a line cycle, the amplitude of phase *a* output leg level in the negative half cycle is higher than it in the positive cycle.

When using the proposed control method, the voltage difference between the average voltage of C_1 and C_2 decreases to zero almost, the system reaches to a steady-state rapidly, and the ripple of v_{c1} or v_{c2} is very low, which satisfies the preset steady-state threshold. Especially, the proposed DCOSPWM method has strong ability to balance the neutral-point voltage at pure inductive load ($\cos(\varphi) = 0$) when the neutral-point voltage is heavy unbalancing. In a line cycle, the amplitude of phase *a* output leg level in the positive half cycle is symmetrical with it in the negative half cycle, so as to the load current. The details of the proposed DCOSPWM method and other two control methods in [2] and [20] are shown in Table III. It can be seen that the OMS method in [2] shows quicker dynamic response ability, but it is at the cost of larger steady-state error, the higher THD value and higher system power loss, which is shown in Figs. 9 and 10. The proposed DCOSPWM method in this paper

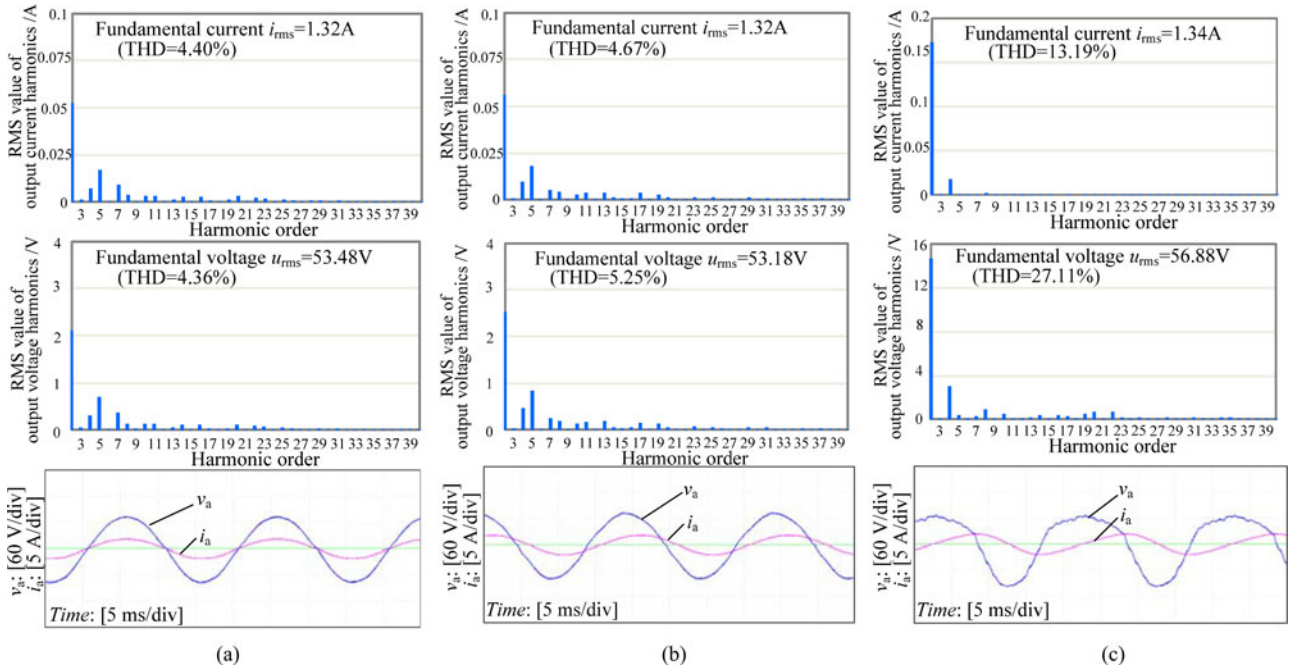

Fig. 18. Experimental waveforms of the traditional SPWM control method in this paper. (a) Cos(φ) =1. (b) Cos(φ) =0.866. (c) Cos(φ) =0.

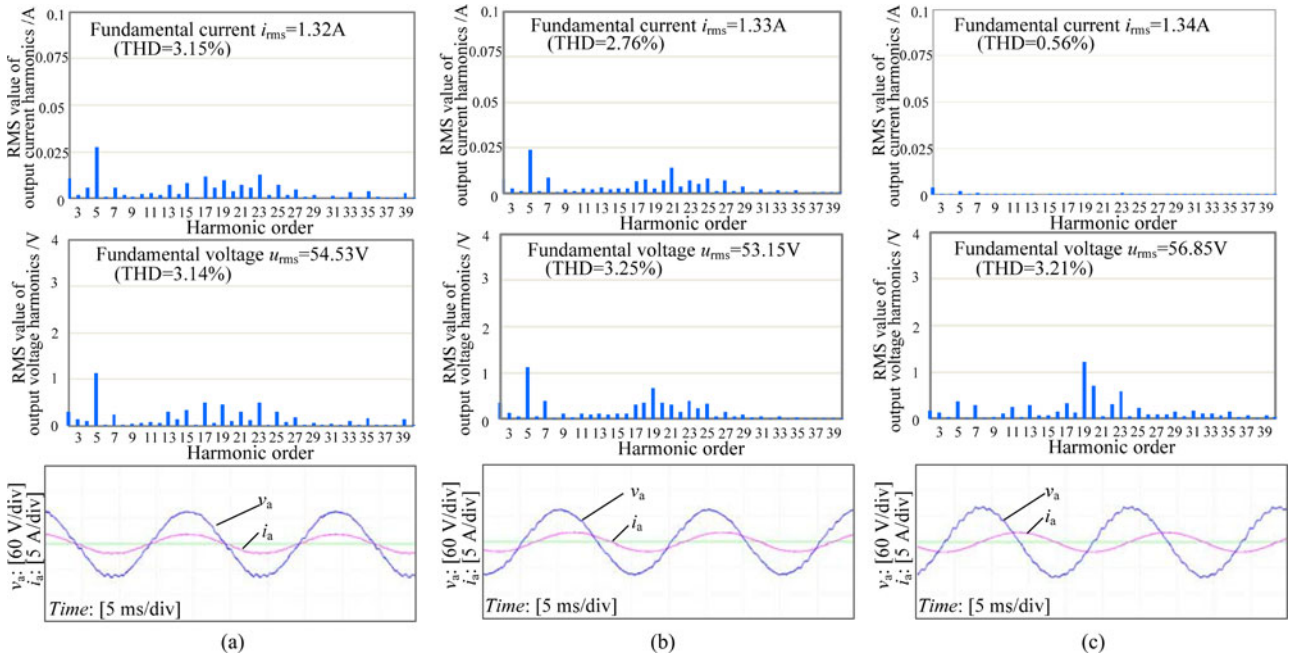

Fig. 19. Experimental waveforms of the proposed DCOSPWM method in this paper. (a) Cos(φ) =1. (b) Cos(φ) =0.866. (c) Cos(φ) =0.

has better performance in terms of control precision and system steady-state error, comparing with the OMS method in [2] and the PISVPWM method in [20].

Figs. 18–21 show the waveforms of v_a and i_a and the **THD analysis of i_a and v_a with the traditional SPWM control, the proposed DCOSPWM method in this paper, the OMS method in [2], and the PISVPWM method in [20], respectively, when the neutral-point voltage of the system is unbalancing, where v_a is the load voltage of phase a. It can be seen that using the proposed DCOSPWM method in this paper, the THD value of i_a decreases from 4.40% to 3.15% at $\cos(\varphi) = 1$, as shown in Figs. 18(a) and 19(a). At $\cos(\varphi) = 0.866$ as shown in Figs. 18(b) and 19(b), the THD value of i_a decreases from 4.67% to 2.76%, and when the system works at $\cos(\varphi) = 0$, the THD value of i_a decreases from 13.19% to 0.56%, as shown in Figs. 18(c) and 19(c). So from Figs. 18–21, it can be seen that using the proposed DCOSPWM method in this paper, the output waveforms show the obvious advantage in terms of THD at various load

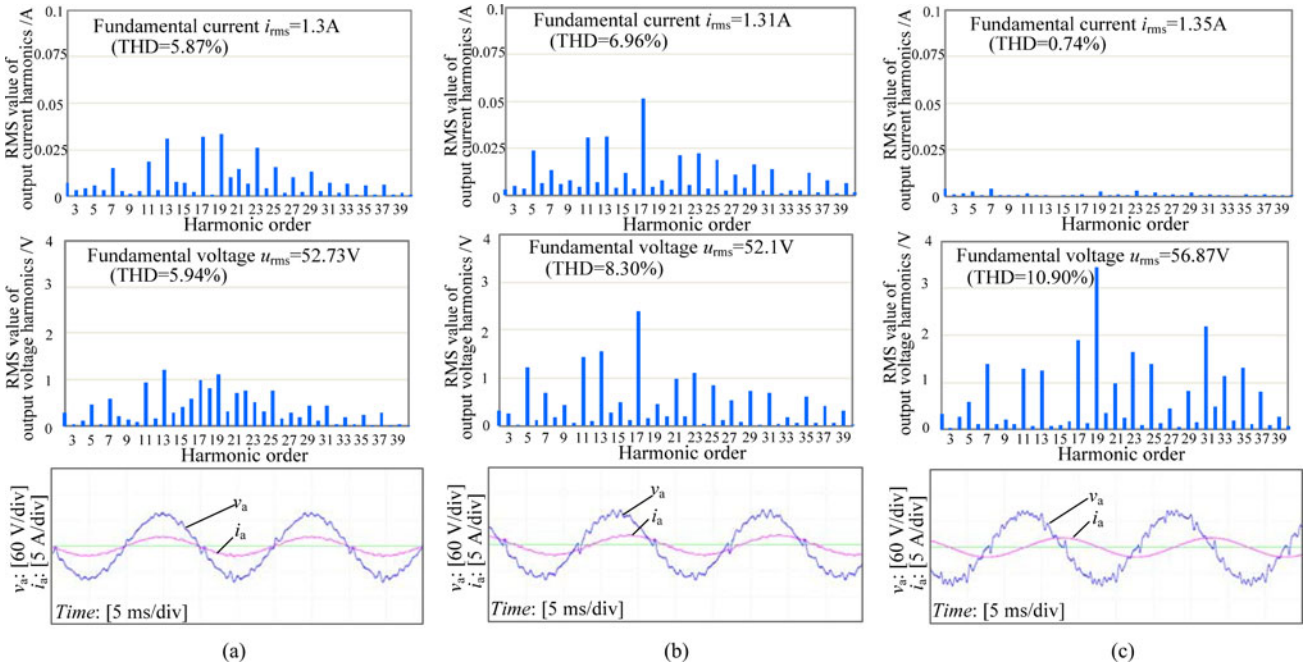

Fig. 20. Experimental waveforms of the OMS method in [2]. (a) Cos(φ) =1. (b) Cos(φ) =0.866. (c) Cos(φ) =0.

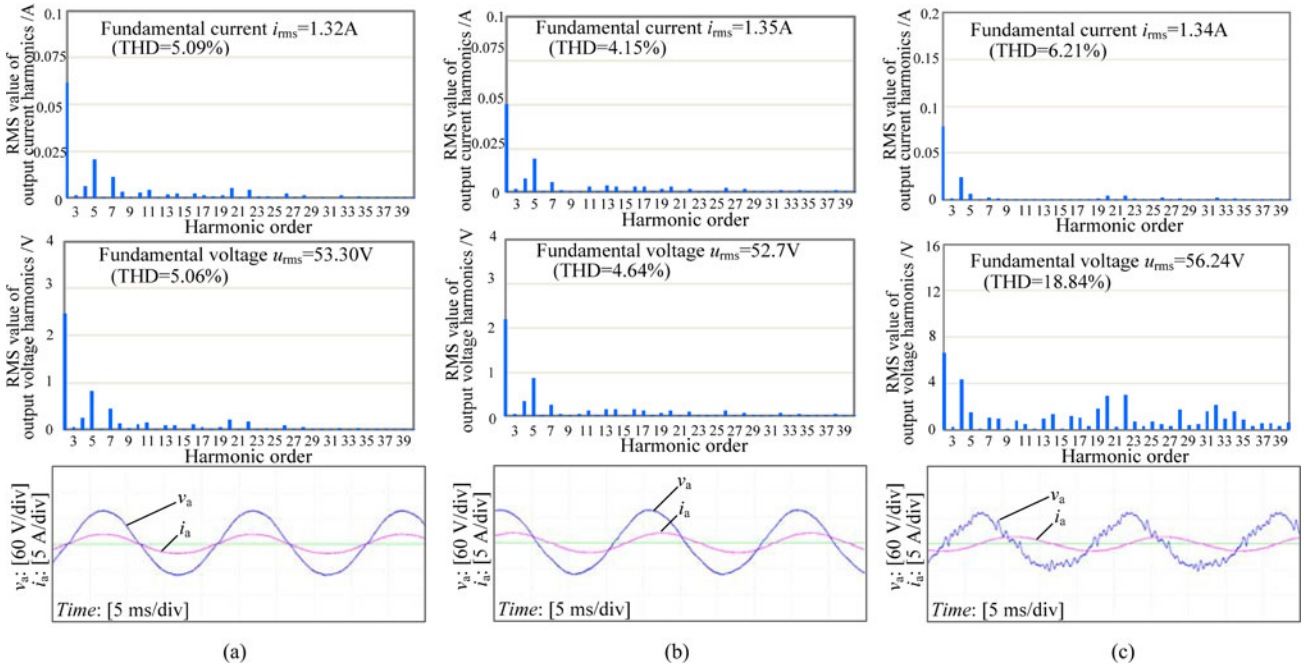

Fig. 21. Experimental waveforms of the PISVPWM method in [20]. (a) Cos(φ) =1. (b) Cos(φ) =0.866. (c) Cos(φ) =0.

power factor conditions, comparing with OMS and PISVPWM methods.

Figs. 22 and 23 show the ripple value of v_{c2} and the THD of the output current at different resistive load conditions with the three control methods (the proposed DCOSPWM, the OMS, and PISVPWM methods). It can be seen that at different output power, comparing with other two control methods, the DCOSPWM method proposed in this paper decreases the ripple value of the neutral-point voltage effectively, and the output waveforms quality is improved.

Also the efficiency curves of the aforementioned three control methods at different resistive load conditions are shown in Fig. 24, it can be seen that at different output power, the DCOSPWM method proposed in this paper achieves the neutral-point voltage balance, which has the highest system efficiency, instead, when using the OMS method in [2], the

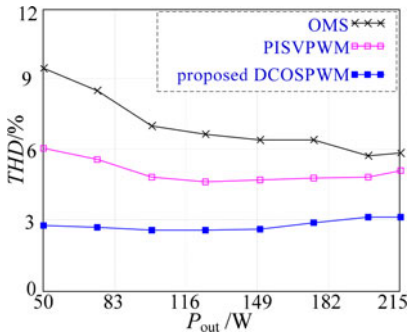

Fig. 22. Measured THD.

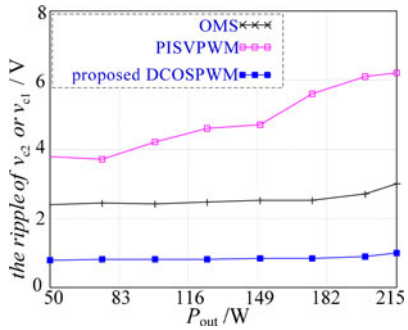

Fig. 23. Measured neutral-point voltage ripple.

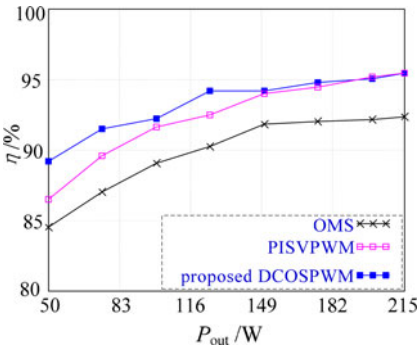

Fig. 24. Measured Efficiency.

system efficiency is decreased and obviously lower than other two methods.

According to the experimental results, when the neutral-point voltage is unbalancing, the proposed DCOSPWM method, which has strong ability to control the neutral-point voltage balancing at different load conditions, not only has the highest system efficiency and the lowest steady-state error, but also improves the output waveforms quality and reduces its THD effectively, comparing with other two methods in [2] and [20].

VI. Conclusion

In order to solve the neutral-point voltage unbalancing problem for three-level inverters, this paper studies the factors that affect the fluctuation of neutral-point voltage, based on the mathematical expressions of unbalancing neutral-point voltage. Theoretically, the mathematical expressions of the neutral-point voltage with the proposed DCOSPWM method are derived, and the mathematical relationship between the fluctuation of neutral-point voltage and adjusting the offset of modulation wave is studied. This proposed DCOSPWM method realizes balancing neutral-point voltage by dynamically calculating the offset superimposed to modulation wave based on SPWM. It also can improve the quality of output waveforms and reduce the harmonic distortion. This DCOSPWM method is very simple, which has good steady-state performance and is easy for digital implementation. Simulation and experimental results verified the feasibility and effectiveness of the proposed method.

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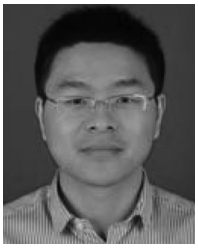

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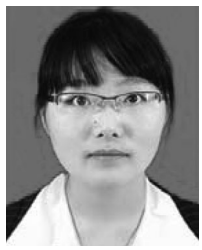

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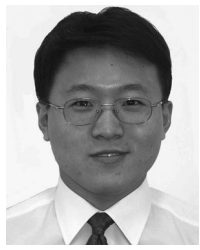

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