Variable-Frequency Phase Shift Modulation of a Dual Active Bridge Converter

Jani Hiltunen, *Member, IEEE*, Vesa Väisänen, *Member, IEEE*, Raimo Juntunen, *Member, IEEE*, and Pertti Silventoinen, *Member, IEEE*

***Abstract*—In this paper, a variable-frequency modulation method for a dual active bridge converter is introduced. The proposed method ensures zero-voltage switching over a wide power range with a minimal circulating current. Unlike previously presented modulation schemes, this modulation method can also be used for half-bridge variants of a traditional dual active bridge converter. The modulation method is given in a closed form, which makes it easy to apply in practice. Further, the phase drift phenomenon is discussed, and a simple phase drift compensation scheme is presented. Finally, a detailed analysis of the proposed modulation method is provided and its feasibility is verified by measurements.**

***Index Terms*—Current control, dc–dc power converters, error correction, modeling, modulation, power system control, switched-mode power supply.**

I. Introduction

OVER the recent years, the dual active bridge (DAB) converter topology has gained popularity because of its favorable zero-voltage switching (ZVS) properties, bidirectional power transfer capabilities, and a low sensitivity to system parasitics. The DAB topology has been widely applied to various energy storage [1] and solid state transformer [2] applications. The DAB is a very attractive topology for applications where bidirectional power flow, galvanic isolation, and a high power density are required.

The DAB topology has been shown to be capable of providing a very high power conversion efficiency [3]. However, the switching and conduction losses of the DAB are heavily dependent on the input-output voltage conversion ratio and the transferred power. When operated outside the nominal voltage conversion ratio, the DAB converter suffers from circulating currents, which significantly increase the conduction losses. Moreover, at light loads, the energy stored in the leakage inductance may not be large enough to discharge the drain-source capacitances of the switching components. This results in a hard-switching that can drastically reduce the power conversion efficiency and increase the electromagnetic interference generated by the converter [4].

Manuscript received June 27, 2014; revised November 28, 2014; accepted January 3, 2015. Date of publication January 12, 2015; date of current version August 21, 2015. This work was supported by the European Union's Seventh Framework Program (FP7/2007-2013) for the Fuel Cells and Hydrogen Joint Technology Initiative under Grant 621213. Recommended for publication by Associate Editor D. Xu.

The authors are with the Department of Electrical Engineering, Lappeenranta University of Technology, Lappeenranta 53850, Finland (e-mail: jani.hiltunen@lut.fi; vesa.vaisanen@lut.fi; raimo.juntunen@lut.fi; pertti.silventoinen@lut.fi).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2390913

Over the recent years, various modulation strategies have been presented to extend the soft-switching region and reduce the circulating current. The proposed methods have often based on manipulation of the transformer current by introducing a zero-voltage sequence either on the primary or secondary side of the transformer. During this sequence, a zero-voltage is applied to the winding. The zero-voltage sequence is achieved by changing the phase shift between the switching legs of an H-bridge. This gives an additional degree of freedom for the control compared with the traditional phase shift modulation (PSM), where only the phase shift between the primary and secondary H-bridges is controlled. By using a zero-voltage sequence, the soft-switching region of a DAB can be extended and the conduction losses can be reduced. According to the transformer current waveform, this type of a modulation scheme is sometimes called a triangular current mode modulation or a trapezoidal current mode modulation [5]. If a zero-voltage sequence is used in both full-bridges of the DAB, the modulation is sometimes called a dual PSM [6], [7].

All of the aforementioned modulation methods are based on the zero-voltage sequence produced by shorting the primary or secondary winding of a transformer through an H-bridge. By using only one modulation scheme, it is difficult to achieve the best efficiency over the whole operating region. Therefore, different modulation methods are often combined to cover a larger operating region. A hybrid modulation method that combines several different modulation methods has been discussed in publications [8]–[10]. However, the hybrid modulation leads to a complex implementation where the modulation strategy has to be changed according to the operating point.

The use of the zero-voltage sequence can increase the overall efficiency, especially in a low power range, where the hard-switching would normally ruin the efficiency. However, the use of the zero-voltage sequence will increase the transformer RMS current by introducing an additional circulating current inside the H-bridge. This additional current may reduce the efficiency in applications where the transformer conduction losses are dominating. Another limitation of the method is present when a half-bridge variant of the DAB is used. In this case, there is no H-bridge that could be used to generate the zero-voltage sequence. Therefore, modulation methods based on the zero-voltage sequence are not feasible for half-bridge-based converters.

Instead of using a zero-voltage sequence to extend the soft-switching region, a variable switching frequency modulation method can be used. This method is not limited to the full-bridge topologies, but it can also be used for half-bridge topologies. The basic idea of using the variable switching frequency modulation in a DAB converter has been proposed in [11]–[13].

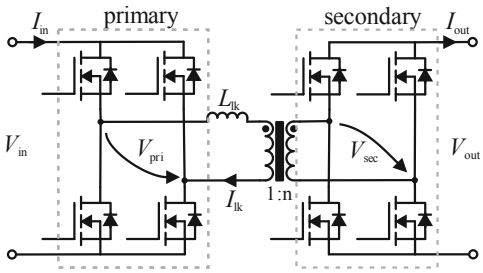

Fig. 1. Circuit diagram of a traditional DAB converter with full-bridges on the primary and secondary side of the transformer.

In [11], a numerical optimization algorithm is used to optimize the switching frequency along with other modulation parameters. This approach gives a freedom to the designer to optimize the modulation method for a specific application and specific hardware. However, it leads to a complicated design process that requires fine-tuning of the parameters. This method also requires the use of a lookup table for implementation. The variable-frequency modulation (VFM) method presented in [12] uses a fixed ratio between the RMS and peak currents to extend the soft-switching range. The method provides a very simple closed-form implementation, but it may result in an unnecessary circulating current and switching at nonoptimal currents.

In this paper, a simple closed-form solution for the VFM is introduced. The presented method is based on switching at a predefined current value. The proposed modulation scheme allows either a ZVS or a zero-current switching (ZCS) depending on how the switching current level is chosen. The modulation method also minimizes the transformer RMS current by limiting the reactive current to some predefined value. The method is most suitable for applications where a half-bridge variant of the DAB converter is preferred over the traditional full-bridge. The feasibility of the proposed modulation method is mainly limited by the transformer ac resistance, turn-off losses, and the gate driving losses.

In this paper, the effect of the phase drift phenomenon [14] is also discussed. The phase drift can distort the phase-shift-to-power relationship in the power flow analysis, which may lead to the failure of the traditional DAB power equation. It can also interfere with the proposed VFM method. The paper introduces a simple phase drift compensation scheme that ensures a proper operation of the variable-frequency modulation. Finally, the effectiveness of the modulation method is demonstrated with a laboratory prototype.

The main contribution of the paper is a closed-form algorithm for the VFM and a generalized power equation for the half-bridge variants of the DAB. The paper demonstrates the effects of the phase drift phenomenon and a method to compensate it. Moreover, a back commutation phenomenon is explained.

II. DAB AND PSM

The DAB converter consists of two semiconductor bridges linked together with a high-frequency transformer (see Fig. 1). In the DAB, the leakage inductance of the transformer ($L_{\rm lk}$) is used as an energy transfer element. The power flow through

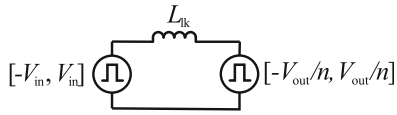

Fig. 2. Simplified operating model of a DAB converter. The model describes the operation of a DAB converter with a sufficient accuracy when the losses are low and the magnetizing inductance is large enough to be neglected.

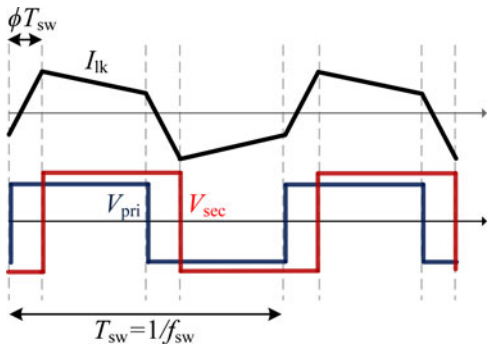

Fig. 3. Idealized operating waveforms of the DAB converter when $V_{\rm in} < V_{\rm out}/n$ and the power flow is from $V_{\rm in}$ to $V_{\rm out}$.

the leakage inductance is controlled by changing the phase shift between the primary and secondary bridges as shown in Fig. 2.

If the losses of the DAB are omitted and the effect of the magnetizing inductance is neglected, the operation of the converter can be simplified into an inductor connected to two equivalent voltage sources (see Fig. 2). By this simplification, idealized operating waveforms can be generated (see Fig. 3). By using the mean-value theorem, the power equation for the converter can be derived as

$$P = \frac{V_{\rm in} V_{\rm out}/n}{f_{\rm sw} L_{\rm lk}} \phi\,(1 - 2\phi) \tag{1}$$

where $f_{\rm sw}$ is the switching frequency and $L_{\rm lk}$ is the leakage inductance of the transformer seen from the primary side. This well-known equation was first presented in [15]. The power equation (1) is sometimes presented in a slightly different form, where the phase shift is presented in radians. However, in this paper, the phase shift ϕ is represented as a percentage of the switching period $T_{\rm sw}$. If radians are preferred, the conversion can be easily made by multiplying the phase shift by 2π.

III. HALF-BRIDGE VARIANTS OF THE TRADITIONAL DAB TOPOLOGY

In some cases, it is beneficial to use a half-bridge structure instead of a full-bridge (see Fig. 4). The half-bridge converter can be a feasible solution in high-voltage and low-current applications when a low number of active components and a high voltage conversion ratio are needed.

The use of the half-bridge inherently doubles the voltage of the transformer winding. Therefore, the half-bridge can be used to reduce the transformer turns ratio. The voltage doubling effect of the half-bridge allows the use of a smaller leakage inductance in the DAB for the same power. This is very useful for low-power converters, where a high leakage inductance value is required to

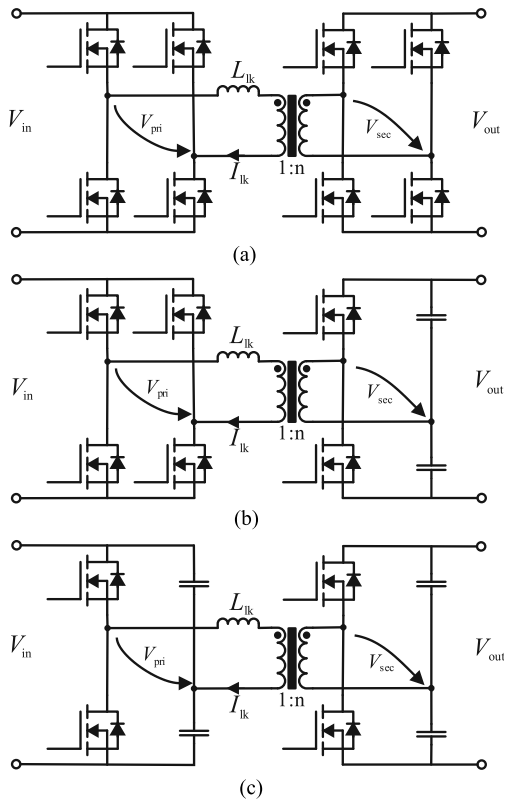

Fig. 4. Three variations of the DAB converter. (a) DAB with a full-bridge primary and a full-bridge secondary. (b) DAB with a full-bridge primary and a half-bridge secondary. (c) DAB with a half-bridge primary and a half-bridge secondary.

limit the power to a desired level. Often, a high inductance value has to be achieved by using an external inductor in series with the transformer. This bulky external inductor may be avoided by using the half-bridge variant of the DAB. The downside of the half-bridge is that it doubles the transformer current compared with an equivalent full-bridge design. Thereby, it increases the conduction losses.

Another benefit gained by the half-bridge is the dc blocking capability. The capacitors used in the half-bridge act as a dc blocking element. This prevents transformer saturation [16] often considered a problem in the DAB converters [17]. The half-bridge can also be used to simplify the converter design; it reduces the number of semiconductor switches and thereby the number of gate drivers and auxiliary components.

The usability of the half-bridge is limited by the increased current stress on the transformer and the power switches. Further, the additional losses in the half-bridge capacitors may restrict the usability. It is often stated that the full-bridge converter can provide a higher power density than the half-bridge converter. However, with the modern ceramic and film capacitors, a very good capacitance to volume ratio and a good high-frequency performance can be achieved. In addition, space and cost savings can be obtained as a result of the reduced number of components. However, the selection between the full-bridge and the half-bridge has to be made on a case-by-case basis, and for many applications, the full-bridge converter is still the more attractive option.

For the design of a half-bridge DAB, a power equation is needed. Unfortunately, the traditional power flow (1) of the DAB has to be modified for the half-bridge converter. This can be done by assuming that the half-bridge capacitors are large enough to be considered constant voltage sources. In addition, the additional voltage conversion ratio caused by the half-bridge has to be taken into account.

The power equation for the half-bridge converter can be derived from (1) by replacing the voltages $V_{\rm in}$ and $V_{\rm out}/n$ with the equivalent voltages V_1 and V_2. These equivalent voltages can be calculated by reducing the transformer winding voltages ($V_{\rm pri}$ and $V_{\rm sec}$) to the same side of the transformer. This yields

$$\begin{cases} V_1 = h_{\rm pri} V_{\rm in} \\ V_2 = h_{\rm sec} V_{\rm out}/n \end{cases} \tag{2}$$

where $h_{\rm pri}$ is a variable describing the structure of the primary-side bridge and $h_{\rm sec}$ represents the structure of the secondary-side bridge. The variables $h_{\rm pri}$ and $h_{\rm sec}$ are valued either 1 or 0.5 depending on the bridge type

$$h_{\rm pri},\ h_{\rm sec} = \begin{cases} 0.5 & |\text{for half bridge} \\ 1 & |\text{for full bridge.} \end{cases} \tag{3}$$

By using the previous definitions, a generalized power equation for the DAB converter and all of its variants can be written as

$$P = \frac{V_1 V_2}{f_{\rm sw} L_{\rm lk}} \phi \left(1 - 2\phi\right) \tag{4}$$

where $L_{\rm lk}$ is the leakage inductance of the transformer seen from the primary side (V_1 side). As mentioned, the phase shift ϕ is represented in percentage of the switching period.

IV. ZVS OF THE DAB

In traditional phase-shift modulation there is always some amount of circulating reactive current between the H-bridge and the dc link capacitors (see Fig. 5). In the zero-voltage-sequence-based modulation [6], [8] there is a circulating current inside the H-bridge in addition to the circulating between the H-bridge and the dc link capacitors. While the circulating current is an inevitable by-product of the ZVS, it will also increase the conduction losses [5]. Therefore, it is desirable to reduce the circulating current to the minimum amount necessary for the zero-voltage switching.

A. Minimum Requirement for the Discharge Energy

When a switching event is taking place in the DAB, the energy stored in the leakage inductance is used to discharge the output capacitances of the semiconductor switches. This stored energy has to be large enough to enable zero-voltage switching. In order to ensure zero-voltage operation, a sufficient amount of inductor current and a dead time has to be applied.

The amount of current needed to discharge the output capacitances can be calculated as shown in several publications [15], [18]. For zero-voltage switching, the following inequality must

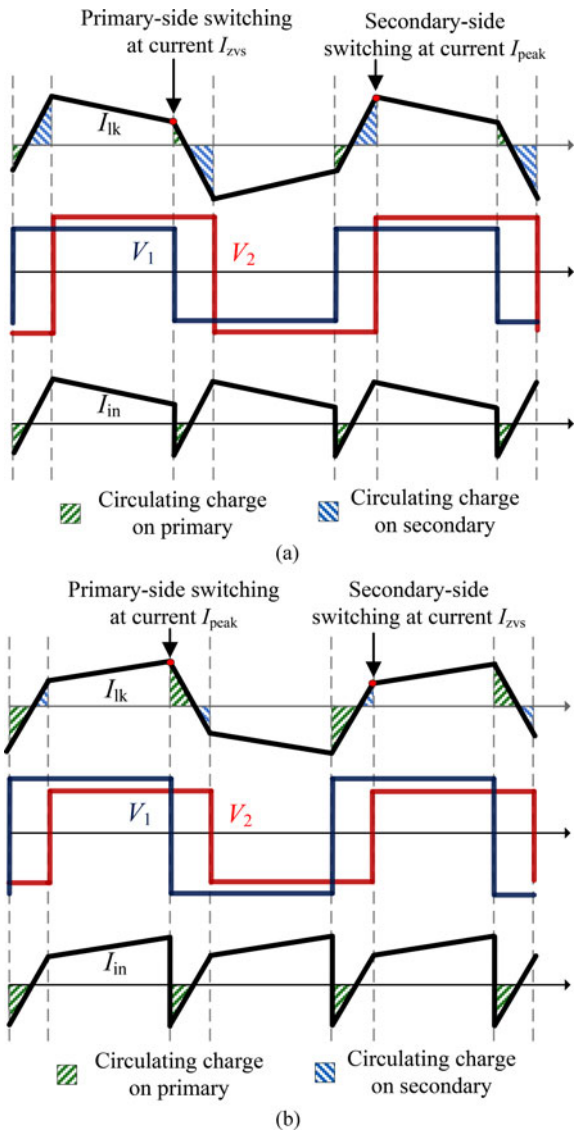

Fig. 5. Idealized operating waveforms of the DAB for two cases. (a) Equivalent secondary voltage (V_2) is higher than the equivalent primary voltage (V_1). The primary-side bridge is zero-voltage switched if the current $I_{\rm zvs}$ is large enough and of the right polarity. The secondary-side bridge is switched at the current $I_{\rm peak}$ and is zero-voltage switched whenever the primary-side bridge is zero-voltage switched (similar switches are assumed for both sides). (b) Equivalent primary voltage (V_1) is higher than the equivalent secondary voltage (V_2). The secondary-side bridge is zero-voltage switched if the current $I_{\rm zvs}$ is large enough and of the right polarity. The primary-side bridge is switched at the $I_{\rm peak}$ current, and it is zero-voltage switched whenever the secondary-side bridge is zero-voltage switched (similar switches are assumed for both sides).

be true:

$$\frac{1}{2}L_{\rm lk}I_{\rm zvs}^2 \geq k\frac{1}{2}C_{\rm o}V_{\rm bridge}^2 \tag{5}$$

where k is the number of switching devices, $I_{\rm zvs}$ is the transformer current at the switching instance, and C_o is the effective output capacitance of the switching device.

B. Back Commutation and the Dead Time

In the case of hard-switching, a dead time between the complementary switching devices is needed to prevent a destructive shoot-through. In a ZVS application, a dead time is needed to complete the zero-voltage transition. If the chosen dead time is too short with respect to the zero-voltage transition time, a hard-switching or a partial ZVS will result. The zero-voltage transition time is the time that is needed for the inductor current to charge or discharge the capacitances of the switching devices. The minimum dead time needed for the zero-voltage transition can be estimated as

$$t_{\rm dead,min} = \frac{Q\left(V_{\rm ds}\right)}{I_{\rm sw}} = \frac{2V_{\rm ds}C_{\rm o,tr}\left(V_{\rm ds}\right)}{I_{\rm sw}} \tag{6}$$

where Q is the charge of the switching leg, $C_{\rm o,tr}$ is the equivalent time-related capacitance of the switching device, and $I_{\rm sw}$ is the current of the switching leg at the switching instance. The current $I_{\rm sw}$ is equal to $I_{\rm zvs}$ or $I_{\rm peak}$ depending on the voltages on the primary and secondary sides (see Fig. 5). The charge Q and the equivalent time-related capacitance $C_{\rm o,tr}$ are functions of drain-source voltage. The capacitance $C_{\rm o,tr}$ is usually given in the datasheet for some fixed value of the drain-source voltage. It must be noted that (6) assumes the current $I_{\rm sw}$ and the voltage $V_{\rm ds}$ to remain constant during the switching transition. In practice, these values change during the transition because of the *LC* oscillation between the leakage inductance and the power switches.

The dead time given by (6) is optimal from the efficiency point of view because it minimizes the conduction time of the body diode. In practice, however, a slightly longer dead time is often required to overcome the inaccuracies in the modulator and the gate driving circuitry. If the dead time is too long, the leakage inductor current can change polarity during the dead time. This will cause the switching leg to back commutate (see Fig. 6), which will lead to increased switching losses. The efficiency in the back commutation case was 92%, while it was 93.7% in the case of Fig. 6(b). The upper limit for the dead time to prevent back commutation can be estimated by assuming linear behavior of the transformer current during the zero-voltage transition. This leads to an inequality

$$t_{\rm dead,max} = \frac{I_{\rm sw}L_{\rm lk}}{V_1 + V_2}. \tag{7}$$

In practice, the transformer current cannot change linearly until the ZVS transition has been completed. Therefore, (7) does not give a fully accurate result and can easily underestimate the maximum dead time. For a better estimation the sum of the zero-voltage transition time (6) and the back commutation time (7) can be used.

In order to achieve an optimal switching transition, a variable length for the dead time is required. Moreover, the dead time should be independently adjusted for both the primary and secondary bridges. In many real-world applications, a fixed dead time is preferred because of the simplicity of the implementation. This may require a tradeoff between the ZVS and the back commutation phenomenon. However, if the current of the switching instance is known and the output capacitance of the switching device is nearly linear within the operating region, a fixed dead time value can be used to achieve sufficient results. Therefore, it would be beneficial if we could force the

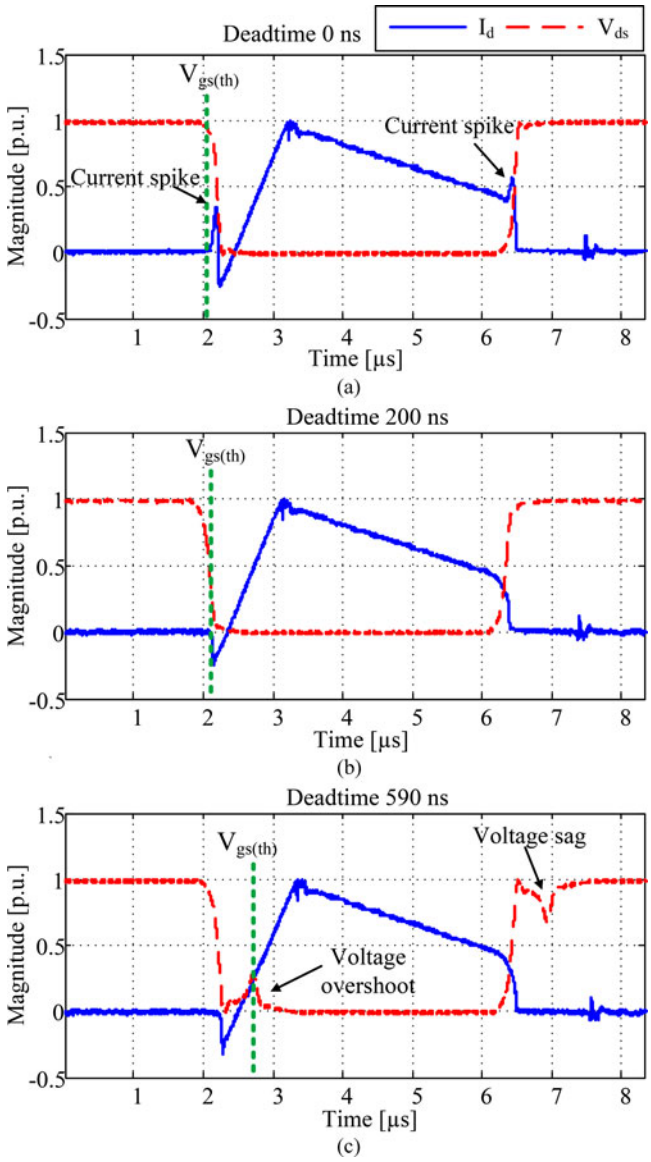

Fig. 6. Three dead time lengths and their effects on the switching waveforms. (a) Dead time is too short to complete full zero-voltage transition. The delivered charge is not enough to fully charge and discharge the capacitances of the switching devices during the dead time. This results in a partial hard-switching that can be seen as current spikes in the figure. (b) Dead time is of the right length, the zero-voltage transition is completed, and the back commutation is prevented. The voltage and current waveforms are smooth without additional overshoots. (c) Dead time is too long. The zero-voltage transition is completed but the inductor current changes polarity and starts to recharge the drain-source capacitances. This results in a back commutation, which can be seen as a voltage sag in the drain-source voltage. The back commutation phenomenon increases the switching losses and the EMI.

switching at a predefined current. The modulation scheme to force switching at a predefined current value is presented in the following.

V. VFM OF THE DAB

In the DAB, the switching frequency together with the leakage inductance defines the maximum power rating of the converter. The selection of the switching frequency is often related to the design process of the magnetic components. Decreasing the switching frequency from its design value would increase the power transfer capability, but is not often possible because of the risk of saturating the magnetic components. Unlike decreasing the switching frequency, increasing the switching frequency limits the power transfer capability of the DAB and reduces the magnetization current of the magnetic cores. While an increase in the switching frequency reduces the power transfer capability, it also extends the soft-switching capability to lower power levels. This makes manipulation of the switching frequency a useful tool for applications where a large soft-switching region is preferred.

A high switching frequency is often undesirable because of the increased switching and gate driving losses. A high switching frequency can also increase the conduction losses as a result of the increased ac resistance. However, a high switching frequency can in some cases provide soft-switching that can compensate for the drawbacks of the increased frequency. Therefore, changing the switching frequency as a function of operating conditions makes sense in cases where the traditional zero-voltage-sequence-based modulation cannot be used to extend the soft-switching region. Altering the switching frequency can be particularly useful in applications where the turn-on losses are dominating over the conduction and turn-off losses. In some cases, the increased switching frequency can also be justified by the side benefits of the soft-switching such as reduced EMI radiation and reduced peak currents.

If we assume that the turn-on losses are dominating over the turn-off losses and all the other losses are considered negligible, it can be argued that the optimal switching frequency would be the lowest switching frequency that provides soft-switching in that specific operating point. This minimum switching frequency can be found by setting the current of the switching instance to the minimum value needed for the zero-voltage switching.

By looking at the power (1) and the idealized operating waveforms in Fig. 3, we can see that the transformer current can be set to a desired value by controlling the switching frequency and the phase shift. By choosing this current value (I_{zvs}) large enough, a ZVS can be achieved. Correspondingly, by setting this current to zero, a ZCS can be achieved.

For the derivation of the VFM algorithm, an equation for the switching current (I_{zvs}) and the phase shift (ϕ) is needed. By using simple algebra and the idealized operational model (see Fig. 2), the equation for the turn-off current can be written as

$$I_{\mathrm{zvs}} = \begin{cases} \dfrac{(4\,|\phi| - 1)\,V_2 + V_1}{4 f_{\mathrm{sw}} L_{\mathrm{lk}}} & |V_1 \le V_2 \\ \dfrac{(4\,|\phi| - 1)\,V_1 + V_2}{4 f_{\mathrm{sw}} L_{\mathrm{lk}}} & |V_1 > V_2\ . \end{cases} \tag{8}$$

By selecting the primary-side input current (I_{in}) as the control variable, the relation between the phase shift and the current reference (I_{ref}) can be derived from (4) as

$$\phi = \mathrm{sign}\,(I_{\mathrm{ref}}) \left(\frac{1}{4} \pm \frac{1}{4} \sqrt{1 - \mathrm{sign}\,(I_{\mathrm{ref}})\, \frac{8 f_{\mathrm{sw}} L_{\mathrm{lk}} I_{\mathrm{ref}} / h_{\mathrm{pri}}}{V_2}} \right). \tag{9}$$

By solving (8) and (9) simultaneously, the algorithm for the VFM can be written as

$$\begin{cases} \phi = \dfrac{1}{4\gamma}\left(\gamma - I_{\mathrm{ref}}\alpha + \mathrm{sign}\left(I_{\mathrm{ref}}\right)\sqrt{\alpha^2 I_{\mathrm{ref}}^2 - 2I_{\mathrm{ref}}\gamma\beta + \gamma^2}\right) \\ f_{\mathrm{sw}} = \dfrac{h_{\mathrm{pri}}V_2}{I_{\mathrm{ref}}L_{\mathrm{lk}}}\phi\left(1 - 2\left|\phi\right|\right) \end{cases} \tag{10}$$

where

$$\alpha = \begin{cases} 1 & |V_1 < V_2 \\ \frac{V_1}{V_2} & |V_1 > V_2 \end{cases} \tag{11}$$

$$\beta = \begin{cases} \frac{V_1}{V_2} & |V_1 < V_2 \\ 1 & |V_1 > V_2 \end{cases} \tag{12}$$

and

$$\gamma = \mathrm{sign}(\mathrm{I_{ref}})I_{\mathrm{ZVS}}h_{\mathrm{pri}}. \tag{13}$$

This algorithm ensures switching of the low-voltage-side switches at an arbitrary current value (I_{zvs}). In this context, the low-voltage side refers to the side having the lowest value of the equivalent primary and secondary voltages (V_1 and V_2). If we assume similar semiconductor devices for both bridges, the high-voltage side is automatically zero-voltage switched if the low-voltage side is zero-voltage switched.

VI. Limitations of the VFM

The proposed variable frequency modulation ensures switching at a predefined current value and thereby ZVS virtually over the whole region. By selecting the value of the switching current and dead time appropriately, the excess circulating current can be limited. However, when the equivalent primary and secondary voltages deviate considerably from each other, the proposed algorithm gives very high switching frequencies. Correspondingly, a very low switching frequency is obtained when these voltages are close to each other. Because of the hardware limitations, the switching frequency has to be limited to remain within certain predefined limits.

Limiting the switching frequency to a certain minimum value will not affect the zero-voltage switching. This is true because the switching frequency proposed by the algorithm ensures the selected I_{zvs} current. If a frequency below its minimum value is obtained, the minimum frequency will be used. This leads to switching at a higher current value than the selected I_{zvs}. Therefore, the ZVS is achieved but the circulating current is increased.

Limiting the maximum switching frequency will result in the loss of zero-voltage switching. However, the maximum switching frequency limit can often be set so high that it is achieved only in very special occasions (a very low power or a large difference in the equivalent voltages).

The effect of frequency limitation is illustrated in Fig. 7. A schematic diagram of the implementation is presented in Fig. 8. Fig. 7 shows that the region of the minimum switching frequency is large when the reference current is high compared with the required I_{zvs} and small when the reference current is low in comparison. It can also be seen that the switching frequency pt

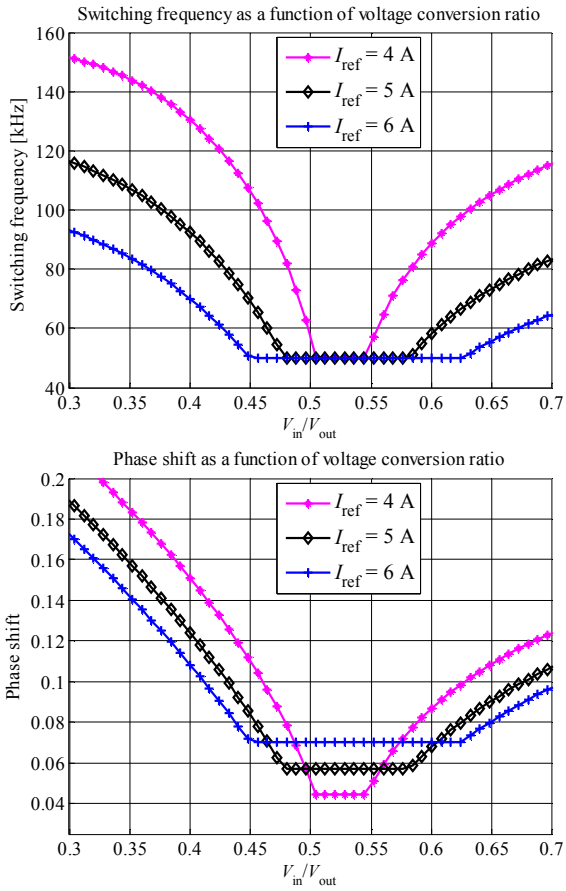

Fig. 7. Switching frequency and phase shift given by the modulation algorithm. In this example, a full-bridge primary, half-bridge secondary converter with a 1:1 transformer is used. The leakage inductance is 26.4 μH and the switching current I_{zvs} is set to 3.5 A.

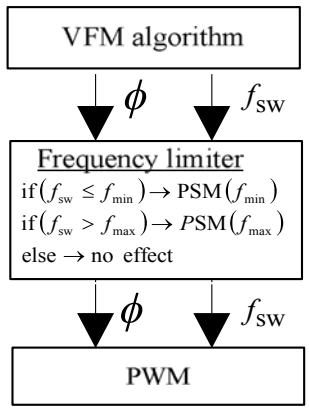

Fig. 8. Switching frequency limitation scheme. When the minimum or maximum frequency level is reached, the traditional PSM is used to continue the operation. The switching frequency limitation is used to prevent extremely high or low frequency values that could damage the hardware.

is related to the transferred power. For a high power, a low switching frequency can be used, but for a low power, a high frequency is needed.

VII. Feedback Control and Compensation of the Phase Drift

In the derivation of the proposed VFM scheme, an ideal converter was assumed. However, an ideal converter does not exist in reality. Instead, nonidealities in the system will cause an error between the actual system and the power flow (1). The VFM algorithm is derived by taking the same assumption of an ideal converter as in the power flow equation. Therefore, the nonidealities will affect this algorithm also.

In most cases, the voltage and current measurement errors are very small and they do not have a significant effect on the actual algorithm. Further, the leakage inductance ($L_{\rm lk}$), the turns ratio (n), and the switching frequency ($f_{\rm sw}$) are usually well known. Relying on the previous reasoning, it can be stated that the main part of the modeling error of the power flow (1) has to originate from the phase shift (ϕ).

The phase-shift-related error is reported in several publications [14], [19], and it is typically referred to as the phase drift phenomenon. In the previous publications, the phase drift is explained by the effects of the dead time and the power losses of the converter. According to our simulations and measurements, the phase drift is mainly caused by the switching delays of the primary and secondary bridges. Based on our measurements, this is true when the dead time is chosen to match the actual zero-voltage transition time, the converter is zero-voltage switched, and the converter losses are low. In the case of hard-switching and a poorly chosen dead time, the phase drift may behave differently. Owing to the limitations of this paper, the latter case is omitted, and it will be discussed in future publications.

The switching delay of a phase leg is related to the capacitances of the power switches and to the switching current. These capacitances are nonlinear functions of the drain-source voltage [20]. Therefore, the phase drift is severest when the difference between the equivalent primary and the secondary voltage is high, and when the switching currents on the primary and secondary sides deviate considerably from each other. When the equivalent voltages and the switching currents are similar, the phase drift is nearly zero. The magnitude of the phase drift can be estimated by calculating the difference of the switching delays

$$t_{\rm drift} = \frac{Q_{\rm pri}\left(V_{\rm ds}\right)}{I_{{\rm sw},pri}} - \frac{Q_{\rm sec}\left(V_{\rm ds}\right)}{I_{\rm sw,sec}}. \tag{14}$$

The effect of the phase drift phenomenon is demonstrated in Fig. 9.

The phase drift problem is severe for converters that are operated outside the nominal operating point with high-capacitance switches, nonsymmetric bridge configurations (full-bridge primary, half-bridge secondary, or *vice versa*) and a high voltage conversion ratio. In modern wide band-gap devices (SiC and GaN), the parasitic capacitance is usually so small that the phase drift may not cause similar problems as with the Si devices. The phase drift phenomenon in the case of hard-switching is not covered in this paper because of its minor effect on the proposed modulation scheme. The phase drift caused by power losses is also omitted in this context as it has only a minor effect on this modulation scheme.

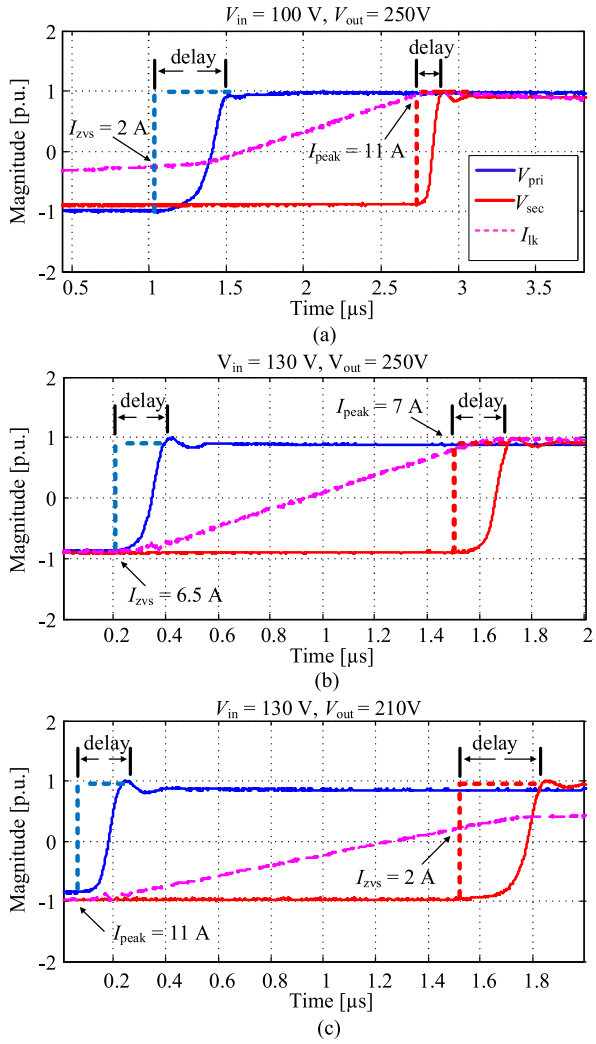

Fig. 9. Measured phase drifts for a DAB converter with a full-bridge primary, half-bridge secondary, and a transformer with a 1:1 turns ratio. For the measurements, STWA88N65M5 MOSFETs were used. (a) Primary-side voltage is smaller than the secondary-side voltage referred to the primary side. The higher voltage and the higher discharging current on the secondary side result in a smaller phase drift on the secondary side. (b) Primary-side voltage is similar to the secondary-side voltage referred to the primary side. The discharging currents are also similar, which results in similar phase drifts on both sides. (c) Secondary-side voltage referred to the primary side is lower than the primary-side voltage. The higher voltage and the higher discharging current on the primary side result in a smaller phase drift on the primary side.

The error caused by the phase drift phenomenon can lead to a failure of the power equation and the VFM algorithm. The phase drift phenomenon can cause severe problems when the modulation algorithm is used in series with the current controller. The current controller will force the error term to zero, which leads to a very different phase shift than is given by the traditional power flow equation. With the VFM algorithm this causes the switching current to drift from its set point ($I_{\rm zvs}$). The phase drift phenomenon can be avoided by using the VFM algorithm as a feedforward term and by compensating the phase drift with a feedback control as shown in Fig. 10.

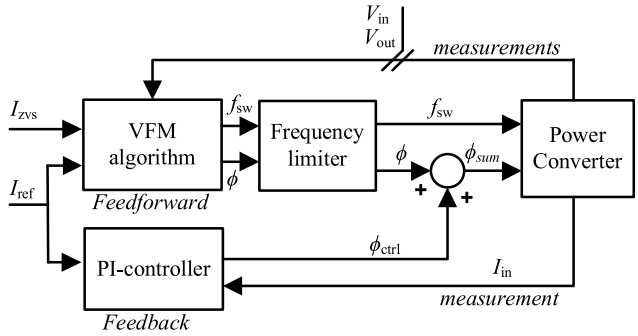

Fig. 10. Phase drift compensation scheme. The VFM algorithm is used as a feedforward, and the phase drift error is compensated by using a feedback controller. The measured voltages ($V_{\rm in}$, $V_{\rm out}$) and current ($I_{\rm in}$) are average values over the switching period. $I_{\rm ref}$ is the desired input current of the converter and $I_{\rm zvs}$ is the desired current value at the switching instant.

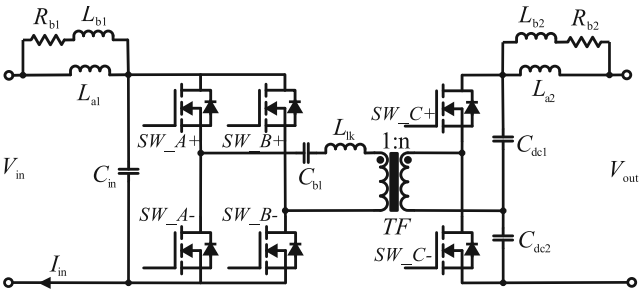

Fig. 11. Schematic diagram of the DAB prototype. Full-bridge on the primary side and half-bridge on the secondary side.

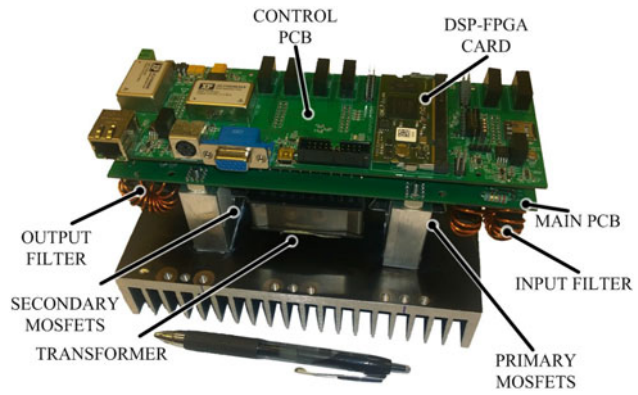

Fig. 12. DAB laboratory prototype. The prototype consists of two printed circuit boards. The bottom one is the main PCB carrying the load current, and the upper one is a control PCB containing the digital signal processor and the measurement electronics. These two PCBs are stacked together by pin headers and mounted on a heat sink.

VIII. Experimental Results

In order to verify the feasibility of the proposed modulation algorithm, a 1-kW prototype was built. The prototype is a variant of the traditional DAB converter with a full-bridge primary and a half-bridge secondary as shown in Fig. 11. The prototype was built on a printed circuit board by using STWA88N65M5 MOSFETs and ADUM3224 gate drivers as shown in Fig. 12. A list of the components and their values is given in Table I.

TABLE I
Component Values for the DAB Prototype

Symbol	Quantity	Value
SW	Power MOSFETs	6 × STWA88N65M5
TF	Transformer	ETD54 N87
n	Turns ratio	1
n1	Primary winding	25 turns 1050 × AWG44 litz
n2	Secondary winding	25 turns 420 × AWG46 litz
$L_{\rm lk}$	Leakage inductance	26.4 μH (internal)
$C_{\rm in}$	Input capacitor	28 × 1 μF/450V ceramic cap.
$C_{\rm dc1}$	Voltage doubler capacitor	14 × 1 μF/450V ceramic cap.
$C_{\rm dc2}$	Voltage doubler capacitor	14 × 1 μF/450V ceramic cap.
$C_{\rm b1}$	Dc-blocking capacitor	10 × 10 μF/25V ceramic cap.
$L_{\rm a1}$	Input choke	63 μH, KoolMu 77930/125μ
$L_{\rm b1}$	Input filter damping choke	31 μH, KoolMu 77930/125μ
$R_{\rm b1}$	Input filter damping resistor	2.2 Ω
$L_{\rm a2}$	Output choke	63 μH, KoolMu 77930/125μ
$L_{\rm b2}$	Output filter damping choke	31 μH, KoolMu 77930/125μ
$R_{\rm b2}$	Output filter damping resistor	2.2 Ω

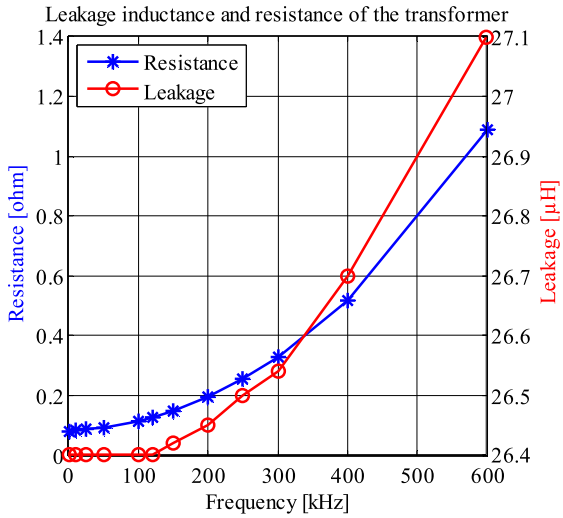

Fig. 13. Leakage inductance and resistance of the transformer as a function of frequency. The measurements are carried out on the primary side with a shorted secondary winding.

The leakage inductance was integrated into the transformer. The transformer was wound on an ETD54 core by using litz wire. The behavior of the leakage inductance and resistance of the transformer is presented in Fig. 13. The winding configuration and the leakage inductance value were not rigorously optimized for the application.

The effectiveness of the proposed modulation method was demonstrated by a set of measurements at various input to output voltage ratios ($V_{\rm in}/V_{\rm out}$ from 0.3 to 0.7) with a fixed dead time of 200 ns. An efficiency comparison of the traditional PSM and the VFM is presented in Figs. 14 and 16. Fig. 14 shows a significant efficiency improvement over the traditional PSM while Fig. 15 shows the efficiency improvement in different load conditions. Fig. 16 illustrates how the VFM scheme forces the switching current to a fixed value by increasing the switching frequency, while the PSM scheme uses a fixed switching frequency that leads to hard switching when operated far outside the nominal voltage conversion ratio.

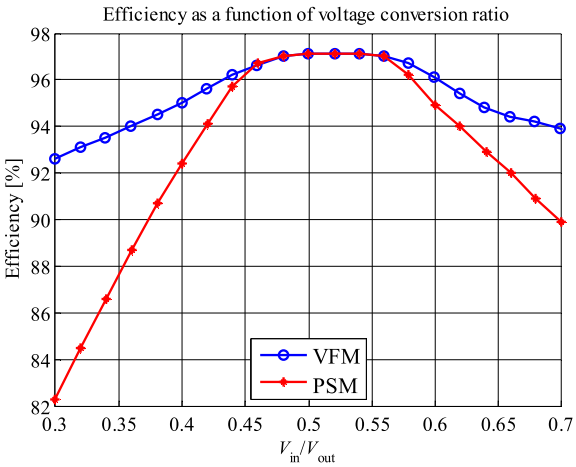

Fig. 14. Measured efficiency for the traditional PSM and for the proposed VFM scheme. During the measurements, the secondary voltage was kept constant at 250 V and the switching current (I_{zvs}) at 3.5 A, and the primary-side current (I_{in}) was controlled to 5 A by using a feedback control to compensate for the phase drift. The VFM algorithm is dynamically seeking the minimum switching frequency that ensures zero-voltage switching. Therefore, it can provide a better efficiency over the operating range than the traditional PSM modulation with a fixed switching frequency.

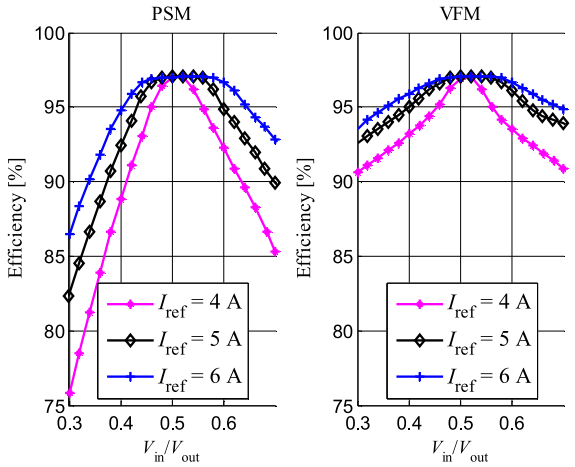

Fig. 15. Measured efficiency curves for the traditional PSM and the VFM at different input current levels (I_{ref}). Efficiencies measured at a 250-V secondary-side voltage and with a fixed 200-ns dead time. For the VFM, a fixed 3.5-A switching current (I_{zvs}) was used.

The loss distributions in various load conditions and voltage conversion ratios are given in Tables II–V. From Tables II–V, it can be seen that the VFM scheme reduces the switching losses as well as the conduction and core losses. However, the auxiliary power consumption is slightly increased due to the increased gate driving power. Despite the significant 50%–65% decrease in the switching losses shown in Tables II–V, the switching losses are higher than would be expected in the case of a complete zero-voltage switching. Thus, we may conclude that the fixed dead time length was not long enough to allow a complete discharge of the output capacitances. Better results could probably be achieved by using a longer dead time or adjusting its value dynamically. The effect of the chosen switching current value

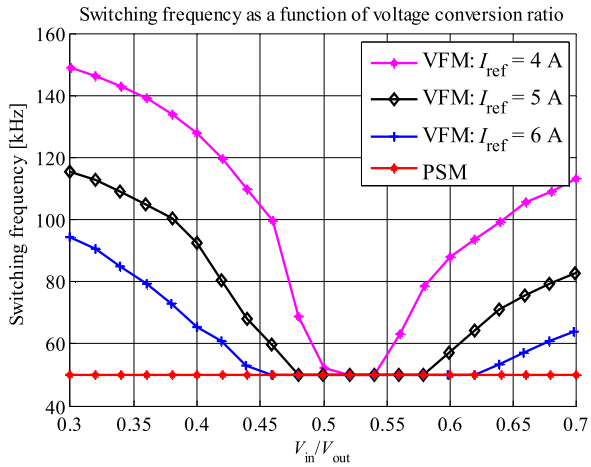

Fig. 16. Switching frequency as a function of voltage conversion ratio for various input current reference values. The switching frequency was measured from the gate transformer primary-side voltage. The effect of the phase drift and slight parameter inaccuracies lead to a slight difference in the frequencies compared with Fig. 7. The measurements were carried out with a fixed switching current of 3.5 A while the secondary voltage was kept constant at 250 V.

TABLE II
LOSS BREAKDOWN AT A VOLTAGE CONVERSION RATIO OF 0.3 AND INPUT CURRENT OF 4 A (VFM F_{sw} = 141 kHz, I_{zvs} = 3.0 A)

Loss type	Loss with PSM [W]	Loss with VFM [W]
Transformer winding	3.3	2.8
Transformer core	0.4	0.1
Input filter winding	1.3	1.4
Output filter winding	0.1	0.1
Primary conduction	2.4	1.1
Secondary conduction	0.9	0.5
Primary switching	59.4	21.2
Secondary switching	0.3	0.2
Control and gate drive	5.9	7.8

TABLE III
LOSS BREAKDOWN AT A VOLTAGE CONVERSION RATIO OF 0.7 AND INPUT CURRENT OF 4 A (VFM F_{sw} = 126 kHz, I_{zvs} = 4 A)

Loss type	Loss with PSM [W]	Loss with VFM [W]
Transformer winding	4.6	5.6
Transformer core	2.3	0.6
Input filter winding	1.3	1.4
Output filter winding	0.4	0.6
Primary conduction	2.6	2.1
Secondary conduction	1.6	1.1
Primary switching	0.5	0.1
Secondary switching	77.7	35.2
Control and gate drive	5.9	7.5

(I_{zvs}) on the efficiency is demonstrated in Fig. 17. For optimal efficiency, the switching current value (I_{zvs}) or the dead time should be adjusted dynamically for different voltage conversion ratios. However, this improvement is beyond the scope of this paper and is thus omitted.

The effect of the variable switching frequency modulation on the switching waveforms and the transformer current stress

TABLE IV
LOSS BREAKDOWN AT A VOLTAGE CONVERSION RATIO OF 0.3 AND INPUT CURRENT OF 6 A (VFM $F_{\mathrm{sw}} = 101$ kHz, $I_{\mathrm{zvs}} = 3.0$ A)

Loss type	Loss with PSM [W]	Loss with VFM [W]
Transformer winding	4.8	4.7
Transformer core	0.4	0.2
Input filter winding	2.9	3.0
Output filter winding	0.2	0.3
Primary conduction	3.0	2.4
Secondary conduction	1.4	1.2
Primary switching	42.5	15.4
Secondary switching	0.6	0.3
Control and gate drive	5.9	7.0

TABLE V
LOSS BREAKDOWN AT A VOLTAGE CONVERSION RATIO OF 0.7 AND INPUT CURRENT OF 6 A (VFM $F_{\mathrm{sw}} = 76$ kHz, $I_{\mathrm{zvs}} = 5$ A)

Loss type	Loss with PSM [W]	Loss with VFM [W]
Transformer winding	7.8	8.6
Transformer core	2.3	1.3
Input filter winding	3.1	3.1
Output filter winding	1.2	1.3
Primary conduction	4.5	4.4
Secondary conduction	2.4	2.2
Primary switching	0.9	0.8
Secondary switching	42.0	17.1
Control and gate drive	5.9	6.4

is demonstrated in Fig. 18. We can see that in addition to the efficiency improvement, the proposed modulation method can reduce voltage and current spikes and lower the peak and RMS current of the transformer.

IX. CONCLUSION AND FUTURE STUDY

In this paper, the use of half-bridge variants of the traditional DAB converter was discussed. The paper introduced a generalized power flow equation covering all the combinations of half-bridge and full-bridge variants of the traditional DAB converter. By using the generalized power equation, a VFM algorithm was derived. The proposed algorithm can be used to ensure ZVS or ZCS over the whole operating range. The effects of the phase drift phenomenon were discussed, and a simple compensation scheme was provided to reduce the effect of the phase drift. Finally, the feasibility of the proposed modulation scheme was demonstrated by a laboratory prototype.

It is emphasized that the proposed phase drift compensation is an essential part of the modulation algorithm. The use of the algorithm without the compensation may lead to a wrong switching current and to an error between the control variable and the reference. By using this algorithm in series with a PI controller, the control error, and consequently, the switching current will drift from its set point. This can lead to undesired hard-switching. It is still unverified whether the presented modulation method can be used without any phase drift compensation when using low-capacitance power switches such as wide band-gap MOSFETs.

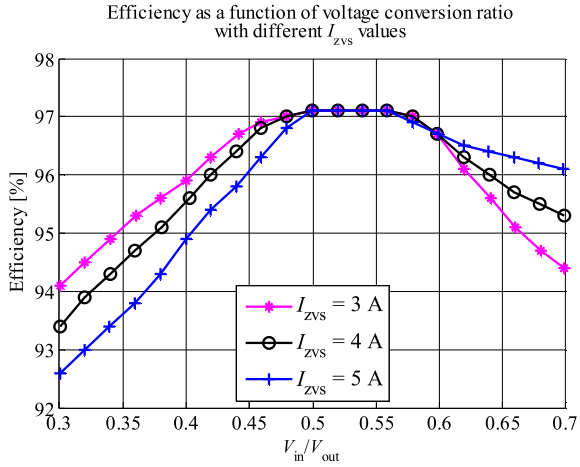

Fig. 17. Measured efficiency for different switching current values. During the measurements, the secondary voltage was kept constant at 250 V, and the primary-side current (I_{in}) was controlled to 6 A by using a feedback control to compensate for the phase drift. The current required for a complete C_{oss} discharge is higher on the secondary side than on the primary side. Therefore, the larger I_{zvs} values improve the efficiency at higher $V_{\mathrm{in}}/V_{\mathrm{out}}$ ratios, while the primary side is already zero voltage switched with smaller I_{zvs} values. If the I_{zvs} reference is larger than the current at which the output capacitances are completely discharged, the increasing switching frequency is only causing additional losses in the converter without bringing any further benefits to the ZVS process.

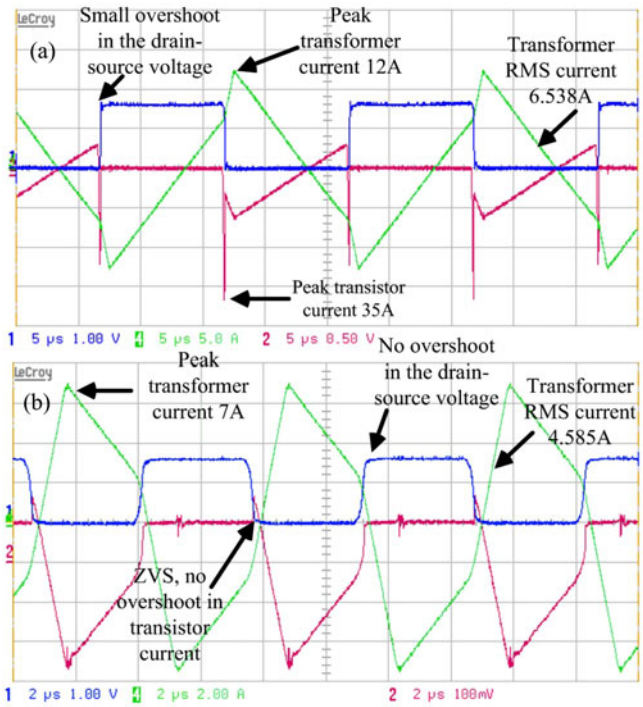

Fig. 18. Measured waveforms for the DAB prototype in the operating point where the primary-side voltage is 80 V and the secondary-side voltage is 250 V. The primary-side current is controlled to match the 4-A reference by using a feedback control to compensate for the phase drift. A fixed dead time of 200 ns is used for both the primary and secondary bridges. (a) Switching waveforms for the fixed-frequency PSM at 50 kHz. (b) Switching waveforms for the VFM at 141 kHz. The measured efficiency for the PSM is 78.5% in this operating point. Correspondingly, the efficiency for the VFM is 91.5%. The VFM also has lower current and voltage peak values and a lower transformer RMS current than the PSM.

Benefits of the proposed modulation scheme:

1) ensures zero-voltage turn-on for all the switches;
2) reduces the EMI by allowing soft-switching in the region where hard-switching would normally be present;
3) removes the excess circulating current from the low-voltage side, which tends to reduce the conduction losses;
4) can reduce the turn-off losses;
5) reduces the current spikes;
6) can reduce the core losses of magnetic components.

Disadvantages of the modulation scheme:

1) increases the switching frequency, which can lead to increased conduction losses as a result of the ac resistance;
2) increases the number of switching events, which can lead to increased losses in some converter designs;
3) increases gate driving losses.

The use of phase drift compensation for zero-sequence-based modulation schemes and the option of combining the VFM with the traditional zero-voltage-sequence-based modulation were not discussed.

REFERENCES

[1] R. T. Naayagi and A. J. Forsyth, "Bidirectional DC-DC converter for aircraft electric energy storage systems," in *Proc. IET Int. Conf. Power Electron., Mach. Drives*, 2010, pp. 1–6.

[2] Q. Hengsi and J. W. Kimball, "Solid-state transformer architecture using AC–AC dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3720–3730, Sep. 2013.

[3] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.

[4] H. Chung, S. R. Hui, and K. K. Tse, "Reduction of power converter EMI emission using soft-switching technique," *IEEE Trans. Electromagn. Compat.*, vol. 40, no. 3, pp. 282–287, Aug. 1998.

[5] F. Krismer, S. Round, and J. W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," in *Proc. IEEE Power Electron. Spec. Conf.*, 2006, pp. 1–7.

[6] B. Hua and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC–DC converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.

[7] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC–DC converter based on dual-phase-shift control for DC distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.

[8] F. Krismer and J. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[9] H. Zhou and A. M. Khambadkone, "Hybrid modulation for dual-active-bridge bidirectional converter with extended power range for ultracapacitor application," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1434–1442, Jul./Aug. 2009.

[10] Y. Wang, S. de Haan, and J. Ferreira, "Optimal operating ranges of three modulation method in dual active bridge converters," in *Proc. IEEE 6th Int. Power Electron. Motion Control Conf.*, 2009, pp. 1397–1401.

[11] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. Kolar, "Optimal ZVS modulation of single-phase single-stage bidirectional DAB AC–DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3954–3970, Aug. 2014.

[12] G. Guidi, M. Pavlovsky, A. Kawamura, T. Imakubo, and Y. Sasaki, "Improvement of light load efficiency of dual active bridge DC–DC converter by using dual leakage transformer and variable frequency," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 830–837.

[13] X. He, Z. Zhang, Y. Cai, and Y. Liu, "A variable switching frequency hybrid control for ZVS dual active bridge converters to achieve high efficiency in wide load range," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1095–1099.

[14] X. Yanhui, J. Sun, and J. Freudenberg, "Power flow characterization of a bidirectional galvanically isolated high-power DC/DC converter over a wide operating range," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 54–66, Jan. 2010.

[15] M. N. Kheraluwala, R. W. Gascoigne, and D. M. Divan, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.

[16] V. Väisänen, T. Riipinen, and P. Silventoinen, "Effects of switching asymmetry on an isolated full-bridge boost converter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2033–2044, Aug. 2010.

[17] H. Sangtaek, I. Munuswamy, and D. Divan, "Preventing transformer saturation in bi-directional dual active bridge buck-boost DC/DC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 1450–1457.

[18] K. Vangen, T. Melaa, and A. K. Adnanes, "Soft-switched high-frequency, high power DC/AC converter with IGBT," in *Proc. IEEE Power Electron. Spec. Conf.*, 1992, pp. 26–33.

[19] S. Inoue and H. Akagi, "A bidirectional dc-dc converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, Nov. 2007.

[20] J. Sabate, R. Farrington, M. Jovanovic, and E. Lee, "Effect of FET output capacitance on ZVS of resonant converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 32, no. 1, pp. 255–266, Jan. 1996.

Jani Hiltunen (M'10) received the M.Sc. degree in electrical engineering from the Lappeenranta University of Technology, Lappeenranta, Finland, in 2011, where he is currently working toward the D.Sc. (Technology) degree.

His current research interests include power converters and their control.

Vesa Väisänen (M'10) received the M.Sc. degree in electrical engineering and the D.Sc. (Technology) degree from the Lappeenranta University of Technology (LUT), Lappeenranta, Finland, in 2005 and 2012, respectively.

He is currently a Postdoctoral Researcher with LUT and his current research interests include power converters, magnetic components and system integration.

Raimo Juntunen (M'10) received the M.Sc. degree in electrical engineering from the Lappeenranta University of Technology, Lappeenranta, Finland, in 2011.

Since 2011, he has worked at the Laboratory of Applied Electronics, Lappeenranta University of Technology. He is working on a dissertation on the control of high-power grid-connected inverters. His research interests include filtering in parallel-connected grid inverter systems.

Pertti Silventoinen (M'11) received the D.Sc. (Technology) degree from the Lappeenranta University of Technology (LUT), Lappeenranta, Finland, in 2001.

He became a Professor of applied electronics in 2004. He is currently the Head of the Degree Program in Electrical Engineering, LUT. His current research interests include power electronics systems in various applications.