# Steep-Gain Bidirectional Converter With a Regenerative Snubber

Jia Yao, *Student Member, IEEE*, Alexander Abramovitz, *Member, IEEE*, and Keyue Ma Smedley, *Fellow, IEEE*

***Abstract*—This paper introduces a SEPIC-derived bidirectional dc–dc converter. The proposed converter utilizes tapped inductor and charge pump techniques to achieve steep voltage conversion ratio and an active lossless regenerative snubber to attain lossless switching and high efficiency. The paper presents the principle of operation, steady-state analyses, and experimental results obtained from a 400-W, 48-V/380-V prototype. The efficiency of the proposed topology is demonstrated to peak at 96.4% for boost mode and 95.0% for buck mode.**

***Index Terms*—Bidirectional dc–dc converter, high conversion ratio, regenerative snubber, tapped inductor (TI).**

## I. Introduction

UNINTERRUPTABLE power supplies (UPSs) [1], renewable energy applications [2], and clean-energy vehicles [3] often require bidirectional dc–dc converters as a buffer stage between the high dc voltage source/storage/load and a low-voltage energy storage battery or supercapacitor banks. It is quite common that the low dc-side source VL of the bidirectional converter is in the 12–48 V range, whereas the high dc-side voltage VH in grid-tied applications and electrical vehicle applications ranges from 100 to 400 V [1]–[3]. Consequently, the voltage conversion ratio of the bidirectional converter of about tenfold is needed.

The simplest bidirectional converter is the buck–boost topology. With only two active switches the two quadrant buck–boost presents a cost-effective solution. However, in practice, the buck–boost converter can attain only a limited conversion ratio as operation at extreme duty cycle severely impairs the efficiency and imposes high voltage stress upon the switches. Transformer-isolated full-bridge [4], [5] topologies take advantage of transformer's turns ratio to attain steep voltage step up/down. Such converters may require eight or more active switches. In order to alleviate the voltage stress caused by the leakage inductances of the transformer, clamp circuits with active flyback regeneration have been utilized [6], [7]. However, such circuits further increase the cost and control complexity. Lower component count can be attained employing the half-bridge topologies [8], [9]. However, for achieving soft-switching performance, more complex and subtle control has been employed. For example, zero-voltage switching (ZVS) performance of the half bridge under pulsewidth modulation (PWM) and phase shift control strategy was demonstrated in [10] and in more complex power stage in [11]. The current-fed half bridge [12] used two extra switches to achieve active regenerative clamp to limit the switch voltage and recycle the leakage energy.

Recently, switched capacitor dc–dc converters [13], [14] have been demonstrated as an alternative for providing bidirectional power flow while attaining lossless switching. Similarly, by using switched capacitor cells, multilevel bidirectional converters have been proposed in [15]–[17]. This method typically leads to increased switch count and their associated drive circuits.

Tapped inductor (TI) based topologies can extend the voltage conversion range by adjusting the TI turns ratio while having a moderate component count. One of the simplest TI-based two-switch bidirectional dc–dc converter can be derived from the boost/buck topology [18]. However, the leakage inductance of the TI causes high voltage spike during switching. A modification of this topology with voltage multipliers was introduced in [19] and has achieved soft-switching performance using four switches. Recently, additional bidirectional TI-based converters were reported. A bidirectional converter with a resonant voltage multiplier [20] achieved steep gain and soft switching. A TI-based SEPIC [21] employed triple winding inductor to realize zero current ripple. However, with the third winding connected to the output, the voltage gain is decreased. TI-based double boost with clamping of the leakage inductance was reported in [22], which only needs three switches but with much lower gain than a TI-based type. Single-switch bidirectional active snubber with an additional inductor for bidirectional converters can be found in [23], which used subtle control of the snubber switches. A two-inductor version was suggested in [24]. To recycle the leakage energy, the boost–flyback topology [25] relied on clamping action of voltage doubler. Better efficiency and higher gain were demonstrated by a five-switch bidirectional step-up/down converter with three voltage multiplier cells [26].

In this study, a bidirectional TI charge pump enhanced SEPIC converter (BTCS) is introduced. Application of a TI and a charge pump provide the converter with a steeper gain than that of the earlier counterpart [21]. A simple active regenerative snubber built of a single extra switch and a snubber capacitor has been employed. The leakage inductance is beneficially exploited as a part of the snubber circuit and helps achieving zero-current switching (ZCS) and zero-voltage switching (ZVS) conditions. The proposed control strategy requires single switching signal in the boost mode and a complementary pair of switching signals

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J. Yao is with the Electrical Engineering Department, Southeast University, Nanjing 210096, China. During 2012-14, she was with the Electrical Engineering Department, University of California, Irvine, CA 92617 USA. (e-mail: seu.yaojia@gmail.com).

A. Abramovitz and K. Ma Smedley are with the Electrical Engineering Department, University of California, Irvine, CA 92617 USA (e-mail: alabr@hotmail.com; smedley@uci.edu).

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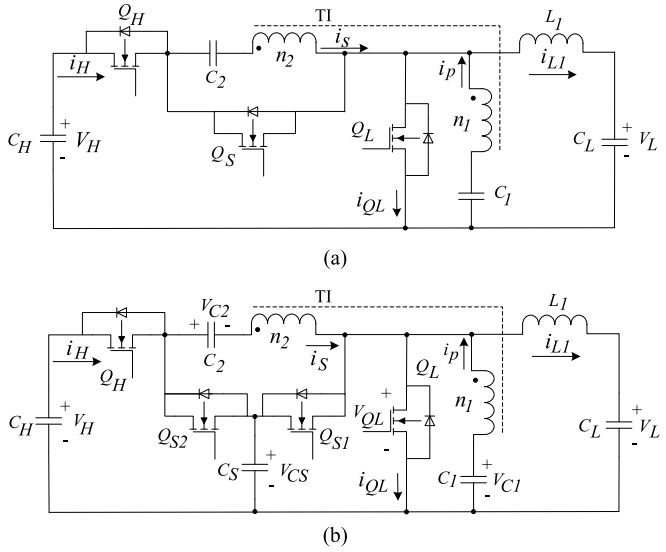


Fig. 1. Proposed topology: (a) basic configuration of the proposed BTCS converter; (b) practical implementation of the proposed BTCS topology with a regenerative snubber.

in the buck mode, and compared to earlier counterparts (see [19] and [25]), it is relatively simple. An additional advantage of BTCS topology is the filtered current on the low side. This potentially benefits the low-side dc source.

This paper is organized as follows. The proposed BTCS topology is presented in Section II; operating principles of the proposed topology are presented in Section III; steady-state operational analysis and stress analysis are given in Sections IV and V, respectively; and the experimental results of a 400-W, 48- to 380-V prototype with 50 kHz switching frequency are shown in Section VI. Some auxiliary issues are discussed in the Appendix; and finally, the conclusion is presented.

## II. Proposed Topology

The conceptual topology of the proposed BTCS converter is shown in Fig. 1(a). The proposed topology was derived from the SEPIC converter, and thanks to the series input inductor $L_1$ inherits SEPIC merit of continuous input current with limited ripple component. The TI and a charge pump $C_2$ modify the converter's gain both for the step-up and step-down modes. However, to attain higher efficiency, the circuit in Fig. 1(a) has to be further modified. Introduction of an active regenerating snubber, as shown in Fig. 1(b), allows capturing and recycling the leakage energy.

The proposed BTCS converter in Fig. 1(b) comprises four power switches $Q_L$, $Q_H$, $Q_{S_1}$, and $Q_{S_2}$, including their antiparallel diodes; a TI; a low-side inductor $L_1$; a low-side filter capacitor $C_L$; a high-side filter capacitor $C_H$; blocking capacitor $C_1$; a charge pump capacitor $C_2$; and a snubber capacitor $C_S$. The low-side voltage and high-side voltages are designated as $V_L$ and $V_H$, respectively.

The parameters of the TI are the primary referred magnetizing inductance $L_m$ and the primary and the secondary leakage inductances $L_{1k}$ and $L_{2k}$, respectively. The leakage inductances

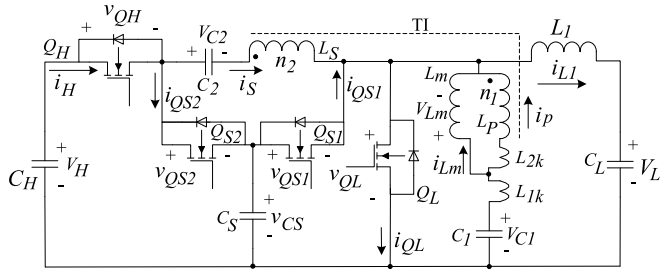

Fig. 2. Equivalent circuit of the proposed BTCS converter.

of the TI are exploited as a part of the snubber circuit. The TI's turns ratio *n* is defined as

$$n = \frac{N_2}{N_1}. \tag{1}$$

Here, $N_1$ and $N_2$ are the primary and the secondary number of turns, respectively.

## III. Principle of Operation

A schematic diagram of the proposed BTCS converter with the TI model is shown in Fig. 2. The analysis to follow relies on several simplifying assumptions:

1) the circuit components are assumed to be ideal, that is, the ON-state resistance of the main switch and of all the diodes, as well as their forward voltage drop and parasitic capacitances, is neglected;
2) the capacitors $C_L$, $C_H$, $C_1$, and $C_2$ are considered sufficiently large and their respective voltages $V_L$, $V_H$, $V_{C_1}$, and $V_{C_2}$ are assumed constant;
3) the inductor $L_1$ and the magnetizing inductance of the TI $L_m$ are considered large; however, their current ripple will be taken into consideration;
4) the dead time between the gating signals is neglected.

### A. BTCS Operation in the Buck Mode

During the buck mode (step down from $V_H$ to $V_L$), the controller gates the high switch $Q_H$ with the desired duty cycle, whereas $Q_{S_1}$ and $Q_{S_2}$ are switched complementarily to $Q_H$. $Q_L$ is constantly off. However, its antiparallel diode is used as a passive switch.

Key waveforms of the proposed BTCS converter in the buck mode are shown in Fig. 3. Examination of the waveforms reveals that the switching cycle consists of five topological states, which equivalent circuits are illustrated in Fig. 4. Description follows in the next section.

*1) State 1 [$t_0$–$t_1$]:* Equivalent circuit of this state is shown in Fig. 4(a). Here, $Q_H$ is switched on at $t = t_0$ while $Q_{S_1}$ and $Q_{S_2}$ are turned off. The body diode of the switch $Q_{S_2}$ is kept at cutoff by the negative voltage difference across it. Meanwhile, the body diode of $Q_{S_1}$, $D_{S_1}$ conducts and allows the snubber capacitor, $C_s$, and the leakage inductance of the TI to resonate for about half a resonant cycle. As a result, the voltage $V_{Cs}$ across $C_s$ increases. State 1 is terminated when the body diode, $D_{S_1}$, turns off at zero current, (see Fig. 3). Note that the smooth voltage rise

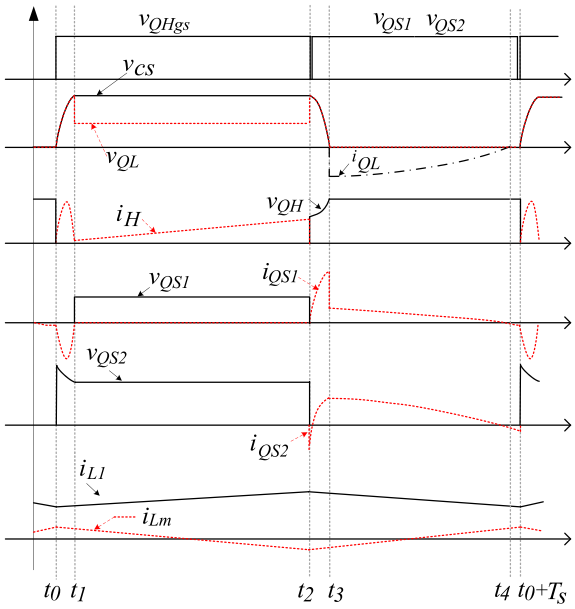


Fig. 3. Key waveforms of the BTCS converter in buck mode.

of $v_{Q_L}$, dictated by $C_S$, assures ZVS turn OFF of $Q_L$, whereas the sinusoidal current pulse in $i_H$ creates ZCS of the switch $Q_H$.

*2) State 2 [$t_1$–$t_2$]:* Equivalent circuit of this state is shown in Fig. 4(b). Neglecting the voltage ripple of $C_1$ and $C_2$, the voltage across $L_m$ and $L_1$ is approximately constant and, therefore, the currents $i_{L_m}$ and $i_{L_1}$ are approximately linear (see Fig. 3). The charge pump capacitor $C_2$ is charged by the current from the high dc-side source, while the blocking capacitor $C_1$ is discharged due to the self-transformer action of the TI. State 2 is terminated by the controller turning off the $Q_H$ switch.

*3) State 3 [$t_2$–$t_3$]:* When the switch $Q_H$ is turned off at $t = t_2$, the $Q_{S_1}$ and $Q_{S_2}$ switches are turned ON. This allows the leakage inductance of the TI and snubber capacitor $C_S$ start resonating discharging $C_S$ [see Fig. 4(c)]. State 3 ends when $v_{C_s}$ reaches zero (see Fig. 3). At this instant, the energy captured by $C_S$ during State 1 is fully regenerated and transferred to capacitor $C_2$ and the TI.

*4) State 4 [$t_3$–$t_4$]:* When $v_{C_s}$ reaches zero, the body diode of the switch $Q_L$, i.e., $D_{Q_L}$ starts conducting under zero-voltage (ZV) condition and freewheels the magnetizing current $i_{L_m}$, the primary current $i_p$, and the inductor current $i_{L_1}$. During this interval, resonance also occurs between leakage inductances $L_{1k}$ and $L_{2k}$ and capacitors $C_1$ and $C_2$ [see Fig. 4(d)]. The resonant current component through $D_{Q_L}$ $i_{Q_L}$ can be noticed in Fig. 3. State 4 ends either when the switch $Q_H$ is switched on or when $i_{Q_L}$ falls to zero.

*5) State 5 [$t_4$–$t_5$]:* State 5 appears in case $i_{Q_L}$ falls to zero during State 4. The equivalent circuit of State 5 [see Fig. 4(e)] is identical to that of State 3. Here, due to the resonant action, the resonant current component polarity reverses and starts charging the snubber capacitor $C_S$ (see Fig. 3). Yet, the currents $i_{L_1}$, $i_{L_m}$, $i_P$ are nearly linear. State 5 is terminated by the turn ON of the switch $Q_H$, which starts the next switching cycle.

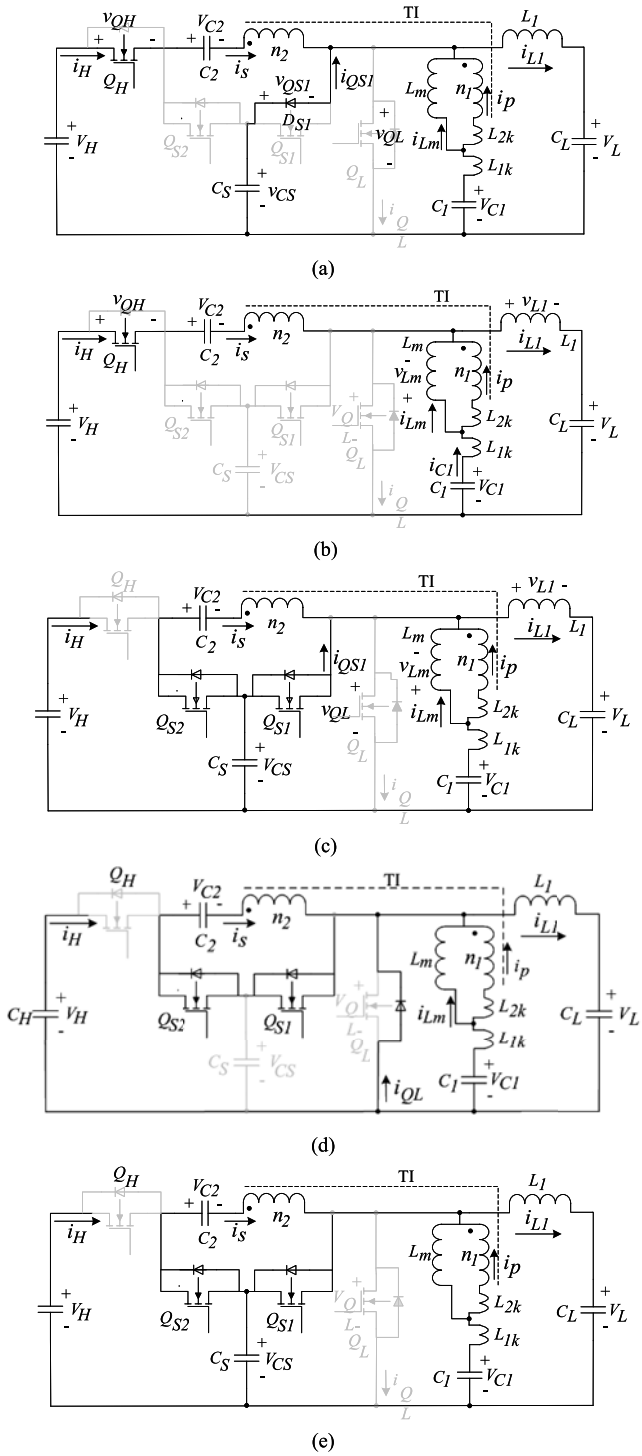


Fig. 4. Topological states of the BTCS converter in buck mode: (a) State 1 [$t_0$–$t_1$]; (b) State 2 [$t_1$–$t_2$]; (c) State 3 [$t_2$–$t_3$]; (d) State 4 [$t_3$–$t_4$]; (e) State 5 [$t_4$–$t_0$].

## *B. BTCS Operation in the Boost Mode*

During the boost mode (step up from $V_L$ to $V_H$), the main switch $Q_L$ is gated by the controller signal with the predetermined duty cycle, while $Q_H$, $Q_{S_1}$, and $Q_{S_2}$ are turned off at all times, with their antiparallel diodes used as naturally

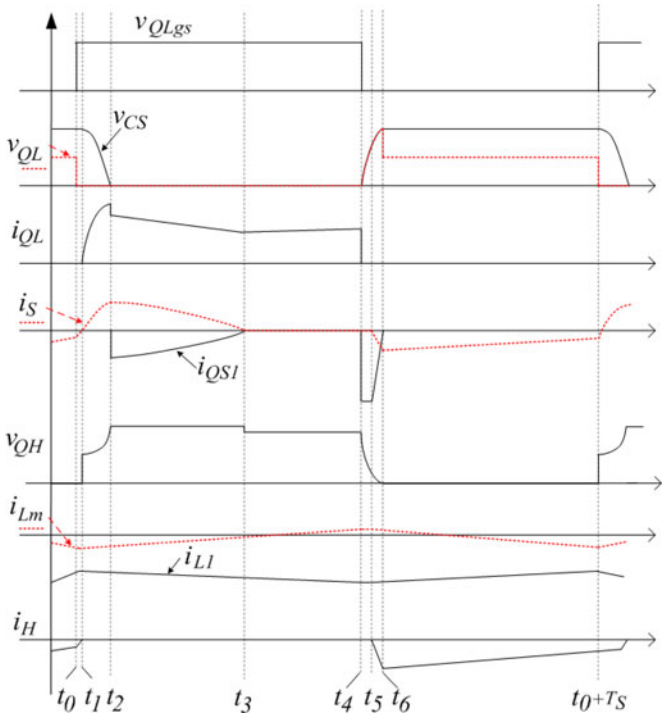


Fig. 5. Key waveforms of the BTCS converter in boost mode.

commutated passive switches. Hence, the snubber operates as a passive regenerative snubber.

The key waveforms of the proposed BTCS converter in the boost mode are shown in Fig. 5. Examination of the waveforms reveals that the switching cycle consists of seven topological states whose equivalent circuits are illustrated in Fig. 6. Description of various states is given in the following sections.

*1) State 1 [$t_0$–$t_1$]:* In this state, see Fig. 6(a), the switch $Q_L$ is turned ON at $t = t_0$ and the switch voltage $v_{Q_L}$ drops. Consequently, the input source voltage $V_L$ is applied across the inductor $L_1$ and the input current, $i_{L_1}$ starts ramping up. In the boost mode, the current polarity of $i_{L_1}$ is negative; hence, during this interval, the waveform of current $i_{L_1}$ in Fig. 5 increases in the negative direction. The secondary leakage inductance keeps discharging the secondary current $i_s$ through $D_{Q_H}$ to the output. State 1 is terminated as the secondary leakage current drops to zero.

*2) State 2 [$t_1$–$t_2$]:* State 2 commences after the secondary current has decayed to zero and the output diode $D_{Q_H}$ has entered the cutoff state [see Fig. 6(b)]. Here, the snubber diode $D_{S_2}$ conducts and allows the snubber capacitor $C_S$ to resonate with the secondary leakage inductance $L_{2k}$ and dump the captured energy mostly into the charge pump capacitor $C_2$. Thus, the secondary current $i_S$ reverses. This state terminates as the snubber capacitor $C_S$ is discharged and the voltage $v_{C_s}$ drops to zero.

*3) State 3 [$t_2$–$t_3$]:* State 3 commences after the snubber diode $D_{S_1}$ starts to conduct and clamps the snubber capacitor $C_S$ to ground [see Fig. 6(c)]. At the end of State 3, at $t = t_3$, the charge pump capacitor $C_2$ is fully charged, the secondary resonant current pulse $i_s$ decays to zero, and, therefore, the diodes $D_{S_1}$ and $D_{S_2}$ are cut off at zero current.

*4) State 4 [$t_3$–$t_4$]:* During State 4, both the input inductor $L_1$ and the magnetizing inductance of the TI $L_m$ keep charging [see Fig. 6(d)]. State 4 lasts until the instant $t = t_4$; here, the controller commands to terminate the on time and turns off the switch $Q_L$.

*5) State 5 [$t_4$–$t_5$]:* State 5 commences at $t = t_4$. After the switch $Q_L$ is turned off [see Fig. 6(e)], the current of the central tap is diverted by the snubber diode $D_{S_1}$ toward the snubber capacitor $C_S$, which moderates the voltage rise across the switch. Since the snubber capacitor voltage is zero at the start of the State 5, true ZVS performance is achieved. The output diode $D_{Q_H}$ cuts in at the instant $t = t_5$, when State 5 is terminated.

*6) State 6 [$t_5$–$t_6$]:* During State 6 [see Fig. 6(f)], the snubber capacitor voltage $v_{C_s}$ keeps rising while the secondary current builds up through the charge pump capacitor $C_2$ and the output diode $D_{Q_H}$. State 6 terminates as the snubber capacitor voltage reaches its peak value and capacitor current falls to zero; at this instant, diode $D_{S_1}$ cuts off.

*7) State 7 [$t_6$–$t_0$]:* During this state, both the input inductance $L_1$ and the magnetizing inductance $L_m$ discharge to the output through the self-transformer action of the TI.

## IV. Steady-State Analysis

The steady-state analysis that follows relies on the assumptions 1)–4) stated earlier. To facilitate the approach the leakage inductances of the TI are neglected. This implies that no leakage energy is discharged into the snubber and also allows neglecting the snubber transients and treating an idealized model of the proposed converter. Later, during the snubber analysis, this assumption will be dropped.

Two useful observations can be made, which hold for both buck and the boost mode. First is regarding the holding capacitor voltage

$$V_{C_1} = V_L. \tag{2}$$

Second, inspection of Fig. 4(d) and Fig. 6 reveals that transformer-like action of the TI allows charging the pump capacitor $C_2$ to approximately

$$V_{C_2} = nV_{C_1}. \tag{3}$$

These relationships are helpful in deriving the desired voltage conversion ratio of the proposed converter.

### A. Boost-Mode Conversion Ratio

In boost mode, the switch $Q_L$ is turned ON for the duration of $D_{\rm bst}T_s$ [see Fig. 6(a)] and the voltage across the magnetizing inductance is

$$V_{L_m} = V_{C_1}. \tag{4}$$

Whereas, during $Q_L$ OFF interval $D'_{\rm bst}T_s$ [see Fig. 6(b)], the voltage of the magnetizing inductance is

$$V'_{L_m} = \frac{1}{n+1}(V_{C_1} + V_{C_2} - V_H). \tag{5}$$

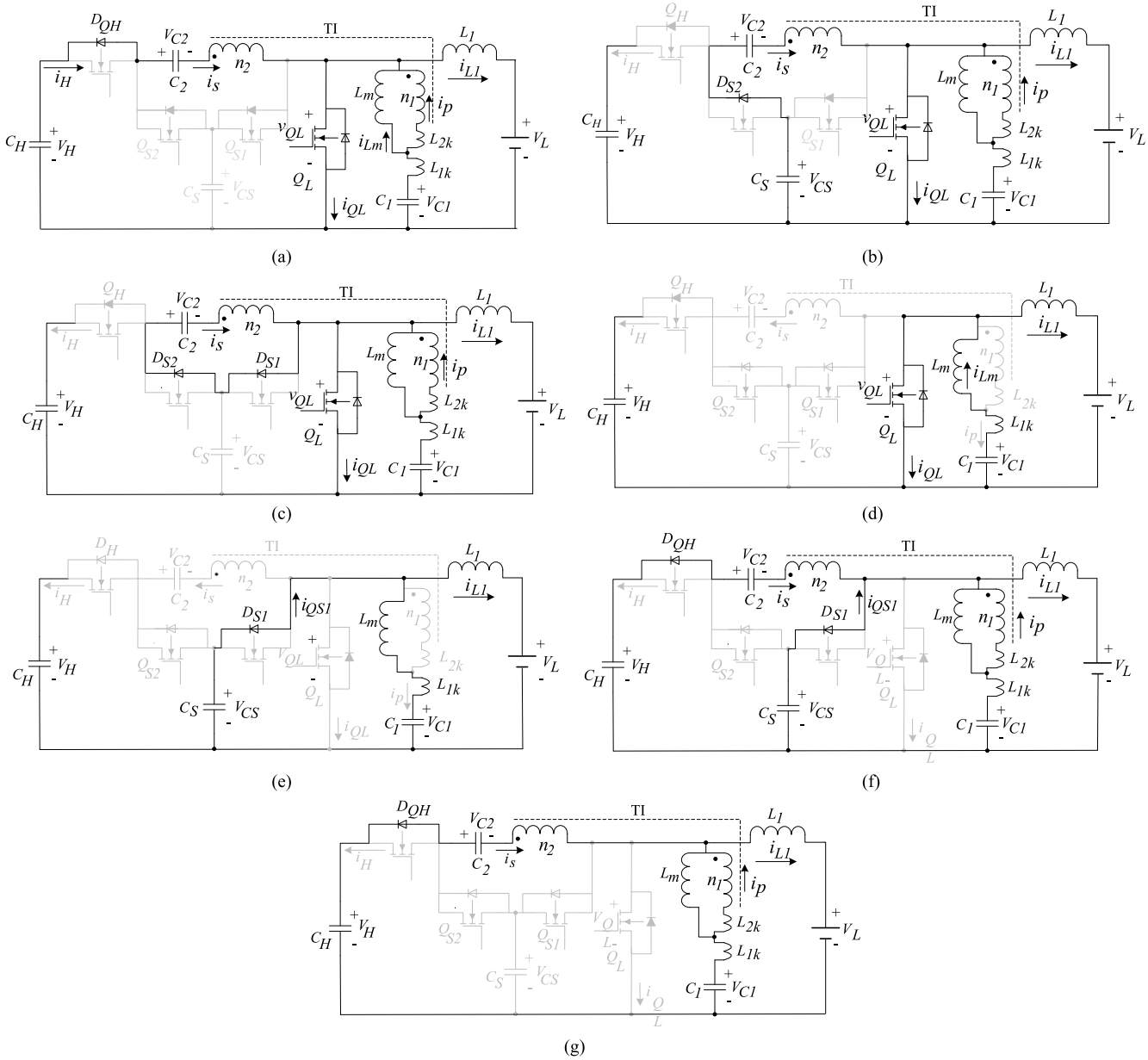


Fig. 6. Topological states of the proposed converter in boost mode: (a) State 1 [$t_0$–$t_1$]; (b) State 2 [$t_1$–$t_2$]; (c) State 3 [$t_2$–$t_3$]; (d) State 4 [$t_3$–$t_4$]; (e) State 5 [$t_4$–$t_5$]; (f) State 6 [$t_5$–$t_6$]; (g) State 7 [$t_6$–$t_0$].

Substitution of (2), (3), (4), and (5) into the equation of the volt–sec balance of magnetizing inductance the CCM voltage conversion ratio of the idealized proposed converter in the boost mode can be found

$$M_{\rm bst} = \frac{V_H}{V_L} = \frac{1+n}{1-D_{\rm bst}}. \tag{6}$$

The derived conversion ratio of the proposed converter in the boost mode as function of the duty ratio *D* and TI turns ratio *n* is illustrated in Fig. 7. This indicates that steep voltage gain *M* can be achieved with a moderate turns ratio *n* avoiding operation at extreme duty ratio $D_{\rm bst}$. Compared with the earlier SEPIC-derived counterpart [21] (which had a voltage gain function *n*/(1 − D) in the boost mode), the proposed topology has a higher gain.

### *B. Buck-Mode Conversion Ratio*

In buck mode, the switch $Q_H$ is turned ON for the duration of $D_{\rm buck}T_s$ [see Fig. 4(b)], and the voltage across the magnetizing inductance is

$$V_{L_m} = -\frac{V_H}{n+1} + V_L. \tag{7}$$

During the OFF interval of the switch $Q_H$, $D'_{\rm buck}T_s$ [see Fig. 4(d)], the voltage of the magnetizing inductance is

$$V'_{L_m} = V_{C_1}. \tag{8}$$

Substituting (2), (3), (7), and (8) into the equation of the volt–sec balance of the magnetizing inductance, the voltage conversion ratio of the idealized proposed converter in the CCM

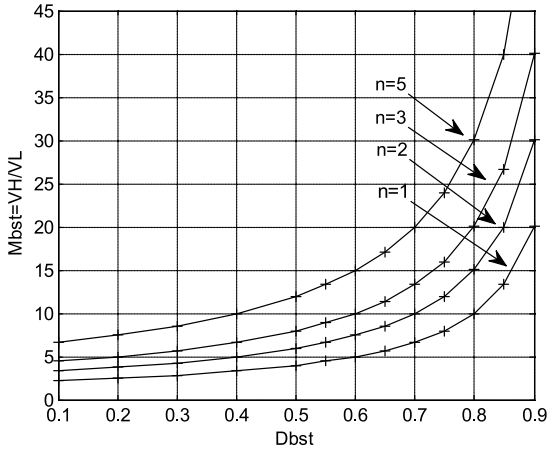


Fig. 7. Boost mode voltage conversion ratio *M* of the BTCS converter as function of the duty ratio $D_{\rm bst}$ and the TI turns ratio *n*.

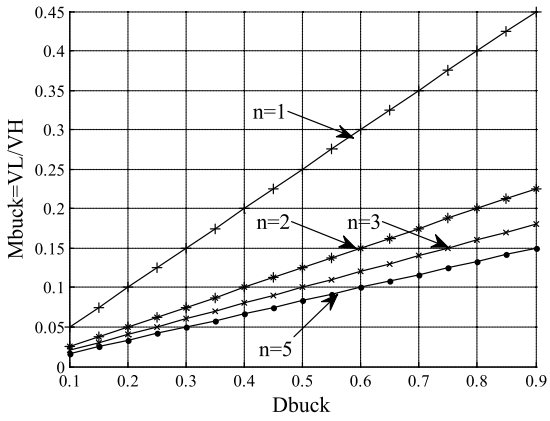


Fig. 8. Buck mode voltage conversion ratio *M* of the BTCS converter as function of the duty ratio $D_{\rm buck}$ and the TI turns ratio *n*.

buck mode can be found as a linear function of $D_{\rm buck}$

$$M_{\rm buck} = \frac{V_L}{V_H} = \frac{D_{\rm buck}}{n+1}. \tag{9}$$

The ideal voltage gain in the buck mode (9) with regard to turns ratio *n* is illustrated in Fig. 8, which shows that steep voltage conversion ratio in the buck mode can be obtained by moderate turns ratio *n* and duty cycle ratio $D_{\rm buck}$.

## V. Stress Analysis

### A. Stress Analysis in the Boost Mode

During the boost mode, the voltage across the switch $Q_L$ $V_{\rm Q_L}$ is peaking at the end of State 6 at $t = t_6$ (see Fig. 5) and equals

$$V_{\rm Q_L\,max\_bst} = \frac{V_H}{1+n} + nZ_0 \left[\frac{P}{V_L} + \frac{D_{\rm bst} V_L}{2\,(n+1)\,f_S}\left(\frac{1}{L_1}+\frac{1}{L_m}\right)\right]. \tag{10}$$

where $Z_0 = \sqrt{(L_{1k}+L_{2k})/C_s}$ and *P* is the converter's power level.

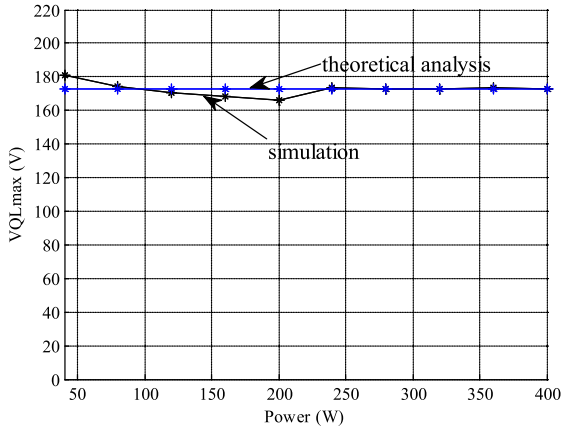


Fig. 9. Comparison of theoretically predicted and simulated peak switch voltage $V_{Q_L\,\max}$ in buck mode (for $n = 3.4$, $L_m = 75$ $\mu$H, $L_1 = 200$ $\mu$H, $L_{1k} = L_{2k} = 0.75$ $\mu$H, $V_L = 48$ V, $V_H = 380$ V).

Equation (10) shows that increasing turns ratio *n* can reduce the voltage stress across $Q_L$ while increasing leakage inductances tend to augment the voltage magnitude across the switch $Q_L$.

The current of switch $Q_L$ is peaking at the end of the State 2 at $t = t_2$ and can be found as

$$I_{Q_L\,\max\_\rm bst} = \frac{2P}{V_L} + \frac{V_H}{nZ_0}. \tag{11}$$

These results are identical to the findings in [28] and presented here as a quick reference and in sake of completeness of this text.

### B. Stress Analysis in Buck Mode

During the buck mode, the peak voltage across the switch $Q_L$ occurs at the end of State 1, $t = t_1$ (see Fig. 3), which is given by

$$V_{Q_L\,\max\_\rm buck} = \frac{2V_H}{1+n}. \tag{12}$$

Equation (12) shows that increasing turns ratio can reduce the voltage stress across $Q_L$ in buck mode. Detailed derivation of switch stress in buck mode is given in the Appendix. Comparison of the theoretically predicted [see (12)] and simulated peak switch voltage is shown in Fig. 9. A good agreement is found.

The current of the switch $Q_L$ $i_{Q_L}$ in the buck mode peaks during State 4 (see Fig. 3) and is bounded by

$$i_{Q_L\,\max\_\rm buck} = \frac{P_o}{V_L} + \frac{(1-D)V_L}{2f_S}\left(\frac{1}{L_1}+\frac{1}{L_m}\right) + i_{p\,\max t_4}. \tag{13}$$

where $i_{p\max t4}$ in (13) is given in (36).

Comparison of the theoretically predicted [see (13)] and simulated peak switch current in buck mode is shown in Fig. 10. Apparently, (13) provides a satisfactory estimate of the peak current $i_{Q\,H\,\max\_\rm buck}$.

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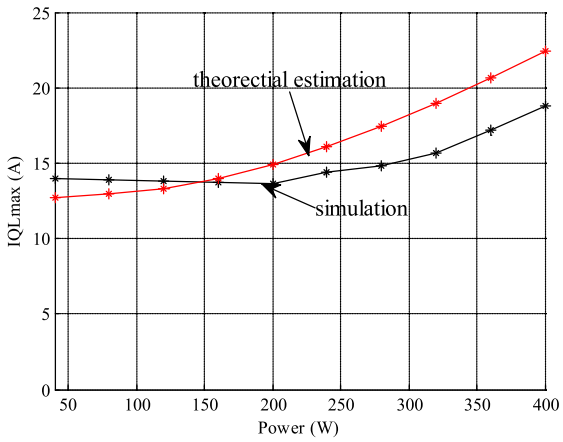


Fig. 10. Comparison of the estimated and simulated peak switch current $I_{Q_L\,\max}$ in buck mode (for $n = 3.4$, $L_m = 75$ $\mu$H, $L_1 = 200$ $\mu$H, $L_{1k} = L_{2k} = 0.75$ $\mu$H, $V_L = 48$ V, $V_H = 380$ V).

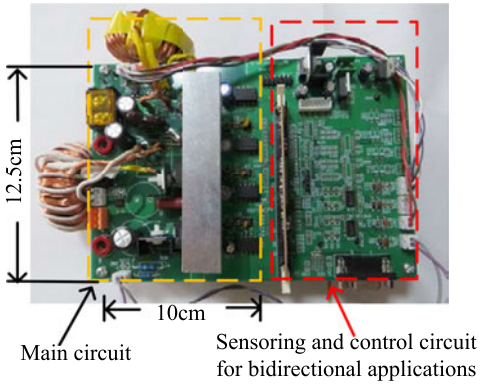


Fig. 11. Experimental BTCS prototype circuit.

## VI. Experimental Results

To verify the theoretical predictions, a 400-W, 48- to 380-V experimental BTCS converter prototype in Fig. 1(b) was built and tested. The circuit parameters are the following: switching frequency, $f_s = 50$ kHz; magnetizing inductance of the TI, $L_m = 75$ $\mu$H; and its turns ratio is $N_1 : N_2 = 22 : 77$; the estimated leakage inductance are $L_{1k} = L_{2k} = 0.75$ $\mu$H (about 1% of the magnetizing inductance, referred to the primary side). Additional parameters are the low-side inductor, $L_1 = 200$ $\mu$H (for DCM/CCM boundary at 40% of $P_{\max}$); the capacitors, $C_S = 10$ nF/400 V; $C_1 = 22$ $\mu$F/100 V; $C_2 = 2$ $\mu$F/400 V; $C_o = 47$ $\mu$F/600 V. Semiconductor devices: $QL$, IRFB4332 (250 V, $R_{\mathrm{DS(on)}} = 29$ m$\Omega$); diodes: $Q_{S_1}$, IRFB4332 (250 V, $R_{\mathrm{DS(on)}} = 29$ m$\Omega$); $Q_{S_2}$ and $D_{S_2}$ : C3D04065A (650 V/8.5 nC/1.2 V); $Q_{\mathrm{H}}$ and $D_{S_2}$ : C3D04065A (650 V/8.5 nC/1.2 V). The prototype is shown in Fig. 11. The main circuit of the proposed topology comprises four switches controlled by a TI-DSP control card (TMDSCNCD2808). Current sensors (ACS712) and voltage-measuring resistors are mounted on a board and connected to the analog-to-digital ports of DSP through operational amplifiers. The total size of the 400 W bidirectional application test bed prototype board is 19 cm $\times$ 12.5 cm, no optimization was attempted.

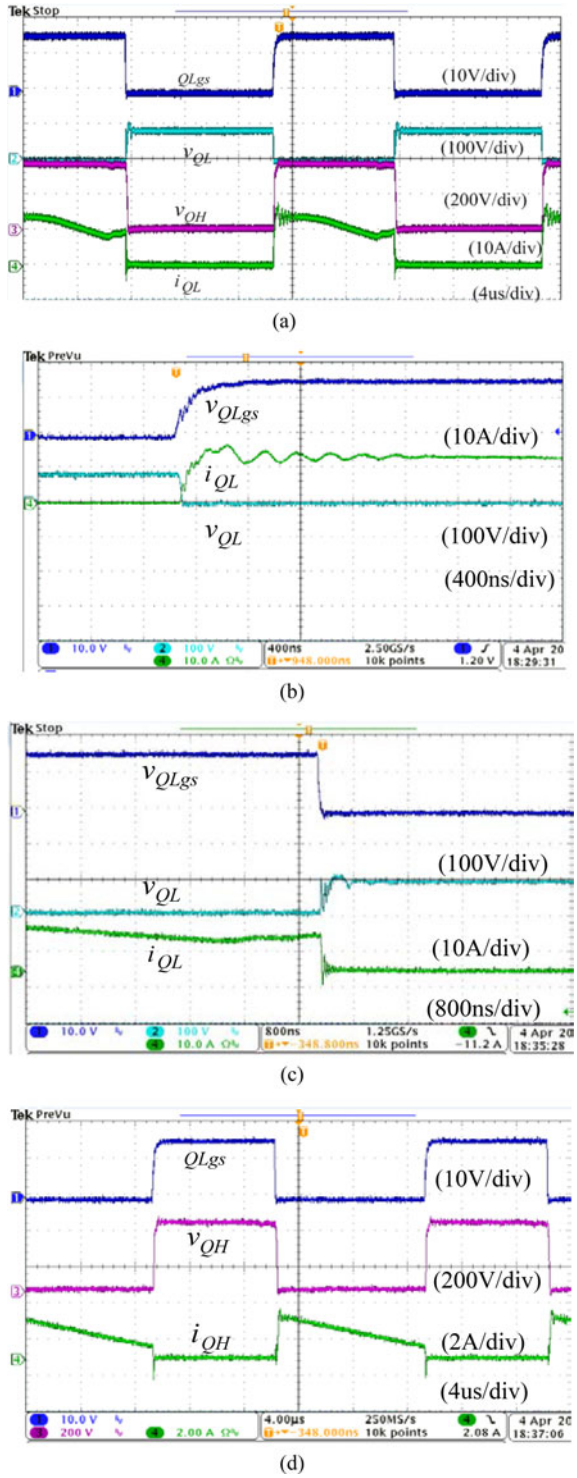


Fig. 12. Experimental BTCS waveforms (boost mode, $P_o = 200$ W): (a) general view of $V_{gs}$, $V_{Q_L}$, $i_{Q_L}$; (b) voltage and current during ZC turn ON of the $Q_L$ switch; (c) voltage and current during ZV turn OFF of the $Q_L$ switch; (d) voltage of the $Q_H$ switch $V_{Q_H}$ versus current $i_{Q_L}$.

The waveforms of the experimental BTCS prototype in the boost mode are shown in Fig. 12, which shows that $Q_{\mathrm{L}}$ achieves proper ZVS and ZCS. Fig. 12 also shows that no voltage overshoot and no ringing can be observed across the output diode $v_{Q_H}$.

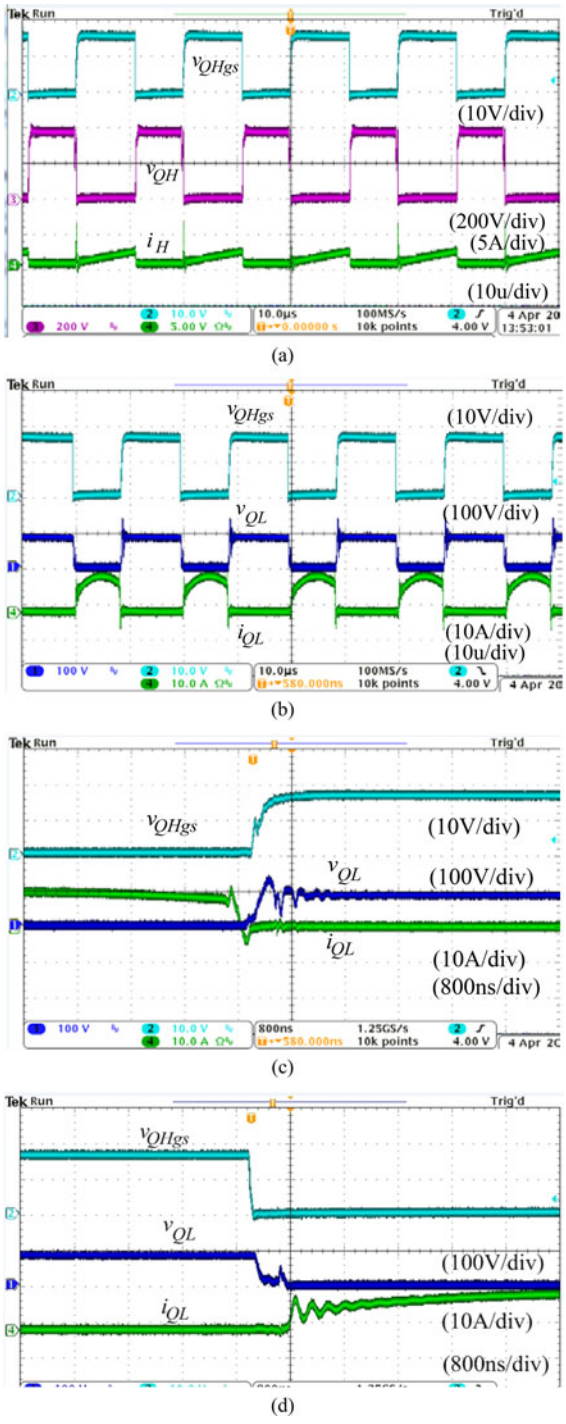


Fig. 13. Experimental BTCS waveforms (buck mode, $P_O = 200$ W): (a) general view of switch $i_{Q_H}$, $V_{Q_H}$; (b) general view of switch $i_{Q_L}$, $V_{Q_L}$; (c) ZVS of switch $Q_L$; (d) ZCS of switch $Q_L$.

The waveforms of the experimental BTCS prototype in the buck mode are shown in Fig. 13. Evidently, ZVS and ZCS are achieved for the switch $Q_L$ in the buck mode. Although the switch $Q_H$ experiences hard switching, there is no voltage spike due to the snubber capacitor clamping action. The current spike, visible on $i_H$ trace in Fig. 13(a), originates due to charging of the parasitic capacitance of $Q_{S_2}$.

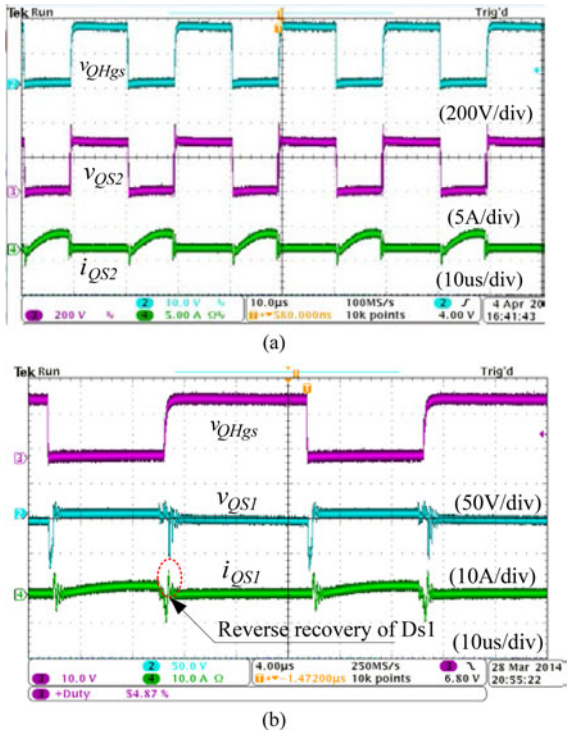


Fig. 14. Experimental BTCS waveforms (buck mode, $P_o = 200$ W): (a) waveforms of switch $Q_{S_2}$: $i_{Q_{S_2}}$, $V_{Q_{S_2}}$; (b) waveforms of switch $Q_{S_1}$: $i_{Q_{S_1}}$, $V_{Q_{S_1}}$. Note the reverse recovery of the body diode of $Q_{S_1}$.

The waveforms of switch $Q_{S_1}$ and $Q_{S_2}$ in the buck mode are shown in Fig. 14. The experimental waveforms of switch $Q_{S_1}$ differ from the ideal waveforms in Fig. 3 due to the reverse recovery of $D_{S_1}$, which occurs during transition from State 1 to State 2. The reverse recovery current of $D_{S_1}$ discharges the capacitor $C_S$. Thus, the voltage across $Q_{S_1}$ drops [see Fig. 14(c)]. One possible solution to alleviate the reverse recovery problem without hardware modification is clamping the voltage across $D_{S_1}$ by gating the switch $Q_{S_1}$ during State 1. As shown in the Appendix, the duration of State 1 is load independent, determined by the leakage inductance and snubber capacitor $C_S$ and is nearly constant $\Delta t_1$ [see (24)]. Therefore, it is possible to modify the switching timing by adding an extra fixed switch-on time of $Q_{S_1}$ in the CCM mode (see Fig. 15).

The proposed BTCS can freely shift between the buck mode and the boost mode by implementing a proper switching and the control scheme. The original switching strategy can be described by the following Boolean functions (14):

$$\begin{aligned} S_{Q_L} &= MS \\ S_{Q_H} &= \bar{M}S \\ S_{Q_{S_1}} &= S_{Q_{S_2}} = \bar{M}\bar{S} \end{aligned} \tag{14}$$

where $S$ is the duty-cycle-dependent switching function

$$S = \begin{cases} 1, & 0 \le t < DT_s \\ 0, & DT_s \le t < T_s \end{cases} \tag{15}$$

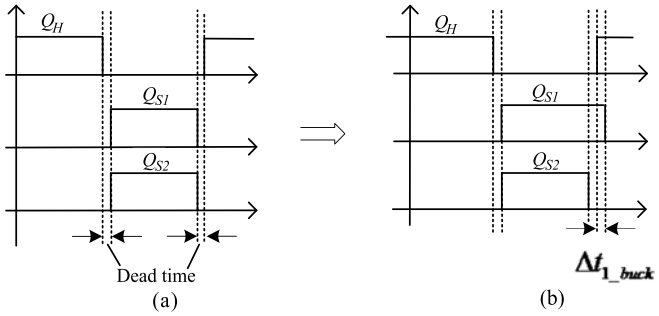


Fig. 15. BTCS switching signals in buck mode. (a) Original timing; (b) improved timing to alleviate the reverse recovery problem of $Q_{S_1}$.

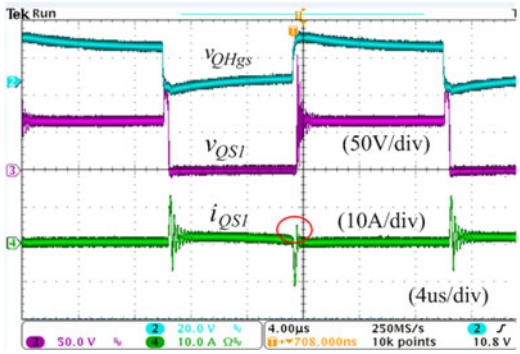


Fig. 16. Experimental BTCS waveforms (buck mode) with improved timing scheme. Note the alleviated reverse recovery current spike of the switch $Q_{S_1}$.

where $M$ is the mode-select switching function

$$M = \begin{cases} 1, & \text{boost} \\ 0, & \text{buck} \end{cases}. \tag{16}$$

For practical reasons, small dead time has to be introduced as shown in Fig. 15(a). However, better performance in the buck mode can be obtained by the improved control scheme, with $Q_{S_1}$ having slight overlap, as illustrated in Fig. 15(b). The later has been also implemented and tested on the prototype circuit. The experimental result using improved timing scheme in the buck mode are shown in Fig. 16. The reverse current of $D_{S_1}$ is significantly reduced and the voltage across $Q_{S_1}$ has no drop. Also, a limited ringing can be observed during the dead time.

Comparison of the simulated, the theoretically predicted and experimentally measured conversion ratio $M_{\text{buck}} = V_L/V_H$ in the buck mode is shown in Fig. 17. It reveals that the theoretical expectation stands in good agreement with experimental results.

The efficiency of the prototype BTCS converter as function of output power is shown in Fig. 18. In the boost mode, the efficiency over 95% was recorded in a wide power range, peaking at 96.4%, whereas in the buck mode, the efficiency over 94% was measured in a wide range, peaking at 95.0%.

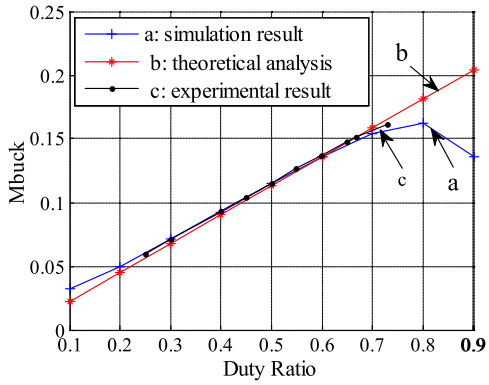


Fig. 17. Comparison of the simulated, experimentally measured and the theoretically predicted BTCS's conversion ratio $M = V_H/V_L$ in buck mode.

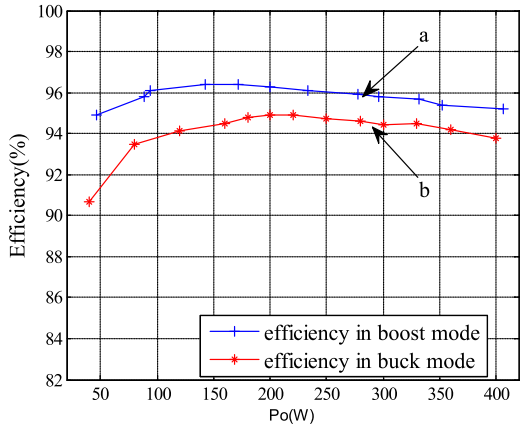


Fig. 18. Efficiency (%) of the BTCS converter as function of power level at $V_L = 48$ V and $V_H = 380$ V: (a) boost mode; (b) buck mode.

## VII. Conclusion

This paper introduced a SEPIC-derived bidirectional converter for battery applications. The proposed BTCS converter utilized TI and charge pump techniques to achieve steep voltage conversion gain. A bidirectional active regenerative snubber circuit is incorporated into the converter to reduce the switch voltage stress and achieve lossless switching. The converter relied on a simple and easily implemented control strategy to activate its four switches. In addition, the filter inductor on the low dc side provided continuous current with limited ripple component.

The paper reported analytical, simulated, and experimental results obtained from a 400-W, 48- to 380-V dc prototype.

## Appendix

The detailed stress analysis of the proposed topology in the buck mode was obtained by state-plane analysis method. A brief introduction can be found in [27].

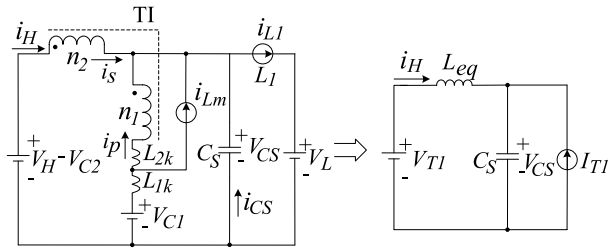


Fig. 19. Equivalent circuit of State 1 of the BTCS converter in the buck mode.

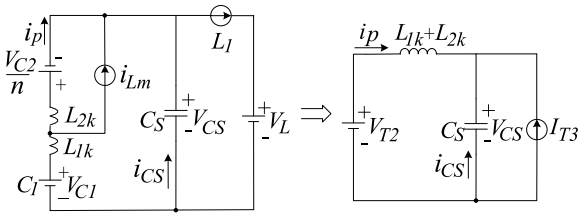


Fig. 20. Equivalent circuit of the BTCS converter in buck mode of State 3.

### A. Voltage Stress of Switch $Q_L$ and Peak Current of Switch $Q_H$

During the buck mode, the switch voltage $v_{Q_L}$ is peaking at the end of State 1 (see in Fig. 3). Here, the switch voltage equals the voltage across capacitor $C_S$ [see Fig. 4(a)].

The simplified equivalent circuit of State 1 of the buck mode is redrawn in Fig. 19. Here, the equivalent inductance $L_{\rm eq}$ is

$$L_{\rm eq} = \frac{L_{1k} + L_{2k}}{(1 + (1/n))^2}. \tag{17}$$

The equivalent current source $I_{T_1}$ and the equivalent voltage source $V_{T_1}$ in Fig. 19 are

$$I_{T_1} = i_{L_1}(0) - i_{L_m}(0) = i_{L_1\_\min} - i_{L_m\_\max} \tag{18}$$

$$V_{T_1} = \frac{V_H}{1+n} \tag{19}$$

and the initial conditions are

$$i_H(0) = I_{T_1} + i_{C_s}(0) = \frac{(n+1)\, I_{T_1}}{n} \tag{20}$$

$$v_{C_S}(0) \approx 0. \tag{21}$$

By applying the state-plane analysis method, the peak voltage of $Q_{\rm L}$ can be obtained as

$$V_{Q_L\,\max\_\rm buck} = \frac{V_H}{1+n} + \frac{V_H}{1+n} \sqrt{1 + \left(\frac{Z_0 (i_{L_1\_\min} - i_{L_m\_\max})}{V_H}\right)^2}. \tag{22}$$

Since the characteristic impedance $Z_0$ is a function of leakage inductances, it assumes a relatively small value ($Z_0 < 10\ \Omega$) in this application. Therefore, considering the high value of $V_H$ ($V_H = 380$ V), (22) can be approximated by (12).

The current of $Q_H$ reaches its peak during State 1 (see Fig. 3) and equals the maximum current of $C_S$. Hence, by the state-plane analysis method $i_{Q_H\,\max}$ is obtained as

$$i_{Q\,H\,\max\_\rm buck} = \frac{1}{n+1} \left[\frac{P_o}{V_L} - \frac{(1-D_{\rm buck})V_L}{2f_s}\left(\frac{1}{L_1} + \frac{1}{L_m}\right) + \frac{V_H}{nZ_0}\right]. \tag{23}$$

The duration of State 1 equals half the resonance cycle, determined by the leakage inductances and the snubber capacitor

$$\Delta t_1 = \frac{T_1}{2} = \frac{n\pi}{n+1}\sqrt{(L_{1k} + L_{2k})\, C_s}. \tag{24}$$

### B. Current Ripple and Peak Current of the Input Inductor $L_1$

Examining the waveforms in Fig. 3 and considering (2) and (8) allow finding the peak magnetizing current of the TI

$$i_{L_m\_\max} = -i_{L_m\_\min} = \frac{(1-D_{\rm buck})\, V_L}{2 f_S L_m}. \tag{25}$$

In buck mode, the voltage across $L_1$ approximately equals $V_L$; thus, the maximum current of $L_1$ can be found as

$$i_{L_1\_\max} = \frac{P}{V_L} + \frac{(1-D_{\rm buck})V_L}{2 f_s L_1}. \tag{26}$$

### C. Peak Current of Switch $Q_{S_1}$

The peak current of switch $Q_{S_1}$ appears at the end of State 3 (see Fig. 3). The equivalent circuit of State 3 is shown in Fig. 20.

The equivalent voltage source $V_{T_3}$ and the equivalent current source $I_{T_3}$ in Fig. 20 are given by

$$I_{T_3} \approx i_{L_1\_\max} - i_{L_m\_\min} \tag{27}$$

$$V_{T_3} = V_{C_1} - \frac{V_{C_2}}{n} \approx 0 \tag{28}$$

where the initial conditions are

$$v_{C_s}(t_2) = V_{c_s\,\max} \approx 2V_{T_1} \tag{29}$$

$$i_p(t_2) = n i_S(t_2) = \frac{n}{n+1}\left(i_{L_1\_\max} - i_{L_m\_\min}\right). \tag{30}$$

At the end of State 3, the voltage across $C_S$ falls to zero, whereas considering (25) and (26) and after some additional manipulation, the capacitor and the primary winding currents at the end of this interval can be found

$$i_{C_s}(t_3) = -\frac{2V_H}{(n+1)\, Z_0} \sqrt{1 + \left[\frac{Z_0\,(I_{L_1\_\max} - I_{L_m\_\min})}{2V_H}\right]^2} \tag{31}$$

$$i_p(t_3) = n i_S(t_3) = (i_{L_1\_\max} - i_{L_m\_\min}) + i_{C_s}(t_3). \tag{32}$$

$$|i_p| \le i_{p\max t_4} = \frac{(1-D_{\text{buck}})V_L}{4L_m f_S} + \sqrt{\left[\frac{P}{V_L} + \frac{(1-D_{\text{buck}})V_L}{f_S}\left(\frac{1}{2L_1}+\frac{1}{L_m}\right) - \frac{2V_H}{(n+1)Z_0}\right]^2 + \left[\frac{nP}{2V_H f_S\sqrt{(L_{1k}+L_{2k})C_{\text{eq}}}}\right]^2} \quad (41)$$

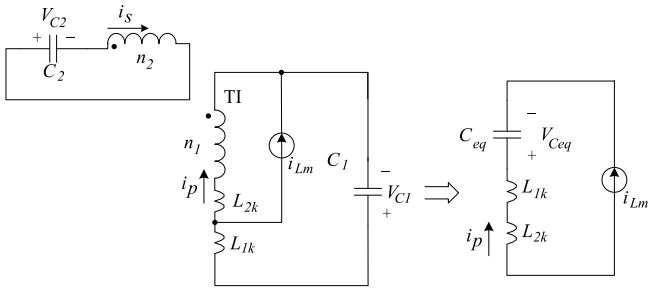


Fig. 21. Equivalent circuit of the BTCS converter in buck mode of State 4.

According to Fig. 4(c), the current of $Q_{S_1}$ during State 3 is the sum of $i_{C_s}$ and the secondary current; therefore

$$i_{Q_{S_1}\max\_\text{buck}} = \frac{1}{n}\left(i_{L_1\_\max} - i_{L_m\_\min}\right) + \left(\frac{n+1}{n}\right) i_{C_s}(t_3). \quad (33)$$

Under the condition

$$\frac{Z_0\left(I_{L_1\_\max} - I_{L_m\_\min}\right)}{2V_H} \ll 1 \quad (34)$$

(33) can be approximated by

$$i_{Q_{S_1}\max\_\text{buck}} \approx \frac{1}{n}\left[\frac{2V_H}{Z_0} - \left(i_{L_1\_\max} - i_{L_m\_\min}\right)\right]. \quad (35)$$

### *D. Peak Current of Switch $Q_{S_2}$ and $Q_L$*

The maximum current of the switch $Q_L$ $i_{Q_L\max}$ occurs during State 4 (see Fig. 3). Derivation of the equivalent circuit of State 4 is shown in Fig. 21.

The equivalent capacitance in Fig. 21 can be derived as

$$C_{\text{eq}} = \frac{n}{((n/C_1) + (1/nC_2))}. \quad (36)$$

The current source $i_{L_m}$ in Fig. 21 can be approximated as half the minimum value of the magnetizing current $i_{L_m\_\min}$ in (25), whereas the initial current of $i_p$ can be found in (32). The initial voltage across $v_{C_{\text{eq}}}(t_3)$ is the voltage difference between $V_{C_1}$ and $V_{C_2}/n$ and can be approximated by

$$v_{C\text{eq}}(t_3) = \frac{1}{2}\left(\frac{\Delta V_{C_2}}{n} - \Delta V_{C_1}\right) \approx \frac{nP}{2V_H f_S C_{\text{eq}}}. \quad (37)$$

The upper boundary of the magnitude of primary current during State 4 can be found applying the state analysis method, as shown in (38) at end of the paper.

Accordingly, the peak current of $Q_{S_2}$ $I_{QS2}$ in the buck mode is bounded by

$$I_{Q_{S_2}} < I_{Q_{S_2}\max} = \frac{i_{p\max t_4}}{n}. \quad (38)$$

Examining Fig. 4(d) reveals that

$$i_{Q_L} = (i_{L_1} - i_{L_m}) - i_P. \quad (39)$$

Therefore, the current of $Q_L$ can be bounded by

$$I_{Q_L} < I_{Q_L\max} = (i_{L_1\_\max} - i_{L_m\_\min}) + i_{p\max t_4}. \quad (40)$$

Further substituting (25) and (26) into (41) shown at the top of the page, yields (13) equation (41) shown on the top of the page.

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