Soft Switching PWM Cascaded Three-Level Combined DC–DC Converters With Reduced Filter Size and Wide ZVS Load Range

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***Abstract*—Two soft switching cascaded three-level (TL) combined dc–dc converters are proposed in this paper. The first converter is composed of a half-bridge cascaded TL dc–dc converter (CTLC) and a full-bridge (FB) CTLC, and the other one is composed of two FB CTLCs. The presented topologies have following common advantages: off-state voltage on all switches is only half of the input voltage; the structure of the primary circuit is simple and compact; all primary switches are directly clamped by the input capacitors and no added clamping devices are required; and the voltage across the output *LC* filter is a TL waveform, which results lower output filter volume and faster system dynamic response. In addition, the input filter can also be minimized. All power switches in the proposed converters can obtain zero-voltage switching in wide load range; furthermore, less conduction loss is added. The operation and technical analysis of the proposed converters are given. Experiments are carried out to validate the proposed converters, and efficiency curves are tested and given.**

***Index Terms*—Cascaded dc–dc converter, three-level (TL) dc–dc converter, zero-voltage switching (ZVS).**

I. Introduction

THREE-level (TL) high-frequency dc–dc converters have attracted worldwide attention for a lot of high input voltage industry applications such as dc–dc converters after three-phase power factor correction circuits and dc interfaces for microgrid power system and distributed power system [1]–[6]. The concept of a TL dc–dc converter was first proposed in 1992 [4]. Then, many good studies have been published on this topic. These studies include novel topologies [7]–[21] [36]–[40], controlling strategies [22]–[25], [41]–[43], soft switching technologies [21]–[23], [27]–[29], reduced filters size solutions [28], [30]–[33], and other useful engineering considerations [34], [35]. All the references listed above have made the TL dc–dc converters more applicable.

In [7], a soft switching pulse width modulation (PWM) half-bridge (HB) cascaded TL dc–dc converter (CTLC) was proposed. The primary circuit of HB CTLC is built of two-level HB cells, and these cells are series connected to fabricate TL structure without auxiliary clamping devices. Thus, HB CTLC has simpler and more compact primary structure to obtain the same output performance compared to other TL dc–dc converters, which may be the most attractive feature to industry customers. Moreover, HB CTLC can be extended to higher voltage level easily due to modular structure, and several HB CTLCs for higher input voltage rating have been proposed [9], [10]. Many other TL dc–dc converters, i.e., diode clamped TL dc–dc converter, can also be extended to higher voltage level. But, as mentioned in [40], the number of achievable voltage levels is limited not only due to the dynamic voltage unbalance problem but also due to the complexity of the primary circuit structure and the modulation strategy [40]. Therefore, HB CTLC may be a better choice for applications with super high input voltage, i.e., 1400 V or higher. In [36], a soft switching PWM full-bridge (FB) CTLC was proposed, which is composed of two-level FB cells. FB CTLC has all the merits belonging to HB CTLC. In addition, FB CTLC has some special advantages compared to HB CTLC, such as smaller VA rating of the input capacitors and lower current stress of each primary switch. Thus, FB CTLC is more suitable for high input and large power dc–dc conversion. Several new FB CTLC topologies were proposed and discussed in [37] and [38]. A new FB CTLC was proposed in [39], wherein a flying capacitor is added to obtain the voltage auto balance ability among series connected modules. Controlling strategies for output parallel-connected FB CTLCs were analyzed in [41]–[43].

However, problems still exist. First, the secondary rectified voltage before the output filter of FB CTLC is a two-level waveform, which requires a larger output inductor to limit the ripple current through it. Larger output inductance may add the overall system volume and slow the possible system dynamic response [44]. Second, the input current of FB CTLC decays to zero during free-wheeling stages, and a large input filter is also requested to confirm corresponding EMC standards [44]. Finally, the zero-voltage switching (ZVS) of the lagging switches in each FB cell is more difficult due to only the energy stored in the leakage inductance can be used. Abovementioned problems are common drawbacks existing in most of TL dc–dc converters, and a number of new TL dc–dc converters with TL rectified voltage waveform and good soft switching characteristics have been developed [28], [30]–[33]. In [30], a ZVZCS hybrid FB TL dc–dc converter was proposed, which can generate TL voltage waveform before the output filter. The main drawback of this converter is uneven voltage stress on the primary switches, which limits its application in high input dc–dc power conversion. In order to achieve TL secondary rectified voltage waveform and

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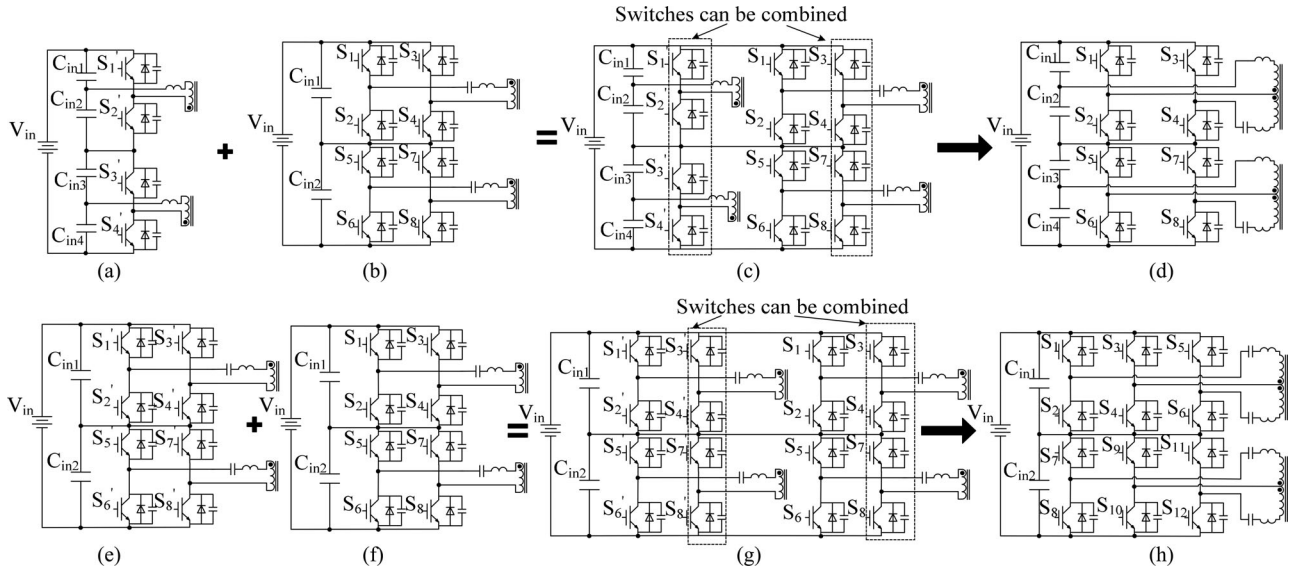

Fig. 1. Derivation of the proposed CTLCCs: (a) HB CTLC; (b) FB CTLC; (c) HB CTLC and FB CTLC with reused input capacitors; (d) HB–FB CTLCC; (e) FB CTLC; (f) FB CTLC; (g) Two FB CTLCs with reused input capacitors; (h) FB–FB CTLCC.

even voltage stress on each switch, a TL combined dc–dc converter (TLCC) with six power switches was proposed in [31]. The converter in [31] is switched in phase shift (PS) mode and may gain more good soft switching characteristics by utilizing ZVZCS technology. A TLCC with four switches was proposed in [32], and this topology has the minimum number of primary switches among all TLCCs. In [28], an FB TLCC was proposed, which can achieve TL secondary rectified voltage waveform before *LC* filter as well as wide ZVS load range for all primary switches. Although the VA rating of the transformers in TLCCs is larger than that of traditional TL dc–dc converters with single transformer under variable input and constant output applications, the overall volume of passive components of TLCCs is still less than traditional TL dc–dc converters due to smaller volume of output and input filters [28], [31], [32]. In addition, all switches in TLCCs can obtain better soft switching characteristics by utilizing either improved ZVS solution [28] or ZVZCS solution [31]. Therefore, TLCC is still an attractive solution to obtain TL secondary rectified voltage waveform and good soft switching characteristics. But, one common problem still exists. The primary power circuits of TLCCs in [28], [31], and [32] are still complex, and this complexity may reduce the interest of customers. Thus, it is still a worthy job to find new TLCCs characterized with TL secondary rectified voltage waveform, simpler and compact power circuit, and good soft-switching characteristics.

In this paper, two cascaded TL combined dc–dc converters (CTLCCs) with TL secondary rectified voltage waveform and wide ZVS load range are proposed. This paper is organized as follows. The deviation of the proposed converters is discussed in Section II. In Section III, the configurations and basic operation principles of the proposed converters are described. Some important technical issues are analyzed in Section IV. Experimental results are presented and discussed in Section V. The main conclusions are given in Section VI.

II. Derivation of the Proposed Converters

Based on the derivation principle of TLCCs mentioned in [28], [31], and [32], two CTLCCs are derived from basic HB or FB CTLCs in this section. The derivation process of HB–FB CTLCC is depicted in Fig. 1(a)–(d), and the derivation steps can be described as follows. *Step 1:* the converter shown in Fig. 1(c) can be deducted by reusing the input capacitors in Fig. 1(a) and (b); *Step 2:* the converter in Fig. 1(c) can be further simplified by combining the switches S_3, S_4, S_7, S_8, and S_1'–S_4'. The final topology is shown in Fig. 1(d); *Step 3:* the switching sequence of the new converter should be examined. The derivation process of FB–FB CTLCC is shown in Fig. 1(e)–(h), and detail information is not discussed in this paper for the sake of simplicity.

III. Configurations and Operation Principles

A. Configurations

Fig. 2 illustrates the circuits of the proposed converters. HB–FB CTLCC is depicted in Fig. 2(a), which is composed of an HB CTLC and an FB CTLC. The HB CTLC is built of the switches S_1, S_2, S_5 and S_6, the primary coils T_{1p} and T_{3p}. And the FB CTLC is composed of the switches S_1–S_8, the primary coils T_{2p} and T_{4p}, and the blocking capacitors C_{BL2} and C_{BL4}.C_{in1}–C_{in4} are input capacitors with the same value. During normal operation, the four input capacitors share the input voltage evenly, i.e., $V_{C\mathrm{in}1} = V_{C\mathrm{in}2} = V_{C\mathrm{in}3} = V_{C\mathrm{in}4} = V_{\mathrm{in}}/4$; during soft start operation, the voltage on each capacitor is uneven due to interleave asymmetrical PWM (IAPWM) modulation applied to HB CTLC cells. But, the midpoint voltage of the four capacitors are still stable with the value of $V_{\mathrm{in}}/2$, i.e., $V_{C\mathrm{in}1} + V_{C\mathrm{in}2} = V_{C\mathrm{in}3} + V_{C\mathrm{in}4} = V_{\mathrm{in}}/2$. The power transformer contains four primary coils and two secondary coils. Each primary coil is wired around an independent magnetic core, and two secondary coils enclose all magnetic cores. L_{1m} and L_{3m} are magnetizing

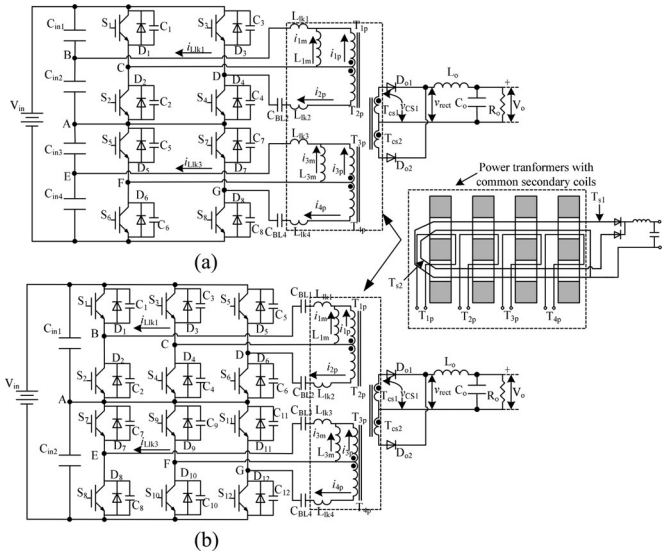

Fig. 2. Soft switching PWM CTLCCs: (a) HB–FB CTLCC; (b) FB–FB CTLCC.

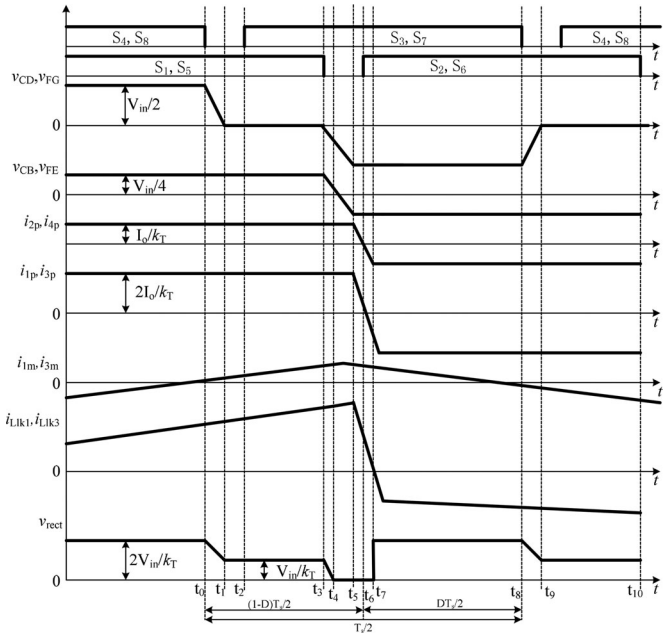

Fig. 3. Key waveforms of HB–FB CTLCC.

inductances of T_{1p} and T_{3p}. L_{lk1} to L_{lk4} are leakage inductances. D_{o1} and D_{o2} are rectifier diodes. Output filter is built of L_o and C_o.

FB–FB CTLCC is illustrated in Fig. 2(b), which is composed of two FB CTLCs. The first cell is built of the switches S_1–S_4 and S_7–S_{10}, the primary coils T_{1p} and T_{3p}, and the blocking capacitors C_{BL1} and C_{BL3}; the other cell is comprised of the switches S_3–S_6 and S_9–S_{12}, the primary coils T_{2p} and T_{4p}, and the blocking capacitors C_{BL2} and C_{BL4}. C_{in1} and C_{in2} are input capacitors with the same value, and these capacitors share the input voltage evenly during all operation stages. The structure of the power transformer in Fig. 2(b) is identical to that of HB–FB CTLCC. L_{1m} and L_{3m} are magnetizing inductances of T_{1p} and T_{3p}. L_{lk1}–L_{lk4} are leakage inductances. D_{o1} and D_{o2} are rectifier diodes. Output filter is built of L_o and C_o.

B. Normal Operation Principles

Before the analysis, some assumptions are set to clarify the explanation: all the components in the circuits are ideal; the voltage ripple on the input capacitors and blocking capacitors is smaller enough to be neglected; the output filter and load are replaced by a constant current source I_o; the magnetizing currents of T_{2p} and T_{4p} are smaller enough to be neglected, and the magnetizing currents of T_{1p} and T_{3p} are designed to a particular value to ensure ZVS operation of the lagging switches, i.e., S_1, S_2, S_5 and S_6 in HB–FB CTLCC; $L_{1m} = L_{3m} = L_m$; the output capacitance of each switch is identical and represented as C_{os} in the following equations. The turn ratios of primary coils in the HB–FB CTLCC are set as $2k_{T1p} = 2k_{T3p} = k_{T2p} = k_{T4p} = k_T$, and the turn ratios of primary coils in FB–FB CTLCC are defined as $k_{T1p} = k_{T3p} = k_{T2p} = k_{T4p} = k_T$.

1) HB–FB CTLCC: The corresponding key waveforms are depicted in Fig. 3. Fig. 4 highlights the six switching stages of the discussed converter during the first half switching cycle.

Stage 1 [see Fig. 4(a)]: Before t_0, the circuit is operated in steady condition and power is transferred from the input source to the load. S_1, S_4, S_5 and S_8 are ON; D_{o1} is ON and D_{o2} is OFF; $v_{CD} = v_{FG} = V_{in}/2$, and $v_{CB} = v_{FE} = V_{in}/4$; $v_{rect} = 2V_{in}/k_T$; $i_{2p} = i_{4p} = I_o/k_T$, $i_{1p} = i_{3p} = 2I_o/k_T$; i_{Llk1} equals the sum of i_{1p} and i_{1m}; i_{Llk3} equals the sum of i_{3p} and i_{3m}; i_{1m} and i_{3m} increase with time linearly, and the slope of these currents is

$$\frac{di_{1m}}{dt} = \frac{di_{3m}}{dt} = \frac{V_{in}}{4L_m}. \tag{1}$$

Stage 2 [see Fig. 4(b), $t_0 - t_1$]: At t_0, S_4 and S_8 are turned OFF at zero voltage due to the existence of C_4 and C_8; i_{2p} charges C_4 and discharges C_3 linearly with time; and i_{4p} charges C_8 and discharges C_7 linearly with time. This stage continues until $v_{C4} = v_{C8} = V_{in}/2$ and $v_{C3} = v_{C7} = 0$. The voltage of point D is

$$v_D(t) = \frac{V_{in}}{2} + \frac{I_o}{2k_T C_{os}}t. \tag{2}$$

The voltage of point G is

$$v_G(t) = \frac{I_o}{2k_T C_{os}}t. \tag{3}$$

The time of this period is

$$T_{10} = \frac{k_T V_{in} C_{os}}{I_o}. \tag{4}$$

Stage 3 [see Fig. 4(c), $t_1 - t_3$]: At t_1, D_3 and D_7 conduct naturally; S_1 and S_5 are ON. Input source powers the load through T_{1p}, T_{3p}, S_1, S_5, D_{o1} and the output filter; T_{2p} and T_{4p} operate in the free-wheeling mode; i_{1m} and i_{3m} keep increasing with time linearly. During this stage, S_3 and S_7 must be turned ON to obtain ZVS. According to

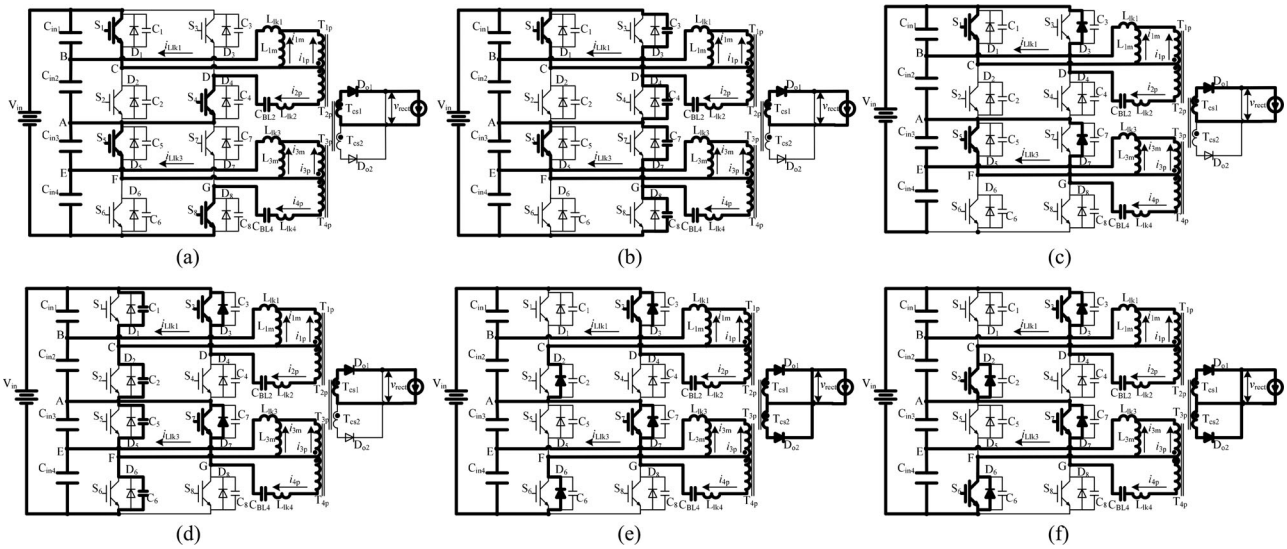

Fig. 4. Operation stages of HB–FB CTLCC: (a) stage 1, (b) stage 2, (c) stage 3, (d) stage 4, (e) stage 5, (f) stage 6.

Fig. 3, S_3 and S_7 are turned ON at the instant t_2. During this interval, $v_{\rm CD} = v_{\rm FG} = 0$ and $v_{\rm CB} = v_{\rm FE} = V_{\rm in}/4$; $v_{\rm rect} = V_{\rm in}/k_T$; $i_{2p} = i_{4p} = I_o/k_T$, $i_{1p} = i_{3p} = 2I_o/k_T$.

Stage 4 [see Fig. 4(d), $t_3 - t_5$]: At t_3, S_1 and S_5 are simultaneous turned OFF at zero voltage due to the existence of C_1 and C_5; i_{Llk1} together with i_{2p} charge C_1 and discharge C_2 linearly with time; i_{Llk3} together with i_{4p} charge C_5 and discharge C_6 linearly with time. During this interval, the value of i_{1m} and i_{3m} can be treated as a constant value, which is represented by I_m in the following equations. The voltage of point C decreases linearly with time before $v_{\rm rect}$ is in the direction of positive, and its value is

$$v_C(t) = V_{\rm in} - \left(3\frac{I_o}{k_T} + I_m\right)\frac{t}{C_{os}}. \tag{5}$$

The voltage of point F decreases linearly with time before $v_{\rm rect}$ is in the direction of positive, and its value is

$$v_{\rm F}(t) = \frac{V_{\rm in}}{2} - \left(3\frac{I_o}{k_T} + I_m\right)\frac{t}{C_{os}}. \tag{6}$$

The voltage of T_{1p} is

$$v_{\rm CB} = v_{\rm C}(t) - v_{\rm B}(t) = \frac{V_{\rm in}}{4} - \left(3\frac{I_o}{k_T} + I_m\right)\frac{t}{C_{os}}. \tag{7}$$

The voltage of T_{2p} is

$$v_{\rm CD} = v_{\rm C}(t) - v_{\rm D}(t) = -\left(3\frac{I_o}{k_T} + I_{2m}\right)\frac{t}{C_{os}}. \tag{8}$$

The voltage of T_{3p} is

$$v_{\rm FE} = v_{\rm F}(t) - v_{\rm E}(t) = \frac{V_{\rm in}}{4} - \left(3\frac{I_o}{k_T} + I_m\right)\frac{t}{C_{os}}. \tag{9}$$

The voltage of T_{4p} is

$$v_{\rm FG} = v_{\rm F}(t) - v_{\rm G}(t) = -\left(3\frac{I_o}{k_T} + I_{2m}\right)\frac{t}{C_{os}}. \tag{10}$$

$v_{\rm rect}$ is defined as

$$v_{\rm rect} = (2v_{\rm CB} + 2v_{\rm FE} + v_{\rm CD} + v_{\rm FG})/k_T. \tag{11}$$

Substituting (7)–(10) into (11) yields

$$v_{\rm rect} = \left[V_{\rm in} - 6\left(3\frac{I_o}{k_T} + I_m\right)\frac{t}{C_{os}}\right]/k_T. \tag{12}$$

When $v_{\rm rect}$ is zero, the voltage of point C can be calculated by (5) and (12), which is $5V_{\rm in}/6$. The voltage of point F can be calculated by (6) and (12), which is $V_{\rm in}/6$. The time of this period is

$$T_{43} = \frac{V_{\rm in} C_{os} k_T}{6(3I_{\rm o} + k_T I_m)}. \tag{13}$$

After t_4, the circuit will be operated into the free-wheeling mode. i_{Llk1} together with i_{2p} charge C_1 and discharge C_2 linearly with time; i_{Llk3} together with i_{4p} charge C_5 and discharge C_6 linearly with time; This stage ends until $v_{C1} = v_{C5} = V_{\rm in}/2$ and $v_{C2} = v_{C6} = 0$.

Stage 5 [see Fig. 4(e), $t_5 - t_6$]: At t_5, D_2 and D_6 are transferred to the ON status naturally. The circuit is operated in the free-wheeling mode; i_{2p} and i_{4p} decay linearly because negative voltage applied to the terminals of L_{lk2} and L_{lk4}; i_{Llk1} and i_{Llk3} decrease due to negative voltage applied to the terminals of L_{lk1} and L_{lk3}; during this stage, S_2 and S_6 must be turned ON to achieve ZVS. According to Fig. 3, S_2 and S_6 are turned ON at the instant t_6.

Stage 6 [see Fig. 4(f), $t_6 - t_7$]: At t_6, S_2 and S_6 are gated ON; S_3 and S_7 have been turned ON at the instant t_2. The primary currents increase in the inverse direction. When these currents reach $-I_o/k_T$ or $-2I_o/k_T$, the free-wheeling mode is over. The primary powers load continuously. After t_7, $v_{\rm CD} = v_{\rm FG} = -V_{\rm in}/2$ and $v_{\rm CB} = v_{\rm FE} = -V_{\rm in}/4$; $v_{\rm rect} = -2V_{\rm in}/k_T$; $i_{2p} = i_{4p} = -I_o/k_T$, $i_{1p} = i_{3p} = -2I_o/k_T$; i_{Llk1} equals the sum of i_{1p} and i_{1m}; i_{Llk3} equals the sum of i_{3p} and i_{3m}; i_{1m} and i_{3m} decreases with time linearly, the slope of these currents are

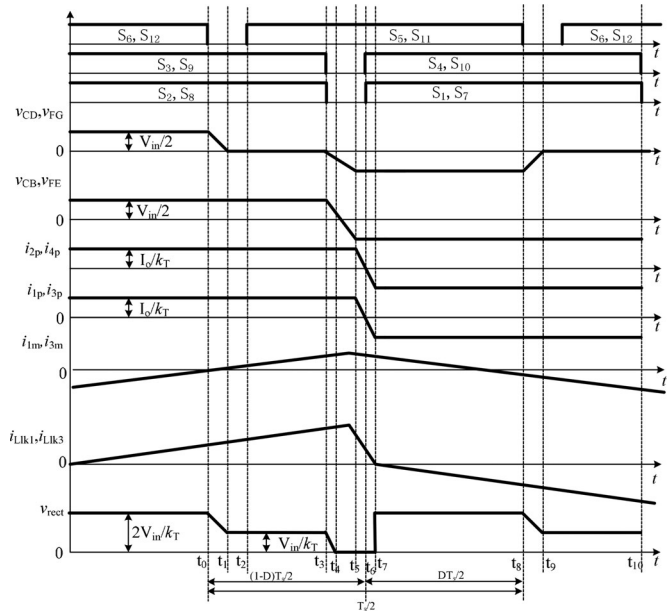

Fig. 5. Key waveforms of FB–FB CTLCC.

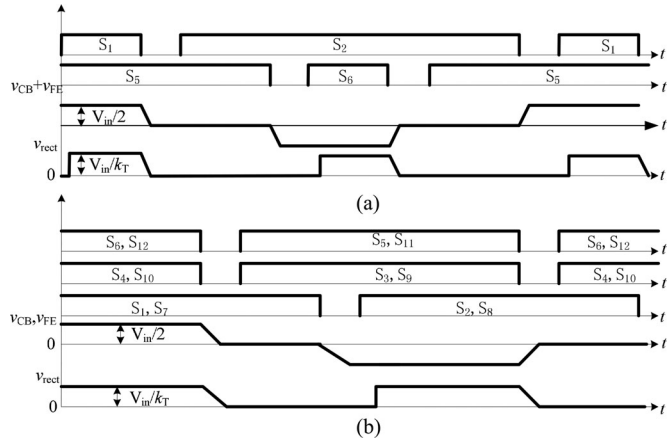

Fig. 6. Gate signals and key waveforms during soft start transition: (a) HB–FB CTLCC; (b) FB–FB CTLCC.

determined by (1). After stage 6, the circuit will be operated in the second half switching cycle.

2) FB–FB CTLCC: The corresponding key waveforms are depicted in Fig. 5. As the operation principle of FB–FB CTLCC is quite similar to that of HB–FB CTLCC, the detail description is not provided here for simplicity.

C. Brief Description of Soft Start Operation Principles

During start up, over load or short-circuit conditions, the output of the proposed converters requires wide regulated range, which is from rated value down to 0 V. Fig. 6 illustrates the soft start operation principles of the proposed converters. The gate signals and key waveforms of soft start operation of HB–FB CTLCC are shown in Fig. 6(a). During soft start operation, S_3, S_4, S_7 and S_8 are OFF, while S_1, S_2, S_5 and S_6 are gated in IAPWM mode. The HB–FB CTLCC can be treated as a HB CTLC, and the output can be regulated down to zero by changing the duty ratios of switching pairs S_1 and S_2, and S_5 and S_6 simultaneously. Detailed operation principle about HB CTLC can be found in [7].

TABLE I
MODULATION STRATEGIES OF THE PROPOSED CONVERTERS

	HB–FB CTLCC		FB–FB CTLCC
Operation stages	HB CTLC	FB CTLC	FB CTLCs
Normal operation	Complementary mode	PS	PS
Soft start	IAPWM	shut down	PS

The gate signals and key waveforms of soft start operation of FB–FB CTLCC are shown in Fig. 6(b). The 12 gate signals are divided into six switching groups, which are S_1 and S_7, S_2 and S_8, S_3 and S_9, S_4 and S_{10}, S_5 and S_{11}, and S_6 and S_{12}. The switches in one group share the same gate signal and the output varied with phase angle among these groups. During soft start operation, the phase angle between S_3 and S_6 is 180°, and the output voltage decreases from $V_{\rm in}/k_T$ to 0 by increasing the phase angle between S_3 and S_2. When this angle is 180°, the output voltage is 0. From Fig. 6(b), we can conclude that gate signals of FB–FB CTLCC during soft start operation are still in PS mode. Therefore, FB–FB CTLCC is more convenience for customers due to simpler configuration of control and drive circuit.

IV. TECHNICAL ANALYSIS

A. Voltage Balance Principle of the Input Capacitors

1) FB–FB CTLCC: The initial voltage on each input capacitor in FB–FB CTLCC is $V_{\rm in}/2$ due to the configuration shown in Fig. 2(b). During the operation, the voltage on the input capacitors can be maintained if the integral of current flowing through these capacitors over one switching cycle is zero. As proved in [36], FB CTLC with PS modulation strategy and series-connected secondary coils of power transformers can keep charge balance for all input capacitors naturally. FB–FB CTLCC is composed of two FB CTLCs. As shown in Table I, the modulation strategy of each FB CTLC is in PS mode. The transformer in FB–FB CTLCC contains four primary coils and two common secondary coils, and the common secondary coils can be treated as eight series-connected secondary coils. Thus, FB–FB CTLCC can stable the midpoint voltage of the input capacitors with symmetrical switching sequence. Under usually applications, an added voltage control circuit is not necessary because only a large asymmetrical switching sequence may affect the midpoint voltage of the input capacitors [36].

2) HB–FB CTLCC: The initial voltage on each input capacitor in HB–FB CTLCC is $V_{\rm in}/4$ due to the configuration shown in Fig. 2(a). During the operation, the voltage on the input capacitors can be maintained if the integral of current flowing through these capacitors over one switching cycle is zero. As proved in [7] and [36], FB or HB CTLCs can maintain

TABLE II
GROUPS LIST OF SWITCHES IN THE PROPOSED CONVERTERS

Converter	Leading Switches	Lagging Switches
HB–FB CTLCC	S_3, S_4, S_7, and S_8	S_1, S_2, S_5, and S_6
FB–FB CTLCC	S_5, S_6, S_{11}, and S_{12}	S_1, S_2, S_3, S_4, S_7, S_8, S_9, and S_{10}

the midpoint voltage of the input capacitors with corresponding modulation strategies listed in Table I and series-connected secondary coils of transformers. HB–FB CTLCC is composed of an HB CTLC and an FB CTLC. The modulation strategies of each cell in HB–FB CTLCC are depicted in Table I. The common secondary coils of the transformer in HB–FB CTLCC can also be treated as eight series-connected secondary coils. Therefore, HB–FB CTLCC can also obtain even and stable midpoint voltage of the input capacitors.

B. Reduction of the Output and Input Filters

The reduction of the filters volume with TL secondary rectified voltage waveform has been discussed in several literature works [28], [30]–[32], [44], [45]. According to these studies, the required output inductance of the converters with TL secondary rectified voltage waveform is about one-third of that of conventional two-level converters. Therefore, the output filter in the proposed converters can be significant reduced.

During normal operation, the input current of the proposed converters has smaller ripple, and it is nearly a constant dc current source. Thus, the input filter can also be minimized [30].

C. ZVS Characteristics

According to the switching pattern in Figs. 3 and 5, the switches in the proposed converters can also be concluded into two groups as traditional PS FB dc–dc converter, which are leading switches and lagging switches as illustrated in Table II. ZVS characteristics of the switches in the presented converters are investigated according to the different groups.

1) Turn-On Intervals for the Leading Switches: During this commutation instant, the output inductance together with the leakage inductances of the transformer charges or discharges related intrinsic capacitances of the leading switches, and the energy stored in these inductances is large enough to conduct the antiparallel diodes of the coming switches even at the light load. Therefore, the leading switches can obtain ZVS in wide load range. S_4 in Fig. 2(a) is selected as an example. The switching instant is shown in Fig. 4(b), and the ZVS criteria for S_4 can be represented as

$$\frac{1}{2}L_p'\left(\frac{I_o}{k_T}\right)^2 \geq C_{os}\left(\frac{V_{\text{in}}}{2}\right)^2 \tag{14}$$

where L_p' is equal to $L_{lk2}+k_T^2 L_o$.

The minimum load current to realize ZVS for S_4 is

$$I_{o\min} = k_T V_{\text{in}}\sqrt{\frac{C_{os}}{2(L_{lk2}+k_T^2 L_o)}}. \tag{15}$$

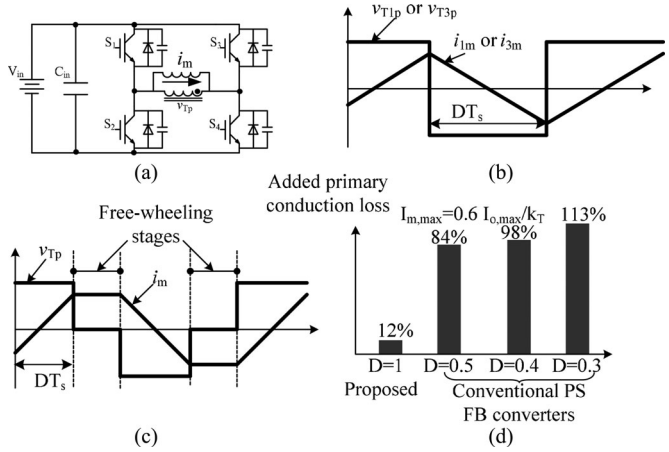

Fig. 7. Magnetizing currents and added primary conduction loss: (a) primary circuit of conventional PS FB dc–dc converter; (b) magnetizing currents of proposed converters; (c) magnetizing current of conventional PS FB dc–dc converter; (d) added primary conduction loss.

2) Turn-On Intervals for the Lagging Switches: In this paper, an HB or FB CTLC is combined with an FB CTLC to obtain TL secondary rectified voltage waveform and enlarge the ZVS load range of the lagging switches. During normal operation, the magnetizing currents of the added HB or FB CTLC are increased to provide more resonant energy for switching commutation among the lagging switches. Fig. 7 shows the magnetizing currents and the added conduction loss of the proposed converters and traditional PS FB dc–dc converter. The primary circuit of traditional PS FB dc–dc converter is shown in Fig. 7(a) and the primary circuits of the proposed converters are in Fig. 2. v_{T1p}, v_{T3p}, and v_{Tp} in Fig. 7 represent the voltages of primary coils of the converters for comparison; i_{1m}, i_{3m}, and i_m represent corresponding magnetizing currents; D in Fig. 7 is the duty ratio of the primary coils. Compared to traditional PS FB dc–dc converter, increasing i_{1m} and i_{3m} in the proposed converters will result less added primary conduction loss and gain more good ZVS characteristics for the lagging switches due to following reasons: First, in the proposed converters, as shown in Fig. 7(b), the average value of i_{1m} and i_{3m} is zero during the half switching period and these currents are not in phase with the load current. Thus, a larger value of i_{1m} and i_{3m} will not cause much added primary RMS current. But, in the traditional PS FB dc–dc converter, as shown in Fig. 7(c), a larger value of i_m will significant increase the primary RMS current and add more conduction loss because this current keeps its peak value during the whole free-wheeling stage [45]. Fig. 7(d) depicts the added conduction loss caused by i_{1m}, i_{3m}, and i_m. $I_{m,\max}$ in Fig. 7(d) is the peak value of i_{1m}, i_{3m}, and i_m, which is set as 60% of the maximum reflected output current $I_{o,\max}/k_T$. As illustrated in Fig. 7(d), the added primary conduction loss in the proposed converters is only 12%. But, the added primary conduction loss in conventional PS FB dc–dc converter is much higher. If D is 0.3, the added primary conduction loss will be 113%. Second, as shown in Fig. 4, i_{1m} and i_{3m} will not flow through the leading switches, which can also reduce the primary

conduction loss. Finally, the peak value of the magnetizing currents of T_{1p} and T_{3p} is increased with input voltage, and more resonant energy can be provided to help the ZVS of the lagging switches. But, in the traditional PS FB dc–dc converter, the peak value of magnetizing current is not varied with the input voltage [45]. Therefore, the proposed converters are expected to have higher efficiency in high input applications compared to the traditional PS FB dc–dc converter.

S_1 in Fig. 2(a) is selected as an example. Fig. 4(d) shows the equivalent circuit of this procedure. When $v_{\rm rect}$ decays to zero, the circuit will be operated in the free-wheeling mode; all the rectifier diodes will conduct, while the load current reflected to the primary-side falls resonantly. Before $v_{\rm rect}$ decays to zero, the voltages applied to T_{1p} and T_{3p} are hold positive and the load current can still be used to charge or discharge corresponding capacitors. It is discussed in Section II, 33% of the final value of the voltage across C_1 has been discharged before $v_{\rm rect}$ decays to zero. Thus, only 67% of the voltage across C_1 needs to be charged. This is an additional advantage of the proposed converters compared to the traditional ZVS PS FB dc–dc converters [45].

In order to achieve ZVS, following equation should be fitted

$$\frac{1}{2}L_{lk2}\left(\frac{I_o}{k_T}\right)^2+\frac{1}{2}L_{lk1}\left(\frac{2I_o}{k_T}+I_m\right)^2\geq 2C_{os}\left(\frac{V_{\rm in}}{3}\right)^2. \tag{16}$$

When the load current is zero, (16) can be simplified as

$$I_m\geq\frac{2V_{\rm in}}{3}\sqrt{\frac{C_{os}}{L_{lk1}}}. \tag{17}$$

The peak to peak value of i_{1m} is

$$\Delta i_{1m}=\frac{V_{\rm in}T_s}{4L_m}=2I_m. \tag{18}$$

Thus, I_m is

$$I_m=\frac{V_{\rm in}T_s}{8L_m}. \tag{19}$$

Substituting (19) into (17) yields

$$L_m\leq\frac{3T_s}{16}\sqrt{\frac{L_{lk1}}{C_{os}}}. \tag{20}$$

Therefore, S_1 can obtain ZVS down to zero load current with a specific value of L_{1m} decided by (20).

3) Minimum ZVS Load Range for all Switches: According to previous discussion, the minimum output current to obtain ZVS for all switches is concluded in Table III.

TABLE III
MINIMUM OUTPUT CURRENT TO OBTAIN ZVS FOR ALL THE SWITCHES

Switches	Minimum Load
S_1 and S_2 in HB–FB; S_5 and S_6 in FB–FB	$I_{\rm omin}=k_{\rm T}V_{\rm in}\sqrt{\frac{C_{os}}{2(L_{lk2}+k_{\rm T}^2L_o)}}$
S_5 and S_6 in HB–FB; S_{11} and S_{12} in FB–FB	$I_{\rm omin}=k_{\rm T}V_{\rm in}\sqrt{\frac{C_{os}}{2(L_{lk4}+k_{\rm T}^2L_o)}}$
S_3 and S_4 in HB–FB; S_1, S_2, S_3, and S_4 in FB–FB	0, $L_{\rm m}\leq\frac{3T_{\rm s}}{16}\sqrt{\frac{L_{\rm lk1}}{C_{os}}}$
S_7 and S_8 in HB–FB; S_7, S_8, S_9, and S_{10} in FB–FB	0, $L_{\rm m}\leq\frac{3T_{\rm s}}{16}\sqrt{\frac{L_{\rm lk3}}{C_{os}}}$

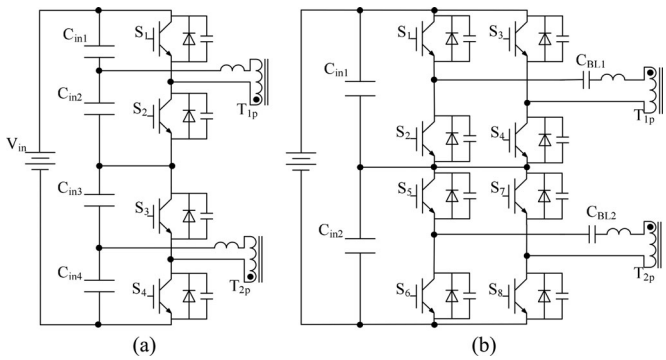

Fig. 8. Primary circuits of CTLCs: (a) HB CTLC; (b) FB CTLC.

D. VA Rating of the Transformer

The VA rating of the transformers in the combined dc–dc converters has been discussed in the paper [28], [31], [45], and a brief review about this problem is provided in this part. Each integrated transformer in the proposed converters can be treated as four independent transformers, and the four transformers are named as T_1–T_4 corresponding to T_{1p}, T_{2p}, T_{3p}, and T_{4p}. The proposed converters can be operated in two modes, i.e., variable input voltage mode and constant input voltage mode. When the proposed converters are operated in variable input voltage mode, T_1 and T_3 will transfer the energy to the load lonely under the maximum input voltage. Therefore, T_1 and T_3 should be designed to be able to deliver the whole power at this situation. With decreasing of the input voltage, the power transferred by T_1 and T_3 to the output reduces, and T_2 and T_4 is involved in the power conversion procedure; thus, T_2 and T_4 should be designed to supply partial output power. So, the total VA rating of the transformers in each proposed converter is slightly higher than that of the conventional TL dc–dc converters with single transformer, and the VA rating of the transformers is [45]

$$\mathrm{VA}_{(T_1+T_2+T_3+T_4)}=V_oI_o\left(2-\frac{V_{\rm inmin}}{V_{\rm inmax}}\right). \tag{21}$$

In the constant input voltage mode, the four transformers share the output power evenly. Thus, the total VA rating of transformers in each proposed converter equals that of the conventional TL dc–dc converters with single transformer.

E. Comparison

1) Comparison Among CTLCCs and Traditional CTLCs: The primary circuits of the converters for comparison are provided in Figs. 2 and 8 and. Table IV illustrates the components number comparison, and the current and VA ratings comparison of primary components are provided in Fig. 9. As depicted in Table IV, the number of main power switches in the FB–FB CTLCC is highest among the four converters. But, as illustrated in Fig. 9(a), the total current rating of main switches in each

TABLE IV
COMPONENTS COMPARISON AMONG THE PROPOSED CONVERTERS AND CTLCS

	Items					
				VA rating of transformers		
Converter	Switch no.	Input capacitor no.	Blocking capacitor no.	Constant input	Variable input	Output inductor value (compared to FB TLCC)
HB–FB CTLCC	8	4	2	$V_o I_o$	Decided by (21)	0.33
FB–FB CTLCC	12	2	4	$V_o I_o$	Decided by (21)	0.33
FB CTLC	8	2	2	$V_o I_o$	$V_o I_o$	1
HB CTLC	4	4	2	$V_o I_o$	$V_o I_o$	1

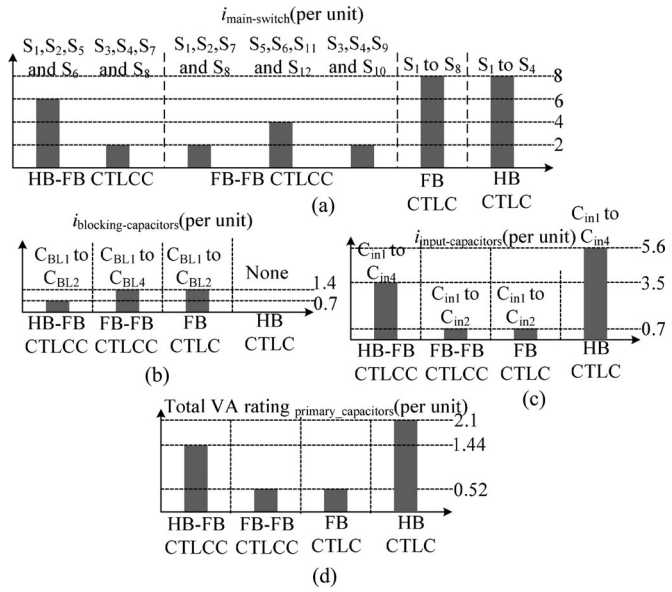

Fig. 9. Primary components comparison among the proposed converters and CTLCs: (a) current rating of main switches; (b) current rating of blocking capacitors; (c) current rating of input capacitors; (d) VA rating of primary capacitors.

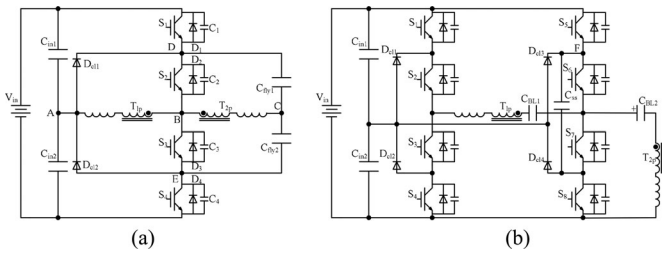

Fig. 10. Primary circuits of TLCCs: (a) Diode clamped HB TLCC. (b) Diode clamped FB TLCC.

circuit is identical. Therefore, the required semiconductor area of main switches in these four topologies is identical. But, the proposed converters are not suitable for small power dc–dc conversion because several extra power switches are required. As proved in Fig. 9(b), the HB–FB CTLCC has smaller current rating of the blocking capacitors compared to FB–FB CTLCC and the converter in Fig. 8(b). As proved in Fig. 9(c), the input capacitors in HB CTLC sustain the highest current stress. The voltage rating of primary capacitors is provided in Table V. As shown in Table V, the voltage rating of the input capacitors in HB–FB CTLCC and HB CTLC is uneven due to IAPWM modulation strategy. HB CTLC is selected as an example to explain the reason. When the duty ratios of HB cells in HB CTLC are 0.5, the four input capacitors share the input voltage evenly and the per unit value is 0.25; when the duty ratios equal 0 or 1, two of the four capacitors share the input voltage evenly and the per unit value is 0.5, while the voltage on other two capacitors is 0. Thus, as shown in Table V, the voltage rating of $C_{\rm in1}$ and $C_{\rm in3}$ is 0.5 per unit, and the voltage rating of $C_{\rm in2}$ and $C_{\rm in4}$ is 0.25 per unit. Total VA rating of primary capacitors can be roughly estimated by Fig. 9(b) and (c) and Table V. As proved in Fig. 9(d), the overall VA rating of primary capacitors in HB CTLC is highest among the four converters. The proposed converters still have compact primary power circuit. Just as HB or FB CTLCs, only one wire between the midpoint of the input capacitors and switching pairs of CTLCCs is required to fabricate TL structure. Thus, CTLCCs also have the merits belonging to traditional CTLCs, i.e., simple and compact circuit layout, modular structure of the power circuit.

According to Table IV, the VA rating of power transformers in CTLCs is smaller in variable input voltage and constant output voltage applications. When the input voltage range is 2:1, the total VA rating is about 0.67 times compared to that of the proposed converters. But, in the constant input voltage and variable output voltage applications, the four circuits have the same VA rating of the transformers. The output inductance of the proposed converters is about one-third of that of CTLCs due to TL voltage waveform before the output filter. Thus, the overall magnetic component volume of the proposed converters is not obviously larger than CTLCs.

The performance comparison is provided in Table VI. As shown in Table VI, the ZVS load range of the lagging switches in the proposed converters is enlarged by increasing the magnetizing currents of $\rm T_{1p}$ and $\rm T_{3p}$. Increasing i_{1m} and i_{3m} can provide enough resonant energy for the lagging switches under light-load or high input voltage condition. Therefore, the light-load or high input efficiency of the proposed converters is higher. Furthermore, the possible system dynamic response of CTLCs is slower compared to others due to larger output inductance.

2) Comparison Among CTLCCs and Other TLCCs: The proposed converters are also compared with two diode clamped TLCCs in this part, and the primary circuits of the converters for comparison are provided in Figs. 2 and 10 [28], [32]. The

TABLE V
VOLTAGE RATING OF PRIMARY CAPACITORS OF THE PROPOSED CONVERTERS AND CTLCS (PER UNIT)

Converter	$C_{\mathrm{in}1}$	$C_{\mathrm{in}2}$	$C_{\mathrm{in}3}$	$C_{\mathrm{in}4}$	$C_{\mathrm{BL}1}$	$C_{\mathrm{BL}2}$	$C_{\mathrm{BL}3}$	$C_{\mathrm{BL}4}$
HB–FB CTLCC	0.5	0.25	0.5	0.25	None	0.125	None	0.125
FB–FB CTLCC	0.5	0.5	None	None	0.125	0.125	0.125	0.125
HB CTLC	0.5	0.25	0.5	0.25	None	None	None	None
FB CTLC	0.5	0.5	None	None	0.125	0.125	None	None

TABLE VI
PERFORMANCE COMPARISON AMONG THE PROPOSED CONVERTERS AND CTLCS

	Items			
			Soft switching characteristic	
Converter	Controlling strategy	System dynamic	Leading switches	Lagging switches
HB–FB CTLCC	PS+ IAPWM	Fast	ZVS, normal	ZVS, (down to no load)
FB–FB CTLCC	PS	Fast	ZVS, normal	ZVS, (down to no load)
HB CTLC	PS	slow	ZVS, normal	ZVS, hard
FB CTLC	IAPWM	slow	ZVS, normal	ZVS, hard

TABLE VII
COMPONENTS COMPARISON AMONG THE PROPOSED CONVERTERS AND TLCCS

	Items				
Converter	Switch no.	Clamping diode no.	Flying capacitor no.	Blocking capacitor no.	Input capacitor no.
HB–FB CTLCC	8	0	0	2	4
FB–FB CTLCC	12	0	0	4	2
Fig. 10(a)	4	2	2	0	2
Fig. 10(b)	8	4	3	1	2

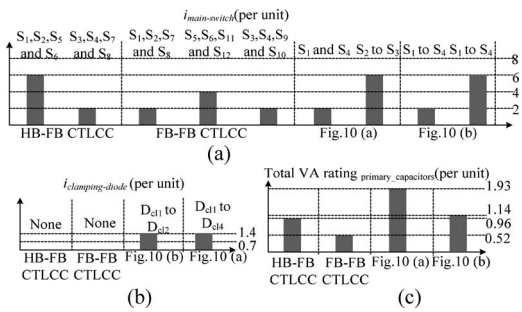

Fig. 11. Primary components comparison among CTLCCs and the converters in Fig. 10: (a) current stress of main switches; (b) current stress of clamping diodes; (c) VA rating of primary capacitors.

basic performance and soft switching characteristics of these four topologies are quite similar. Table VII illustrates the component comparison among the four converters and Fig. 11 provides the current and VA rating comparison of primary components. As shown in Fig. 2, the proposed converters can balance the voltage of main switches without added primary clamping devices. Only one more wire between the midpoint of the input capacitors and switching pairs is required to fabricate the TL structure. Therefore, the primary structure of the proposed converters is more compact among the four converters, which may be the most attractive feature to industry applications. Furthermore, off voltage of the switches in the proposed converters is directly clamped by the input capacitors, and these capacitors can absorb more resonant energy stored in the parasitic inductances, which means the switches can be kept in the safe operating area even under fast dynamic transition instant. As illustrated in Table VII, the converter in Fig. 10(a) has the minimum number of main switches. But, as depicted in Fig. 11(a), the total current stress of main switches in the four converters is identical. Thus, the required semiconductor chip area of main switches in the proposed converters equals that of other two circuits for comparison. As shown in Fig. 11(b), the total current stress of clamping diodes of the converters in Fig. 10 is about 1.4 per unit because the primary currents flow through these clamping diodes during free-wheeling stages. From Table VII and Fig. 11(a) and (b), we can conclude that the overall required primary semiconductor chip area of the proposed converters is smaller than that of the converters in Fig. 10. From Fig. 11(c), we can conclude that the total VA rating of primary capacitors in Fig. 10(a) is the highest among the four converters, which may be another drawback of the converter in Fig. 10(a). Finally, the proposed converters can be extended to higher voltage level easily due to the modular structure.

V. EXPERIMENTAL RESULTS

The basic operation principles of the proposed converters are verified in this section. The efficiency test is carried out among the converters in Figs. 2, 8(b), and 10(a). The main parameters of the prototypes are shown in Table VIII. k_{Tip} in Table VIII represents turn ratios of different primary coils in each circuit. The current ripple of output inductors in the prototypes is identical; thus, the required output inductance of the converter in Figs. 2 and 10(a) is much smaller than that of the converter in Fig. 8(b). The prototype photo of HB–FB CTLCC is provided in Fig. 12.

TABLE VIII
MAIN PARAMETERS OF THE PROTOTYPES

Common parameters	
Input voltage	600 V–800 V
Output voltage	48 V
Output current	200 A
Switching frequency	20 kHz
IGBT	75 A/600 V
Rectifier Diodes	400 A/400 V
C_o	1000 μF
Special for HB–FB CTLCC	
$2k_{T1p} = 2k_{T3p} = k_{T2p} = k_{T4p} = k_T$	20:1
L_o	7 μH
Special for FB–FB CTLCC	
$k_{T1p} = k_{T2p} = k_{T3p} = k_{T4p} = k_T$	20:1
L_o	7 μH
Special for FB CTLC	
$k_{T1p} = k_{T2p} = k_T$	10:1
L_o	20 μH
Special for the converter in Fig. 10(a)	
$k_{T1p} = 2k_{T2p} = k_T$	10:1
L_o	7 μH

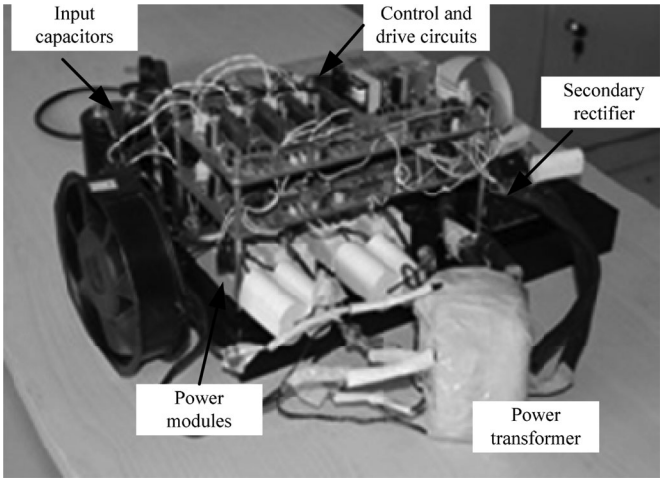

Fig. 12. Prototype of HB–FB CTLCC.

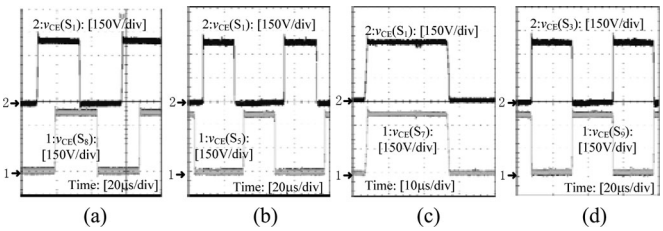

Fig. 13. Off-state voltage of the switches: (a) normal operation of HB–FB CTLCC; (b) soft start transition of HB–FB CTLCC; (c) normal operation of FB–FB CTLCC; (d) soft start transition of FB–FB CTLCC.

Fig. 13 shows the off-state voltages on the switches of the proposed converters, and $v_{ce}(S_i)$ in Fig. 13 represents the collector–emitter voltages of corresponding switches. As shown in Fig. 13(a), the off-state voltage of switches in HB–FB CTLCC is even during normal operation stages, and the midpoint voltage of the input capacitors is stable and equals $V_{\rm in}/2$. HB–FB CTLCC cannot be soft started from zero in PS mode; thus, the duty ratio of $v_{ce}(S_1)$ and $v_{ce}(S_5)$ in Fig. 13(b) is not 50%. As suggested in Fig. 13(b), the off-state voltages of the switches and midpoint voltage of the input capacitors in HB–FB CTLCC are balanced during soft start transition. Fig. 13(c) and (d) proves that the blocking voltage of switches and the midpoint voltage of the input capacitors in FB–FB CTLCC are also balanced during normal and soft start operation.

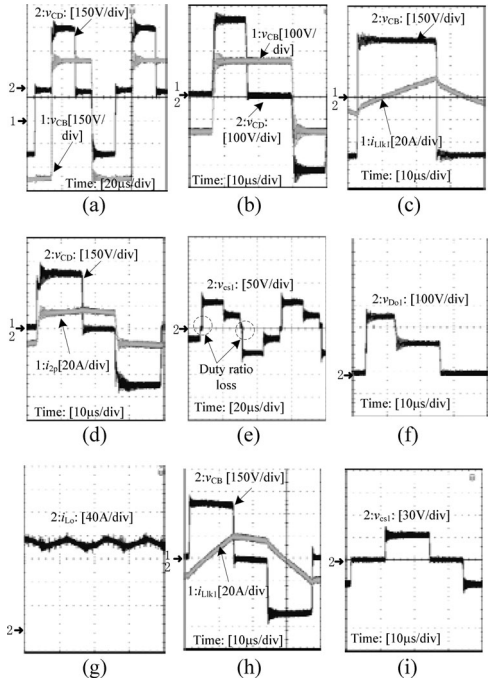

Fig. 14. Waveforms of the proposed converters: (a) $v_{\rm CB}$ and $v_{\rm CD}$ of FB–FB; (b) $v_{\rm CB}$ and $v_{\rm CD}$ of HB–FB; (c) i_{Llk1} and $v_{\rm CB}$ of FB–FB; (d) i_{2p} and $v_{\rm CD}$ of FB–FB; (e) $v_{\rm CS1}$ of FB–FB; (f) v_{Do1} of FB–FB; (g) i_{Lo} of FB–FB; (h) $v_{\rm CB}$ and i_{Llk1} of FB–FB during soft start; (i) $v_{\rm CS1}$ of FB–FB during soft start.

The basic operation principles of the proposed converters are illustrated in Fig. 14. The waveforms of HB–FB CTLCC are similar to FB–FB CTLCC except the primary coils voltage waveform. So, the key waveforms of FB–FB CTLCC are provided in Fig. 14, and only the primary coils voltage waveforms of HB–FB CTLCC are shown in Fig. 14(b) for simplicity. As shown in Fig. 14(a), the voltage applied to each primary coil of FB–FB CTLCC is $V_{\rm in}/2$. As shown in Fig. 14(b), one primary coil of HB–FB CTLCC sustains $V_{\rm in}/2$ and another sustains only $V_{\rm in}/4$.

As shown in Fig. 14(c), i_{Llk1} is not a constant value during power transfer stages because the magnetizing current is enlarged to help ZVS of the lagging switches. As the magnetizing current is not in phase with load current, the added primary RMS current is smaller. Thus, the added conduction loss is also smaller. The duty ratio of $\rm T_{1p}$ is 100% and uncontrolled during the whole operation stages, which means this coil together with $\rm T_{3p}$ will transfer whole output power under maximum input and rated output power condition. As depicted in Fig. 14(d), i_{2p} keeps constant during power delivery and free-wheeling stages, and $v_{\rm CD}$ is $V_{\rm in}/2k_T$ during power delivery stage and equals

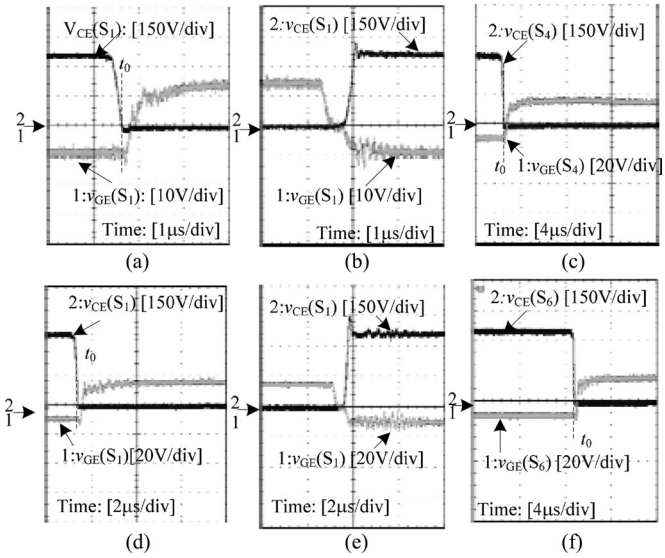

Fig. 15. ZVS characteristics with 10% load current: (a) $v_{\mathrm{GE}}(\mathrm{S}_1)$ and $v_{\mathrm{CE}}(\mathrm{S}_1)$ of HB–FB at turn-on instant; (b) $v_{\mathrm{GE}}(\mathrm{S}_1)$ and $v_{\mathrm{CE}}(\mathrm{S}_1)$ of HB–FB at turn-off instant; (c) $v_{\mathrm{GE}}(\mathrm{S}_4)$ and $v_{\mathrm{CE}}(\mathrm{S}_4)$ of HB–FB at turn-on instant; (d) $v_{\mathrm{GE}}(\mathrm{S}_1)$ and $v_{\mathrm{CE}}(\mathrm{S}_1)$ of FB–FB at turn-on instant; (e) $v_{\mathrm{GE}}(\mathrm{S}_1)$ and $v_{\mathrm{CE}}(\mathrm{S}_1)$ of FB–FB at turn-off instant; (f) $v_{\mathrm{GE}}(\mathrm{S}_6)$ and $v_{\mathrm{CE}}(\mathrm{S}_6)$ of FB–FB at turn-on instant.

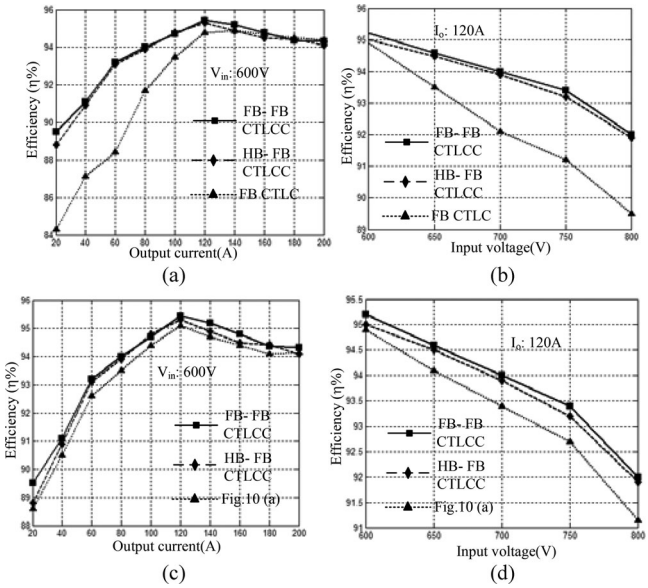

Fig. 16. Efficiency comparison: (a) compared to FB CTLC (variable output current); (b) compared to FB CTLC (variable input voltage); (c) compared to the converter in Fig. 10(a) (variable output current); (d) compared to the converter in Fig. 10(a) (variable input voltage).

zero during free-wheeling stage. The output voltage is adjusted by changing the time of free-wheeling stages. But the input current cannot decrease to zero during the free-wheeling stages because two of the four primary coils have no free-wheeling time. Therefore, the input current ripple is much smaller than traditional CTLCs. The secondary coil voltage is provided in Fig. 14(e). The zero value marked by dash circles in Fig. 14(e) is the duty ratio loss, and the time of the duty ratio loss will be enlarged with increasing of load current. The voltage on rectifier diode and the current of output inductor is provided in Fig. 14(f) and (g), respectively. The soft start waveform of FB–FB CTLCC is provided in Fig. 14(h) and (i). At this operation mode, the primary current keeps its maximum value during the free-wheeling stages; thus, the added conduction loss is larger than normal operation stages.

The ZVS characteristics of the switches in the proposed converters are tested with 10% load current. The waveforms of the gate signals and the collector–emitter voltages of the lagging switch S_1 and leading switch S_4 in HB–FB CTLCC are depicted in Fig. 15(a)–(c), and t_0 in Fig. 15(a) and (c) represents the instant when the voltage on corresponding switch decays to zero. As shown in Fig. 15(a), the gate–emitter voltage of S_1 is much lower than gate–emitter threshold voltage when the collector–emitter voltage of S_1 decreases to zero; thus, S_1 can obtain ZVS. According to Fig. 15(b), the voltage on the S_1 increases from zero to final voltage after the gate signal decreases to zero, so the turn-off loss of S_1 can also be minimized. As shown in Fig. 15(c), S_4 can obtain ZVS in wide load range. The waveforms of the gate signals and the collector–emitter voltages of the lagging switch S_1 and leading switch S_6 in FB–FB CTLCC are shown in Fig. 15(d), (e) and (f). According to Fig. 15(d)–(f), S_6 and S_1 in FB–FB CTLCC can also obtain ZVS in wide load range.

TABLE IX
VOLUME COMPARISON OF THE TRANSFORMERS AND FILTERS

Item	FB–FB CTLCC		FB CTLC
	Variable input	Constant input	
Transformer	3250 cm^3	2428 cm^3	2437 cm^3
output inductor	473 cm^3	473 cm^3	1576 cm^3
input filter	604 cm^3	604 cm^3	1089 cm^3
Overall	4327 cm^3	3505 cm^3	5102 cm^3

During the efficiency test, the converters in Figs. 8(b) and 10(a) are also tested for comparison. Fig. 16(a) shows the efficiency comparison among the proposed converters and FB CTLC under different load current with the 600-V input voltage. As all the switches can obtain ZVS in wide load range, the proposed converters have higher efficiency at the light-load zone. The efficiency comparison among the proposed converters and FB CTLC under different input voltage with a constant load is provided in Fig. 16(b), and the efficiency of all the converters decreases with increasing of input voltage. As the lagging switches can obtain more resonant energy, the proposed converters have higher efficiency under high input condition. As shown in Fig. 16(c) and (d), the efficiency of the converter in Fig. 10(a) are slightly smaller than the proposed converters.

Table IX shows the volume comparison of the transformers and filters between the converters in Figs. 2(b) and 8(b). The comparison is made under following assumptions: output voltage is 48 V, and output current is 200 A; switching frequency is set to be 20 kHz; both transformers and inductors are fabricated by nanocrystalline magnetic material; the current

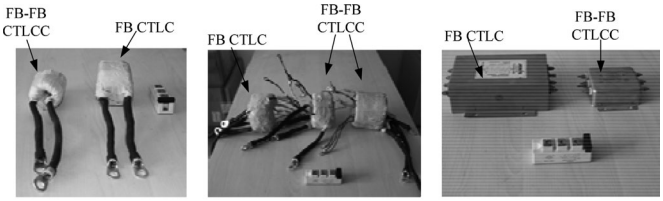

Fig. 17. Transformers and filters used in prototypes: (a) output inductors; (b) transformers; (c) input filters.

ripple is selected as $0.2I_o$. From Table IX, we can conclude that the overall magnetic component volume of FB–FB CTLCC is smaller than that of FB CTLC. The photos of these components are provided in Fig. 17.

VI. Conclusion

Two new soft switching CTLCCs with reduced filters size and wide ZVS load range are proposed. The operation principles and characteristics of the presented converters are discussed. Experimental results are agreed with theoretical predictions properly. After discussion, following conclusions can be derived:

1) all switches can obtain ZVS in wide load range;
2) secondary rectified voltage is a TL waveform, which can significant reduce the input and output filters;
3) proposed converters can be extended to higher voltage rating applications easily due to modular structure;
4) proposed converters are not suitable for small power dc–dc applications due to several extra primary switches are required.

The main drawback of the proposed converters is that the VA rating of the transformers is larger than other TL topologies with one transformer in variable input and constant output applications.

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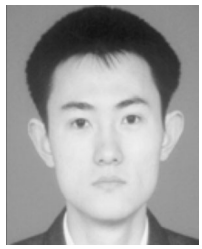

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