Power Control of Asymmetrical Frequency Modulation in a Full-Bridge Series Resonant Inverter

Jingang Hu, Chuang Bi, Kelin Jia, and Yong Xiang

***Abstract*—The traditional power control schemes for induction heating device mainly focus on the pulse frequency modulation (PFM) and the pulse density modulation. But they cannot solve the problems of power control, efficiency, and load-adaption well. This paper presents and analyzes the asymmetrical frequency modulation (AFM) control scheme used in the full-bridge series resonant inverter. With the proposed AFM control technique, the output power is controlled by two variables: the operation frequency and the division factor. Better efficiency performance can be achieved in the medium and low output power range when compared with PFM. The principles as well as the zero-voltage switching condition of the AFM are explained and the power losses of switches are analyzed. A control algorithm that schedules the three control modes of AFM is experimentally verified with a digital signal processor based induction heating prototype. The load-adaption, noise and thermal distribution problem of switches are also analyzed.**

***Index Terms*—Asymmetrical frequency modulation (AFM), digital control, induction heating (IH), power control, series resonant inverter.**

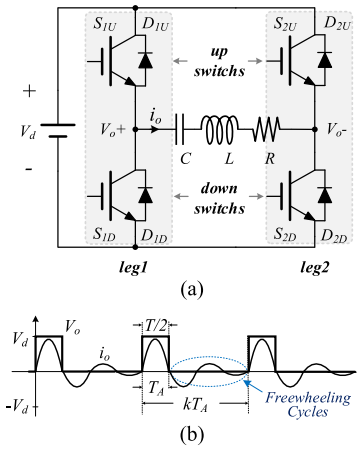

Fig. 1. (a) Schematic of Class-D voltage-source full-bridge resonant inverter. (b) Nonregular PDM waveforms.

I. Introduction

With the remarkable development of the power semiconductor devices and microprocessors, the digitally controlled induction heating (IH) devices are increasingly being used in industry process, home appliance, and other areas [1]. The voltage-source full-bridge resonant inverter which consists of two legs (*leg1* and *leg2* with their up switches and down switches), as shown in Fig. 1(a), allows more control possibilities and power extensions.

Several power control strategies have been proposed to achieve high efficiency and wide power range control, besides, user performance is also a concern in some specific appliances [2]. Power control by varying the switching frequency in PFM [3]–[6] can achieve continuous output power and zero-voltage switching (ZVS) by above resonant frequency operation [7], [8]. However, the inverter performs poor electromagnetic interference [5], [9] and lower efficiency at low-medium output power levels due to the higher switching frequency.

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The fixed-frequency modulations, such as phase-shift (PS) control [10], [11] and asymmetrical duty cycle [12], [13], are proposed to realize simple power control, but they cannot guarantee soft-switching operation for wide output power variations [14].

Pulse density modulation (PDM) [15]–[17] is another fixed-frequency control technique, which covers the complete power range with high efficiency. In [18], the regular PDM and nonregular PDM are distinguished by the minimum length of freewheeling cycles [see Fig. 1(b)]. That is, in the nonregular PDM, both the freewheeling cycles and the active resonance ($V_o = \pm V_d$) are integer multiple of half a switching period ($T/2$), instead of integer multiple of switching period (T) in the regular PDM. Both the two PDM modes face the problem of discontinuous output current in the light-load condition. In addition, small PDM length will lead to discrete or poor resolution control of the output power. The asymmetrical pulse density modulation method proposed in [19] is to achieve the nonregular PDM power control, and is aimed to bring less fluctuation of the output current than the regular PDM in the small PDM length case; however, power control is not referred to. Large PDM length is required to have continuous or fine resolution of the transmitted power [18], [20]; however, it is conflicted with the requirements for continuous output current. Flicker emission problem also arises as the PDM length becomes large enough [2]. In addition, PDM control is also faced with acoustic noise problem if the PDM pattern period is within audible range (20 Hz up to 20 kHz) [21].

The aim of this paper is to present a narrow frequency-range control technique which is named asymmetrical frequency

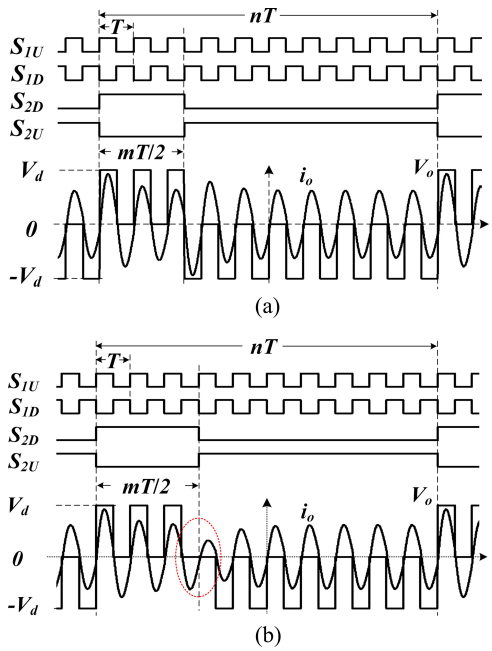

Fig. 2. AFM diagrammatic waveforms. (a) *m* is odd number. (b) *m* is even number (with adjacent freewheeling cycles).

modulation (AFM). The complete power range is segmented into three piecewise ranges by AFM, and within each range the output power is controlled by varying switching frequency near the resonant frequency. Continuous output power and resonant current as well as high efficiency is therefore achieved even low quality factor load is used. A control algorithm that applied to the AFM is discussed, and is implemented with a 4.5 kW, 30–42 kHz, domestic IH appliance with low quality factor load.

This paper is organized as follows. In Section II, AFM is introduced with its characteristics of power range, ZVS, and efficiency. Section III gives a brief explanation of the modulation strategy with its digital implementation. Section IV introduces the experimental results and efficiency performance. In Section V, the extra work to be done to improve the performance of the proposed power control strategy is briefly outlined, and comparison with PFM and PDM is given. Finally, the main conclusions are presented in Section VI.

II. AFM

A. AFM Description

For the full-bridge typology displayed in Fig. 1(a), the corresponding driving signals, the output voltage V_o, and the output current i_o for the proposed AFM control technique is displayed in Fig. 2. The two switches S_{1U} and S_{1D} in *leg1* are complementarily operated with the switching frequency f_s ($f_s = 1/T$) and the 50% duty cycle as usual. While for the two complementarily operated S_{2U} and S_{2D} in *leg2*, the switching period is integer multiples (*n* is division factor) of that of *leg1*, and the switching on operation of S_{1U} and S_{2D} occurs simultaneously. The switching on time of S_{2D} is integer multiples (*m*) of *T*/2. Fig. 2(a) and (b) shows the output voltage and its driving signals when *m* is odd and even, respectively.

TABLE I
OUTPUT VOLTAGE V_o VERSUS THE STATES OF THE SWITCHES

V_o	S_{1U} (ON)	S_{1D} (ON)
S_{2U} (ON)	0	$-V_d$
S_{2D} (ON)	V_d	0

The control technique defined by Fig. 2 is named the AFM. The output voltage V_o is determined by three control variables at most: the division factor (*n*), the duty cycle of *leg2* (*m*/2*n*), and the switching frequency ($f_s = 1/T$). The output voltage V_o repeats active resonance ($V_o = \pm V_d$) and freewheeling ($V_o = 0$) which is determined by the states of the switches, as is outlined in Table I.

The time variation in steady state of the output voltage V_o can be expanded by the following Fourier series:

$$V_o(t) = \frac{m-n}{2n}V_d + \sum_{h=1}^{\infty} V_{oh} \sin\left(h\frac{\omega_s}{n}t + \varphi_h\right) \tag{1}$$

where V_d is the dc input voltage, *h* is the harmonic number, and $\omega_s = 2\pi/T$ is the angular switching frequency of *leg1*. The amplitude and phase of the *h*th harmonic of V_o are denoted as V_{oh} and φ_h, respectively

$$V_{oh} = \frac{V_d}{h\pi}\sqrt{a_h^2 + b_h^2} \tag{2}$$

$$\varphi_h = \tan^{-1}\frac{a_h}{b_h} \tag{3}$$

where $a_h = \sin\frac{hm\pi}{n}$, $b_h = \sum_{i=0}^{2n}(-1)^i \cos\frac{hi\pi}{n} - \cos\frac{hm\pi}{n}$.

The input impedance of the resonant tank circuit corresponding to the *h*th harmonic is given by

$$Z_h = R + j\left(h\frac{\omega_s}{n}L - \frac{n}{h\omega_s C}\right). \tag{4}$$

The *h*th harmonic of output current i_{oh} is denoted as

$$i_{oh}(t) = I_h \sin\left(h\frac{\omega_s}{n}t + \varphi_h - \emptyset_h\right) \tag{5}$$

and I_h is the amplitude of the *h*th harmonic output current

$$I_h = \frac{V_{oh}}{|Z_h|} \tag{6}$$

where $|Z_h| = R\sqrt{1 + Q^2\left(h\frac{\omega_n}{n} - \frac{n}{h\omega_n}\right)^2}$, Q is quality factor of load, and ω_n is the normalized switching frequency which is defined as follows:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}},\ \omega_n = \frac{\omega_s}{\omega_0},\ \omega_0 = \frac{1}{\sqrt{LC}} \tag{7}$$

with ω_0 being the angular resonant frequency.

The phase lag ϕ_h between the *h*th harmonic voltage and the corresponding current i_{oh} can be obtained as

$$\emptyset_h = \tan^{-1}\frac{h\frac{\omega_s}{n}L - \frac{n}{h\omega_s C}}{R} = \tan^{-1}\left(Q\left(\frac{h\omega_n}{n} - \frac{n}{h\omega_n}\right)\right). \tag{8}$$

For the even number m ($n \geq 2$) in Fig. 2(b), there are two adjacent freewheeling cycles ($2^*T/2$) distributed in both sides of switching on process of S_{2U}. For an above resonance frequency operation, the ZVS condition of S_{2U} will be lost because the lagged output current i_o can only discharge one of the up switches. In addition, too many freewheeling cycles may lead to the discontinuous resonant current when a low quality factor load is used. So m is set to be an odd number to avoid adjacent freewheeling cycles [see Fig. 2(a)].

B. AFM Power Analysis (m Is Odd Number)

The average output power P can be obtained as

$$P = \sum_{h=1}^{\infty} R\left(\frac{I_h}{\sqrt{2}}\right)^2 = \sum_{h=1}^{\infty} \frac{V_{oh}^2}{2R\left(1+Q^2\left(h\frac{\omega_n}{n} - \frac{n}{h\omega_n}\right)^2\right)}. \tag{9}$$

The resonant tank behaves the minimal impedance when the harmonic frequency equals the resonant frequency ($h = n$); in addition, the harmonic amplitude V_{oh} behaves the maximum value when $h = n$, too. Assuming that the power delivered by the nonresonant frequency harmonics ($h \neq n$) can be neglected, the expression (9) can be simplified as

$$P(n,\omega_n) = \frac{2V_d^2\,(n+1)^2}{n^2\pi^2 R\left(1+Q^2\left(\omega_n - \frac{1}{\omega_n}\right)^2\right)}. \tag{10}$$

This assumption provides an accurate analysis when the switching frequency is close to the resonant frequency of the tank.

The delivered power P in expression (10) is determined by two control variables of AFM(n, ω_n): the division factor n and the normalized switching frequency ω_n. In order to analyze the delivered power versus n separately, ω_n is set to be 1. Thus, the output power $P(n, 1)$ in expression (10) can be expressed as

$$P(n,1) = \frac{2V_d^2}{\pi^2 R}\left(1+\frac{1}{n}\right)^2. \tag{11}$$

The maximum output power ($P_{\max}$) that the inverter can deliver based on the square-wave modulation method is obtained when $n = 1$ that

$$P_{\max} = P(1,1) = \frac{8V_d^2}{\pi^2 R}. \tag{12}$$

The normalized output power P_n (n, 1) is defined as

$$P_n(n,1) = \frac{P(n,1)}{P_{\max}} = \frac{1}{4}\left(1+\frac{1}{n}\right)^2. \tag{13}$$

Fig. 3 shows the delivered power of AFM at resonant frequency with different division factors, the whole power range ($0 \sim P_{\max}$) is segmented into several minor ranges with different value of n, where, during each range, narrow operating frequency range should be guaranteed, and the acoustic noise problem and the control complexity are considered in the selection of number and value of n.

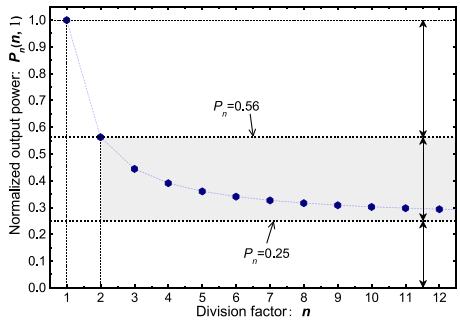

Fig. 3. AFM normalized power versus the division factor n.

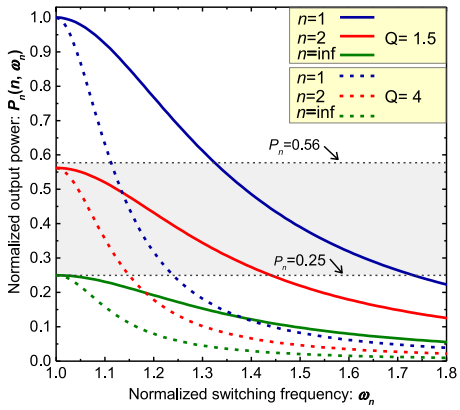

Fig. 4. Normalized output power versus normalized switching frequency.

The fundamental harmonic of resonant current i_o is determined by the operation frequency of *leg2*, which is a division of switching frequency f_s by n. In order to avoid the acoustic noise, the switching frequency f_s is restricted by [21]:

$$f_s/n > 20\,\text{kHz} \quad \text{or} \quad f_s/n < 20\,\text{Hz}.$$

Thus, n shall be large enough or small enough to leave enough frequency bandwidth for the inverter load.

Considering all the constraints, the appropriate value of n is chosen to be $n = 1$, $n = 2$, and $n \to +\infty$, and their corresponding normalized output power versus switching frequency is expressed as

$$P_n(1,\omega_n) = \frac{1}{1+Q^2\left(\omega_n - \frac{1}{\omega_n}\right)^2} \tag{14}$$

$$P_n(2,\omega_n) = \frac{9}{16\left(1+Q^2\left(\omega_n - \frac{1}{\omega_n}\right)^2\right)} \tag{15}$$

$$P_n(+\infty,\omega_n) = \frac{1}{4\left(1+Q^2\left(\omega_n - \frac{1}{\omega_n}\right)^2\right)}. \tag{16}$$

Fig. 4 shows the normalized output power P_n from (14) to (16) as a function of the normalized switching frequency ω_n. To achieve the narrow frequency range control, $P(1, \omega_n)$ is used

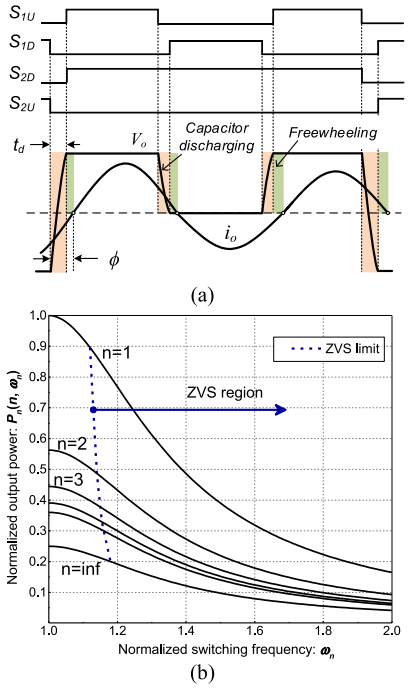

Fig. 5. (a) ZVS waveforms, (b) ZVS region with C_s being 9.4 nF and Q being 1.4 for different division factor.

to control the high power range ($0.56 < P_n < 1$) instead of the whole power range ($0 < P_n < 1$), which is traditionally controlled by PFM. $P(2, \omega_n)$ is used to regulate the medium output power range ($0.25 < P_n < 0.56$).

For the situation when $n \to +\infty$, one switch in *leg2* is kept ON and the other is kept OFF, while *leg1* works at the switching frequency f_s, which makes the inverter perform the behavior of half-bridge mode (HBM). The delivered power is therefore lower than 0.25 $P_{\max}$.

C. ZVS Implementation

ZVS operation is commonly pursued in all active devices to obtain good efficiency results [22]. The previous analysis assumes that the snubber circuit and the dead time are negligible. However, power transistors have intrinsic output capacitances and besides, the lossless snubber circuit is usually used to reduce *dv*/*dt* and spike voltage at the turn off [23]. In this design, snubbing capacitors ($C_{1U} = C_{1D} = C_{2U} = C_{2D} = C_s$) connected in parallel with each IGBT are used as snubber circuits.

For each IGBT, ZVS operation is achieved if its paralleled capacitors are fully discharged (followed by diode freewheeling) before the resonant current crosses zero. Fig. 5(a) shows that the blank time t_d is added to the driving signals to allow the typical capacitors discharging processes for AFM ($n = 2$) within one switching period. A laggard resonant current is required which can be achieved by increasing the switching frequency. The minimum phase difference $\phi_{\min}$ between V_o and i_o to guarantee ZVS operation is obtained when the freewheeling time equals zero [24]

$$t_d = \frac{\emptyset_{\min}}{\omega_0} = \frac{1}{\omega_0}\cos^{-1}\left(1 - \frac{2\omega_0 C_s V_d}{I_m}\right) \tag{17}$$

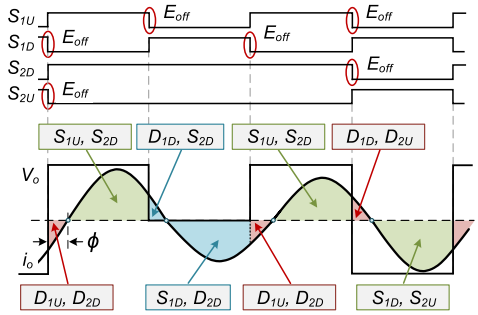

Fig. 6. Distribution of power loss in the inverter.

where I_m represents the peak current at resonant frequency ($\omega_n = 1$), which is different based on the division factor n. It can be concluded from (6) that

$$I_m = \begin{cases} \frac{4V_d}{\pi R} & \text{for } n = 1 \\ \frac{3V_d}{\pi R} & \text{for } n = 2 \\ \frac{2V_d}{\pi R} & \text{for } n \to \infty. \end{cases} \tag{18}$$

The power control curves and the ZVS region with different division factor for $Q = 1.4$ are outlined in Fig. 5(b). It is shown that the ZVS region is dependent on the frequency and the division factor. With the three modes all implemented in the inverter, the blank time t_d is obtained at the situation of $n \to +\infty$ to guarantee fully ZVS operation universally.

D. Power Loss Analysis

Efficiency is a key design parameter of the proposed inverter and, consequently, a detailed power loss analysis is performed in this section. Assuming lossless passive components, power losses in the converter can be divided into two terms: conduction and switching losses [12], [25]. Both of them are caused by the nonidealities in the switching devices: nonzero switching times and nonzero on resistance. As a result, switching waveforms in the inverter have a direct impact on the entire inverter losses.

1) Conduction Losses: Conduction losses can be calculated using the average I_{avg} and root mean square I_{rms} current values through the devices [4], [26]. Since a bidirectional switch is used, there are two components in each switch to compute the conduction losses: the IGBT ($P_{\text{ON,IGBT}}$) and the antiparallel diode ($P_{\text{ON,DIODE}}$). The instantaneous current waveform [i_o for AFM (2, f_s)] through the IGBTs and diodes can be outlined in Fig. 6. As the full-bridge inverter, two semiconductor devices in series with the resonant circuit are used as the current-carrying routes. In a general way, the average on-state losses in a switching period T can be expressed as

$$P_{\text{on}} = 2(I_{\text{avg}} V_{\text{on}} + I_{\text{rms}}^2 R_{\text{on}}) \tag{19}$$

where V_{on} and R_{on} are the collector-to-emitter saturation voltage and the on-state resistance, respectively. The block is composed of the switching device, the antiparallel diode, and the snubber capacitance that conduct the entire load current. The snubber charge/discharge times are neglected ($t_{\text{snb}} \ll T$), and the on-state voltage drop and resistance for the IGBT and its antiparallel diode are assumed to be the same. Thus, I_{avg} and

$I_{\rm rms}$ can be represented as

$$I_{\rm avg} = \frac{1}{T}\int_0^T |I_m \sin(\omega_s t - \emptyset)|\, dt = \frac{2}{\pi} I_m \tag{20}$$

$$I_{\rm rms} = \sqrt{\frac{1}{T}\int_0^T |I_m \sin(\omega_s t - \emptyset)|^2\, dt} = \frac{I_m}{\sqrt{2}} \tag{21}$$

where I_m represents the peak current at resonant frequency and is defined in (18).

2) Switching Losses: Due to the ZVS operation, the turn-on losses can be neglected; thus, the average switching losses $P_{\rm sw}$ of each IGBT in a switching period can be defined as a function of the turn-off energy losses ($E_{\rm off}$)

$$P_{\rm sw} = f_{\rm sw} \cdot E_{\rm off} \tag{22}$$

where $f_{\rm sw}$ is the switching frequency for the IGBTs, it equals to f_s for the IGBTs in *leg1*, and equals to f_s/n for the IGBTs in *leg2*. The IGBT switching-off losses $E_{\rm off}$ depend on the instantaneous device voltage (v_t) and current (i_t) during intervals $t_{\rm off}$, which results

$$E_{\rm off} = \int_{t_{\rm off}} v_t(t)\, i_t(t)\, dt. \tag{23}$$

The voltage waveform in the turn-off transition depends on the snubber capacitance [27], and the output current can be considered constant during the charge intervals, whereas the IGBT current waveform can be linearly modeled as a function of the device current fall time, t_f. Assuming $I_{\rm off}$ denotes the device current through the switching devices at the beginning of the turn-off transition [6]. As a result, the voltage and current across the device during the switching becomes linear

$$v_t(t) = \frac{I_{\rm off}}{2C_s} t \quad (0 \le t \le t_{\rm snb}) \tag{24}$$

$$i_t(t) = I_{\rm off}\left(1 - \frac{t}{t_f}\right) \quad (0 \le t \le t_f) \tag{25}$$

where $t_{\rm snb}$ denotes the required time to charge/discharge the snubber capacitance which can be calculated as

$$t_{\rm snb} = V_d \frac{2C_s}{I_{\rm off}}. \tag{26}$$

The total switching losses $P_{\rm sw,total}$ in different division factor situation have the result

$$P_{\rm sw,total} = \left(2 + \frac{2}{n}\right) f_{\rm s} \frac{I_{\rm off}^2}{12C_s} t_f^2. \tag{27}$$

III. Modulation Strategies and Digital Implementation

A. Modulation Strategy

From AFM power control methods analyzed earlier, the delivered power $P(n, f_s)$ in expression (10) is determined by two control variables: the division factor n and the switching frequency f_s. The proposed control algorithm is based on the use of AFM (1, $f_s > f_0$) in the high power range and AFM (2, $f_s > f_0$), AFM ($+\infty$, $f_s > f_0$) in the medium and low power range, respectively.

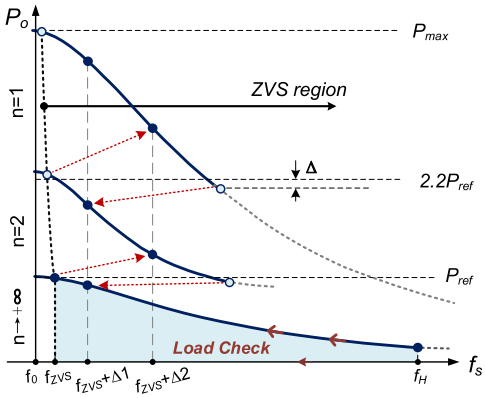

Fig. 7. Power regulation diagram.

The power control for AFM is implemented by first setting the division factor, n, and then adjust the switching frequency (see Fig. 7). Based on these considerations, transitions from higher power to lower power range (n varies from 1 to 2 or from 2 to $+\infty$) can be implemented by the PL algorithm [2]. The PL algorithm is based on the change of the modulation when a certain power level ($P_{\rm ref}$, or $2.2P_{\rm ref}$) is reached, independently of the switching frequency.

The transitions from lower power to higher power range (n varies from $+\infty$ to 2 or from 2 to 1) are based on the proposed $f_{\rm ZVS}$ control algorithm. The $f_{\rm ZVS}$ control algorithm is based on the change of the modulation when ZVS condition of the switches is not fulfilled; in this situation, the switching frequency cannot be decreased if higher output power is required. Hence, it can maximize the use of switching frequency that is closed to the resonant frequency with high efficiency.

Since transitions among the three power range lead to drastic change of f_s, thus compensations ($f_{\rm ZVS} + \Delta 1$, $f_{\rm ZVS} + \Delta 2$) are applied to f_s with the transitions to accelerate the stability of the inverter.

For a multipurpose induction appliance, different pans will lead to the uncertainty of the resonant frequency (f_0) and the maximum power ($P_{\rm max}$) [28], [29]. Thus, a load check (see Fig. 7) process based on frequency sweeping is needed to sample the hardware parameters, mainly to find the boundary switching frequency ($f_{\rm ZVS}$) to maintain the ZVS condition and measure the corresponding output power ($P_{\rm ref}$). The switching frequency f_s of the load check starts from higher frequency f_H. After a certain time that the power converter reaches the steady state, ZVS condition is checked based on the phase lag time t_d between V_o and i_o, which is given in (17).

A target output power P preset by the user is compared to the reference power $P_{\rm ref}$ to decide the power control range (see Fig. 8). Inside each range, the output power is adjusted by varying the switching frequency. Since the thermal system is much slower than transient response of the power converters, the speed of the power adjustment is not critical. As a consequence, the changes of f_s are taken in fixed steps (>50 ms) to avoid the possible acoustic noise. Moreover, hysteresis (Δ) is added to the target power P and the reference power $P_{\rm ref}$ to ensure the algorithm stability.

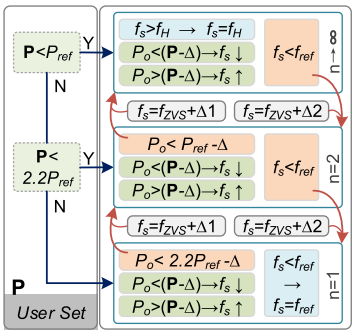

Fig. 8. Dynamic power control algorithm.

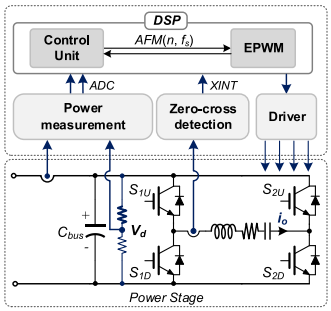

Fig. 9. Proposed control block diagram of the class-D inverter.

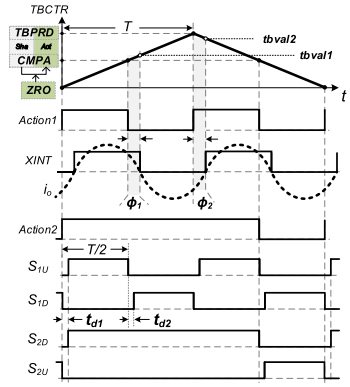

Fig. 10. EPWM implementation for AFM when $n = 2$.

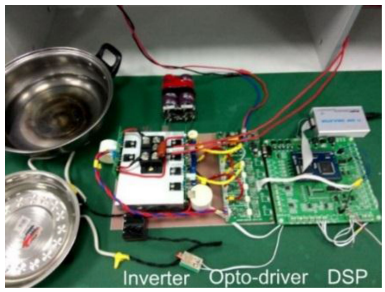

Fig. 11. Experimental setup of IH device.

B. Digital Control Implementation

The proposed power-control strategy is implemented in a digital signal processor (DSP) to arrange a versatile test bench. The modulation parameters such as the sampled power, phase lag are computed in the DSP. The overall block diagram of the proposed test bench is outlined in Fig. 9.

The output power measurement is added to bring the close loop for power control. The commonly used method is to acquire the load voltage and current simultaneously by the analog-to-digital converters, and then compute the sum of products as average power over the required period [30], [31]. The phase difference ϕ between the output voltage V_o and the output current i_o is measured by zero-cross detection circuit, whose output is a square-wave external interrupt signal (XINT) for DSP.

The PWMs are based on two 16-bit up-down-count mode counters with and the same clock (*TBCLK* unit: Hz). *TBPRD* and *CMPA* are the registers defining the period ($T = TBPRD/TBCLK$) and duty, respectively; they are composed of shadow and active registers as displayed in Fig. 10. The shadow registers can be modified by the user program at any time, and are updated to their corresponding active registers only when *TBCTR* equals *ZRO*. Comparisons between *TBCTR* and the active registers as well as *ZRO* determine the set high or clear low actions (*Action1* and *Action2*). The driving signals for switches are obtained after dead times (t_{d1} and t_{d2}) are added to the actions.

The ZVS condition is identified by ensuring the minimum phase difference ($\phi_{\min}$) between V_o and i_o. Each time the resonant current cross the zero, the edge-triggered interrupt occurs, and the value of the *TBCTR* is transferred to user-defined registers (*tbval1* or *tbval2*) immediately (see Fig. 10). The phase difference is expressed as follows:

$$\emptyset_1 = \frac{tbval1 - CMPA - \Delta t \cdot TBCLK}{TBPRD} \times 360^\circ \quad (28)$$

$$\emptyset_2 = \frac{TBPRD - tbval2 - \Delta t \cdot TBCLK}{TBPRD} \times 360^\circ \quad (29)$$

where Δt represent the transmission delay of the optocoupler driver and the interrupt response time.

IV. Experimental Verification

An experimental prototype has been built to verify the proposed control strategy described in Section III. The experimental setup (see Fig. 11) is based on full-bridge inverter (IGBT: IKW40N120H3), isolated optocoupler gate driver (HCPL-316J) board, and DSP (TMS320F28335) control board which includes power measurement, zero-cross detecting, filtering, and other safety circuits. The inductor must be designed to ensure the power level up to 4.5 kW for 300 VDC power supply voltage; thus, the inductor resistance must be lower than 16.2 Ω using (12), so two coils, with 30 turns each, in series are used as a load. The equivalent inductor-pot system resistance R_{eq} and inductance L_{eq} versus switching frequency are outlined in Table II. The measurements have been performed by means of a precision *LCR* meter from HP/Agilent (4284A).

The appropriate resonant frequency is set to 30 kHz, and resonant capacitor is therefore chosen to be 0.27 μF; thus, the

TABLE II
INDUCTION LOAD PARAMETER VERSUS SWITCHING FREQUENCY

Parameter	Value					
f_s/kHz	20	25	30	40	50	60
L_{eq}/μH	136	119	110	90	81	75
R_{eq}/Ω	10.8	12.9	14.5	16.8	18.5	19.6

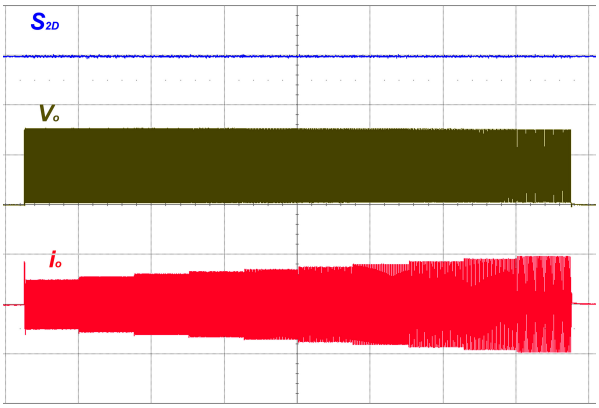

Fig. 12. Load check waveforms (S_{2D}: 10 V/div, V_o: 200 V/div, i_o: 12 A/div; 2 ms/div).

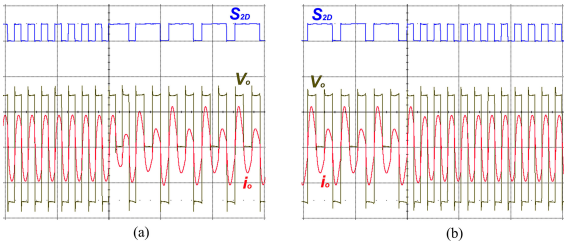

Fig. 13. (a) Transition from PFM to AFM2 (S_{2D}: 10 V/div, V_o: 200 V/div, i_o: 20 A/div; 100 μs/div). (b) Transition from AFM2 to PFM (S_{2D}: 10 V/div, V_o: 200 V/div, i_o: 20 A/div; 100 μs/div).

value of the quality factor of load (Q) is around 1.4. The snubber capacitor C_s of 9.4 nF is selected to suppress the voltage spike, and to reduce switching losses; besides, the dead time t_d is set as 0.8 μs. Thus, the maximum available output power is

$$P_o \le \frac{8V_d^2}{\pi^2 R_{\text{eq}}} = \frac{8 \cdot 300^2}{\pi^2 \cdot 14.5} = 5.0\,\text{kW}. \tag{30}$$

The startup load check process begins by configuring the AFM control parameter with $P(+\infty$, 60 kHz), the half-bridge operation mode and the maximum available switching frequency $f_H = 60$ kHz are used to obtain the minimum output power. With *TBCLK* being 25 MHz, the further check continues by increasing *TBPRD* in fixed steps. Fig. 12 shows the increased step of *TBPRD* is 40. The amplitude of i_o increases with the increase of *TBPRD*. The check finishes at $TBPRD = 817$ where the ZVS condition is lost, and the measured power by DSP is 1.1 kW. They are stored as references for the following control.

Fig. 13(a) shows the output power P_o(1, 38.5 kHz) is lower than the threshold power (2.2 kW), and the division factor is

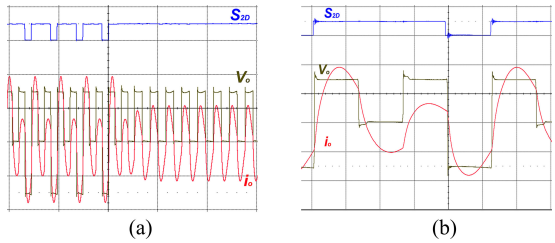

Fig. 14. (a) Transition from AFM2 to HBM. (S_{2D}: 10 V/div, V_o: 200 V/div, i_o: 10 A/div; 100 μs/div). (b) ZVS condition of AFM2 (S_{2D}: 10 V/div, V_o: 200 V/div, i_o: 10 A/div; 10 μs/div).

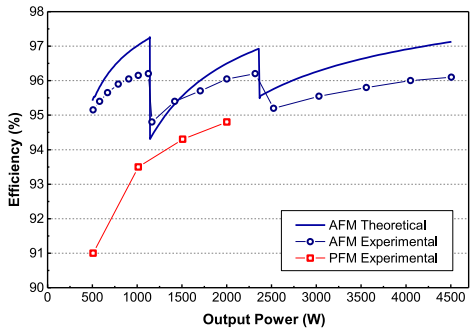

Fig. 15. Theoretical and experimental results of device efficiency.

changed from $n = 1$ to $n = 2$, the *TBPRD* delivered to AFM ($n = 2$) is adjusted to 717 with a compensation of $\Delta_{TBPRD} = 100$. The output power is then corrected with minor step of *TBPRD* every $\Delta t = 50$ ms. Fig. 13(b) shows the transition of AFM from $n = 2$ to $n = 1$ because of the loss of ZVS condition. A compensation $\Delta_{TBPRD} = 150$ is applied to the delivered *TBPRD* of AFM ($n = 1$), which accelerate the stability of the inverter.

Fig. 14(a) shows the transition of AFM from $n = 2$ to $n \to \infty$ when the target power is lower than 1 kW. Because of the use of shadow registers in *TBPRD* and *CMPA*, the changing of modes occurs only when a complete period is finished; thus, smooth transition with continuous current is obtained. Fig. 14(b) shows the i_o lags behind V_o with the maximum available switching frequency of AFM ($n = 2$); even in low quality factor load, the ZVS condition is still achieved because the current does not damp much.

The inverter efficiency has been measured using the power analyzer HIOKI PW3337 as the ratio between the input power and the power delivered to the load (see Fig. 15). The theoretical and experimental results all show that the efficiency of PFM decreases as the switching frequency is increased. In order to maintain high efficiency, the switching frequency should be limited; thus AFM, due to its narrow switching frequency near the resonant frequency and the lower switching frequency in one leg, is proposed to reduce the switching losses. The different division factor of AFM along with narrow frequency operation can ensure high efficiency in most of the output power operation range.

TABLE III
CONTROL STRATEGY COMPARISON

Characteristic	Power level	PFM	PDM	AFM
Power control	High	Good	Good	Good
	Low	Poor		
Efficiency	High	Good	Good	Good
	Low	Poor		
Power resolution		Good	Neutral	Good
Load-adaptive		Good	Poor	Good
Noise or Flicker		Good	Poor	Neutral
Thermal distribution		Good	Poor	Poor
Complexity		Neutral	Good	Poor

V. IMPROVEMENT STUDY

A. Acoustic Noise

Switching frequencies near to an audible range (20 Hz up to 20 kHz) generate acoustic noise due to the vibration of the magnetic element, the inductor, and the pan [32]. Experimental test has shown that when AFM works with the condition $n = 2$, $f_s = 30$ kHz, there is still a little acoustic noise due to the $f_s/2$ harmonic. Thus, the AFM (2, f_s) power control mode lost some frequency band (20–30 kHz) if noise problems are a concern.

B. Diverse Thermal Distribution

The AFM (2, f_s) and AFM (∞, f_s) modes are achieved by asymmetrical operation of *leg1* and *leg2*, which leads to diverse thermal distribution in *leg1* and *leg2* and the up switches and down switches. This problem can be solved by alternate use of *leg1* and *leg2* [33], and alternating use of the up switches and down switches. However, for AFM (∞, f_s), to solve the unequal thermal problem, the high-side and low-side IGBTs should be used alternately. Thus, the division factor *n* cannot be infinity; a large number of *n* that makes $1/n\mathrm{T} < 20$ Hz is feasible. These efforts are to increase the lifetime of the inverter.

C. Control Strategy Comparison

Table III compares the traditional control schemes PFM, PDM with the proposed AFM control schemes applied to the same inverter. It is shown that the use of a single traditional control strategy is unfeasible due to the several main considerations. Efficiency decreases much with PFM in the low power range due to the high switching loss. PDM achieves higher efficiency, but it has a poor load-adaptive ability with the fixed frequency control, which obviously limit its use in most applications. AFM is proposed to solve these problems; it combines the good features in PFM and PDM. However, these features increase the control complexity.

VI. CONCLUSION

This paper presents the AFM power control scheme used in the full-bridge inverter. The principles of the AFM are explained and mathematically calculated. A control strategy that schedules the three control modes of AFM is experimentally verified with a DSP-based IH prototype. The main aspects concerning the design of an IH appliance have been analyzed, including load-adaptive, high resolution power control, efficiency, and acoustic noise problems. It can be concluded that the proposed control scheme has the following advantages:

1) the AFM (2, f_s) and AFM (∞, f_s) are good choice to segment the complete power range, and better efficiency performance is achieved in the medium/low power range compared to the traditional PFM;
2) due to the combination use of division factor and narrow frequency control, the AFM can avoid the conflict between the flicker performance and continuous power control, which occurs in PDM power control appliances;
3) continuous resonant current can be achieved in low-quality factor load with AFM in the low power range, for its minimum adjacent freewheeling process;
4) the various modes of AFM can be operated with variable frequency, which provides the possibility for the load-adaptive process.

Thus, the proposed AFM control scheme can be applied to other full-bridge inverter topologies that require a wide output power range and high efficiency.

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