Letters

Novel High Step-Up DC–DC Converter With an Active Coupled-Inductor Network for a Sustainable Energy System

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***Abstract*—In this letter, a novel high step-up dc–dc converter with an active coupled-inductor network is presented for a sustainable energy system. The proposed converter contains two coupled inductors which can be integrated into one magnetic core and two switches. The primary sides of coupled inductors are charged in parallel by the input source, and both the coupled inductors are discharged in series with the input source to achieve the high step-up voltage gain with appropriate duty ratio, respectively. In addition, the passive lossless clamped circuit not only recycles leakage energies of the coupled inductor to improve efficiency but also alleviates large voltage spike to limit the voltage stresses of the main switches. The reverse-recovery problem of the output diode is also alleviated by the leakage inductor and the lower part count is needed; therefore, the power conversion efficiency can be further upgraded. This letter shows the key waveforms of the proposed converter and the detailed derivation of the steady-state operation principle. The voltage conversion ratio, the effect of the leakage inductance and the parasitic parameters on the voltage gain are discussed. The voltage stress and current stress on the power devices are illustrated and the comparisons between the proposed converter and other converters are given. Finally, a prototype circuit rated 200-W output power is implemented in the laboratory, and the experimental results show the satisfactory agreement with the theoretical analysis.**

***Index Terms*—Active coupled-inductor network (ACLN), high step-up voltage gain dc–dc converter, low voltage stress.**

I. Introduction

As generally recognized, the distributed PV generation systems based on the renewable energy sources have been a most promising candidate for the exhaustion of fossil fuel [1]–[3]. However, the PV source is the low-voltage source which cannot provide enough dc voltage for generating ac line voltage. Although the PV cells can connect in series to obtain the sufficient dc voltage, it is difficult to avoid the shadow effect and to obtain a constant dc voltage [4], [5]. Thus, the high step-up dc–dc converters with a large conversion ratio, high efficiency, and small volume are dispensable as the dc link between the PV source and inverter [6].

In general, the boost converter is widely used in such applications. Theoretically, the boost converter can provide a high step-up voltage gain with an extremely high duty cycle. In practice, the voltage conversion ratio is limited below four or five by parasitic parameters effect dramatically [7]. Consequently, if the voltage conversion ratio is desired to be over five, the high step-up converter topologies are needed [8]–[19].

The isolated converter topologies like the flyback converter can achieve a high step-up voltage gain by adjusting the turns ratio of the transformer. However, the leakage inductor can cause the high voltage spike, and therefore, a high-voltage rated switch is needed [8]. Although the passive-clamped circuits and active-clamped circuits can be employed, the efficiency is degraded and the cost is increased [9].

In [10] and [11], the voltage lift technique is presented. High step-up voltage gain is achieved by the transferred energy from the intermediate capacitor, but the voltage and current stresses on the intermediate capacitor are serious. In [12] and [13], the high step-up voltage gain can be achieved by using the switched capacitor and switched inductor technique.

The problems in the conventional boost converter which works under the high step-up condition can be solved by introducing a coupled inductor [14], [15]. The voltage gain is extended and the voltage stress on the switch is reduced. Moreover, the cores can be integrated and the volume is reduced. However, the leakage inductance may cause the same problems as in isolated converters. Compared to the boost converter, an active network converter (ANC) has been proposed in [16], where the voltage stresses and current stresses of the switches are much lower, and the voltage conversion ratio is higher. However, there exists the switch voltage resonance due to the switches parameters inconsistency. Switched inductor ANC is proposed to extend the voltage gain, but the voltage conversion gain can only be controlled by duty cycle and the overall system volume is larger [17]. The ANC with the switched inductor and switched capacitor is proposed in [18], but the system volume is large and part count is increased greatly under the high voltage conversion gain. The ANC with coupled inductors is further proposed in [19], and the voltage gain is increased by adjusting turns ratio of the coupled inductor and the duty cycle, but the part count is still high.

This letter proposes a novel high efficiency high step-up voltage gain converter which combines an active coupled-inductor network (ACLN) and a traditional boost converter with a passive

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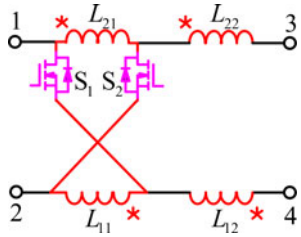

Fig. 1. The active coupled-inductor network (ACLN).

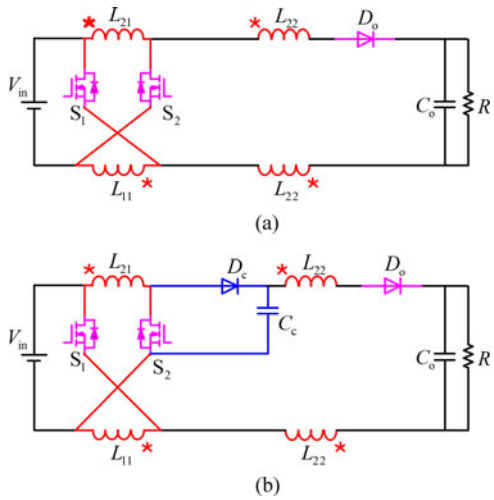

Fig. 2. Proposed high step-up ACLN dc–dc boost converter. (a) ACLNC. (b) ACLNC with a passive lossless clamped circuit.

clamping circuit, called the ACLN converter (ACLNC). The proposed converter has the following advantages: high voltage conversion gain, small volume, low voltage stresses on switches, low diodes count, and low conduction losses on switches. The basic operating principle is first illustrated in detail, then the stresses expressions are deduced, and finally, some experimental results are provided to verify the effectiveness of the proposed converter.

II. Proposed High Step-up Converter

The proposed converter contains an ACLN which is shown in Fig. 1. The ACLN consists of two coupled inductors (L_{11} and L_{12}, L_{21} and L_{22}) which have the same inductance value and two same switches (S_1 and S_2) which share the same operation signal.

By combining the ACLN with the traditional boost converter, the ACLN dc–dc boost converter (ACLNC) is obtained, as shown in Fig. 2(a), in which the output voltage is greatly enhanced. The proposed high step-up converter is constructed by two coupled inductors made up of four windings L_{11}, L_{12}, L_{21}, and L_{22}, two switches S_1 and S_2, one output diode D_o, and one output capacitor C_o.

The leakage inductance is inevitable in the proposed ACLNC, which results in high voltage spikes, large switching losses, and severe EMI problems. In general, the dissipated RCD circuit can be used for absorbing the leakage inductance, but the losses

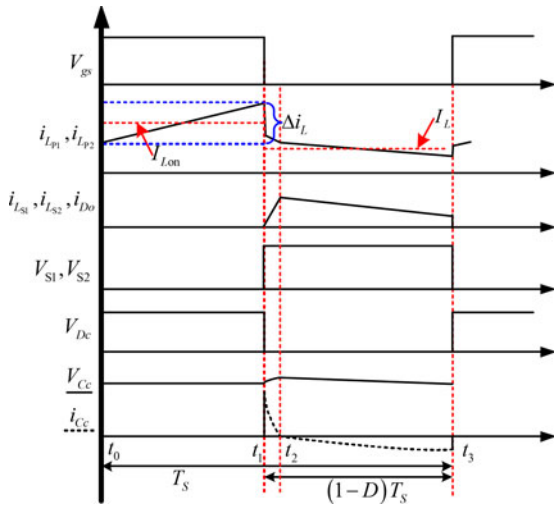

Fig. 3. Some typical waveforms of the proposed ACLNC.

induced by the RCD circuit are significant and the efficiency is degraded. Therefore, passive lossless clamped circuits are applied here to recycle the leakage energy and to suppress the voltage spikes as shown in Fig. 2(b) [6].

III. Basic Operating Principle

Fig. 3 briefly illustrates the key waveforms of the proposed ACLNC. Only the operating principle in continuous-conduction mode (CCM) is discussed in this letter. The transient states in operating principle will not be discussed here because the parasitic resistance and the parasitic capacitance of the two active switches and diodes are neglected. Fig. 4(b)–(d) shows the equivalent circuits of the proposed ACLNC under the following assumptions:

1) The capacitors C_c and C_o are large enough so that the voltages on them are considered to be constant.
2) The switches and diodes are ideal. In order to clearly show the current flows, the ideal switches take the place of MOSFETs in ON state or OFF state, as shown in Fig. 4(a).
3) The equivalent circuit model of the coupled inductor includes two ideal coupled inductors L_{Pi} and L_{Si} and two leakage inductors L_{ki} $(i = 1, 2)$.
4) To make the following derivation simple, define K as $L_{Pi}/(L_{Pi} + L_{ki})$ and the turns ratio of L_{P1} to L_{S1} and L_{P2} to L_{S2} is $1 : N$ $(N > 1)$. L_{P1}, L_{P2} and L_{S1}, L_{S2} share the same inductance, respectively.

A. CCM Operation

The three steady operating modes are described as follows.

1) *Mode I [t_0,t_1]*: During this time interval, the switches S_1 and S_2 are turned ON. Diodes D_c and D_o are reverse biased. The current-flow path is shown in Fig. 4(b). The primary sides of both coupled inductors are in parallel charged. The currents inductor $i_{L_{P1}}$ and $i_{L_{P2}}$ are increased linearly. Output capacitor C_o provides its energy to the load R. When the switches S_1 and S_2 are turned OFF at t_1,

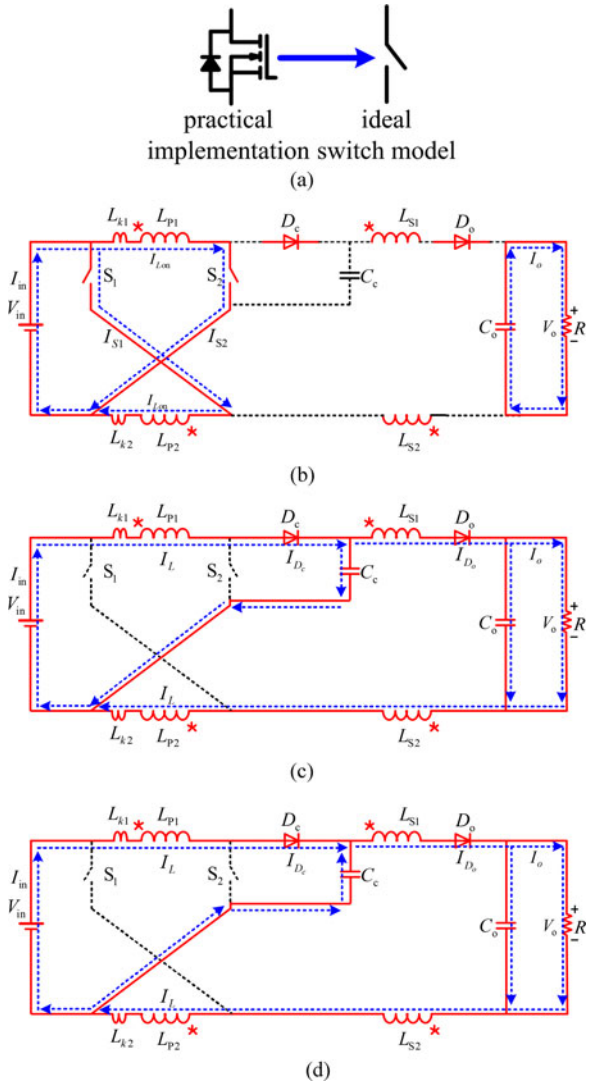

Fig. 4. Equivalent circuits of the proposed ACLNC.

this operating mode ends. Thus, according to the KVL, the voltage equation across coupled inductors is expressed as follows:

$$V_L^I = 2\,(NK+1)\,V_{\rm in}. \tag{1}$$

where V_L represents the voltage on both the coupled inductors.

2) *Mode II [t_1,t_2]*: During this time interval, the switches $\rm S_1$ and $\rm S_2$ are turned OFF. Diodes $\rm D_c$ and $\rm D_o$ are forward biased. The leakage energy flows into the clamped capacitor C_c. Meanwhile, the dc source $V_{\rm in}$ and the energies stored in the coupled inductors are transferred to output capacitor $C_{\rm o}$ and the load R. This operating mode is ended when the charging current of clamped capacitor i_{Cc} is equal to zero, as shown in Fig. 4(c). The voltage across both coupled inductors can be expressed as

$$V_L^{II} = V_{\rm in} - V_{\rm o}. \tag{2}$$

3) *Mode III [t_2,t_3]*: During this time interval, the switches $\rm S_1$ and $\rm S_2$ remain OFF. Diodes $\rm D_c$ and $\rm D_o$ are still forward biased. The current-flow path is shown in Fig. 4(d). The clamped capacitor C_c is discharging. Concurrently, the dc source $V_{\rm in}$ and the energies stored in the coupled inductors are transferred to output capacitor $C_{\rm o}$ and the load R. This operating mode is ended when the switches $\rm S_1$ and $\rm S_2$ are turned ON at t_3. The voltage across both coupled inductors can be written as

$$V_L^{III} = V_{\rm in} - V_{\rm o}. \tag{3}$$

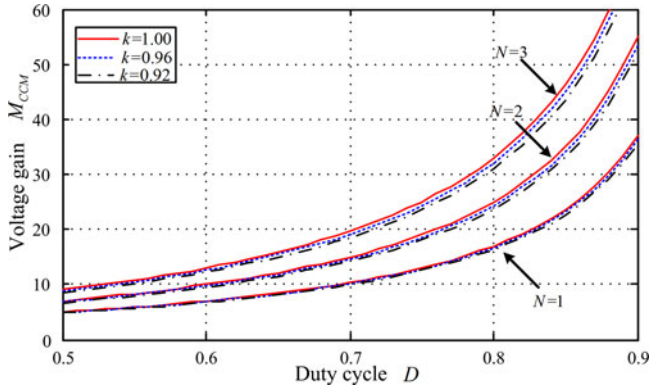

Fig. 5. Effect of leakage inductance and turns ratio on voltage gain.

IV. Circuit Performance Analysis

A. Steady-State Analysis

By applying the volt–second balance principle on coupled inductors, the following equation is formed:

$$\int_{t_0}^{t_1} V_L^I\,dt + \int_{t_1}^{t_2} V_L^{II}\,dt + \int_{t_2}^{t_3} V_L^{III}\,dt = 0. \tag{4}$$

Substituting (1)–(3) into (4) and collecting terms, the voltage gain is obtained as

$$M_{\rm CCM} = (D(2NK+1)+1)/(1-D). \tag{5}$$

By employing the clamp circuits, the voltage strikes caused by the leakage inductance are suppressed and the energy stored in the leakage inductance is recycled to the load. Especially, the reverse-recovery problem of the diodes $\rm D_o$ is solved. However, the leakage inductance causes the duty ratio losses. The schematic of the voltage gain versus the duty ratio under various leakage inductance L_{k1} and various turns ratio of the coupled inductors is shown in Fig. 5. As the turns ratio increases, the voltage gain of this converter increases. On the contrary, as the leakage inductance increases, the voltage gain of this converter decreases. In order to further clearly show the effect of the leakage inductance, Table I shows the effect of the leakage inductance and the turns ratio on the voltage conversion gain when the converter operate under $D=0.6$. Therefore, some consideration should be made when the leakage inductance is big during the design. When leakage inductance is zero, the ideal voltage gain can be written as

$$M_{\rm CCM} = (D\,(2N+1)+1)\,/(1-D). \tag{6}$$

TABLE I
SPECIFIC EFFECT OF THE LEAKAGE INDUCTANCE AND THE TURNS RATIO ON THE VOLTAGE GAIN

k \ N	1	2	3
1	7	10	13
0.96	6.88	9.76	12.64
0.92	6.76	9.52	12.28

B. Voltage Stresses and Current Stresses on Power Devices

The voltage ripples on the capacitors and the leakage inductances are ignored to simplify the voltage stresses analysis on the components of the proposed converter. The voltage stresses of the main switch S_1, S_2 and clamped capacitor C_c are given by

$$V_{S1} = V_{S2} = V_{C_c} = V_{in}/(1-D). \tag{7}$$

The voltage stresses on diodes D_o and D_c related to the turns ratio and the input voltage can be derived as

$$V_{D_o} = V_{in}(2N+1)/(1-D) \tag{8}$$

$$V_{D_c} = V_{in}/(1-D). \tag{9}$$

The on-state average currents of the output diode D_o and clamped diode D_c are calculated as

$$I_{D_o} = I_{D_c} = I_o/(1-D). \tag{10}$$

The root-mean-square (RMS) currents through the switches can be obtained by assuming the inductor current ripples of primary sides of coupled inductors as $\Delta i_L = K_L I_{Lon}$,

$$I_{S1-RMS} = I_{S2-RMS} = \frac{(1+N)\sqrt{D}}{1-D} \cdot \frac{P_o}{V_o}\sqrt{\frac{K_L^2}{12}+1} \tag{11}$$

where P_o is the output power.

C. Comparison with Other Converters

Due to the dual-switch structure, the current ripple is minimized to reduce the conduction loss, the passive component size is reduced, and the power level is increased. In order to clearly demonstrate the circuit advantages of the proposed converter, a detailed comparison is made among the conventional boost converters, boost converter with switching coupled-inductor [Boost-SCL] in [20], ultralarge gain step-up switched-capacitor dc–dc converter with coupled inductor [USC-CL] in [21], a coupled inductor SEPIC converter [CL-SEPIC] in [22], passive clamp-mode coupled-inductor boost converters with coupled inductor [CM-Boost-CL] in [6], and the proposed ACLNC are highlighted in Table II.

Some specific variable symbols of all parasitic components are assumed as follows: V_D is the forward voltage drop of diodes; r_L is the ESR of inductors; r_{DS} is the on-state resistance of the switch; r_D represents the forward resistance of diode; and R represents the load. According to the previous work [23], [24], the theoretical dc gain and efficiency influenced by the parasitic parameters and duty cycle are also obtained in Table II.

Some variables in Table II are shown as follows:

$$A1 = 1 - V_D(1-D)/V_{in}$$

$$B1 = 1 - D(r_L + Dr_{DS} + (1-D)r_D)/((1-D)R)$$

$$A2 = ND + 1 - V_D(1-D)/V_{in}$$

$$B2 = 1 - D + \frac{(N+1)r_L + r_D}{R} + \frac{D(N+1)^2(r_L + r_{DS})}{(1-D)R}$$

$$A3 = 1 + N(D+1) - 4V_D(1-D)/V_{in}$$

$$B3 = 1 - D + N(r_L + r_D)/2R + (Nr_L + r_D)(1+D)/DR + N\left(1 + D + D^2\right)(r_L + r_{DS})/D^2(1-D)R$$

$$C3 = 1 + N(D+1), A4 = D(N+1) - V_D(1-D)/V_{in}$$

$$B4 = 1 - D + r_{DS}D(N+1)^2/(1-D)R + (N_L + r_D)/R + \left(1 - 2D + 2D^2 + DN^2 - 2D^3 - 2D^2N^2\right)r_L/(1-D)R,$$

$$C4 = D(N+1)$$

$$A5 = ND + 1 - 2V_D(1-D)/V_{in}$$

$$B5 = 1 - D + \frac{(2r_D + r_L(N+1))}{R} + \frac{(r_L + r_{DS})D(N+1)^2}{(1-D)R}$$

$$A6 = D(2N+1) + 1 - 2V_D(1-D)/V_{in}$$

$$C6 = (2N+1)D + 1$$

$$B6 = 1 - D + \frac{2(r_L + Nr_L + r_d)}{R} + \frac{2D(N+1)^2(r_L + r_{DS})}{R(1-D)}.$$

Although the different voltage stresses and current stresses of the power switches make different models of power switch available in different converters, here we assume that all the parasitic parameters are same. In order to show how different output power influences the efficiency, some parameters are assumed as follows:

$$V_D = 1\text{ V},\ r_L = 0.05\ \Omega,\ r_{DS} = 0.085\ \Omega,\ r_D = 0.02\ \Omega,$$
$$V_{in} = 20\text{ V},\ V_o = 200\text{ V},\ N = 2.$$

Fig. 6 shows the calculated efficiency under different load. One can see that the efficiency of the boost converter and the CL-SEPIC converter is higher than the proposed converter in the case of light load, only the efficiency of the CL-SEPIC converter is higher than the proposed converter in the case of overloading. So, although the numbers of components in the proposed converter compared with the boost converter are increased, the efficiency cannot be degraded. On the contrary, because of decreasing voltage stress and current stress, it is easy to achieve decent efficiency in high step-up applications.

Fig. 7 calculates the voltage gain under different duty cycle. When the duty cycle is lower than about 0.65, only the voltage

TABLE II
PERFORMANCE COMPARISON AMONG DIFFERENT CONVERTERS

Topology	Boost	Boost-SCL	USC-CL	CL-SEPIC	CM-Boost-CL	ACLNC
Active switches	1	1	1	1	1	2
Diodes	1	2	4	2	2	2
Magnetic cores	1	1	1	2	1	1
Voltage gain	$\frac{1}{1-D}$	$\frac{1+ND}{1-D}$	$\frac{C3}{1-D}$	$\frac{(1+N)D}{1-D}$	$\frac{ND+1}{1-D}$	$\frac{C6}{1-D}$
Voltage stress of active switch	$\frac{V_{\rm in}}{1-D}$	$V_{\rm in}\frac{1+ND}{1-D}$	$\frac{V_{\rm in}}{1-D}$	$V_{\rm in}\frac{1+ND}{1-D}$	$\frac{V_{\rm in}}{1-D}$	$\frac{V_{\rm in}}{1-D}$
Current stress of active switch	$\frac{I_{\rm o}}{1-D}$	$\frac{I_{\rm o}(N+1)}{1-D}$	$\frac{I_{\rm o}N(D+1)}{D(1-D)}$	$\frac{I_{\rm o}(D+N)}{1-D}$	$\frac{I_{\rm o}(N+1)}{1-D}$	$\frac{I_{\rm o}(N+1)}{1-D}$
Voltage stress of output diode	$\frac{V_{\rm in}}{1-D}$	$V_{\rm in}\frac{1+ND}{1-D}$	$\frac{NV_{\rm in}}{1-D}$	$V_{\rm in}\frac{1+ND}{1-D}$	$\frac{NV_{\rm in}}{1-D}$	$\frac{(1+2N)V_{\rm in}}{1-D}$
Cost	small	medium	medium	medium	small	medium
Voltage gain with parasitic resistance	$\frac{A1}{B1}$	$\frac{A2}{B2}$	$\frac{A3}{B3}$	$\frac{A4}{B4}$	$\frac{A5}{B5}$	$\frac{A6}{B6}$
Efficiency with parasitic resistance	$\frac{A1(1-D)}{B1}$	$\frac{A2(1-D)}{B2(1+ND)}$	$\frac{A3(1-D)}{B3C3}$	$\frac{A4(1-D)}{B4C4}$	$\frac{A5(1-D)}{B5(ND+1)}$	$\frac{A6(1-D)}{B6C6}$

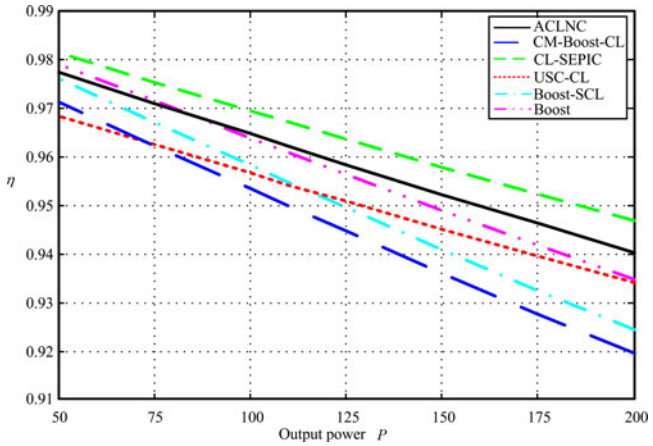

Fig. 6. Efficiency curves of different converters which is influenced by parasitic parameters and duty cycle under different output power.

TABLE III
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
Input voltage $V_{\rm in}$	20 V
Output voltage $V_{\rm o}$	200 V
Rated power $P_{\rm o}$	200 W
Switching frequency $f_{\rm s}$	50 kHz

TABLE IV
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

Components	Specifications
Switches S_1, S_2	IRFP250
Diodes D_o, D_c	VS-EPU6006-N3
Output capacitor $C_{\rm o}$	470 μF/450 V
Clamped capacitor C_c	22 μF/100 V
Coupled inductors	Core-NPS306060
	$N_{\rm P}:N_{\rm S}=1:2$
	$L_{\rm P1}=232\,\mu{\rm H}, L_{\rm S1}=942\,\mu{\rm H}$
	$L_{\rm P2}=212\,\mu{\rm H}, L_{\rm S2}=922\,\mu{\rm H}$

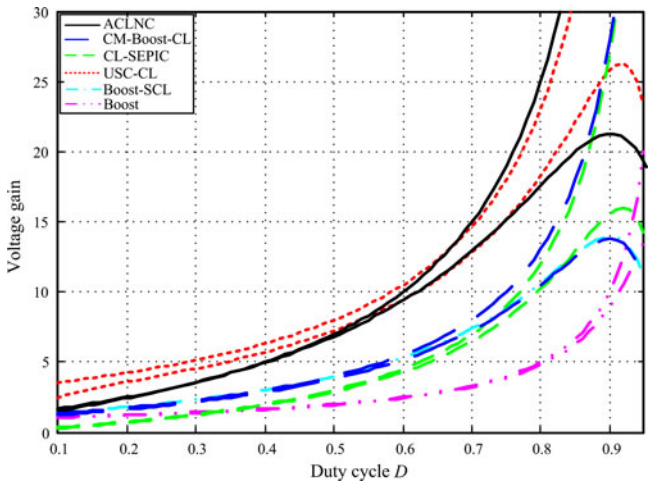

Fig. 7. Comparison of the voltage gain among different converters (solid line: ideal voltage gain, dashed line: voltage gain influenced by parasitic parameters).

gain of USC-CL is higher than the gain of the proposed converter. When the duty cycle is lower than about 0.55, the parasitic parameters have little impact on the voltage gain of the converters, except USC-CL converter. As the duty cycle increases, the ideal voltage gain of the proposed converter is beyond the ideal voltage gain of the USC-CL converter. Meanwhile, parasitic parameters make the practical voltage gain lower than the ideal voltage gain in all converters. But, the practical voltage gain of the proposed converter is still higher than the practical voltage gain of other converters, except USC-CL converter.

Compared with the boost converter, both the ideal voltage gain and the practical voltage gain of the ACLNC are higher. Also, the voltage stresses and the current stresses of the switches in the ACLNC are dramatically reduced. Although the numbers of part in the ACLNC are more than those of the boost converter, the efficiency of the ACLNC is superior to the boost converter.

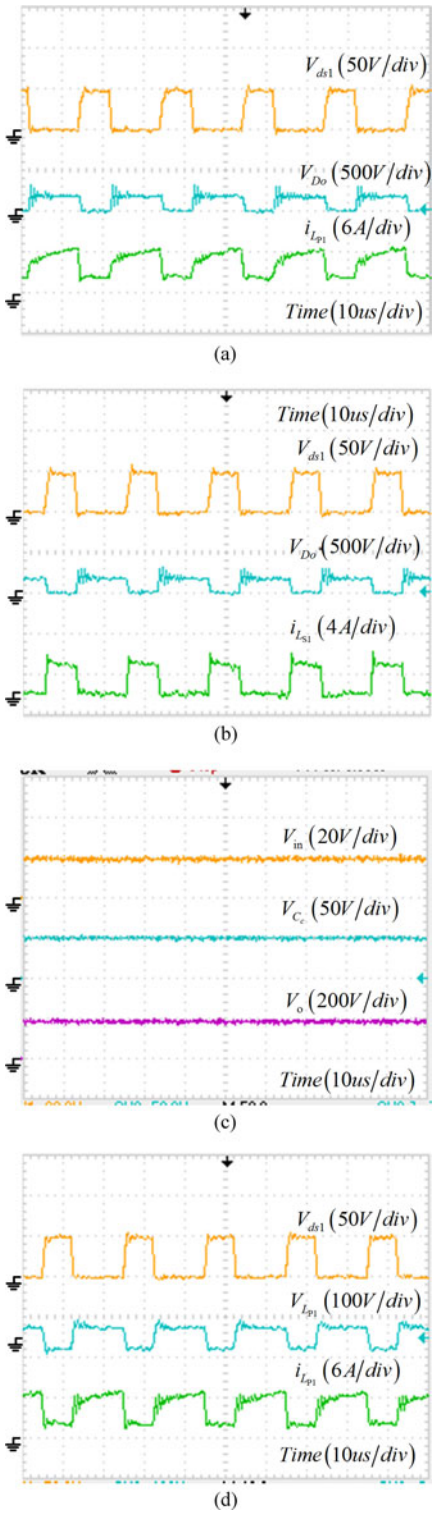

Fig. 8. Experimental waveforms of the proposed ACLNC with passive lossless clamping.

Compared with the Boost-SCL, both the ideal voltage gain and the practical voltage gain of the ACLNC are higher. The voltage stresses of the switches in the ACLNC are reduced, the low on-resistance switch can be used. Meanwhile, the current stresses of the main switches are also reduced. Therefore,

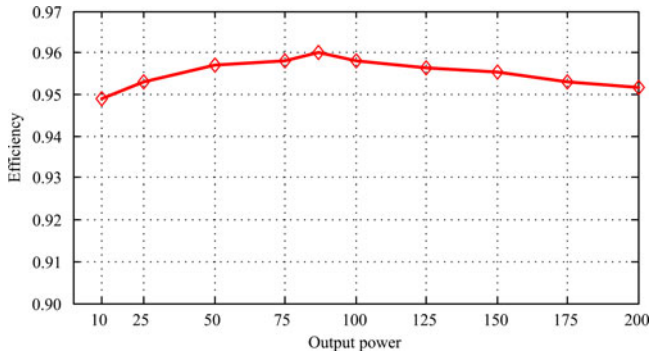

Fig. 9. Efficiency under different output power.

although the ACLNC contains two MOSFETS, the efficiency can be effectively upgraded.

Compared with the USC-CL, when the duty cycle is smaller, the voltage gain of the USC-CL is higher; and when the duty cycle is larger, the voltage gain of the ACLNC is higher. Although the ACLNC contains two active switches, the numbers of diodes in the ACLNC are lower. In addition, the current stress of the switch in the ACLNC is also reduced, especially the inrush current of the capacitor is avoided in the ACLNC. Therefore, the efficiency of the ACLNC is higher than that of the USC-CL.

Compared with the CL-SEPIC, the voltage gain of the ACLNC is higher. The voltage stresses and the current stresses of the switches in the ACLNC are reduced. Therefore, the low on-resistance switch can be used. It is helpful to upgrade the efficiency. In addition, the numbers of the magnetic core in the ACLNC are lower than that of the CL-SEPIC. In summary, the cost in the ACLNC is lower than that of the CL-SEPIC.

Compared with the CM-Boost-CL, the voltage gain of the ACLNC is also higher. This causes the voltage stresses and the current stresses of the switches lower in the ACLNC. Therefore, although the two switches are used in the ACLNC, the efficiency in the ACLNC is higher.

V. Experimental Results

Before this topic is discussed, there are some specifications given as follows. Table III shows the system specifications of the proposed converter, and the Table IV shows the component specifications used in the proposed converter.

Fig. 8 illustrates the measured waveforms for $P_{\rm o} = 200\,{\rm W}$ and $V_{\rm in} = 20$ V. The steady analysis can be demonstrated in the experimental results. In the measured waveforms, the voltage $V_{\rm ds}$ across the switches is clamped at approximately 50 V (i.e., $V_{\rm in}/(1-D)$) during the switch-off period. Therefore, a low-voltage rated switch can be adopted to make the proposed converter reduce its conduction loss and upgrade the efficiency. Fig. 8(a) shows the output diode voltage $V_{\rm Do}$, the voltage stress on the output diode is equal to 250 V (i.e., $V_{\rm in}\,(2N+1)\,/\,(1-D)$). Fig. 8(a) and (b) show the inductor current $i_{L_{\rm P1}}$ and $i_{L_{\rm S1}}$, the waveforms are corresponding to the theoretical analysis. Fig. 8(c) shows the input voltage $V_{\rm in}$, the clamped capacitor voltage V_{C_c}, and the output voltage $V_{\rm o}$. Fig. 8(d) shows the primary-side voltage of coupled inductor

and the corresponding current waveforms. They show high consistency. All the experimental waveforms are corresponding to the theoretical analysis.

Furthermore, Fig. 9 shows the tested curve of efficiency versus output power. From Fig. 9, it can be seen that the efficiency is above 95% all over the output power range, and the maximum efficiency can be up to 95.9%.

VI. Conclusion

In this letter, a novel ACLNC topology with high voltage ratio is proposed and the steady-state analysis is given. A passive lossless clamped circuit is introduced to suppress the voltage spike across the switches. Compared to the traditional high step-up dc/dc converter, it has the following advantages:

1) high voltage gain can be achieved with the reduced magnetic size;
2) lower part count contributes not only to the lower cost but also to higher power conversion efficiency;
3) low voltage power switches can be selected, which can help to reduce the on-state resistance of the switch and the loss.

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